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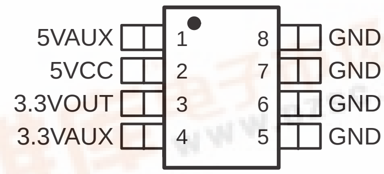
TPPM0301
400-mA LOW-DROPOUT REGULATOR WITH AUXILIARY POWER MANAGEMENT

SLVS315 – SEPTEMBER 2000

- **Automatic Input Voltage Source Selection**
- **Glitch-Free Regulated Output**
- **5-V Input Voltage Source Detector With Hysteresis**
- **400-mA Load Current Capability With 5-V or 3.3-V Input Source**
- **Low $r_{DS(on)}$ Auxiliary Switch**
- **Thermally Enhanced Packaging Concept for Efficient Heat Management**

D PACKAGE (TOP VIEW)



description

The TPPM0301 is a low-dropout regulator with auxiliary power management that provides a constant 3.3-V supply at the output capable of driving a 400-mA load.

The TPPM0301 provides a regulated power output for systems that have multiple input sources and require a constant voltage source with a low-dropout voltage. This is a single output, multiple input intelligent power source selection device with a low-dropout regulator for either 5VCC or 5VAUX inputs, and a low- resistance bypass switch for the 3.3VAUX input.

Transitions may occur from one input supply to another without generating a glitch, outside of the specification range, on the 3.3-V output. The device has an incorporated reverse blocking scheme to prevent excess leakage from the input terminals in the event that the output voltage is greater than the input voltage.

The input voltage is prioritized in the following order: 5VCC, 5VAUX, and 3.3VAUX.

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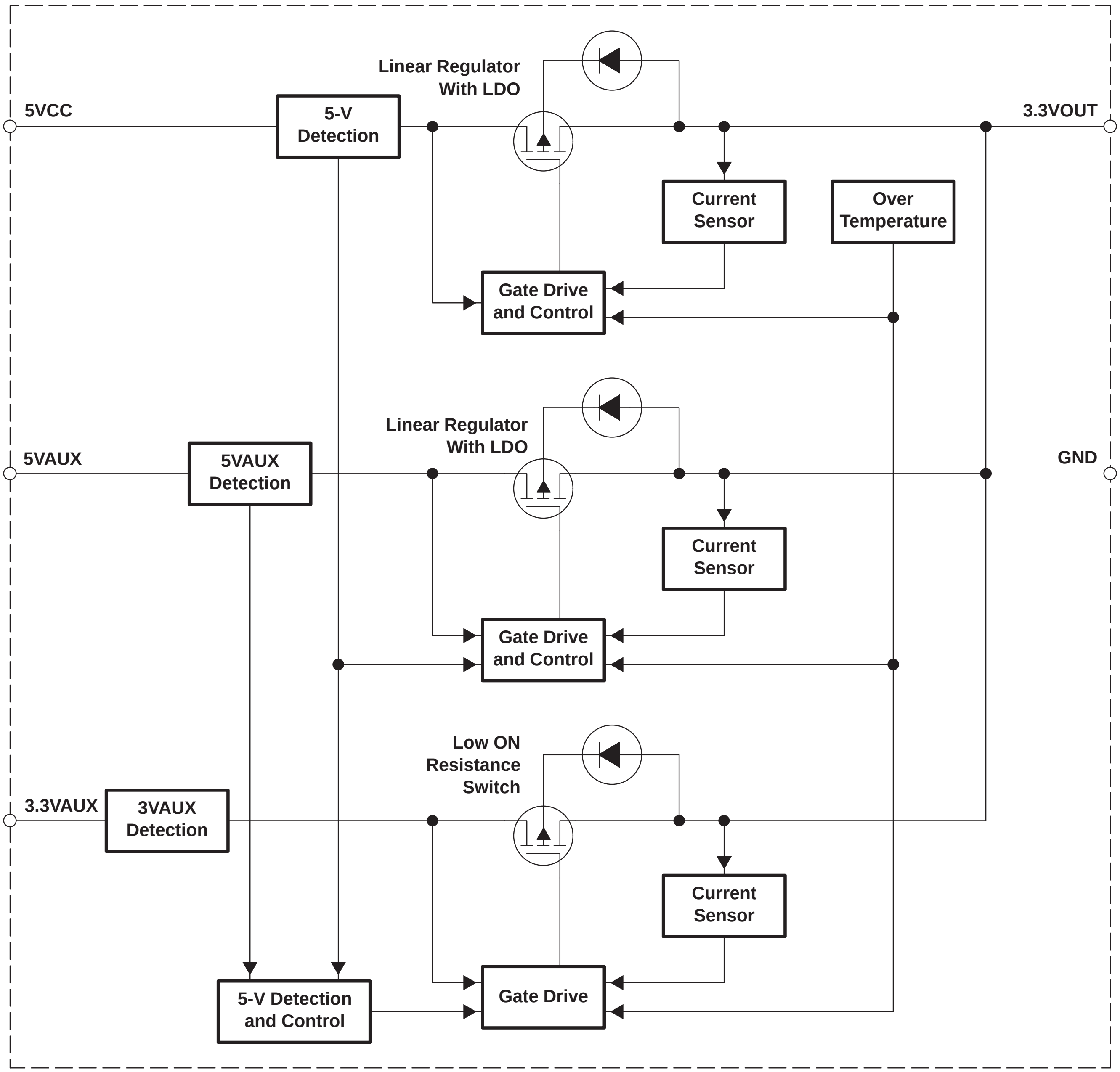
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3.3VAUX	4	I	3.3-V auxiliary input
3.3VOUT	3	O	3.3-V output with a typical capacitance load of 4.7 µF
5VAUX	1	I	5-V auxiliary input
5VCC	2	I	5-V main input
GND	5, 6, 7, 8	I	Ground

Table 1. Input Selection

INPUT VOLTAGE STATUS (V)			INPUT SELECTED	OUTPUT (V)	OUTPUT (I)
5VCC	5VAUX	3.3VAUX	5VCC/5VAUX/3.3VAUX	3.3VOUT	I_L (mA)
0	0	0	None	0	0
0	0	3.3	3.3VAUX	3.3	375
0	5	0	5VAUX	3.3	400
0	5	3.3	5VAUX	3.3	400
5	0	0	5VCC	3.3	400
5	0	3.3	5VCC	3.3	400
5	5	0	5VCC	3.3	400
5	5	3.3	5VCC	3.3	400

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, 5-V main input, $V_{(5VCC)}$ (see Notes 1 and 2) . . . 7 V
Auxiliary voltage, 5-V input, $V_{(5VAUX)}$ (see Notes 1 and 2) . . . 7 V
Auxiliary voltage, 3.3-V input, $V_{(3.3VAUX)}$ (see Notes 1 and 2) . . . 5 V
3.3-V output current limit, $I_{(LIMIT)}$ . . . 1.5 A
Continuous power dissipation, P_D (see Note 3) . . . 1 W
Electrostatic discharge susceptibility, human body model, $V_{(HBMESD)}$ . . . 2 kV
Operating ambient temperature range, T_A . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . –55°C to 150°C
Operating junction temperature range, T_J . . . –5°C to 120°C
Lead temperature (soldering, 10 second), $T_{(LEAD)}$ . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminal should not be below –0.5 V.
3. $R_{\theta JA}$ must be less than 55°C/W, typically achieved with two square inches of copper printed circuit board area connected to the GND terminals for heat dissipation or equivalent.

recommended operating conditions

	MIN	TYP	MAX	UNIT
5-V main input, $V_{(5VCC)}$	4.5		5.5	V
5-V auxiliary input, $V_{(5VAUX)}$	4.5		5.5	V
3.3-V auxiliary input, $V_{(3.3VAUX)}$	3		3.6	V
Load capacitance, C_L	4.23	4.7	5.17	µF
Load current, I_L	0		400	mA
Ambient temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range, T_A = 0°C to 70°C, C_L = 4.7 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(5VCC)}$/ $V_{(5VAUX)}$	5-V inputs		4.5	5	5.5	V
$I_{(Q)}$	Quiescent supply current	From 5VCC or 5VAUX terminals, I_L = 0 to 400 mA		2.5	5	mA
		From 3.3VAUX terminal, I_L = 0 A		250	500	µA
I_L	Output load current		0.4			A
$I_{(LIMIT)}$	Output current limit	3.3VOUT = 0 V		1	1.5	A
$T_{(TSD)}$†	Thermal shutdown	3.3VOUT output shorted to 0 V	150		180	°C
T_{hys}†	Thermal hysteresis	3.3VOUT output shorted to 0 V		15		°C
$V_{(3.3VOUT)}$	3.3-V output	I_L = 400 mA	3.135	3.3	3.465	V
C_L	Load capacitance	Minimal ESR to insure stability of regulated output		4.7		µF
$I_{lkg(REV)}$	Reverse leakage output current	Tested for input that is grounded. 3.3VAUX, 5VAUX or 5VCC = GND, 3.3VOUT = 3.3 V			50	µA

† Design targets only. Not tested in production.

5-V detect

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TO\_LO)}$	Threshold voltage, low	5VAUX or 5VCC ↓	3.85	4.05	4.25	V
$V_{(TO\_HI)}$	Threshold voltage, high	5VAUX or 5VCC ↑	4.1	4.3	4.5	V

auxiliary switch

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(SWITCH)}$	Auxiliary switch resistance	5VAUX = 5VCC = 0 V, 3.3VAUX = 3.3 V, I_L = 150 mA			0.4	Ω
$\Delta V_{O(\Delta VI)}$	Line regulation voltage	5VAUX or 5VCC = 4.5 V to 5.5 V		2		mV
$\Delta V_{O(\Delta IO)}$	Load regulation voltage	20 mA < I_L < 400 mA		40		mV
$V_I - V_O$	Dropout voltage	I_L < 400 mA			1	V

thermal characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case			38	°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient			97	°C/W

THERMAL INFORMATION

To ensure reliable operation of the device, the junction temperature of the output device must be within the safe operating area (SOA). This is achieved by having a means to dissipate the heat generated from the junction of the output structure. There are two components that contribute to thermal resistance. They consist of two paths in series. The first is the junction to case thermal resistance, $R_{\theta JC}$; the second is the case to ambient thermal resistance, $R_{\theta CA}$. The overall junction to ambient thermal resistance, $R_{\theta JA}$, is determined by:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

The ability to efficiently dissipate the heat from the junction is a function of the package style and board layout incorporated in the application. The operating junction temperature is determined by the operating ambient temperature, T_A, and the junction power dissipation, P_J.

The junction temperature, T_J, is equal to the following thermal equation:

$$T_J = T_A + P_J\,(R_{\theta JC}) + P_J\,(R_{\theta CA})$$

$$T_J = T_A + P_J\,(R_{\theta JA})$$

This particular application uses the enhanced 8-pin SO package with an integral fused lead frame (terminals 5 to 8). By incorporating a dedicated heat spreading copper plane of at least two square inches on a double-side printed-circuit board (PCB), a thermal resistance of junction to ambient, $R_{\theta JA}$, of 50°C/W can be obtained.

Alternatively, if no dedicated copper plane is incorporated for this device and the PCB has a multilayer construction, the ground terminals (5 to 8) could be electrically connected to the ground plane of the board. This will provide a means for heat spreading through the copper plane associated within the PCB (GND layer). This concept could provide a thermal resistance from junction to ambient, $R_{\theta JA}$, of 70°C/W if implemented correctly.

Hence, maximum power dissipation allowable for an operating ambient temperature of 70°C, and a maximum junction temperature of 150°C is determined as:

$$P_J = (T_J - T_A) \,/\, R_{\theta JA}$$

$$P_J = (150 - 70) \,/\, 50 = 1.6\ \text{W}$$

Using two square inches of dedicated copper plane on double-sided PCB,

$$P_J = (150 - 70) \,/\, 70 = 1.14\ \text{W}$$

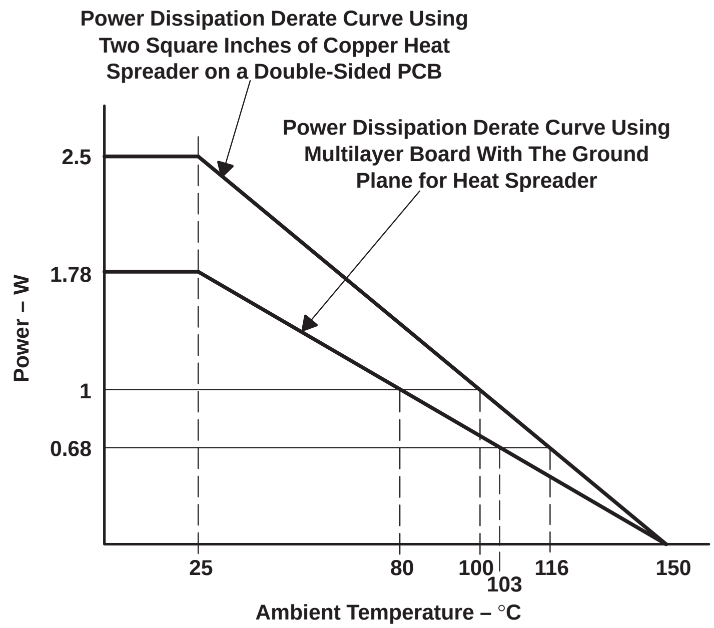
Using a multilayer board and utilizing the ground plane for heat spreading, worst case maximum power dissipation is determined by:

$$P_D = (5.5 - 3) \times 0.4 = 1\ \text{W}$$

Normal operating maximum power dissipation is (see Figure 1):

$$P_D = (5 - 3.3) \times 0.4 = 0.68\ \text{W}$$

THERMAL INFORMATION



NOTE: These curves are to be used for guideline purposes only. For a particular application, a more specific thermal characterization is required.

Figure 1. Power Dissipation Derating Curves

APPLICATION INFORMATION

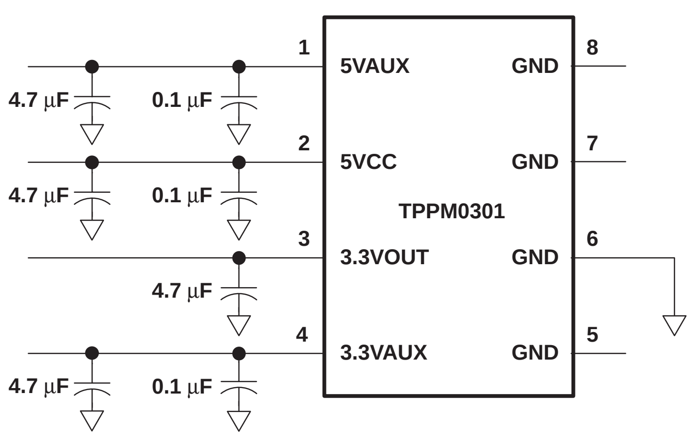
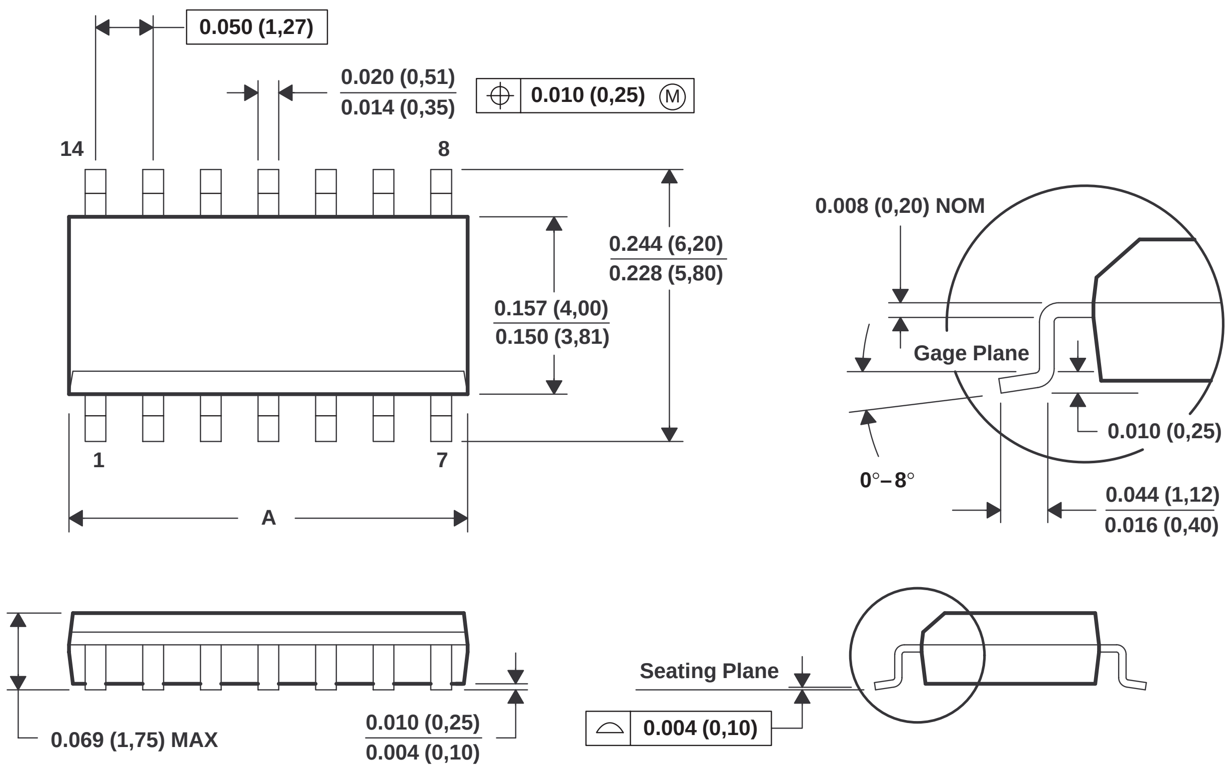


Figure 2. Typical Application Schematic

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPPM0301DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPPM0301DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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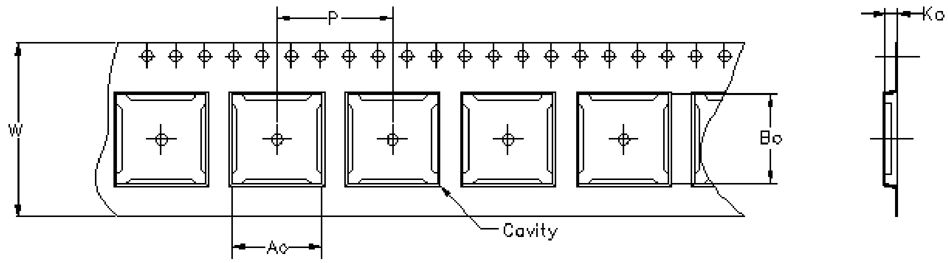
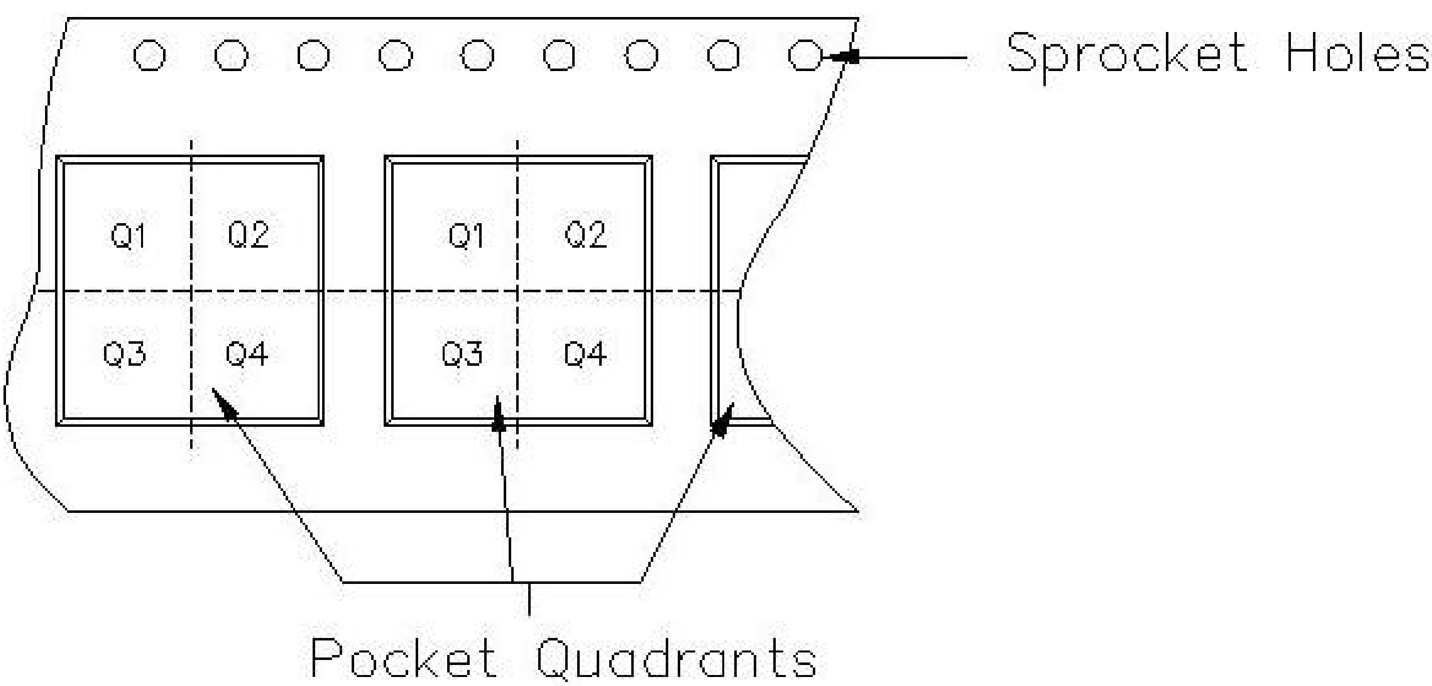


Carrier tape design is defined largely by the component lentgh, width, and thickness.

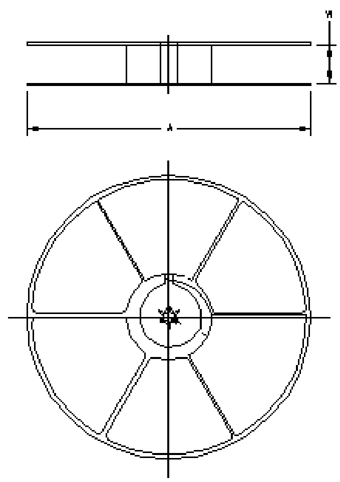
Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

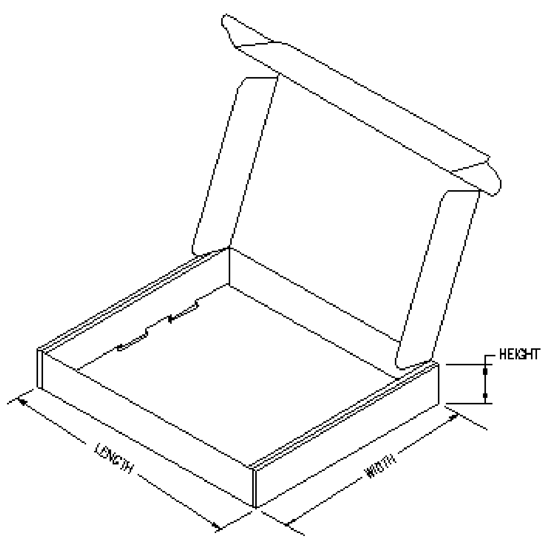
PACKAGE MATERIALS INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPPM0301DR	D	8	FMX	330	0	6.4	5.2	2.1	8	12	PKGORNT1TR-MSP

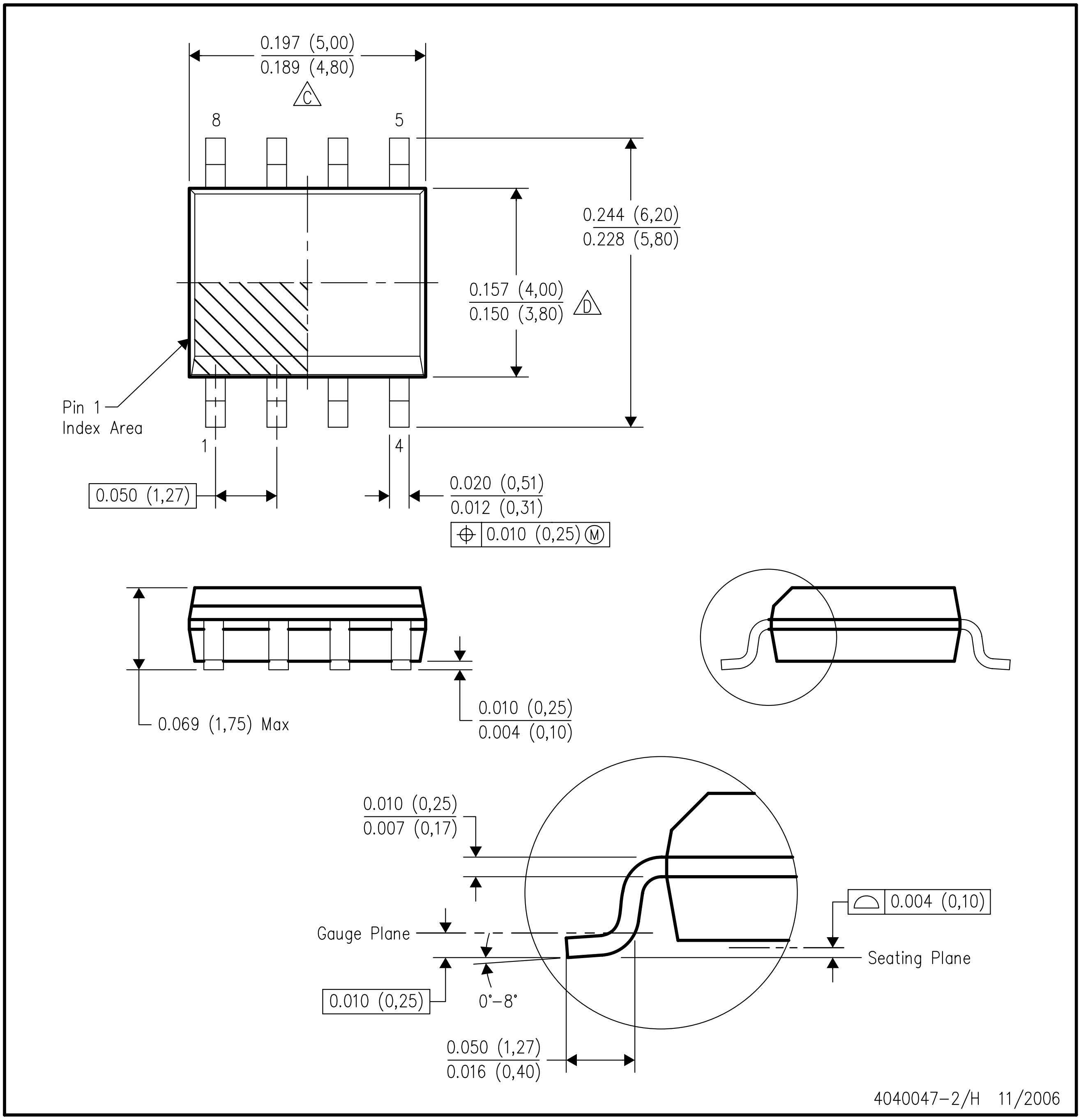


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPPM0301DR	D	8	FMX	342.9	336.6	20.6



D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

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