TPS40140
DUAL OR 2-PHASE, STACKABLE CONTROLLER
SLUS660A−SEPTEMBER 2005−REVISED JULY 2006

1 INTRODUCTION

1.1 FEATURES

- **VDD From 4.5 V to 15 V, With Internal 5-V Regulator**
- **V_{OUT} From 0.7 V to 5.8 V**
- **Converts From 15V Input to 0.7V Output at 1MHz**
- **Dual-Output or 2-Phase Interleaved Operation, Stackable to 16 Phases**
- **Supports Pre-Biased Outputs**
  Programmable Switching Frequency Up to 1 MHz/Phase
- **0.5% Internally Trimmed 0.7-V Reference**
- **10-μA Shutdown Current**
- **Current Mode Control with Forced Current Sharing**[1]
- **1V to 40V Power Stage Operation Range**
- **Power Sharing from Different Input Voltage Rails, (e.g. Master From 5 V, Slave From 12 V)**
- **True Remote Sensing Differential Amplifier**
- **Programmable Input Undervoltage Lockout**
- **Resistive or Inductor DCR Current Sensing**
- **Provide a 6-Bit Digitally-Controlled Output When Used With TPS40120**
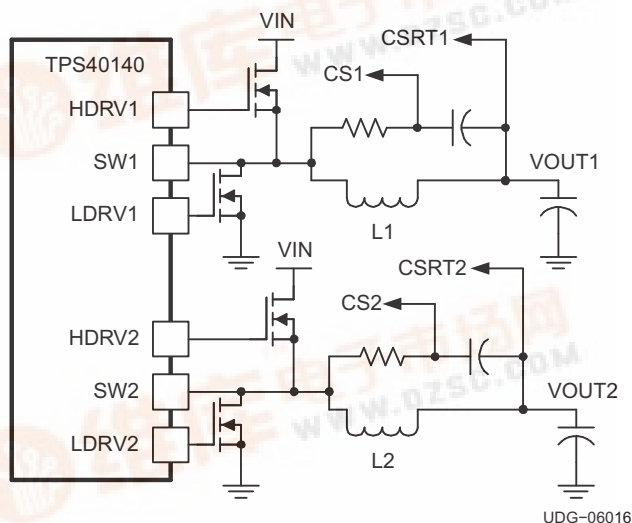- **36-pin QFN Package**

1.2 APPLICATIONS

- **Graphic Cards**
- **Internet Servers**
- **Networking Equipment**
- **Telecommunications Equipment**
- **DC Power Distributed Systems**

(1)   Patents Pending

UDG−06016

1.3 DESCRIPTION

The TPS40140 is a multifunctional synchronous buck controller that can be configured to provide either a single-output two-phase power supply or a power supply that supports two independent outputs. Several TPS40140 controllers can be stacked up to a 16-phase multiphase single output power supply. Alternatively, several controllers providing multiple independent outputs can be synchronized in an interleaving pattern for improved input ripple current.

The TPS40140 is capable of converting from a 15-V input to a 0.7-V output at 1MHz.

Each phase operates at a switching frequency of up to 1 MHz. The two phases in one device operate 180° out-of-phase. In a multiple device stackable configuration, the phase shift of the slaves, relative to a master, is programmable.

1.4 ORDERING INFORMATION

PACKAGE	TAPE AND REEL QTY.	PART NUMBER
Plastic Quad Flatpack 36-pin RHH (PQFP)	250	TPS40140RHHT
	3000	TPS40140RHHR

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Contents

2 DEVICE RATINGS

2.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage range	VDD, UVLO_CE1, UVLO_CE2	−0.3 to 16	V
	SW1, SW2	−1 to 44	
	SW1, SW2, transient < 50ns	−5	
	BOOT1, BOOT2, HDRV1, HDRV2	V_{SW} + 6.0	
All other pins		−0.3 to 6.0	
Output current	RT	200	μA
Junction Temperature, T_J	Operating	−40 to 125	°C
Junction Temperature, T_J	Storage	−55 to 150	°C

2.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage	VDD, UVLO_CE1, UVLO_CE1	−0.3		15	V
	SW1, SW2	−1		40	
	BOOT1, BOOT2, HDRV1, HDRV2		V_{SW}+5.5		
	All other pins	−0.3		5.5	
Maximum output current	RT			25	μA
Operating free-air temperature		−40		85	°C

2.3 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	MIN	TYP	MAX	UNIT
Human body model		3000		V
CDM		1500		V

2.4 PACKAGE DISSIPATION RATINGS[1]

THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
48	2	0.8

(1) For more information on the RHH package and the test method, refer to TI technical brief, literature number SLUA271.

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2.5 ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, (unless otherwise noted), V_{VDD} = 7 V, V_{BP5} = 5 V, UVLO_CE1, UCLO_CE2: 10 kΩ, Pullup to BP5, f_{SW} = 300 kHz, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT SUPPLY						
	Operating Voltage Range		4.5	12	15	V
	Shutdown Current	UVLO_CE1 = UVLO_CE2 =GND		1	10	µA
BP5 INPUT SUPPLY						
	Operating Voltage Range		4.5	5.0	5.5	V
	BP5 Operating Current		2	3	5	mA
	Rising BP5 Turn-On		4.0	4.25	4.45	V
	BP5 Turn-Off Hysteresis		100	220	400	mV
	Standby Mode Current[1]	UVLO_CEx =1.7V		2.8		mA
VREG						
		7 V < V_{DD} <15 V	4.5	5.1	5.5	V
		Output current	0		100	mA
OSCILLATOR, RT						
	Phase Frequency Accuracy	R_{RT}= 110 kΩ		300		kHz
	Phase Frequency Set Range		150		1000	kHz
	RT[1]	25 kΩ≤ R_{RT}≤ 500 kΩ		0.7		V
UNDERVOLTAGE LOCKOUT (UVLO_CE1, UVLO_CE2)						
	Enable threshold, standby mode	Internal 5VREG regulator enabled	0.5	1.0	1.5	V
	UVLO threshold	PWM Switching enabled	1.9	2	2.1	V
	UVLO hysteresis	At the UVLO_CEx pin		40		mV
	UVLO_CE1, UVLO_CE2 bias current[1]				1	µA
PWM						
D	Maximum duty cycle per channel[1]	2-phase, 4-phase, 8-phase or 16-phase		87.5%		
		3-phase, 6-phase, or 12-phase		83.3%		
VSHARE						
		I_{VSHR} = 0	1.785	1.8	1.815	V
	[1]	-30µA<i_{VSHR} < 50µA	1.785	1.8	1.815	V
ERROR AMPLIFIER CH1, ERROR AMPLIFIER CH2						
	Input Common Mode Range[1]		0	0.7	2.0	V
	Input Bias Current[1]	V_{FB} = 0.7 V		10		nA
	FBx Voltage[1]		0.6965	0.700	0.7035	V
	Output Source Current	V_{COMP} = 1.1 V, V_{FB} = 0.6 V	1	2		mA
	Output Sink Current	V_{COMP} = 1.1V, V_{FB} = BP5	1	2		mA
	BW[1]		8	12		MHz
	Open Loop Gain[1]		60	90		dB
VOLTAGE TRACKING (TRK1, TRK2)						
	SS source current	After EN, before PWM and during hiccup mode	5	6.0	7.3	µA
		After first PWM pulse	10	12.5	15	µA
	Fault Enable Threshold[1]			1.4		V
	Internal Clamp Voltage[1]			2.4		V
	SS sink resistance[1]	Pull-down resistance			1	kΩ

(1) Ensured by design. Not 100% production tested.

ELECTRICAL CHARACTERISTICS *(continued)*

T_J = –40°C to 85°C, (unless otherwise noted), V_{VDD} = 7 V, V_{BP5} = 5 V, UVLO_CE1, UCLO_CE2: 10 kΩ, Pullup to BP5, f_{SW} = 300 kHz, unless otherwise noted

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE AMPLIFIERS (CS1, CS2)						
	Differential input voltage		-60		60	mV
	Input offset voltage	CS1, CS2, Trimmed	-2.0	0	2.0	mV
Ac	Gain transfer to PWM COMP	5 mV < V_{CS} < 60 mV, V_{CSRT} = 1.5 V	12	13	14	V/V
	Input common mode[1]		0		5.8	V
CSA	Input bias current			100		nA
DIFFERENTIAL AMPLIFIER (DIFFO)						
	Gain	1.0 V < V_{OUT} < 5.8 V	0.997	1	1.003	V/V
	Input Common Mode Range[1]		0		5.8	V
	Output Source Current[1]	V_{OUT}– V_{VGSNS} = 2 V, V_{DIFFO} > 1.98 V, VDD-V_{OUT} > 2 V			2	
	Output Source Current[1]	V_{OUT}– V_{VGSNS} = 2 V, V_{DIFFO} > 2.02 V VDD-V_{OUT} =1 V			1	mA
	Output Sink Current[1]	V_{OUT}– V_{VGSNS} = 2 V, V_{DIFFO} > 2.02 V			2	
	Unity gain bandwidth[1]		5	8		MHz
	Input Impedance, non inverting[1]	V_{OUT} to GND		60		kΩ
	Input Impedance, inverting[1]	GSNS to DIFFO		60		
GATE DRIVERS						
	HDRV1, HDRV2 Source On Resistance	V_{BOOT1}, V_{BOOT2} = 5 V, V_{SW1} = V_{SW2} = 0 V, Sourcing 100 mA	1	2	3	
	HDRV1, HDRV2 Sink On Resistance	V_{VREG} = 5 V, V_{SW1} = V_{SW2} = 0 V, Sinking 100 mA	0.5	1.2	2	
	LDRV1, LDRV2 Source On Resistance	V_{VREG} = 5 V, V_{SW1} = V_{SW2} = 0 V, Sourcing 100 mA	1	2	3	Ω
	LDRV1, LDRV2 Sink On Resistance	V_{VREG} = 5V, V_{SW1} = V_{SW2} = 0 V, Sinking 100 mA	0.3	0.65	1	
t_{RISE}	HDRVx rise time[1]	C_{LOAD}= 3.3 nF		25	75	
t_{FALL}	HDRVx fall time[1]	C_{LOAD}= 3.3nF		25	75	
t_{RISE}	LDRVx rise time[1]	C_{LOAD}= 3.3nF		25	75	ns
t_{FALL}	LDRVx fall time[1]	C_{LOAD}= 3.3nF		20	60	
	Minimum Controllable On-Time	C_{LOAD}= 3.3nF		50		
OUTPUT UNDERVOLTAGE FAULT						
		V_{FB} relative to V_{REF}	-19%	-16.5%	-14%	
	Undervoltage delay[1]			3		µs
CURRENT LIMIT						
I_{ILIM}	Output current		18.8	20	21.2	µA
POWER GOOD						
	PGOOD transition low threshold	V_{FB} rising relative to V_{REF}	10%	12.5%	15%	
	PGOOD transition low threshold	V_{FB} falling relative to V_{REF}	-15%	-12.5%	-10%	
	PGOOD trip hysteresis		2%		5%	
	PGOOD Delay[1]			10		µs
	Low level output voltage, VOL	I_{PGOOD} = 4 mA		0.35	0.4	V
	PGOOD Bias Current	V_{PGOOD}= 5.0 V	-2	1	2	µA

(1) Ensured by design. Not 100% production tested.

ELECTRICAL CHARACTERISTICS *(continued)*

T_J = −40°C to 85°C, (unless otherwise noted), V_{VDD} = 7 V, V_{BP5} = 5 V, UVLO_CE1, UCLO_CE2: 10 kΩ, Pullup to BP5, f_{SW} = 300 kHz, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP					
Ramp Amplitude[1]		0.421	0.5	0.526	V
VIN BALANCE					
V_{IN} Balance Gain, A_{VB}		0.23	0.25	0.27	V/V
THERMAL SHUTDOWN					
Shutdown Temperature[1]			155		°C
Hysteresis[1]			30		
DIGITAL CLOCK SIGNAL (CLKIO)					
Pull-up resistance[1]	I_{OH} = 5 mA		27		Ω
Pull-down resistance[1]	I_{OL} = 10 mA		27		Ω
Output leakage[1]	Three-state			1	μA

(1) Ensured by design. Not 100% production tested.

3 TYPICAL CHARACTERISTICS

BP5 TURNOFF HYSTERESIS VOLTAGE
vs
TEMPERATURE

Figure 3-1.

BP5 TURNON THRESHOLD VOLTAGE
vs
TEMPERATURE

Figure 3-2.

CURRENT SENSE GAIN
vs
TEMPERATURE

Figure 3-3.

OSCILLATOR FREQUENCY
vs
TEMPERATURE

Figure 3-4.

DIFFERENTIAL AMPLIFIER VOLTAGE GAIN
vs
TEMPERATURE

Figure 3-5.

BP5 CURRENT
vs
TEMPERATURE

Figure 3-6.

SHUTDOWN QUIESCENT CURRENT
vs
TEMPERATURE

Figure 3-7.

TRKx SOFT START CURRENT
vs
TEMPERATURE

Figure 3-8.

DIFFERENTIAL AMPLIFIER INPUT OFFSET VOLTAGE
vs
TEMPERATURE

Figure 3-9.

HDRV SOURCE AND SINK RESISTANCE
vs
TEMPERATURE

Figure 3-10.

LDRV SINK RESISTANCE
vs
TEMPERATURE

Figure 3-11.

FEEDBACK VOLTAGE
vs
TEMPERATURE

Figure 3-12.

V_{REG} OUTPUT VOLTAGE
vs
TEMPERATURE

Figure 3-13.

V_{SHARE} VOLTAGE
vs
TEMPERATURE

Figure 3-14.

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**UVLO_CEx THRESHOLD VOLTAGE
vs
TEMPERATURE**

Figure 3-15.

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4 DEVICE INFORMATION

4.1 TERMINAL CONFIGURATION

The package is an 36-pin PQFP (RHH) package. Note: The thermal pad is an electrical ground connection.

RHH PACKAGE
(TOP VIEW)

The TPS40140 is a versatile controller that can operate as a single controller or 'stacked' in a multi-controller configuration. A TPS40140 has two channels that may be configured as a multi-phase (single output) or as a dual, with two independent output voltages. The two channels of a single controller always switch 180 degrees out of phase. See below for further discussion on the Clock and Voltage Master and Clock and Voltage Slave.

Some pins are used to set the operating mode, and other pins' definition change based on the mode selected.

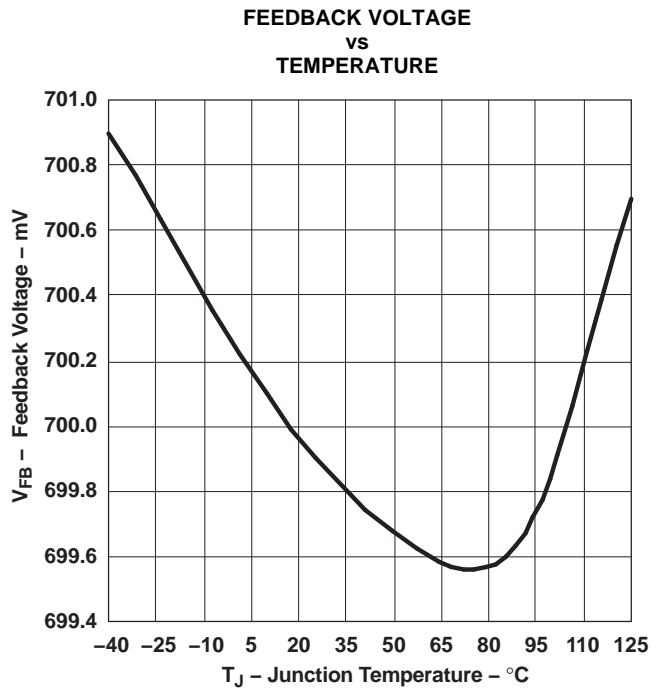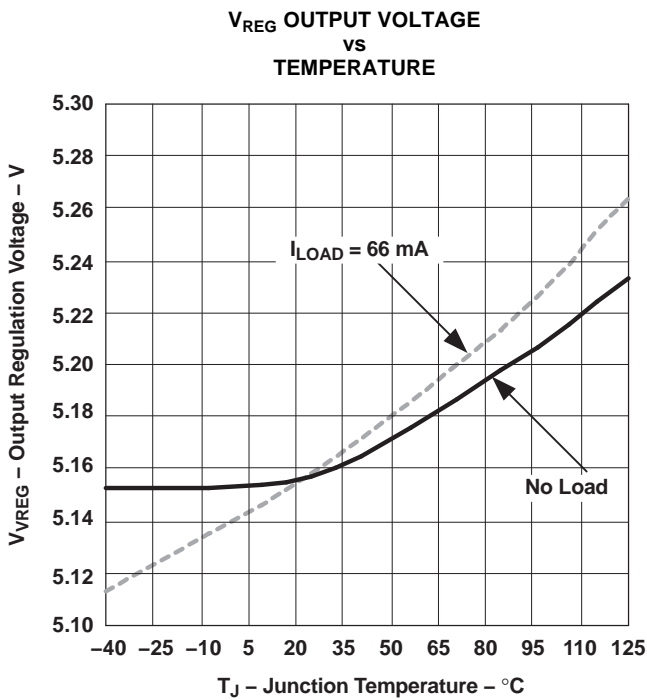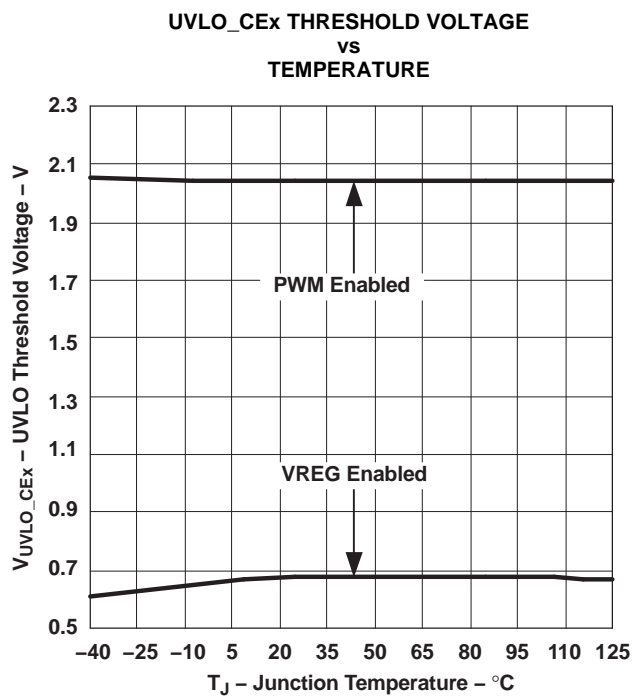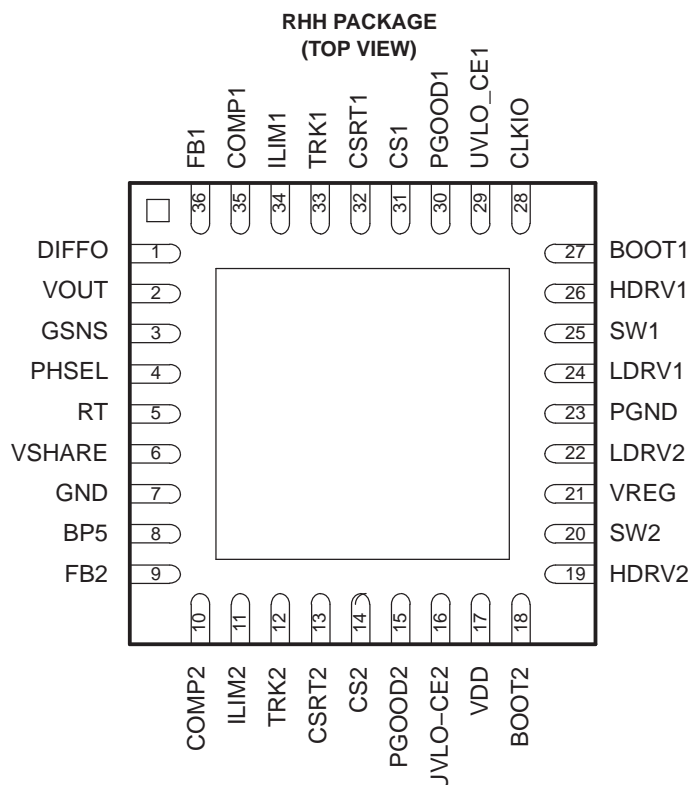It is often necessary to refer to a pin or pins that are used in CH1 and/or CH2. The short cut nomenclature used is the pin name with a lower case 'x' to mean either or both channels. For example, TRKx refers to TRK1 and/or TRK2.

4.2 CLOCK MASTER AND CLOCK SLAVE

A controller may function as a 'Clock Master' or a 'Clock Slave'. The term ' Clock Master' designates the controller, in a multi-controller configuration, that generates the CLKIO signal for clock synchronization between the Clock Master and the Clock Slaves. The CLKIO signal is generated when the 'RT' pin of the Clock Master is terminated with a resistor to ground and the PHSEL pin of the Clock Master is terminated with a resistor, or resistor string, to ground. The 'Clock Slave' is configured by connecting the RT pin to BP5. Then the Clock Slave receives the CLKIO signal from the Clock Master. The phasing of the Slave is accomplished with a resistor string tied to the PHSEL pin. More information is covered in the *CLOCK MASTER, PHSEL AND CLKIO CONFIGURATIONS* section.

4.3 VOLTAGE MASTER AND VOLTAGE SLAVE

A Voltage Master has the channel that monitors the output voltage and generates the 'COMP' signal for voltage regulation. A Voltage Slave channel is configured by connecting the TRKx pin to BP5. Then the COMP signal from the Master is connected to the COMPx pin on the Voltage Slave. When the TRKx pin is connected to BP5 the COMPx output for that channel is put in a high impedance state, allowing the regulation for that channel to be controlled by the Voltage Master COMP signal.

4.3.1 TERMINAL FUNCTIONS

Table 4-1. TERMINAL FUNCTIONS

| TERMINAL NAME	NO.	I/O	DESCRIPTION
BP5	8	O	Filtered input from the VREG pin. A 10-Ω resistor should be connected between VREG and BP5 and a 1.0-µF ceramic capacitor should be connected from BP5 to ground.
GND	7	-	Low noise ground connection to the device.
BOOT1	27	I	BOOT1 provides a bootstrapped supply for the high side FET driver for PWM1, enabling the gate of the high side FET to be driven above the input supply rail. Connect a capacitor from BOOT1 to SW1 pin and a Schottky diode from this pin to VREG.
BOOT2	18	I	BOOT2 provides a bootstrapped supply for the high side FET driver for PWM2, enabling the gate of the high side FET to be driven above the input supply rail. Connect a capacitor from BOOT2 to SW2 pin and a Schottky diode from this pin to VREG.
CLKIO	28	O	Digital clock signal for synchronizing slave controllers to the master CLKIO frequency and is either 6 or 8 times the PWM switching frequency.
COMP1	35	O	Output of the error amplifier, CH1. The voltage at this pin determines the duty cycle for the PWM1.
COMP2	10	O	Output of the error amplifier, CH2. The voltage at this pin determines the duty cycle for the PWM2.
CS1	31	I	These pins are used to sense the CH1 phase current. Inductor current can be sensed with an external current sense resistor or by using an external R-C circuit and the inductor's DC resistance. The traces for these signals must be connected directly at the current sense element.
CS2	14	I	These pins are used to sense the CH2 phase current. Inductor current can be sensed with an external current sense resistor or by using an external R-C circuit and the inductor's DC resistance. The traces for these signals must be connected directly at the current sense element.
CSRT1	32	O	Return point of CH1 current sense voltage. The trace for this signal must be connected directly at the current sense element.
CSRT2	13	O	Return point of CH1 current sense voltage. The trace for this signal must be connected directly at the current sense element.
DIFFO	1	O	Output of the differential amplifier. The output voltage of the differential amplifier is limited to 5.8 V. For remote sensing, the voltage at this pin represents the true output voltage without I × R drops that result from high current in the PCB traces. The VOUT and GSNS pins must be connected directly at the point of load where regulation is required. See *Layout Guidelines* for more information.
FB1	36	I	Inverting input of the error amplifier for CH1. In closed loop operation, the voltage at this pin is nominally 700 mV. This pin is also monitored for PGOOD1 and undervoltage on CH1.
FB2	9	I	Inverting input of the error amplifier for CH2. In closed loop operation, the voltage at this pin is nominally 700 mV. This pin is also monitored for PGOOD2 and undervoltage on CH2.
GSNS	3	I	Inverting input of the differential amplifier. This pin should be connected to ground at the load. If the differential amplifier is not used, tie this pin to GND or leave open.
HDRV1	26	O	Gate drive output for the high side N-channel MOSFET switch for CH1. Output is referenced to SW1 and is bootstrapped for enhancement of the high side switch.
HRDV2	19	O	Gate drive output for the high side N-channel MOSFET switch for CH2. Output is referenced to SW2 and is bootstrapped for enhancement of the high side switch.
ILIM1	34	I	Used to set the cycle-by-cycle current limit threshold for CH1. If the ILIM1 threshold is reached, the PWM pulse is terminated and the converter delivers limited current to the output.
ILIM2	11	I	Used to set the cycle-by-cycle current limit threshold for CH2. If the ILIM2 threshold is reached, the PWM pulse is terminated and the converter delivers limited current to the output.
LRDV1	24	O	Gate drive output for the low side synchronous rectifier (SR) N-channel MOSFET for CH1.
LRDV2	22	O	Gate drive output for the low side synchronous rectifier (SR) N-channel MOSFET for CH2.

Table 4-1. TERMINAL FUNCTIONS (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
PGOOD1	30	O	Power good indicators for CH1 output voltage. This open-drain output connects to a voltage via an external resistor
PGOOD2	15	O	Power good indicators for CH2 output voltage. This open-drain output connects to a voltage via an external resistor
PGND	23	-	Power ground reference for the controller lower gate drivers. There should be a high current return path from the sources of the lower MOSFETs to this pin.
PHSEL	4	O	A 20μA current flows from this pin. In a single controller design, this pin should be grounded. In a multi controller configuration, a 39- kΩ resistor string sets the voltage on this pin determines the proper phasing for the slaves. See the section on ' *CLOCK MASTER, PHSEL AND CLKIO CONFIGURATIONS'*
VREG	21	O	The output of the internal 5-V regulator. A 4.7-μF ceramic capacitor should be connected from this pin to PGND.
RT	6	I	Connecting a resistor from this pin to ground sets the oscillator frequency.
SW1	25	I	Connect to the switched node on converter CH1. It is the return for the CH 1 upper gate driver. There should be a high current return path from the source of the upper MOSFET to this pin. This pin is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
SW2	20	I	Connect to the switched node on converter CH2. It is the return for the CH 2 upper gate driver. There should be a high current return path from the source of the upper MOSFET to this pin. This pin is also used by the adaptive gate drive circuits to minimize the dead time between upper and lower MOSFET conduction.
TRK1	33	O	This is an input to the non-inverting input of the error amplifier CH1. This pin is normally connected to the soft-start capacitor or to another voltage that is tracked.
TRK2	12	O	This is an input to the non-inverting input of the error amplifier CH2. This pin is normally connected to the soft-start capacitor or to another voltage that is tracked.
UVLO_CE1	29	I	A voltage divider from V_{IN} to this pin determines the input voltage that CH1 starts. When the voltage is between 0.5 V and 1.5 V the VREG regulator is enabled . When the voltage is 2.1 V or above CH1 soft start is allowed to begin.
UVLO_CE2	16	I	A voltage divider from V_{IN} to this pin determines the input voltage that CH2 starts. When the voltage is between 0.5 V and 1.5 V the VREG regulator is enabled . When the voltage is 2.1 V or above CH2 soft start is allowed to begin.
VDD	17	I	Power input for the controller 5V regulator and differential amplifier. A 1.0-μF ceramic capacitor should be connected from this pin to ground.
VOUT	2	I	Non-inverting input of the differential amplifier. This pin should be connected to the output of the converter close to the load point. If the differential amplifier is not used, leave this pin open.
VSHARE	6	O	The 1.8 V reference output.

4.4 FUNCTIONAL BLOCK DIAGRAM
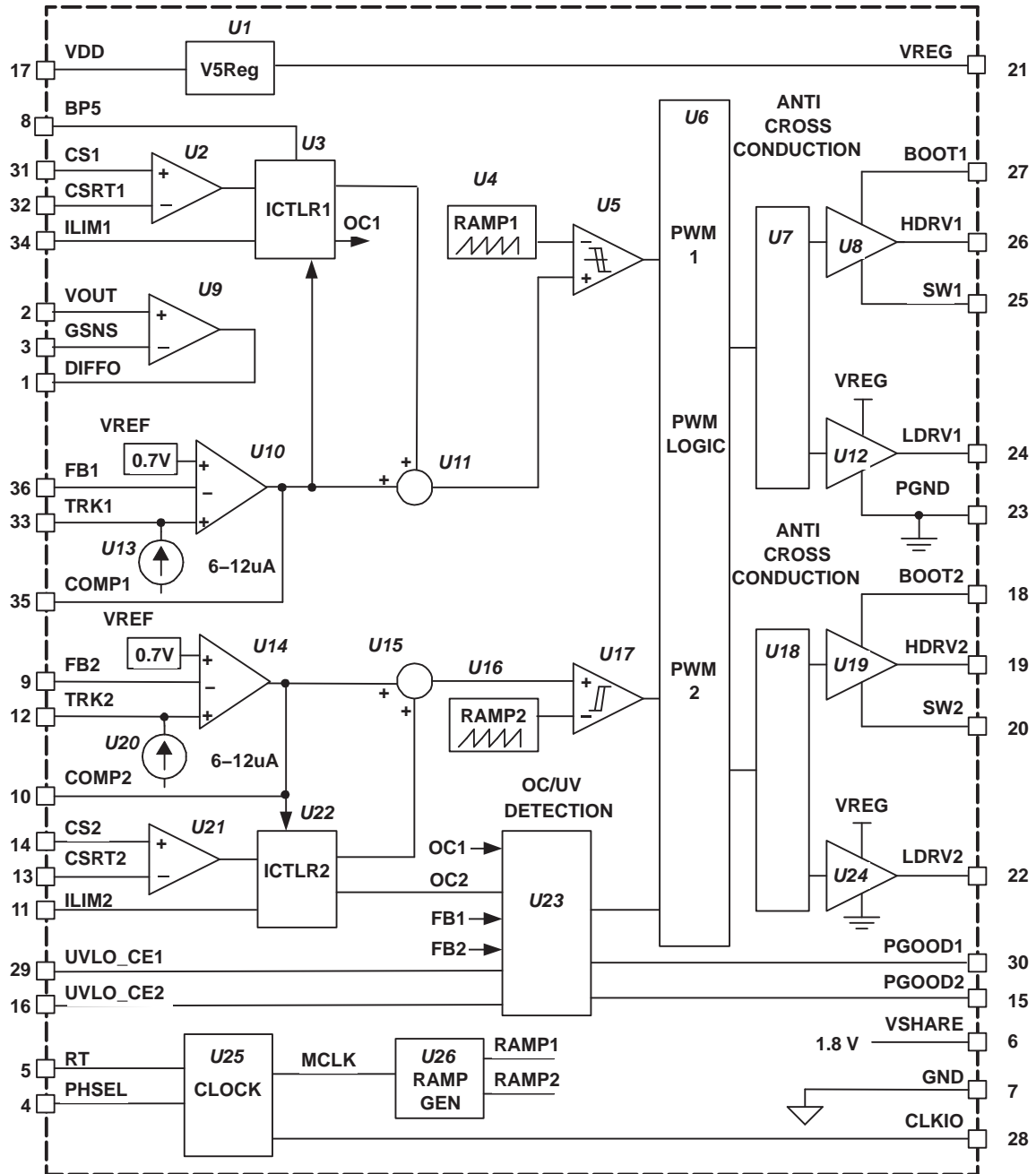
5 APPLICATION INFORMATION

5.1 FUNCTIONAL DESCRIPTION

The TPS40140 operates with a programmable fixed switching frequency. It is a current feedback controller with forced phase current balancing. When compared to voltage mode control, the current feedback controller results in a simplified feedback network and reduced input line sensitivity. Phase current is sensed by using either the DCR (direct current resistance) of the filter inductors or current sense resistors installed in series with the output. See the section on *INDUCTOR DCR CURRENT SENSE*. The current signal is then amplified and superimposed on the amplified voltage error signal to provide current mode PWM control.

Other features include programmable input Under Voltage Lock Out (UVLO), differential input amplifier for precise output regulation, user programmable operation frequency, programmable pulse-by-pulse overcurrent protection, output under-voltage shutdown and re-start, capacitor to set soft-start time and power good indicators.

5.2 DATA SHEET ORGANIZATION

The Application Information is partitioned into sections to facilitate applying the TPS40140 in various modes and configurations. The first sections describe functions that are used in all configurations. The following sections are specific to the configuration (i.e., single controller, multiple controllers, Master and Slave).

5.3 TYPICAL START UP SEQUENCE

Figure 5-1 shows a typical start up with the VDD applied to the controller and then the UVLO-CEx being enabled. Shut down occurs when the VDD is removed.
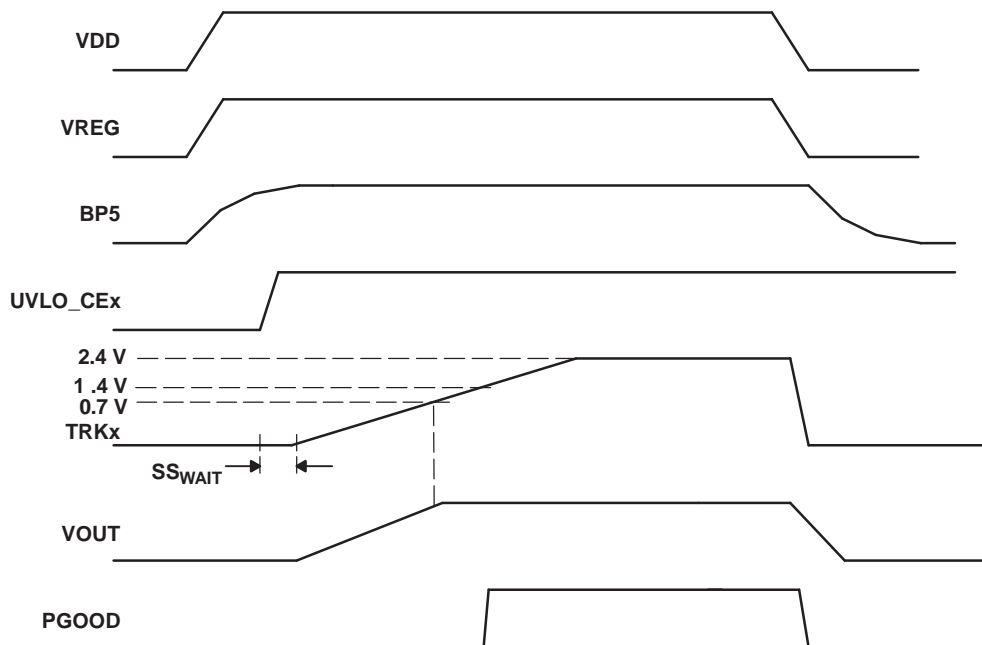

Figure 5-1. Typical Start Up and Shut Down Sequence

5.4 TRACK (SOFT-START WITHOUT PRE-BIASED OUTPUT)

A capacitor connected to the TRKx pins sets the power-up time. When UVLO_CEx is high and the internal power-on reset (POR) is cleared, the calibrated current source, starts charging the external soft start capacitor with 12-μA. The PGOOD pin is held low during the start up. The rising voltage across the capacitor serves as a reference for the error amplifier, U10 and U14. When the soft start voltage reaches the level of the reference voltage, V_{REF} = 0.7 V, the converter's output reaches the regulation point and further voltage rise of the soft-start voltage has no effect on the output. When the soft start voltage reaches 1.4 V, the powergood (PGOOD) function is cleared to be reported on the PGOOD pin. Normally the PGOOD pin goes high at this time. Equation 1 is used to calculate the value of the soft-start capacitor. Css is in Farads and Tss is given in seconds.

$$T_{SS} = C_{SS} \times 58 \times 10^3$$

(1)

5.5 SOFT-START WITH PRE-BIASED OUTPUTS

For pre-biased outputs the TPS40140 uses two levels of soft-start current that charge the soft-start capacitor connected to the TRKx pin(s). PWM switching begins when the TRKx voltage rises to the voltage present on the FBx pin. When the first PWM pulse occurs, the charging current is increased to 12 μA. Figure 5-2 shows the typical waveforms present on the TRACKx pin and the output voltage, VOUT when VOUT is pre-biased. TRKx rises due to the 6μA current, until at T1 the voltage on TRKx equals the pre-biased voltage on the FBx pin, at time t1. At this time the soft-start current is increased to 12 μA and TRKx rises with an increase in it's slope. When TRKx reaches 0.7 V, at time t2, the output should be in regulation. The voltage on the TRKx pin continues to rise. When the TRKx voltage is 1.4 V, at time t3, the PGOODx signal is enabled. The TRKx voltage continues to rise to 2.4 V where is is clamped internally. This approach provides for an accurate detection of the threshold where FBx = TRKx. Figure 5-3 is a block diagram of the implementation. The calculation for the soft start time, due to pre-bias, includes the time from t0 to t1, plus the time from t1 to t2, as shown in Equation 2 through Equation 4.

$$t1 = \frac{C_{SS}}{6 \ \mu A} \times \left(\frac{V_{OUT} \times R_{BIAS}}{R1 + R_{BIAS}} \right)$$

(2)

$$t2 = \frac{C_{SS}}{12 \ \mu A} \times \left(0.7 \ V - \left(\frac{V_{OUT} \times R_{BIAS}}{R1 + R_{BIAS}} \right) \right)$$

(3)

where
- Css is in Farads
- Tss is in seconds

$$T_{SS} = t1 + t2$$

(4)

If there is no pre-bias (V_{OUT} = 0 V), the equation reduces to case without pre-bias.
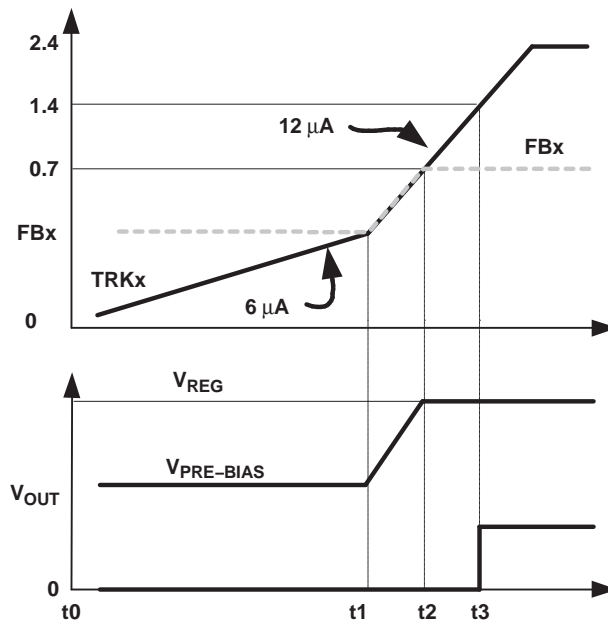
Figure 5-2. Soft-Start with PreBiased Output Waveforms
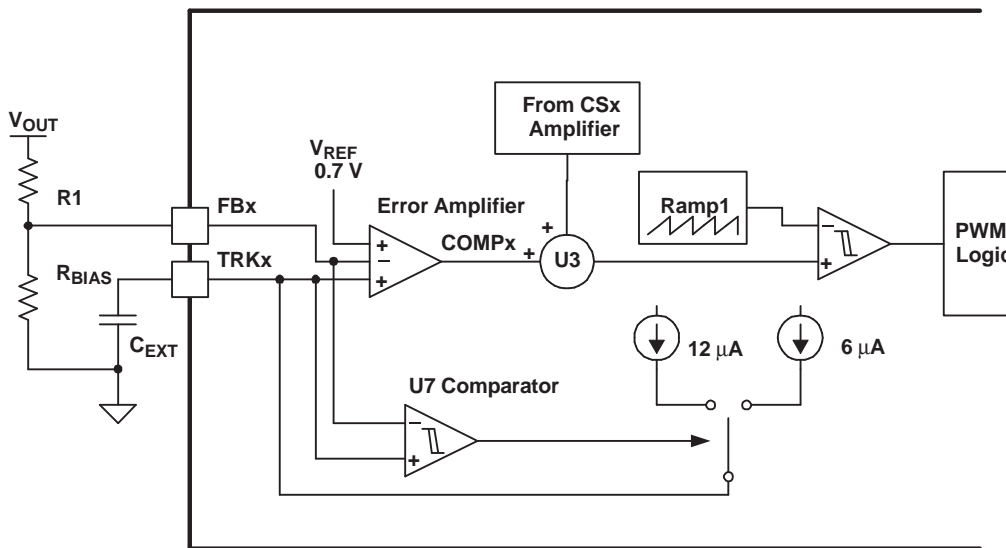
Figure 5-3. Implementation of PreBiased Output

DESIGN HINT: If the pre-biased is greater than the regulation voltage, the controller does not start. This is a condition of an overvoltage being applied before the controller starts PWM switching.

5.6 TRACK FUNCTION IN CONFIGURING A SLAVE CHANNEL

The TRACKx pin is internally clamped to 2.4 V. To configure a channel as a Slave, the TRACKx pin is pulled up externally to 5 V. This configures the output of the error amplifier, COMPx, for that channel to be a high impedance, allowing the Master COMP signal to control the Slave channel.

5.7 DIFFERENTIAL AMPLIFER, U9

The unity gain differential amplifier has high bandwidth to achieve improved regulation at user defined point of load and ease layout constrains. The output voltage is sensed between the VOUT and GSNS pins. The output voltage programming divider is connected to the output of the amplifier, the DIFFO pin.
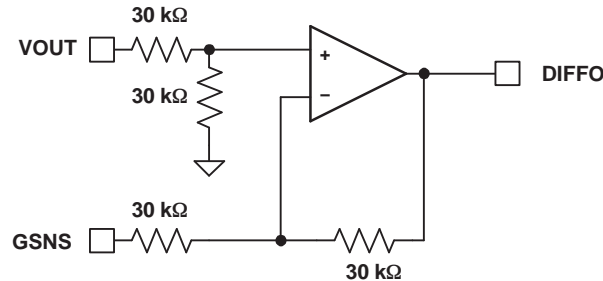
Figure 5-4. Differential Amplifier Configuration

DESIGN HINT: Because of the resistor configuration of the differential amplifier, the input impedance must be kept very low or errors result in setting the output voltage.

5.8 POWER GOOD

The PGOOD1, PGOOD2 pins indicate when the inputs and output are within their specified ranges of operation. Also monitored are the UVLO_CE1, UVLO_CE2 and TRK1 and TRK2 pins. The PGOOD has a high impedance when indicating inputs and outputs are within specified limits and is pulled low to indicate an out of limits condition. The PGOOD signal is held low until the respective TRK1 or TRK2 pin voltages exceed 1.4 V, then the undervoltage, overcurrent or overtemperature controls the state of PGOOD.

5.9 SETTING THE OUTPUT VOLTAGE

Two resistors, R1 and R_{BIAS} sets the output voltage as shown in Figure 5-5.
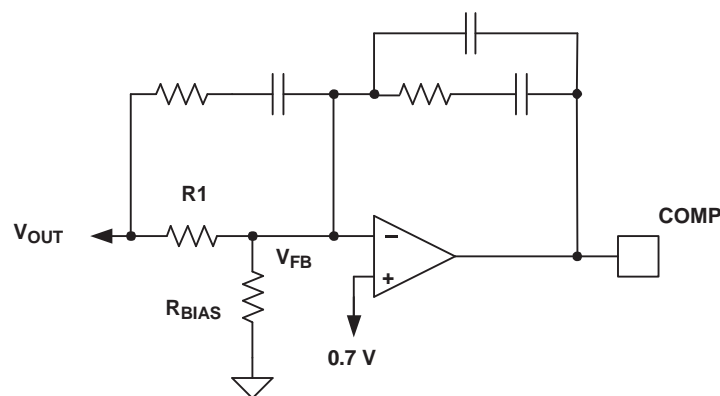
Figure 5-5. Setting the Output Voltage with R_{BIAS}

R_{BIAS} is calculated in Equation 5.

$$R_{BIAS} = 0.7 \times \left(\frac{R1}{\left(V_{OUT} - 0.7 \right)} \right)$$

(5)

5.10 PROGRAMMABLE INPUT UNDERVOLTAGE LOCK OUT PROTECTION

A voltage divider that sets 2 V on the UVLO_CEx pins determines when the controller begins to operate. The internal regulators are enabled when the voltage on the UVLO_CEx pins exceeds 1 V, but switching commences when the voltage is 2 V.

5.11 POWER ON RESET (POR)

The internal POR function ensures the VREG and BP5 voltages are within their regulation windows before the controller is allowed to start.

5.12 OVERCURRENT

The operation during an overcurrent condition is described in the '*Overcurrent Detection and Hiccup Mode*' section. In summary, when the controller detects 7 clock cycles of an overcurrent condition, the upper and lower MOSFETs are turned off and the controller enters a 'hiccup' mode'. After seven soft start cycles, normal switching is attempted. If the overcurrent has cleared, normal operation resumes, otherwise the sequence repeats.

5.13 OUTPUT UNDERVOLTAGE PROTECTION

If the output voltage, as sensed by U23 of the Functional Block Diagram on the FB pin becomes less than 0.588 V, the undervoltage protection threshold (84% of V_{REF}), the controller enters the hiccup mode as described in the *Overcurrent Detection and Hiccup Mode* section.

5.14 OUTPUT OVERVOLTAGE PROTECTION

Output overvoltage is defined as any voltage greater than the regulation level that appears on the output. Overvoltage protection is accomplished by the feedback loop monitoring the output voltage via the FB pin. If, during operation the output voltage experiences an overvoltage condition the FB pin voltage rises and the control loop turns the upper FET off and the lower FET is turned on until the output returns to set level. This puts the overvoltage channel in a *boost mode* configuration and tends to cause the input voltage to be *boosted* up.

If the output overvoltage condition exists prior to the controller PWM switching starting, i.e., no switching has commenced, the overvoltaged channel does not start PWM switching. This controller allows for operating with a pre-biased output. Since the output is greater than the regulation voltage, no PWM switching occurs.

DESIGN HINT: Care must be taken to insure there is sufficient load on the input voltage to prevent excessive boosting.

5.15 CLKFLT, CLKIO PIN FAULT

If the CLKIO signal is to be distributed from the Master to the Slave controllers, and is not there, the Slave controller enters a 'Standby' mode. The upper and lower MOSFETs are turned off but the internal 5-V regulator is still active and VREG is present. The CLKIO signal could be turned off at the Master controller or the connection to the Slave CLKIO input could be opened. If the CLKIO signal is restored, normal operation continues.

5.16 PHSEL PIN FAULT

The PHSEL pin is normally terminated with a resistor string, or tied directly to ground. If this string becomes open, the PHSEL pin voltage is pulled up internally to greater than 4V. The controller enters a 'Standby' mode. The upper and lower MOSFETs are turned off but the internal 5V regulator is still active and VREG is present. If the PHSEL connection is restored, normal operation continues after 64 PWM clock cycles.

5.17 OVERTEMPERATURE

If the temperature of the controller die is detected to be above 155°C, the upper and lower MOSFETs are turned off and the 5-V regulator, VREG, is turned off. When the die temperature decreases 30°C the controller performs a normal start up.

5.18 FAULT MASKING OPERATION

If the TRKx pin voltage is externally limited below the 1.4-V threshold, the controller does not respond to an Undervoltage fault and the PGOOD output remains low. Other fault modes remain operational. The overcurrent protection continues to terminate PWM cycle every time the threshold is exceeded, but the hiccup mode is not entered.

5.19 PROTECTION AND FAULT MODES

There are modes of normal operation during start up and shut down as well various fault modes that may be detected. It is often necessary to know the state of the upper and lower MOSFETs in these modes. Table xx shows a summary of these modes and the state of the MOSFETs. A description of each mode follows the table.

Table 5-1. Fault Mode Summary

MODE	UPPER MOSFET	LOWER MOSFET
PROGRAMMABLE UVLO_CEx = LOW	OFF	OFF
POWER ON RESET: FIXED UVLO, BP5 < 4.25V	OFF	OFF
OVERCURRENT	OFF, HICCUP MODE	OFF, HICCUP MODE
OUTPUT UNDERVOLTAGE	OFF, HICCUP MODE	OFF, HICCUP MODE
OUTPUT OVERVOLTAGE, PRIOR TO PWM SWITCHING	OFF	OFF
OUTPUT OVERVOLTAGE, WHILE PWM SWITCHING	PWM SWITCHING	PWM SWITCHING
CLKFLT, MISSING CLKIO AT SLAVE	OFF	OFF
PHSEL VOLTAGE > 4V, or open to ground	OFF	OFF
OVERTEMPERATURE	OFF	OFF

5.20 SETTING THE SWITCHING FREQUENCY

The clock frequency is programmed by the value of the timing resistor connected from the RT pin to ground. See Equation 6. This equation gives the frequency for an 8-phase system. For a 6-phase system the frequency is 1 1/3 times higher.

$$R = 1.33 \times \left(39.2 \times 10^3 \times f_{PH}^{-1.041} - 7 \right);$$

(6)

f_{PH} is a single phase frequency, kHz. The R_t resistor value is expressed in kΩ. See Figure 5-6.

PHASE FREQUENCY
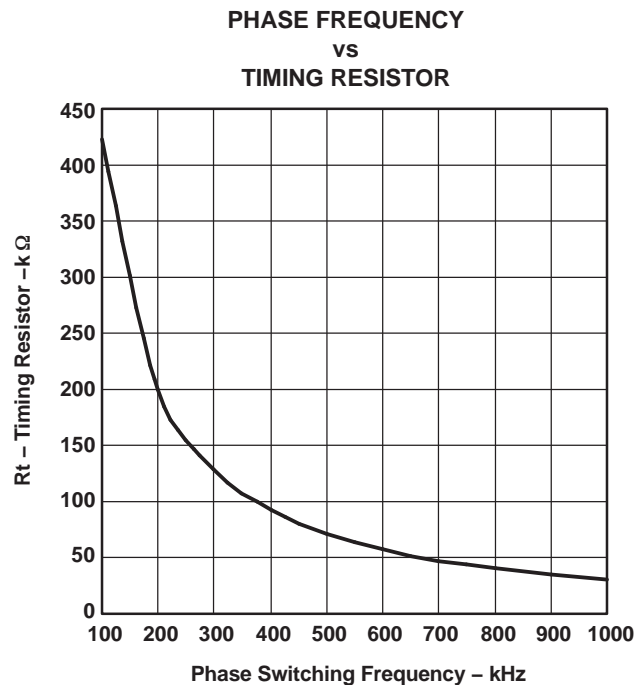**vs**
TIMING RESISTOR

Figure 5-6. Phase Switching Frequency vs R_T

5.21 SYNCHRONIZING A SINGLE CONTROLLER TO AN EXTERNAL CLOCK

The TPS40140 has the ability to synchronize a single controller to an external clock. The clock must be a pulse stream at 6 or 8 times the Master PWM frequency. See Figure 5-7.

Synchronizing the single controller to an external clock is similar to synchronizing a clock slave to a clock master. The single controller is put in clock slave mode by connecting the RT pin to BP5, disabling the internal clock generator. If the external CLKIO signal is a clock stream without any missing pulses, the master synchromizes to an arbitrary pulse so there is no determinant phase synchronization. Without a missing pulse, the PWM frequency will be 1/8 of the external clock. If the external CLKIO signal has a missing pulse every 6 cycles or 8 cycles, the controller synchronizes based on the missing pulse which would be in the 6th or 8th position. With the missing pulse, the phase synchronization of the master, to the missing pulse, can be controlled by the voltage on the PHSEL pin. See the section on *DIGITAL CLOCK SYNCHRONIZATION*. Phase shifting would also be desirable if more than one controller were to be synchronized to the same external clock.

Figure 5-7 shows a time slice of the two external clock possibilities and the resulting PWM signal. EXT CLK-A is the continuous clock with no missing pulse and the PWM-A signal could be frequency synchronized anywhere in the clock stream. The PWM signal is at 1/8 of the EXT CLK-A frequency. EXT CLK-S is the external clock stream with a missing pulse every 8 cycles. The phasing of the PWM-S is based on the voltage on the PHSEL pin. For PHSEL grounded, the PWM-S signal is shifted 90 degrees from what would be the falling edge of the missing pulse as shown.
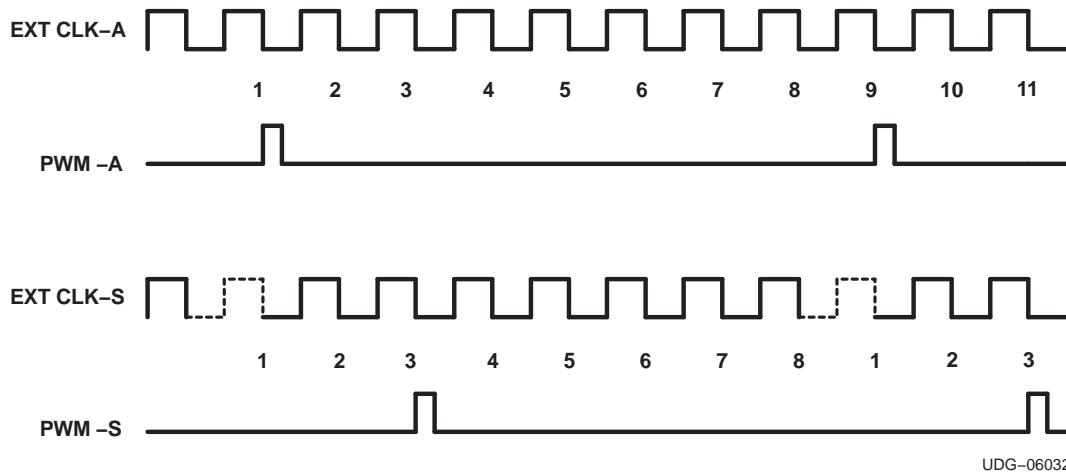
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Figure 5-7. Synchronizing a Single Controller to an External Clock

5.22 SPLIT INPUT VOLTAGE OPERATION

It may be advantageous to operate a master controller's power stages from V_{IN1}, different from the Slave controller(s) power stages, V_{IN2} where $V_{IN1} > V_{IN2}$. This enables the system designer to optimize the current taken from the system input voltages. In order to balance the output currents, a programmed offset is applied to ILIM2 of the slave controller(s). The voltage on this pin sets the offset current for channel 2.

The ramp offset is determined by a resistor, R_{SET}, connected to the ILIM2 pin of the slave, and is given by:

$$R_{SET} = V_{OUT}\left(\frac{1}{V_{IN2}} - \frac{1}{V_{IN1}}\right)100 \text{ k}\Omega$$

(7)

5.23 CURRENT SENSE

The current sensing and overcurrent detection architecture is shown in Figure 5-8.
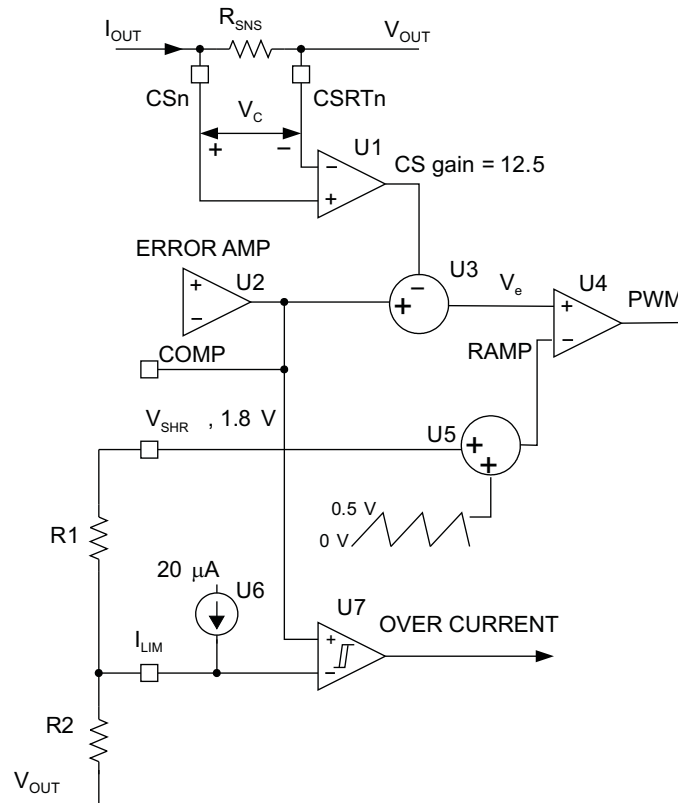
Figure 5-8. Output Current Sensing and OverCurrent Detection

The output current, I_{OUT}, flows through R_{SNS} and develops a voltage, V_C across it, representative of the output current. The voltage, V_C, could also be derived from an R-C network in parallel with the output inductor. This voltage is amplified with a gain of 12.5 and then subtracted from the Error Amp output, COMP, to generate the V_e voltage. The V_e signal is compared to the slope-compensation RAMP signal to generate the PWM for the modulator. As the output current is increased, the amplified V_C causes the V_e signal to decrease. In order to maintain the proper duty cycle (PWM), the COMP signal must increase. Therefore the magnitude of the COMP signal contains the output current information:

$$\text{COMP} = V_e + (I_{PEAK} \times R_{SNS}) \times 12.5$$

(8)

This is integral in the overcurrent detection as can be seen at comparator U7, comparing the I_{LIM} voltage with COMP. In order to have the proper duty cycle at PWM, V_e is:

$$V_e = \text{RAMP} \times \frac{V_{OUT}}{V_{IN}} + V_{SHR}$$

(9)

Combining equations:

$$\text{COMP} = \text{RAMP} \times \frac{V_{OUT}}{V_{IN}} + V_{SHR} + (I_{PEAK} \times R_{SNS}) \times 12.5$$

(10)

This equation for COMP shows the reason for resistors R1 and R2 being tied to V_{SHR} and V_{OUT} respectively.

5.24 CURRENT SENSING AND BALANCING

The controller employs peak current mode control scheme, thus naturally provides certain degree of current balancing. With current mode, the level of current feedback should comply with certain guidelines depending on duty factor known as "slope compensation" to avoid the sub-harmonic instability. This requirement can prohibit achieving a higher degree of phase current balance. To avoid the controversy, a separate current loop that forces phase currents to match is added to the proprietary control scheme. This effectively provides high degree of current sharing independent of the controller's small signal response and is implemented in U3 and U22, ICTLR.

High bandwidth current amplifiers, U2 and U21 can accept as an input voltage either the voltage drop across dedicated precise current sense resistors, or inductor's DCR voltage derived by an RC network, or thermally compensated voltage derived from the inductor's DCR. The wide range of current sense arrangements ease the cost/complexity constrains and provides superior performance compared to controllers utilizing the low-side MOSFET current sensing.

See the *Inductor DCR Current Sense* sectionfor selecting the values of the RC network.

5.25 OVERCURRENT DETECTION AND HICCUP MODE

In order to reduce the input current and component dissipation during on overcurrent event, a hiccup mode is implemented. Hiccup mode refers to a sequence of 7 soft-start cycles where no MOSFET switching occurs and then a re-start is attempted. If the fault has cleared, the re-start results in returning to normal operation and regulation. This is shown in Figure 5-9.

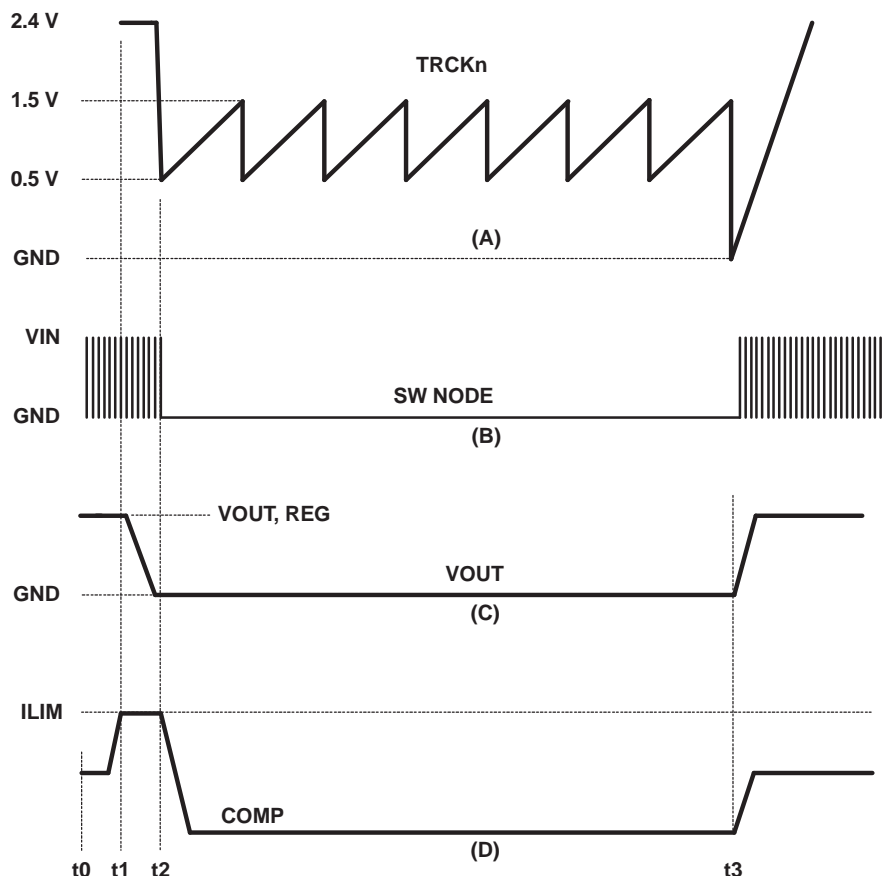**Figure 5-9. Hiccup Mode and Recovery**

In Figure 5-9, normal operation is occurring between t0 and t1 as shown by V_{OUT} being at the regulated voltage, (C) and normal switching on the SW NODE (B) and COMP at it's nominal level, (D). At t1, an overcurrent load is experienced. The increased current forces COMP to increase to the ILIM level as shown in (D). If the COMP voltage is above the ILIM voltage for 7 switching cycles, the controller enters a hiccup mode. During this time the controller is not switching and the switching MOSFETs are turned off. The TRCKn voltage goes through 7 cycles of charging and discharging the soft-start capacitor. At the end of the 7 cycles the controller attempts another normal re-start. If the fault has been cleared, the output voltage comes up to the regulation level as shown at time t3. If the fault has not cleared, the COMP voltage again rises above the ILIM voltage and the hiccup mode repeats.

If the overcurrent condition exists for seven (7) PWM clock cycles the converter turns off the upper and lower MOSFETs and initiates a hiccup mode restart. In hiccup mode, the TRKx pin is periodically charged and discharged. After seven hiccup cycles, the controller attempts another soft-start cycle to restore normal operation. If the overload condition persists, the controller returns to the hiccup mode. This condition may continue indefinitely.

5.26 CALCULATING OVERCURRENT PROTECTION LEVEL

In order to set the desired overcurrent (I_{OC}), a few variables must be known. The input and output voltage, the output inductor value and it's DC resistance (DCR), as well as the switching frequency. Also known are the ramp voltage which is 0.5 V and the V_{SHARE} voltage, V_{SH} which is 1.8 V. See the list of variables and their values at the end of this section.

The overcurrent set point is in terms of the DC output current, but the current sense circuit monitors the peak of the current. Therefore, the current ripple is needed and is calculated from

- input voltage (V_{IN})
- output voltage (V_{OUT})
- switching frequency (f_{SW})
- output inductance (L)

The ripple current is given by Equation 11.

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

(11)

The peak current detected is given by Equation 12, and used in Equation 14.

$$I_{PEAK} = \frac{I_{RIPPLE}}{2} + I_{OC}$$

(12)

It is this I_{PEAK} current that is detected by the current sense circuit. The two resistors needed to set the peak overcurrent protection threshold and their connection for each channel is shown in Figure 5-10.

DESIGN HINT: Resistor R2 may be connected to the output voltage, Vout, or to the output of the differential amplifier, DIFFO, if used.
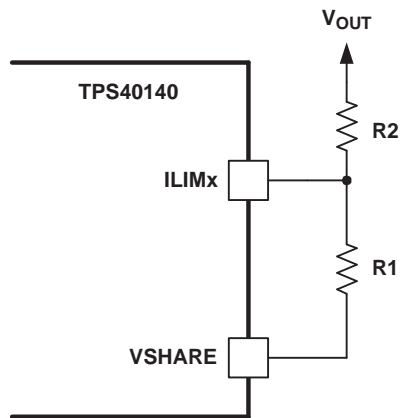
Figure 5-10. Selecting Overcurrent Threshold Resistors, R2 and R1

The two factors, alpha and beta help simplify the final equations and are given by Equation 13 and Equation 14.

$$\alpha = \frac{V_{RAMP}}{V_{IN}}$$

(13)

$$\beta = DCR \times A_C \times I_{PEAK} + \left(\frac{V_{RAMP}}{2 \times Nph} \right)$$

(14)

R1 is shown in Equation 15.

$$R1 = \frac{\beta + \alpha \times V_{SH}}{(1 - \alpha) \times I_{LIM}}$$

(15)

R2 is shown in Equation 16.

$$R2 = \frac{\beta + \alpha \times V_{SH}}{\alpha \times I_{LIM}}$$

(16)

where (for Equation 13 through Equation 16)
- V_{RAMP}[1] is the ramp amplitude (0.5 V typ)
- V_{IN} is the input voltage
- DCR is the inductor equivalent DC resistance
- A_C[1] is the gain transfer to comparator
- I_{OC} is the single-phase DC overcurrent trip point
- I_{PEAK} is the peak single-phase inductor current
- N_{ph} is 6 if PHSEL voltage = 1.6 V ±0.2 V, otherwise N_{ph} = 8
- V_{SHR}[1] is the V_{SHARE} reference voltage (typ 1.8 V)
- I_{LIM}[1] is the current limit, output current (typ 20 µA)

(1) Range of variable is specified in

5.27 CONFIGURING SINGLE AND MULTIPLE ICS

The controller may be configured for a single output, 2 Phase mode or a Dual output voltage mode. In the Dual output mode the input voltages and the output voltages are independent of each other. In 2 Phase mode the input voltages and output voltages are tied together, respectively and certain other pins must be configured. The two phases of a single controller are always 180° out of phase. The entry in the following tables that refer to' TO NETWORK' means the normal resistor-capacitor network used for control loop compensation. The other entries refer to components that are typically connected to the Device Pin.

5.27.1 Single Device Operation

A single controller may be configured as a 2 Phase or Dual output. A summary of the modes and device pin connections for a single controller is given in Table 5-2. The basic schematic of a single controller operating in a 2 Phase mode is shown in Figure 5-11 . The Dual output schematic is shown in Figure 5-14.

Table 5-2. TPS40140 SINGLE device MODE SELECTION AND PIN CONFIGURATION

DEVICE PIN	FOR 2 PHASE MODE	FOR DUAL OUTPUT MODE
COMP1	TO NETWORK	TO NETWORK
COMP2	COMP1	TO NETWORK
TRK1	TO SS CAPACITOR	TO SS CAPACITOR
TRK2	TO BP5	TO SS CAPACITOR
ILIM1	TO SET RESISTORS	TO SET RESISTORS
ILIM2	GND	TO SET RESISTORS
FB1	TO NETWORK	TO NETWORK
FB2	GND	TO NETWORK
PHSEL	GND	GND
PGOOD1	TO PULL-UP RESISTOR	TO PULL-UP RESISTOR
PGOOD1	TO PULL-UP RESISTOR	TO PULL-UP RESISTOR
CLKIO	OPEN	OPEN

Figure 5-11. Typical Applications Circuit, 2 PHASE Mode

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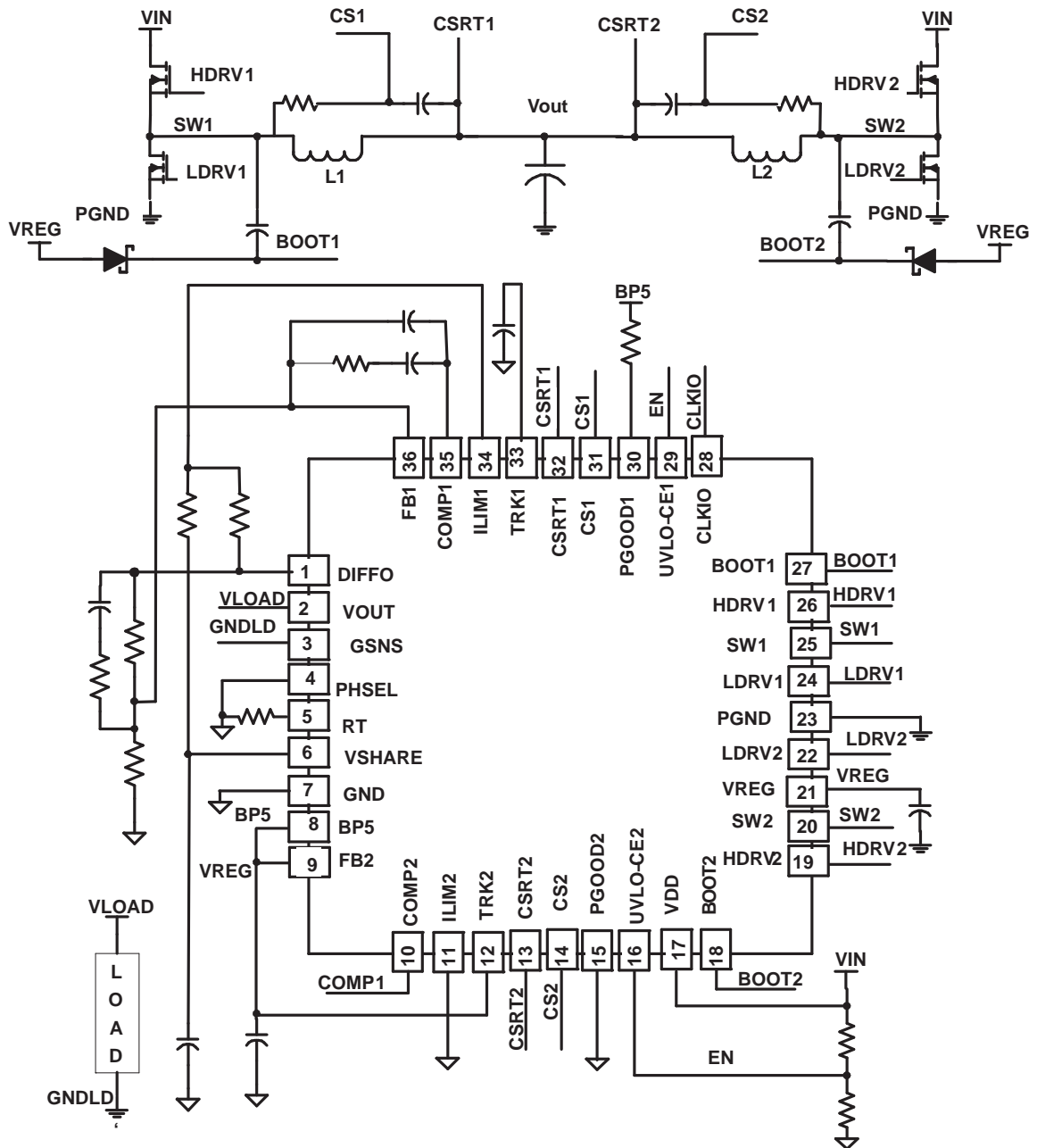SLUS660A–SEPTEMBER 2005–REVISED JULY 2006

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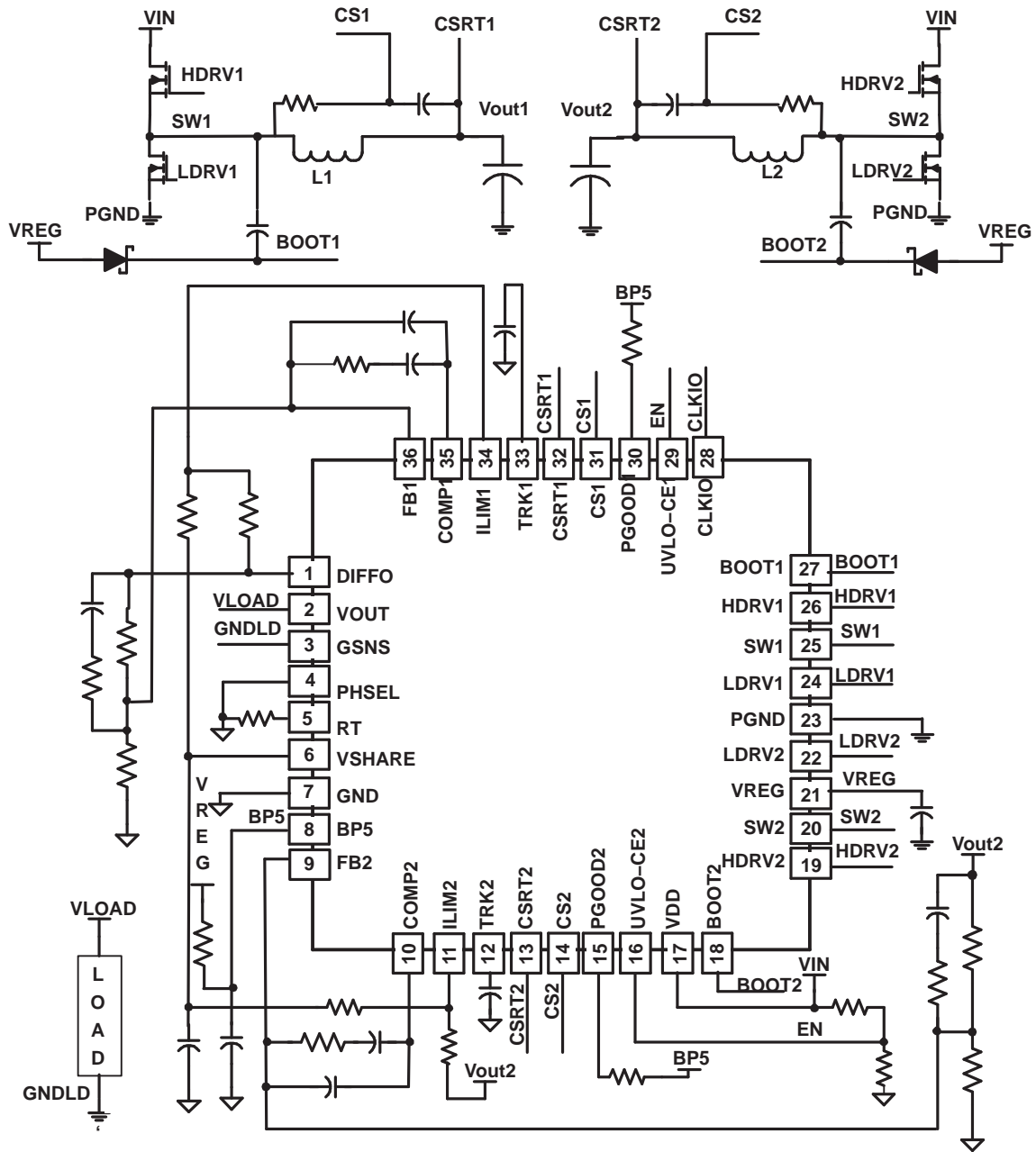
Figure 5-12. Typical Applications Circuit, DUAL Mode

5.27.2   MULTIPLE ICs

In a multiple device system it is often desireable to synchronize the clocks of all the ICs to minimize input ripple current as well as radiated and conducted emissions. This is accomplished by designating one of the controllers as the 'Master' and the other ICs as 'Slaves'. The Master generates the system clock, CLKIO , and it is distributed to the Slaves. This is the most useful configuration of multiple ICs and the one that is demonstrated in this data sheet. It is described in more detail in the ' *Clock Master, PHSEL AND CLKIO Configurations*' section.

To increase the total current capability, or number of outputs, a single Slave controller can be added to a Master controller as shown in Figure 5-15. The configuration of the 2 Phase Master and a 2 Phase Slave controller is also shown in Table 5-3 It is possible to have the Master controller operate on one switching frequency and the Slave controllers on another, independent frequency. In a multi-phase system the Slave controllers would still share load current with the Master. This is not a preferred configuration and is mentioned here only for completeness.

Table 5-3. TPS40140 TWO DEVICE, 4 PHASE MODE SELECTION AND PIN CONFIGURATION

DEVICE PIN, MASTER	MASTER, 2 PHASE	DEVICE PIN, SLAVE	SLAVE, 2 PHASE
COMP1	TO NETWORK	COMP1	TO MASTER, COMP1
COMP2	COMP1	COMP2	TO MASTER, COMP1
TRK1	TO SS CAPACITOR	TRK1	TO BP5
TRK2	TO BP5	TRK2	TO BP5
ILIM1	TO SET RESISTORS	ILIM1	GND
ILIM2	GND	ILIM2	GND
FB1	TO NETWORK	FB1	GND
FB2	GND	FB2	GND
PHSEL	39KΩ TO GND	PHSEL	GND
PGOOD1	TO PULL-UP RESISTOR	PGOOD1	TO PULL-UP RESISTOR
PGOOD1	TO PULL-UP RESISTOR	PGOOD1	TO PULL-UP RESISTOR
CLKIO	TO SLAVE, CLKIO	CLKIO	TO MASTER, CLKIO

Figure 5-13. Typical Applications Circuit, 4 Phase Mode

In this configuration, the Master senses that there is one Slave controller, by the 39-kΩ resistor on the PHSRL pin, and distributes the CLKIO signal. The Slave controller senses the zero-volt level on its PHSEL pin and delays the proper number of CLKIO pulses to be 90° out of phase with the Master.

Two ICs could also be configured as a 2 Phase, single output Master and a Slave which has two independent outputs, but is synchronized with the Master controller clock. The configuration is shown in Table 5-4.

Table 5-4. TPS40140 TWO DEVICE, 2 PHASE MASTER AND A DUAL OUTPUT SLAVE CONFIGURATION

DEVICE PIN, MASTER	MASTER, 2 PHASE	DEVICE PIN, SLAVE	SLAVE, DUAL OUTPUT
COMP1	TO NETWORK	COMP1	TO NETWORK
COMP2	COMP1	COMP2	TO NETWORK
TRK1	TO SS CAPACITOR	TRK1	TO SS CAPACITOR
TRK2	TO BP5	TRK2	TO SS CAPACITOR
ILIM1	TO SET RESISTORS	ILIM1	TO SET RESISTORS
ILIM2	GND	ILIM2	TO SET RESISTORS
FB1	TO NETWORK	FB1	TO NETWORK
FB2	GND	FB2	TO NETWORK
PHSEL	39-kΩ TO GND	PHSEL	GND
PGOOD1	TO PULL-UP RESISTOR	PGOOD1	TO PULL-UP RESISTOR
PGOOD1	TO PULL-UP RESISTOR	PGOOD1	TO PULL-UP RESISTOR
CLKIO	TO SLAVE, CLKIO	CLKIO	TO MASTER, CLKIO

5.27.3 CLOCK MASTER, PHSEL AND CLKIO CONFIGURATIONS

The clock synchronization between the Master and the Slave controller(s) is implemented in a simple configuration of series 39-kΩ resistors. There is a 20-μA current source from the PHSEL pin of the Master controller. Depending on the number of Slave controllers connected, the Slave controllers will select the proper delay from the Master CLKIO signal to accomplish phase interleaving. On a given Master or Slave controller, the two phases are always 180° out of phase.

The CLKIO signal has either six or eight clocks for each cycle of the switching period.

For maximum flexibility the Master and Slave controllers can be either in a 2 Phase configuration or a Dual output configuration

5.27.3.1 One device Operation

The basic configuration of a single device is shown in Figure 5-14.
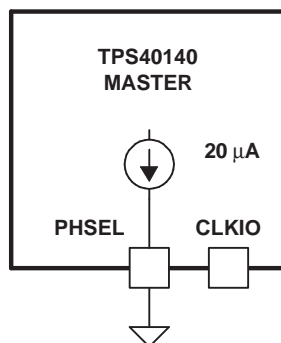
Figure 5-14. Single Controller only, Two Phases

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5.27.3.2 Two ICs Operation

To increase the total current capability, or number of outputs, a single Slave controller can be added as shown in Figure 5-15

Figure 5-15. Master Controller and One Slave Controller, Four Phases

In this configuration, the Master senses that there is one Slave controller, and distributes the CLKIO signal. The Slave controller senses the zero-volt level on its PHSEL pin and delays the proper number of CLKIO pulses to be 90° out of phase with the Master.

5.27.3.3 Three ICs Operation

To increase the total current capability to six phases, or to increase the number of outputs, two Slave controllers can be added as shown in Figure 5-16. In this configuration for perfect interleaving, the Master and Slaves are 120° out of phase. The CLKIO signal has six clocks for each cycle of the switching period; therefore, the switching period is reduced. In this six-phase mode, the switching frequency is increased 33%.

Figure 5-16. Master Controller and Two Slave Controllers, Six Phases

In this configuration, the Master senses that there are two Slave controllers, and distributes a six-phase CLKIO signal. The Slave controllers sense the voltage on their PHSEL pins, and delay the proper number of CLKIO pulses to be 60° or 120° out of phase with the Master.

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5.27.3.4 Four ICs Operation

To further increase the total current capability to eight phases, or to increase the number of outputs, three Slave controllers can be added as shown in Figure 5-17

Figure 5-17. Master Controller and Three Slave Controllers, 8 Phases

In this configuration, the Master senses that there are three Slave controllers, and distributes a eight-phase CLKIO signal. The Slave controllers sense the voltage on their PHSEL pins and delay the proper number of CLKIO pulses to be 45° or 90° out of phase with the Master.

5.27.3.5 Six ICs Operation

To further increase the total current capability to twelve phases, or to increase the number of outputs, five Slave controllers can be added as shown in Figure 5-18
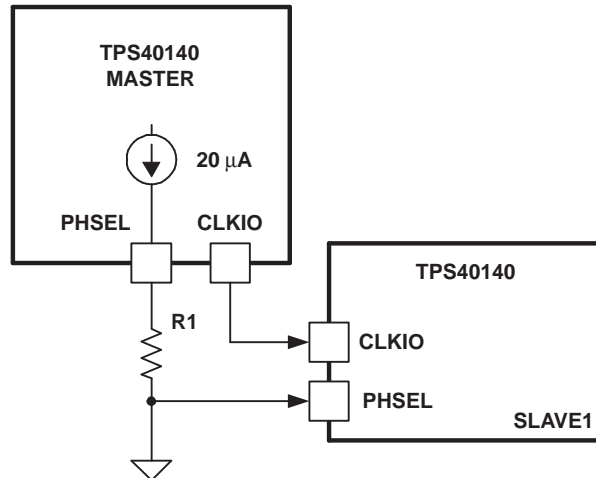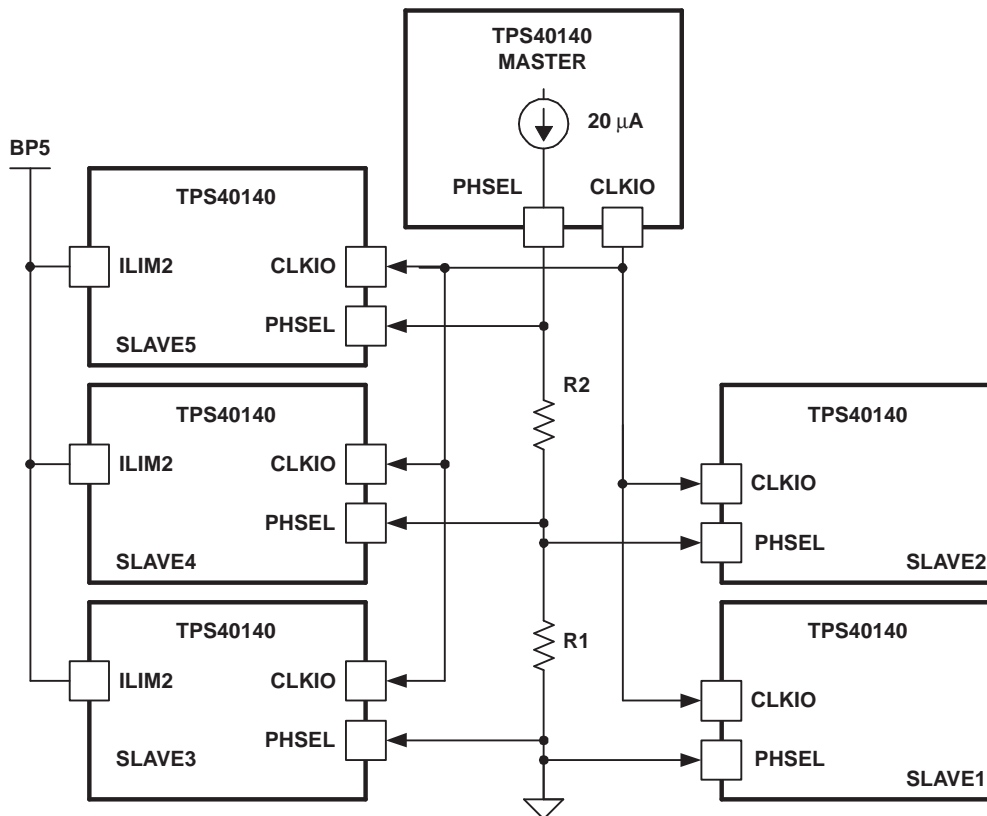

Figure 5-18. Master Controller and Five Slave Controllers, 12 Phases

In this configuration, the Master senses that there are two Slave controllers (due to the 2 resistors) and distributes a six-phase CLKIO signal. Slaves 1 and 2 are turned on at 60° and 120° respectively, as before with 2 Slaves. However, to get 12 phases with a 6-phase clock, both edges of the CLKIO signal are used to control the slaves. With the ILIM2 tied high on Slaves 3, 4, and 5, they turn on at the rising edge of CLKIO while the Master and Slaves 1 and 2 turn on at the falling edge of CLKIO.

If 4 Slaves are desired, just delete one of the Slaves from Figure 5-18. The interleaving will not be perfect because there will be 30 degrees between the Master and 3 Slaves. The deleted Slave will cause 60° between the 2 adjacent Slaves. See Figure 5-20 for phasing details.

5.27.3.6 Eight ICs Operation

To further increase the total current capability to sixteen phases, or to increase the number of outputs, seven Slave controllers can be added as shown in Figure 5-19.
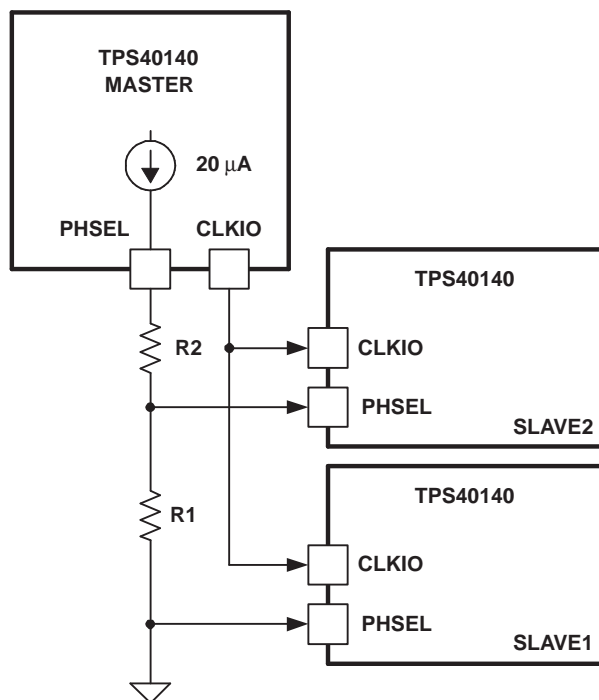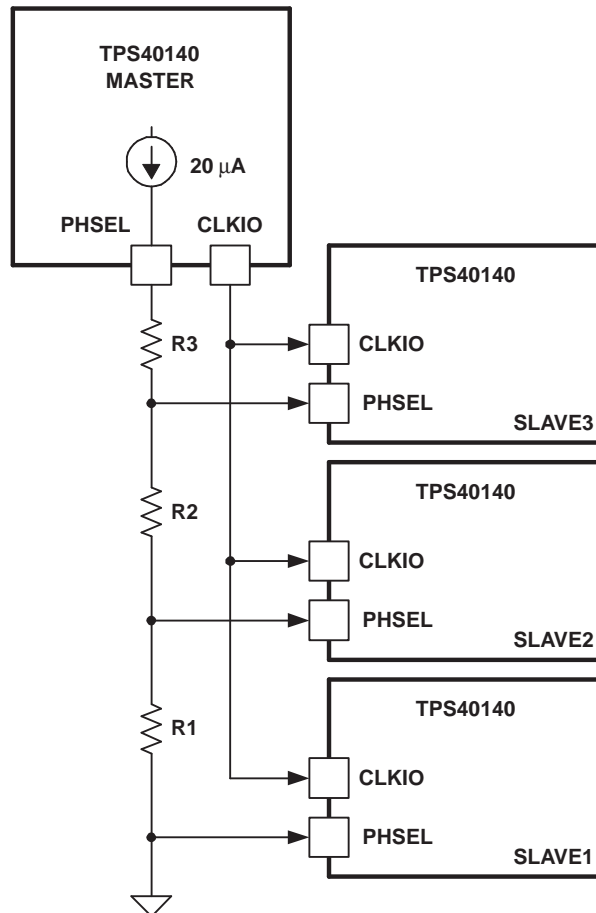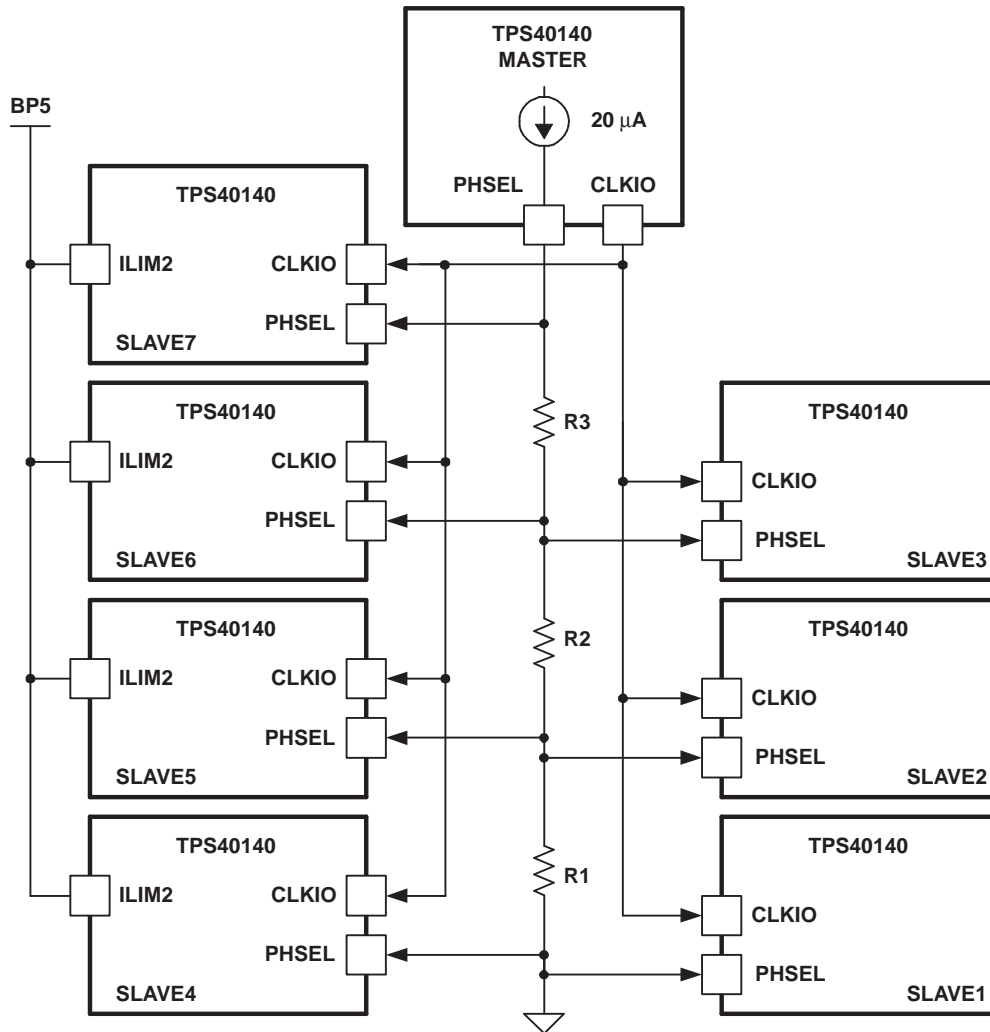

Figure 5-19. Master Controller and Seven Slave Controllers, 16 Phases

In this configuration, the Master senses that there are three Slave controllers (due to the 3 resistors) and distributes an eight-phase CLKIO signal. Slaves 1, 2 and 3 are turned on at 45° and 90° respectively as before with 3 Slaves. However, to get 16 phases with an 8-phase clock, both edges of the CLKIO signal are used to control the slaves. With the ILIM2 tied high on Slaves 4, 5, 6, and 7 they turn on at the rising edge of CLKIO, while the Master and Slaves 1, 2, and 3 turn on at the falling edge of CLKIO. If 6 Slaves are desired, just delete one of the Slaves from Figure 5-19. The interleaving will not be perfect because there will be 22.5° between the Master and 3 Slaves. The deleted Slave will cause 45° between the 2 adjacent Slaves. See Figure 5-20 for a phasing details.

5.28 DIGITAL CLOCK SYNCHRONIZATION

Figure 5-20 is a summary of the Master and Slave clock phasing. The Master and the Slaves can be selected to be a multi-phase, single output configuration and/or several independent output voltage rails, independent of the clocking.

(A) Two Phase Master

(B) Four Phase , Master and one Slave

(C) SixPhase, Master and two Slaves

(D) Eight Phase, Master and three Slaves

(E) 'Missing' Pulse with six and eight CLKIO pulses

(F) Twelve Phase , Master and five Slaves

(G) Sixteen Phase, Master and seven Slaves

Figure 5-20. Clock Phasing Summary

5.28.1 BASIC CONFIGURATIONS FOR 2, 4, 6, 8, 12 OR 16 PHASES

The solid square boxes in Figure 5-20 represent the PHSEL pin of the Master (M) controller or a numbered Slave controller (S1-S7). The labels on the spokes of the wheels indicate a Master Channel 1 and Master Channel 2 (M_CH1 and M_CH2) and numbered Slaves Channel 1 and Slave Channel 2 (Sn_CH1 and Sn_CH2). The Channel 1 and Channel 2 of a given Master or Slave is always 180° out of phase.

The Master and Slaves are automatically configured for proper phasing based on the resistor string from the Master to the Slaves. All the resistors are 39 kΩ to 41.2 kΩ. Part (A) above shows a single controller operating two phases 180° out of phase. Part (B) above shows four phase operation. This is configured by connecting a single resistor from the Master PHSEL to GND and grounding the Slave PHSEL pin. The individ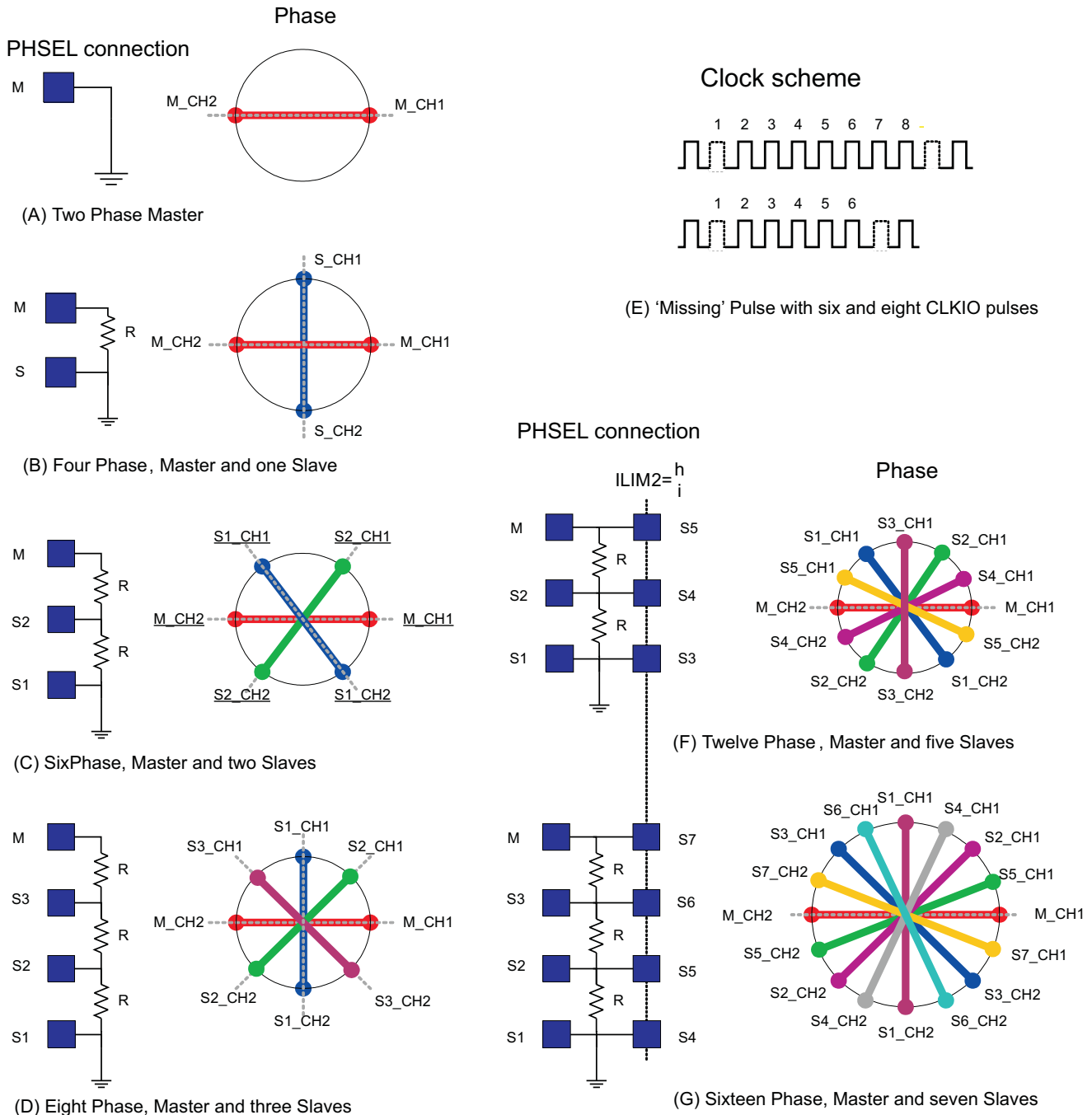ual channels are 90° out of phase. Part (C) above shows six phase operation. This is configured by connecting two resistors from the Master PHSEL to GND. The first resistor tap is connected to Slave2 PHSEL pin and then grounding the Slave1 PHSEL pin. The individual channels are 60° out of phase. Part (D) above shows eight phase operation. This is configured by connecting three resistors from the Master PHSEL to GND. The first resistor tap is connected to Slave3 PHSEL pin. The second resistor tap is connected to Slave2 PHSEL pin and then grounding the Slave1 PHSEL pin. The individual channels are 45° out of phase. Part (F) above shows twelve phase operation. This is configured by connecting two resistors from the Master PHSEL to GND. The Master PHSEL pin is also connected to Slave5 PHSEL pin. The first resistor tap is connected to Slave2 and Slave4 PHSEL pins and then grounding the Slave1 and Slave3 PHSEL pins. The individual channels are 30° out of phase. Additionally, the ILIM2 pins of Slave5, Slave4 and Slave3 are left open (internal pull-up) or externally connected to BP5. Part (G) above shows sixteen phase operation. This is configured by connecting three resistors from the Master PHSEL to GND. The Master PHSEL pin is also connected to Slave7 PHSEL pin. The first resistor tap is connected to Slave3 and Slave6 PHSEL pins. The second resistor tap is connected to Slave2 and Slave5 PHSEL pins and then grounding the Slave1 and Slave4 PHSEL pins. The individual channels are 22.5° out of phase. Additionally, the ILIM2 pins of Slave7, Slave6, Slave5 and Slave4 are left open (internal pull-up) or externally connected to BP5.

5.28.2 CONFIGURING FOR OTHER NUMBER OF PHASES

Configuring for other than 2, 4, 6, 8, 12 or 16 phases is simply a matter of not attaching one or more Slave controllers. The phasing between Master and populated Slaves is as shown above. For example a 3-phase system could be configured with a Master CH1 and Master CH2 and 1 phase of a Slave. Referring to part (B) above, the 3 phases could be Master CH1, Master CH2 and Slave CH1 or Slave CH2 as shown in Figure 5-21.
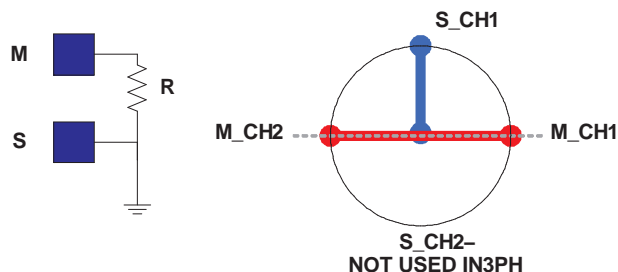
Figure 5-21. Phase System: 2 Channels of the Master and 1 Channel of the Slave

The 3-phase system could also be configured with 1 channel of the Master and 2 channels of the Slave. Referring to part (B) above, the 3 phases could be Master CH1 or Master CH2 and Slave CH1 and Slave CH2. In either of these configurations there will be 90° between two of the channels and 180° between the other channel. The unused channel could be another independent output voltage whose clocking would occupy the phase not used in the 3-phase system. This philosophy can be used for any number of phases not shown in Figure 5-20, *Clock Phasing Summary*.

For example, a 10-phase system could be configured as shown in Figure 5-22.

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PHSEL connection

Phase

ILIM 2=hi
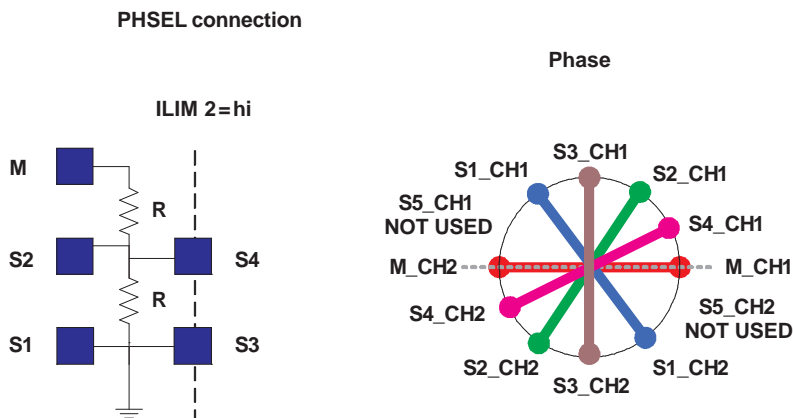
Figure 5-22. Ten-Phase System with Slave5 Not Attached

Clocking between the attached slave channels is as shown.

5.29 DESIGN EXAMPLES INFORMATION

5.29.1 INDUCTOR DCR CURRENT SENSE

The preferred method for sampling the output current for the TPS40140 is known as the *inductor DCR* method. This is a *lossless* approach, as opposed to using a discrete current sense resistor which occupies board area and impacts efficiency as well. The inductor DCR implementation is shown in Figure 5-23.
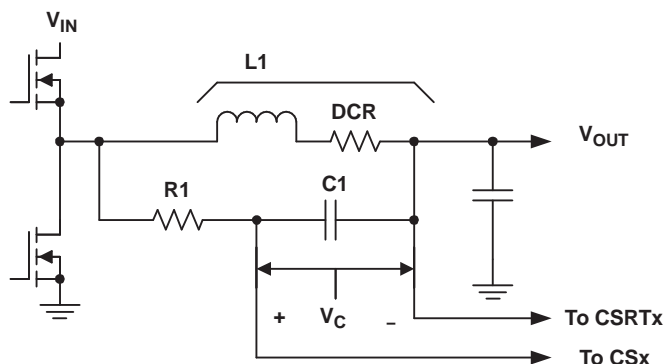
Figure 5-23. Inductor DCR Current Sense Approach

The inductor L1 consists of inductance, L, and resistance, DCR. The time constant of the inductor: L / DCR should equal the R1×C1 time constant. Then choosing a value for C1 (0.1 µF is a good choice) solving for R1 is shown in Equation 17.

$$R1 = \frac{L1}{DCR \times C1}$$

(17)

The voltage into the current sense amplifier of the controller , V_C, is calculated in Equation 18.

$$V_C = \left(V_{IN} - V_{OUT}\right) \times \frac{V_{OUT}}{R1 \times C1 \times f_{SW} \times V_{IN}} + I_{OC} \times DCR$$

(18)

As the DC load increases the majority of the voltage, V_C, is determined by ($I_{OC} \times$ DCR), where I_{OC} is the per phase DC output current. It is important that at the overcurrent set point that the peak voltage of V_C does not exceed 60 mV, the maximum differential input voltage. If the voltage V_C exceeds 60 mV, a resistor, R2,can be added in parallel with C1 as shown in Figure 5-24. Adding R2 reduces the equivalent inductor DCR by the ratio shown in Equation 20
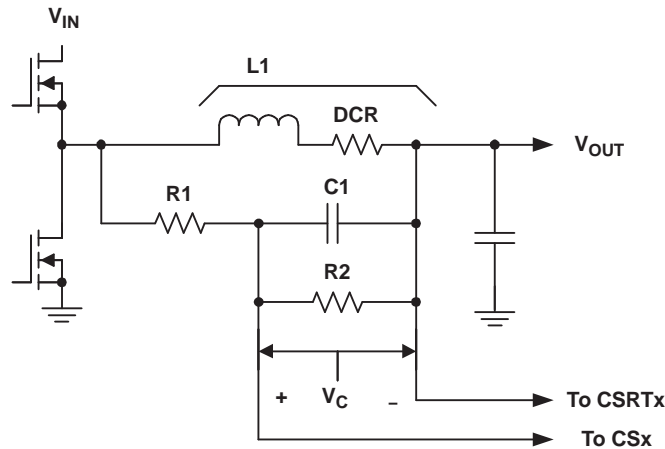
Figure 5-24. Using Resistor R2 to Reduce the Current Sense Amplifier Voltage

The parallel combination of R1 and R2 is shown in Equation 19.

$$R1 \parallel R2 = \frac{L1}{DCR \times C1}$$

(19)

The ratio shown in Equation 20 provides the required voltage attenuation.

$$\frac{R2}{R1 + R2}$$

(20)

6 DESIGN EXAMPLES

6.1 Example 1: Dual-Output Configuration from 12 V to 3.3 V and 1.5 V DC-to-DC Converter Using a TPS40140

The following example illustrates the design process and component selection for a dual output synchronous buck converter using TPS40140. The design goal parameters are given in Table 6-1. Only the calculated numbers for the 1.5-V output are shown, however, the equations are suitable for both channel design. A list of symbol definitions is found at the end of this section.

Table 6-1. Design Goal Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT1}	Output voltage 1			1.5		V
V_{OUT2}	Output voltage 2			3.3		V
V_{RIPPLE}	Output ripple	I_O = 20 A		2%Vo		V
I_{OUT1}	Output current 1			20		A
I_{OUT2}	Output current 2			20		A
f_{sw}	Switching frequency			500		kHz

6.1.1 Step 1: Inductor Selection

The inductor is determined by the desired ripple current. The required inductor is calculated by:

$$L = \frac{V_{IN(max)} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN(max)}} \times \frac{1}{f_{SW}}$$

(1)

Typically the peak-to-peak inductor current, I_{RIPPLE} is selected to be around 20% of the rated output current. In this design, I_{RIPPLE} is targeted at 15% of IOUT1. The calculated inductor is 0.89 μH and in practical a 1-μH, 32-A inductor from Vishay is selected. So, the inductor ripple current is 2.66 A.

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6.1.2 Step 2: Output Capacitor Selection

The output capacitor is typically selected by the output load transient response requirement. Equation 2 estimates the minimum capacitor to reach the undervoltage requirement with load step up. Equation 3 estimates the minimum capacitor for overvoltage requirement with load step down. When $V_{IN(min)} < 2 \times V_{OUT}$, the minimum output capacitance can be calculated using Equation 2. Otherwise, Equation 3 is used.

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^2 \times L}{\left(V_{IN(min)} - V_{OUT}\right) \times V_{UNDER}}$$
(2)

when $V_{IN(min)} < 2 \times V_{OUT}$

$$C_{OUT(MIN)} = \frac{I_{TRAN(MAX)}^2 \times L}{V_{OUT} \times V_{OVER}}$$
(3)

when $V_{IN(min)} > 2 \times V_{OUT}$

In this design, $V_{IN(min)}$ is much larger than $2 \times V_{OUT}$, so Equation 3 is used to determine the minimum capacitance. Based on a 10-A load transient with a maximum of 80-mV deviation, a minimum 833-µF output capacitor is required. In the design, four 220-µF, 4-V, SP capacitor are selected to meet this requirement. Each capacitor has an ESR of 5 mΩ.

Another criterion for capacitor selection is the output ripple voltage. The output ripple is determined mainly by the capacitance and the ESR.

$$ESR_{Co} = \frac{V_{RIPPLE(TotOUT)} - V_{RIPPLE(COUT)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(TotOUT)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}}$$
(4)

With 880-µF output capacitance, the ripple voltage at the capacitor is calculated to be 863-µV. In the specification, the output ripple voltage should be less than 30 mV, so based on Equation 4, the required maximum ESR is 9.5 mΩ. The selected capacitors can meet this requirement.

6.1.3 Step 3: Input Capacitor Selection

The input voltage ripple depends on the input capacitance and the ESR. The minimum capacitor and the maximum ESR can be estimated by:

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{RIPPLE(CIN)} \times V_{IN} \times f_{SW}}$$
(5)

$$ESR_{Cin} = \frac{V_{RIPPLE(CinESR)}}{I_{OUT} + \frac{1}{2}I_{RIPPLE}}$$
(6)

For this design, assume $V_{RIPPLE(CIN)}$ is 100 mV and $V_{RIPPLE(CinESR)}$ is 50 mV, so the calculated minimum capacitance is 50µF and the maximum ESR is 2.3 mΩ. Choosing four 22-µF, 16-V, 2-mΩ ESR ceramic capacitors meets this requirement.

Another important consideration for the input capacitor is the RMS ripple current rating. The RMS current in the input capacitor is estimated by:

$$I_{RMS\_CIN} = \sqrt{D \times (1 - D)} \times I_{OUT}$$
(7)

D is the duty cycle. The calculated RMS current is 6.6 A. Each selected ceramic capacitor has a RMS current rating of 4.3 A, so it is sufficient to reach this requirement.

6.1.4 Step 4: MOSFET Selection

The MOSFET selection determines the converter efficiency. In this design, the duty cycle is very small so that the high-side MOSFET is dominated with switching losses and the low-side MOSFET is dominated with conduction loss. To optimize the efficiency, choose smaller gate charge for the high-side MOSFET and smaller $R_{DS(on)}$ for the low-side MOSFET.

The RENESAS RJK0305 and RJK0301 are selected as the high-side and low-side MOSFETs respectively. To reduce the conduction loss, two RJK0301 components are used.

The power losses in the high-side MOSFET is calculated with the following equations:

The RMS current in the high side MOSFET is show in Equation 8.

$$I_{SWrms} = \sqrt{D \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12} \right)} = 7.07 \text{ A} \tag{8}$$

The $R_{DS(on)}$ is 13 mΩ when the MOSFET gate voltage is 4.5 V.

The conduction loss is:

$$P_{SWcond} = \left(I_{SWrms} \right)^2 \times R_{DS(on)} (sw) = 0.65 \text{ W} \tag{9}$$

The switching loss is:

$$Psw_{sw} = \frac{Ipk \times Vin \times f_{sw} \times R_{drv} \times (Qgd_{sw} + Qgs_{sw})}{Vgtdrv} = 0.26W \tag{10}$$

The calculated total loss in the high-side MOSFET is:

$$P_{SWtot} = P_{SWcond} + P_{SWsw} = 0.91 \text{ W} \tag{11}$$

The power losses in the low-side SR MOSFET is calculated by:

The RMS current in the low side MOSFET is shown in Equation 12.

$$I_{SRrms} = \sqrt{(1 - D) \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12} \right)} = 18.7 \text{ A} \tag{12}$$

The $R_{DS(on)}$ is 4mΩ when the MOSFET gate voltage is 4.5V.

The total conduction loss in the two low-side MOSFETs is:

$$P_{SRcond} = \left(I_{SRrms} \right)^2 \times \frac{R_{DS(on)} (sr)}{N} = 0.7 \text{ W} \tag{13}$$

N is the number of MOSFET. Here, it is equal to 2.

The total power loss in the body diode is:

$$P_{diode} = 2 \times I_{OUT} \times t_d \times V_f \times f_{sw} = 0.77W \tag{14}$$

So the calculated total loss in the SR MOSFET is:

$$P_{SRtot} = P_{SRcond} + P_{DIODE} = 1.47 \text{ W} \tag{15}$$

6.1.5 Step 5: Peripheral Component Design

6.1.5.1 Switching Frequency Setting (RT pin 5):

$$R = 1.33 \times \left(39.2 \times 10^3 \times f_{SW}^{-1.041} - 7 \right) = 71.5 \text{ k}\Omega \tag{16}$$

In the design, a 62-kΩ resistor is selected. The actual switching frequency is 510kHz.

6.1.5.2 Output Voltage Setting (FB1 pin 36):

Substitute R1 with 10 kΩ and then calculate R_{BIAS}.

$$R_{BIAS} = 0.7 \times \frac{R1}{V_{OUT} - 0.7} = 8.75 \text{k}\Omega \tag{17}$$

6.1.5.3 Current Sensing Network Design (CS1 pin 31 and CSRT1 pin32)

For small pulse width, to avoid the sub-harmonics brought by the loop delay, a resistor divider is usually used to attenuate the current feedback information as described in the *Inductor DCR Current Sense* section.

Choosing C1 a value for 0.1-μF, and let R1 and R2 be equal, calculating R1 and R2 with the following equations:

$$R1//R2 = \frac{L}{DCR \times C1} = 5 \text{k}\Omega \tag{18}$$

$$R1 = R2 = 10 \text{k} \tag{19}$$

There is a simplified equation to check if the design will have sub-harmonics or not.

$$\frac{L}{DCR_{(eqv)}} > \frac{V_{IN} \times Ac}{2 \times V_{ramp} \times f_{sw}} \tag{20}$$

$$DCR_{(eqv)} = \frac{R2}{R1 + R2} \times DCR = \frac{DCR}{2} \tag{21}$$

In this design, a 1-μF capacitor is placed at the CSRT1 pin for the purpose of eliminating noise. It can be removed without degrading performance.

6.1.5.4 Overcurrent Protection (ILIM1 pin 34)

The resistor selection equations in the **CALCULATING OVERCURRENT PROTECTION LEVEL**section are simplified to calculate the over current setting resistors. Set the DC over current rating at 25A.

$$R1 = \frac{I_{PK} \times DCR_{eqv} \times Ac + V_{OS} + \frac{0.9}{V_{IN}}}{\left(1 - \frac{0.5}{V_{IN}} \right) \times 20 \times 10^{-6}} = 22.5 \text{ k}\Omega \tag{22}$$

$$R2 = \frac{I_{PK} \times DCR_{eqv} \times Ac + V_{OS} + \frac{0.9}{V_{IN}}}{\left(\frac{0.5}{V_{IN}} \right) \times 20 \times 10^{-6}} = 510 \text{ k}\Omega \tag{23}$$

V_{OS} is defined as the internal offset, which is typically about 50 mV.

6.1.5.5 VREG (pin 21)

A 4.7-μF capacitor is connected to VREG pin to filter noise.

6.1.5.6 BP5 (pin 8)

A 4.7Ω and 1μF capacitor is placed between VREG and BP5.

6.1.5.7 PHSEL (pin 4)

For this dual output configuration, the PHSEL pin is directly tied to GND. The channel 1 and channel 2 has a 180° phase shift.

6.1.5.8 VSHARE (pin 6)

A 1μF capacitor is tied from VSHARE pin to GND.

6.1.5.9 PGOOD1 (pin 30)

The PGOOD1 pin is tied to BP5 with a 10-kΩ resistor.

6.1.5.10 UVLO_CE1 (pin 29)

It is connected to the input voltage with a resistor divider. The two resistors have the same value of 10-kΩ. When the input voltage is higher than 2 V, the chip is enabled.

6.1.5.11 CLKIO (pin 28)

CLKIO is floating as no clock synchronization required for dual output configuration.

6.1.5.12 BOOT1 and SW1 (pin 27 and 25)

A bootstrap capacitor is connected between the BOOT1 and SW1 pin. The bootstrap capacitor depends on the total gate charge of the high side MOSFET and the amount of droop allowed on the bootstrap capacitor.

$$C_{boot} = \frac{Qg}{\Delta V} = \frac{8nc}{0.5V} = 16nF \tag{24}$$

For this application, a 0.1-μF capacitor is selected.

6.1.5.13 TRK1 (pin 33)

A 22-nF capacitor is tied to TRK1 pin to provide 1.28 ms soft start time.

$$Tss = Css \times 58 \times 10^3 = 22 \times 10^{-9} \times 58 \times 10^3 = 1.28ms \tag{25}$$

6.1.5.14 DIFFO, VOUT and GSNS (pin 1, pin 2 and pin 3)

VOUT and GSNS are connected to the remote sensing output connector. DIFFO is connected to the feedback resistor divider. If the differential amplifier is not used, VOUT and GSNS are suggested to be grounded, and DIFFO is left open.

6.1.6 Feedback Compensator Design (COMP1 pin 35)

Peak current mode control method is employed in the controller. A small signal model is developed from the COMP signal to the output.

$$Gvc(s) = \frac{1}{DCR \times Ac} \times \frac{1}{s \times \tau_s + 1} \times \frac{(s \times C_{OUT} \times ESR + 1) \times R_{OUT}}{s \times C_{OUT} \times R_{OUT} + 1} \tag{26}$$

The time constant is defined by:

$$\tau_s = \frac{T}{\ln(\dfrac{\dfrac{V_{ramp}}{T} - \dfrac{V_{OUT}}{L} \times DCR \times Ac}{\dfrac{V_{ramp}}{T} - \dfrac{V_{IN} - V_{OUT}}{L} \times DCR \times Ac - \dfrac{2 \times V_{OUT}}{L} \times DCR \times Ac})} \tag{27}$$

The low frequency pole is calculated by:

$$f_{VCP1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}} = 2.36 \text{kHz}$$

(28)

The ESR zero is calculated by:

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} = 176.8 \text{kHz}$$

(29)

In this design, a Type II compensator is employed to compensate the loop.
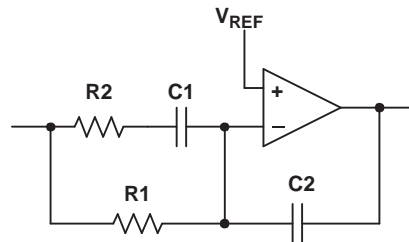
Figure 6-1. Type II Compensator

The compensator transfer function is:

$$Gc(s) = \frac{1}{R1 \times C2} \times \frac{s \times (R1 + R2) \times C1 + 1}{s \times (s \times R2 \times C1 + 1)}$$

(30)

The loop gain transfer function is:

$$Tv(s) = Gc(s) \times Gvc(s)$$

(31)

Assume the desired crossover frequency is 60 kHz, then set the compensator zero about 1/10 of the crossover frequency and the compensator pole equal to the ESR zero. The compensator gain is then calculated to achieve the desired bandwidth. In this design, the compensator gain, pole and zero are selected as following:

$$f_p = \frac{1}{2 \times \pi \times R2 \times C1} = 176.8 \text{kHz}$$

(32)

$$f_z = \frac{1}{2 \times \pi \times (R1 + R2) \times C1} = 6 \text{kHz}$$

(33)

$$|Tv (j \times 2 \times \pi \times fc)| = 1$$

(34)

From the above equation, the compensator gain is solved as 3.978×10^5.

$$A_{CM} = \frac{1}{R1 \times C2} = 3.978 \times 10^5$$

(35)

where

- C1 = 2.6 nF
- C2 = 250 pF
- R2 = 350Ω
- Set R1 equal to 10-kΩ, and then calculate all the other components

In the real laboratory practice, the final components are selected as following to increase the phase margin and reduce PWM jitter.

- R1 = 10 kΩ
- C2 = 330 pF
- R2 = 50Ω
- C1 = 2.2 nF

6.1.7 Design Example Summary

Figure 6-2 shows the schematic of the dual output converter design.
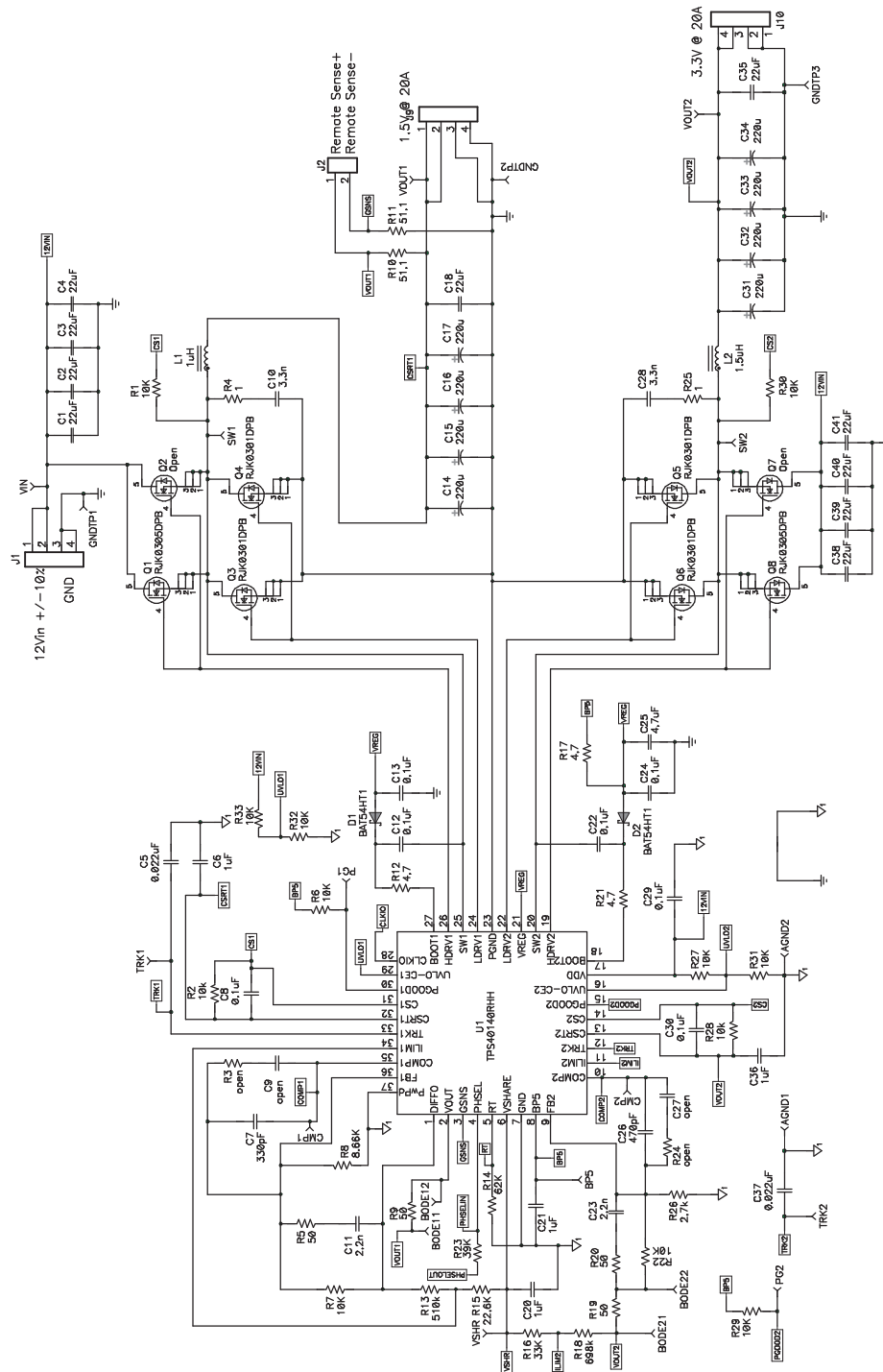
Figure 6-2. Dual Output Converter Schematic

6.2 Example 2: Two-Phase Single Output Configuration From 12 V to 1.5 V DC/DC Converter Using a TPS40140

The following example illustrates the design process and component selection for a two phase single output synchronous buck converter using TPS40140. The design goal parameters are given in Table 6-2. The inductor and MOSFET selection equations are quite similar to the dual output converter design, so they will not be repeated here.

Table 6-2. Design Goal Parameters

| PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.5		V
V_{RIPPLE}	Output ripple	$I_O = 32A$		2%Vo		V
I_{OUT1}	Output current			32		A
f_{sw}	Switching frequency			500		kHz

6.2.1 Step 1: Output Capacitor Selection

The output capacitor is typically selected by the output load transient response requirement. Equation 3 in the dual output design example is used. The inductor L in the equation will be equal to the phase inductance divided by number of phases.

Based on a 15-A load transient with a maximum of 30 mV deviation, a minimum 1.32-µF output capacitor is required. In the design, four 330-µF, 2 V, SP capacitor are selected to meet this requirement. Each capacitor has an ESR of 6 mΩ.

Another criterion for capacitor selection is the output ripple voltage that is determined mainly by the capacitance and the ESR.

Due to the interleaving of channels, the total output ripple current is smaller than the ripple current from a single phase. The ripple cancellation factor is expressed in Equation 36.

$$\Delta I_{OUT}(N_{PH}, D) = \frac{\prod_{i=1}^{N_{PH}} |i - N_{PH} \times D|}{\prod_{i=1}^{N_{PH}-1} (|i - N_{PH} \times D| + 1)}$$

(36)

Where:

D is the duty cycle for a single phase

N_{PH} is the number of active phases, here it is equal to 2

Then the maximum output ripple current is calculated by:

$$I_{RIPPLE} = \frac{V_{OUT}}{L \times f_{SW}} \times \Delta I_{OUT}(N_{PH}, D) = 4.374 \text{ A}$$

(37)

With 1.32 mF output capacitance, the ripple voltage at the capacitor is calculated to be 828 µV. In the specification, the output ripple voltage should be less than 30mV, so based on Equation 4, the required maximum ESR is 6.7 mΩ. The selected capacitors can meet this requirement.

6.2.2 Step 2: Input Capacitor Selection

The input voltage ripple depends on the input capacitance and the ESR. The minimum capacitor and the maximum ESR can be estimated by Equation 5 and Equation 6 in the dual output design example.

For this design, $V_{RIPPLE(CIN)}$ assume is 100mV and $V_{RIPPLE(CinESR)}$ is 50mV, also the inductor ripple current $I_{RIPPLEwill}$ is 30%, so the calculated minimum capacitance is 40µF and the maximum ESR is 2.7 mΩ. Choosing four 22-µF, 16-V, 2-mΩ ESR ceramic capacitors meet this requirement.

Another important thing for the input capacitor is the RMS ripple current rating. Due to the interleaving of multi-phase, the input RMS current is reduced. The input ripple current RMS value over load current is calculated by:

$$\Delta I_{IN(nom)}(N_{PH}, D) =$$

$$\sqrt{\begin{array}{l} [(D - \frac{k(N_{PH}, D)}{N_{PH}}) \times (\frac{k(N_{PH}, D) + 1}{N_{PH}} - D)] + (\frac{N_{PH}}{12 \times D^2}) \times [\frac{V_{OUT} \times (1-D)}{L \times f_{sw} \times I_{OUT}}]^2 \times \\ [(k(N_{PH}, D) + 1)^2 \times (D - \frac{k(N_{PH}, D)}{N_{PH}})^3 + k(N_{PH}, D)^2 \times (\frac{k(N_{PH}, D) + 1}{N_{PH}} - D)^3] \end{array}}$$

(38)

where

- $k(N_{PH}, D) = $ floor $(N_{PH} \times D)$, in this example, $k(N_{PH}, D) = 0$
- Floor(x) is the function to return the greatest integer less than or equal to x
- N_{PH} is the number of active phases, in this example, $N_{PH}=2$

So in this design, the maximum input ripple RMS current is calculated to be 7.2 A with the minimum input voltage. It is about 34% reduction compared with a 32-A single-phase converter design. Each selected ceramic capacitor has a RMS current rating of 4.3 A and, therefore, sufficient to reach this requirement.

6.2.3 Step 3: Peripheral Component Design

6.2.3.1 Switching Frequency Setting (RT pin 5)

$$R = 1.33 \times \left(39.2 \times 10^3 \times f_{SW}^{-1.041} - 7\right) = 71.5 \text{ k}\Omega$$

(39)

Here, f_{sw} represents the phase switching frequency. In the design, a 64.9-kΩ resistor is selected. The actual switching frequency is 490 kHz.

6.2.3.2 COMP1 and COMP2 (pin 35 and pin 10)

COMP1 is connected to the compensator network. The selection of compensation components is similar to the dual output design example.

COMP2 is directly tied to COMP1.

6.2.3.3 TRK1 and TRK2 (pin 33 and pin 12)

A soft start capacitor is connected between TRK1 and GND. TRK2 is directly tied to BP5 to set this channel as a salve.

6.2.3.4 ILIM1 and ILIM2 (pin 34 and pin 11)

ILIM1 is connected to the resistor network that has the same design as the dual output example. The peak current in Equation 22 and Equation 23 is the peak current of each phase.

ILIM2 is grounded.

6.2.3.5 FB1 and FB2 (pin 36 and pin 9)

FB1 is tied to the feedback network. FB2 is connected to GND.

6.2.3.6 PHSEL (pin 4)

For this two phase configuration, the PHSEL pin is directly tied to GND.

6.2.3.7 PGOOD1 and PGOOD2 (pin 30 and pin 15)

Both of PGOOD1 and PGOOD2 are tied to BP5 with a 10-kΩ resistor.

6.2.3.8 CLKIO (pin 28)

CLKIO is open as no clock synchronization required for two phase configuration.

6.2.3.9 DIFFO, VOUT and GSNS (pin 1, pin 2 and pin 3)

VOUT and GSNS should be connected to the remote sensing output connector. DIFFO is connected to the feedback resistor divider. If the differential amplifier is not used, VOUT and GSNS are suggested to be grounded, and DIFFO is left open.

6.2.4 Design Example Summary

Figure 6-3 shows the schematic of the two phase single output converter design.
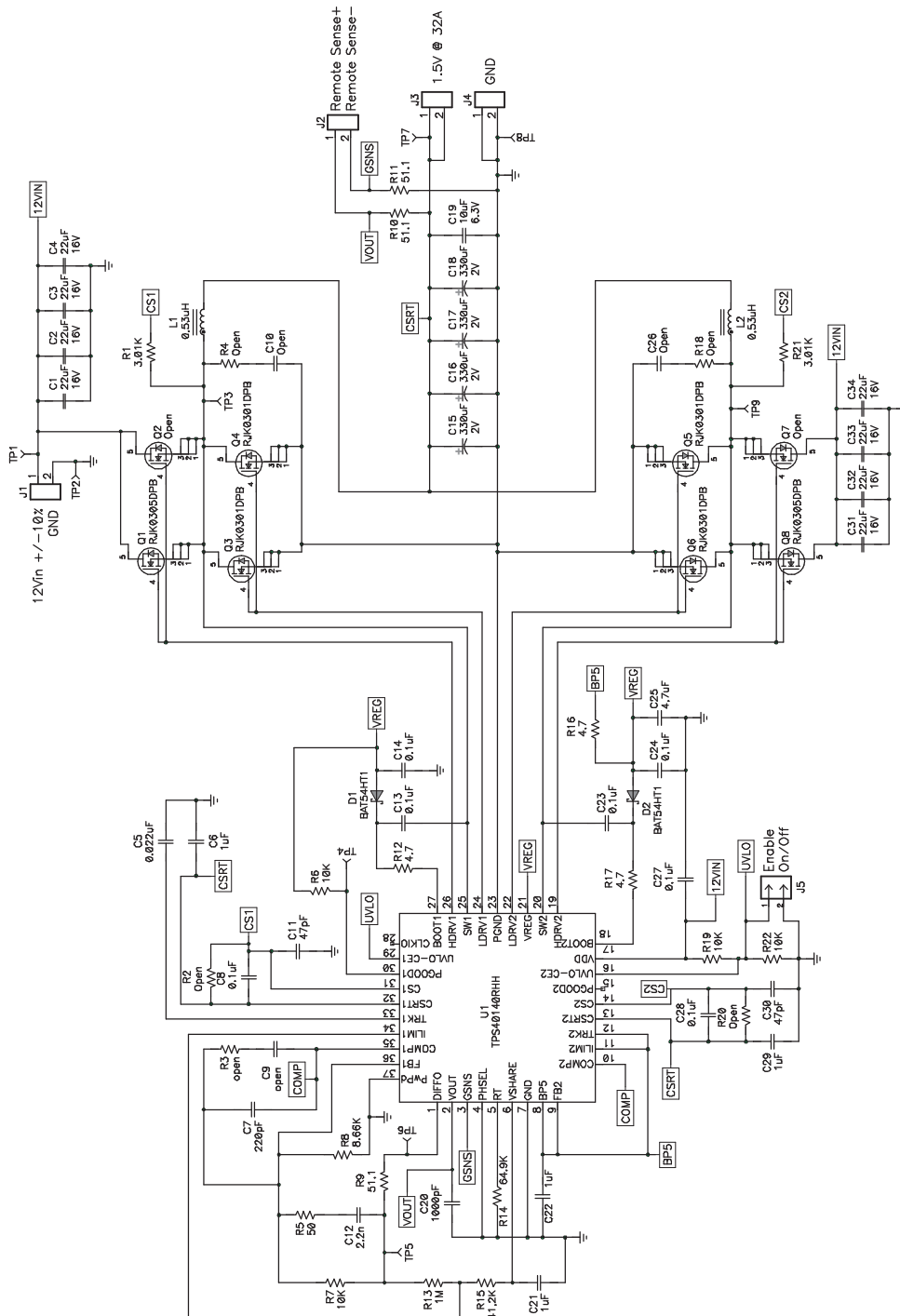

Figure 6-3. Two phase Single Output Converter Schematic

6.3 Example 3: Four-Phase Single Output Configuration From 12 V to 1.8 V DC-to-DC Converter Using Two TPS40140

The following example illustrates the design process and component selection for a four phase single output synchronous buck converter using two TPS40140.

Here, two modules are designed. One is a master module. The other one is a slave module. Each module contains two phases and each phase handle 5-A. The two modules are stacked together to form a 4-phase converter. More slave modules can be stacked to this converter to get the desired phases. The modules are plugged into a mother board.

The design goal parameters are given in Table 6-3.

Table 6-3. Design Goal Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.8		V
V_{RIPPLE}	Output ripple	$I_O = 20A$		1%V_O		V
I_{PH}	Phase current			5		A
f_{sw}	Switching frequency			650		kHz
N_{PH}	Phase number			4		

6.3.1 Step 1: Output Capacitor Selection

The output capacitor is typically selected by the output load transient response requirement. Equation 3 in the dual output design example is used. Also, as mentioned in the two phase design example, the inductor is equivalent to $\dfrac{L}{N_{PH}}$. Based on a 10A load transient with a maximum of 30 mV deviation, a minimum 370μF output capacitor is required. In the design, one 180μF, 6.3V, SP capacitor is placed on the mother board. Four 22-μF, 6,3V ceramic capacitors are placed on each module. The total output capacitance is 356μF.

The output ripple current cancellation factor is calculated to be 0.455 based on Equation 36.

So the maximum output ripple current is calculated by:

$$I_{RIPPLE} = \frac{V_{OUT}}{L \times f_{sw}} \times 0.455 = 1.573A \tag{40}$$

With 356μF output capacitance, the ripple voltage at the capacitor is calculated to be 850 μV. In the specification, the output ripple voltage should be less than 18 mV, so based on Equation 4, the required maximum ESR is 11 mΩ. The selected capacitors can reach this requirement.

6.3.2 Step 2: Input Capacitor Selection

The input voltage ripple depends on the input capacitance and the ESR. The minimum capacitor and the maximum ESR can be estimated by Equation 5 and Equation 6 in the dual output design example.

For this design, assume is 50mV and is 30mV, also each phase inductor ripple current is 50%, so the calculated minimum capacitance is 93-μF and the maximum ESR is 4.6 mΩ. In this case, one 33-μF 6.3-V SP-capacitor is placed on the mother board and each module has two 22-μF, 6.3-V ceramic capacitors.

The maximum input ripple RMS current is calculated to be 2.57 A with the minimum input voltage based on Equation 38. The selected capacitors are sufficient to meet this requirement.

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6.3.3 Step 3: Peripheral Component Design

6.3.3.1 Master Module

6.3.3.1.1 RT (pin 5)

It is connected to GND with a resistor that sets the switching frequency.

$$R = 1.33 \times \left(39.2 \times 10^3 \times f_{SW}^{-1.041} - 7\right) = 52.2 \text{ k}\Omega \tag{41}$$

Here, f_{sw} represents the phase switching frequency. In the design, a 47-kΩ resistor is selected. The actual switching frequency is 650 kHz.

6.3.3.1.2 COMP1 and COMP2 (pin 35 and pin 10)

COMP1 is connected to the compensator network.

COMP2 is directly tied to COMP1.

6.3.3.1.3 TRK1 and TRK2 (pin 33 and pin 12)

A soft start capacitor is connected between TRK1 and GND. TRK2 is directly tied to BP5 to set this channel as a salve.

6.3.3.1.4 ILIM1 and ILIM2 (pin 34 and pin 11)

ILIM1 is connected to the resistor network that has the same design as the dual output example. The peak current in Equation 22 and Equation 23 is the peak current of each phase.

ILIM2 is grounded.

6.3.3.1.5 FB1 and FB2 (pin 36 and pin 9)

FB1 is tied to the feedback network. FB2 is connected to GND.

6.3.3.1.6 PHSEL (pin 4)

For this four phase configuration, the PHSEL pin is tied to GND with a 39-kΩ resistor.

6.3.3.1.7 PGOOD1 and PGOOD2 (pin 30 and pin 15)

Both of PGOOD1 and PGOOD2 are tied to BP5 with a 10-kΩ resistor.

6.3.3.1.8 CLKIO (pin 28)

CLKIO is connected to the same pin in the salve module.

6.3.3.2 Slave Module:

6.3.3.2.1 RT (pin 5)

It is connected to BP5. The slave module receives the clock from the master module.

6.3.3.2.2 COMP1 and COMP2 (pin 35 and pin 10)

Both of COMP1 and COMP2 are directly tied together to COMP1 or COMP2 in the master module.

6.3.3.2.3 TRK1 and TRK2 (pin 33 and pin 12)

Both TRK1 and TRK2 are directly tied to BP5.

6.3.3.2.4 ILIM1 and ILIM2 (pin 34 and pin 11)

Both ILIM1 and ILIM2 are grounded.

6.3.3.2.5 FB1 and FB2 (pin 36 and pin 9)

Both FB1 and FB2 are connected to GND.

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6.3.3.2.6   PHSEL (pin 4)

The PHSEL pin is directly tied to GND.

6.3.3.2.7   PGOOD1 & PGOOD2 (pin 30 & pin 15)

Both of PGOOD1 and PGOOD2 are tied to BP5 with a 10-kΩ resistor.

6.3.3.2.8   CLKIO (pin 28)

CLKIO is connected to the master module CLKIO.

6.3.4 Design Example Summary

Figure 6-4, Figure 6-5 and Figure 6-6 shows the schematics of the four phase converter design.
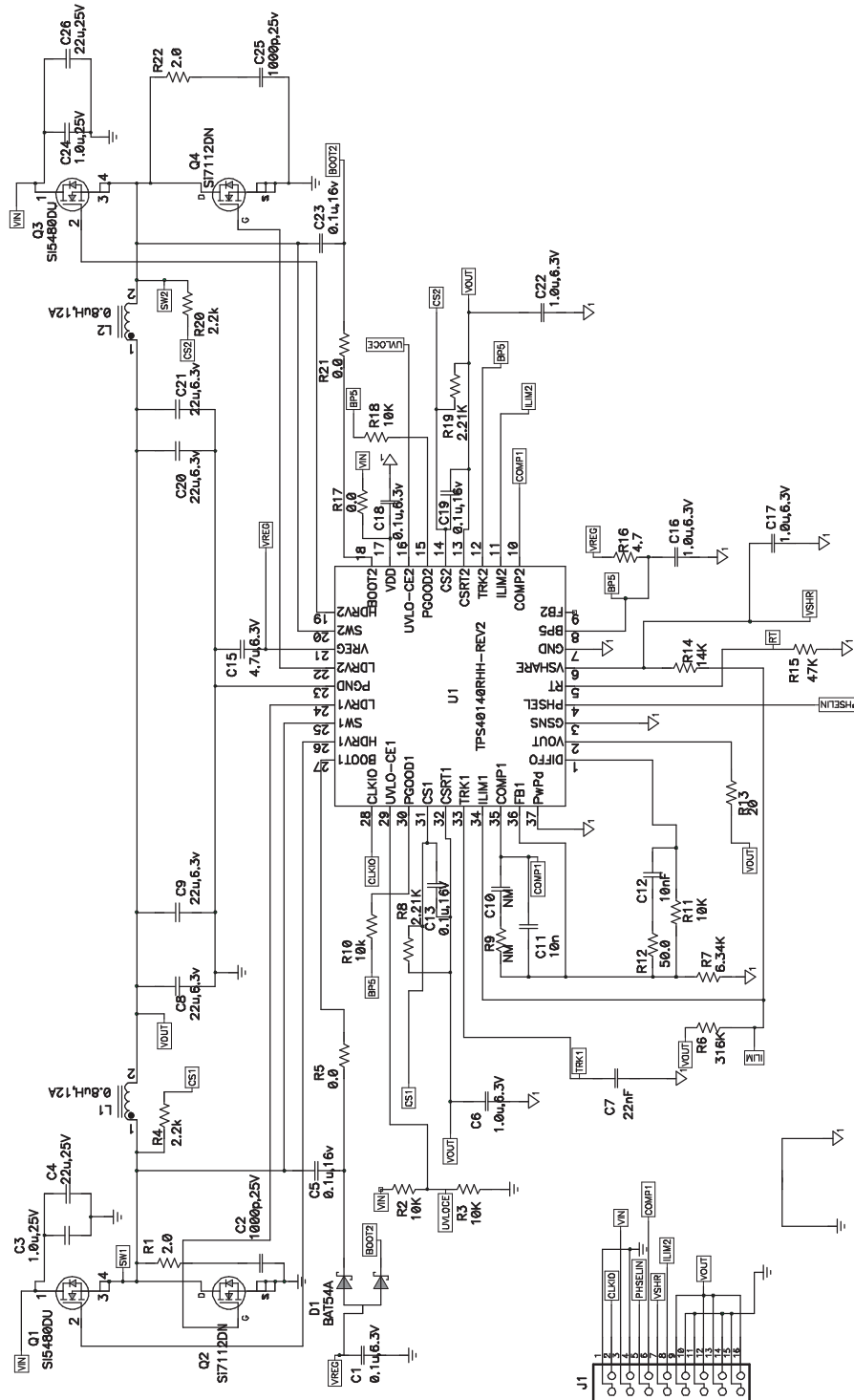

Figure 6-4. Master Module Schematic
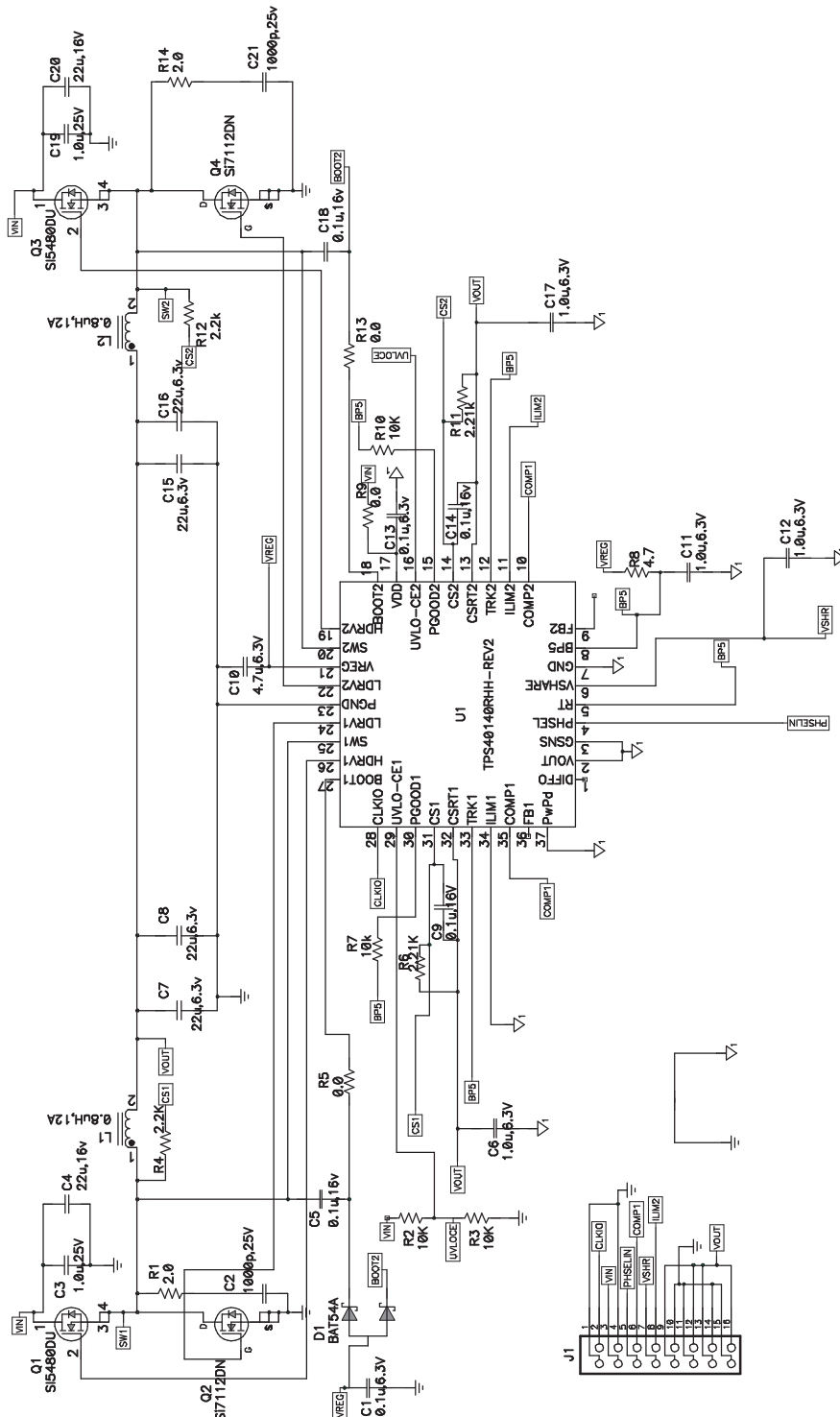
Figure 6-5. Slave Module Schematic
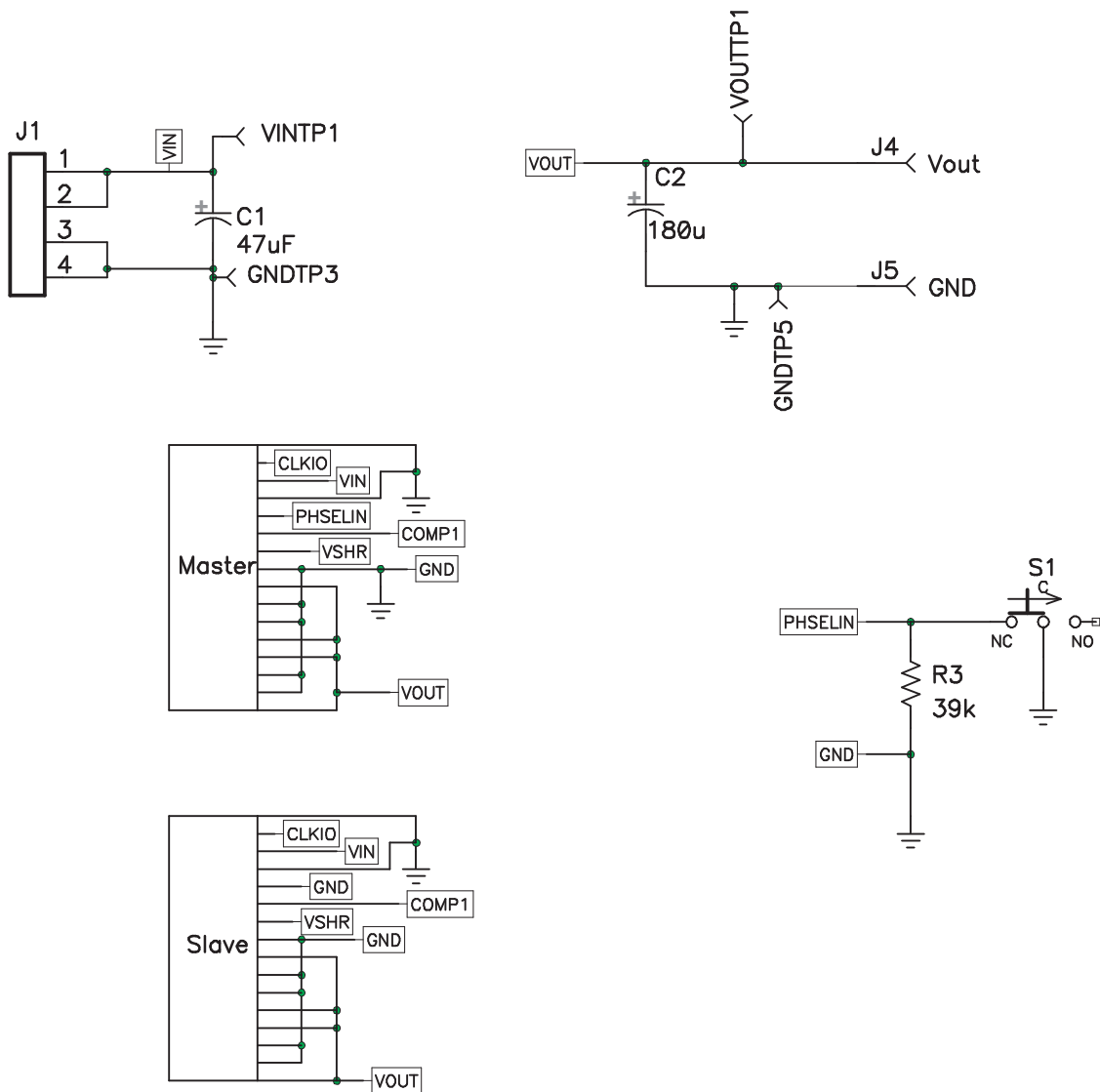
Figure 6-6. Mother Board Schematic

6.4 ABBREVIATIONS

Table 6-4. Definition of Symbols

SYMBOL	DESCRIPTION
$V_{IN(min)}$	Minimum Operating Input voltage
$V_{IN(max)}$	Maximum Operating Input Voltage
V_{OUT}	Output Voltage
I_{RIPPLE}	Inductor Peak-Peak Ripple Current
$I_{TRAN(MAX)}$	Maximum Load Transient
V_{UNDER}	Output Voltage Undershot
V_{OVER}	Output Voltage Overshot
$V_{RIPPLE(TotOUT)}$	Total Output Ripple
$V_{RIPPLE(COUT)}$	Output Voltage Ripple Due to Output Capacitance
$V_{RIPPLE(CIN)}$	Input Voltage Ripple Due to Input Capacitance
$V_{RIPPLE(CinESR)}$	Input Voltage Ripple Due to the ESR of Input Capacitance
Psw_{cond}	High Side MOSFET Conduction Loss
Isw_{rms}	RMS Current in the High Side MOSFET
Rdson(sw)	*ON* Drain-Source Resistance of the High Side MOSFET
Psw_{sw}	High Side MOSFET Switching Loss
Ipk	Peak Current Through the High Side MOSFET
R_{drv}	Driver Resistance of the High Side MOSFET
Qgd_{sw}	Gate to Drain Charge of the High Side MOSFET
Qgs_{sw}	Gate to Source Charge of the High Side MOSFET
Vgsw	Gate Drive Voltage of the High Side MOSFET
Psw_{gate}	Gate Drive Loss of the High Side MOSFET
Qg_{sw}	Gate Charge of the High Side MOSFET
Psw_{tot}	Total Losses of the High Side MOSFET
Psr_{cond}	Low Side MOSFET Conduction Loss
Isr_{rms}	RMS Current in the Low Side MOSFET
Rdson(sr)	*ON* Drain-Source Resistance of the low Side MOSFET
Psr_{gate}	Gate Drive Loss of the Low Side MOSFET
Qg_{sr}	Gate Charge of the Low Side MOSFET
Vgsr	Gate Drive Voltage of the Low Side MOSFET
P_{diode}	Power Loss in the Diode
t_d	Dead Time Between the Conduction of High and Low Side MOSFET
V_f	Forward Voltage Drop of the Body Diode of the Low Side MOSFET
Psr_{tot}	Total Losses of the Low Side MOSFET
DCR	Inductor DC Resistance
Ac	The Gain of the Current Sensing Amplifier, typically it is 13
R_{OUT}	Output Load Resistance
V_{ramp}	Ramp Amplitude, typically it is 0.5V
T	Switching Period
Gvc(s)	Control to Output Transfer Function
Gc(s)	Compensator Transfer Function
Tv(s)	Loop Gain Transfer Function
Acm	Gain of the Compensator
f_p	The Pole Frequency of the Compensator
f_z	The Zero Frequency of the Compensator

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6.5 LAYOUT CONSIDERATIONS

6.5.1 Power Stage

A synchronous BUCK power stage has two primary current loops – The input current loop which carries high AC discontinuous current while the output current loop carries high DC continuous current. The input current loop includes the input capacitors, the main switching MOSFET, the inductor, the output capacitors and the ground path back to the input capacitors. To keep this loop as small as possible, it is generally good practice to place some ceramic capacitance directly between the drain of the main switching MOSFET and the source of the synchronous rectifier (SR) through a power ground plane directly under the MOSFETs. The output current loop includes the SR MOSFET, the inductor, the output capacitors, and the ground return between the output capacitors and the source of the SR MOSFET. As with the input current loop, the ground return between the output capacitor ground and the source of the SR MOSFET should be routed under the inductor and SR MOSFET to minimize the power loop area. The SW node area should be as small as possible to reduce the parasitic capacitance and minimize the radiated emissions. The gate drive loop impedance (HDRV-gate-source-SW and LDRV-gate-source- GND) should be kept to as low as possible. The HDRV and LDRV connections should widen to 20mils as soon as possible out from the IC pin.

6.5.2 Device Peripheral

The TPS40140 provides separate signal ground (GND) and power ground (PGND) pins. It is required to separate properly the circuit grounds. The return path for the pins associated with the power stage should be through PGND. The other pins especially for those sensitive pins such as FB, RT and ILIM should be through the low noise GND. The GND and PGND plane are suggested to be connected at the output capacitor with single 20 mil trace. A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and GND as possible with at least 15-mil wide trace from the bypass capacitor to the GND. A 4.7-µF ceramic capacitor should be placed as close to VREG pin and GND as possible. BP5 is the filtered input from the VREG pin. A 4.7 -Ω resistor should be connected between VREG and BP5 and a 1-µF ceramic capacitor should be connected from BP5 to GND. Both components should be as close to BP5 pin as possible. When DCR sensing method is applied, the sensing resistor is placed close to the SW node. It is connected to the inductor with Kelvin connection. The sensing traces from the power stage to the chip should be away from the switching components. The sensing capacitor should be placed very close to the CS and CSRT pins. The frequency setting resistor should be placed as close to RT pin and GND as possible. The VOUT and GSNS pins should be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They should be away from the switching components. The PowerPAD should be electrically connected to GND.

6.5.3 PowerPAD™ Layout

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0,33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter plus 0,1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to PowerPAD™ Thermally Enhanced Package for more information on the PowerPAD™ package.

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7 ADDITIONAL REFERENCES

7.1 Related Parts

The following parts have characteristics similar to the TPS40140 and may be of interest.

DEVICE	DESCRIPTION
TPS40130	Two-Phase Synchronous Buck Controller with Integrated MOSFET Drivers
TPS40090	4-Channel Multi-Phase DC/DC Controller with Three State
TPS40120	Feedback Divider, Digitally Controlled

7.2 References

These references may be found on the web at www.power.ti.com under Technical Documents. Many design tools and links to additional references, including design software, may also be found at www.power.ti.com

1. *Under The Hood Of Low Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series

2. *Understanding Buck Power Stages in Switchmode Power Supplies* (SLVA057) March 1999

3. *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series

4. *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series

5. Additional PowerPAD^{TM} information may be found in Applications Briefs (SLMA002) and (SLMA004)

6. QFN/SON PCB Attachment, Texas Instruments (SLUA271), June 2002

7.3 Package Outline

The outlines of the mechanical dimensions of the RHH package are shown.

7.4 Recommended PCB Footprint

The outlines the recommended PCB layout are shown.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS40140RHHR	ACTIVE	QFN	RHH	36	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS40140RHHRG4	ACTIVE	QFN	RHH	36	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS40140RHHT	ACTIVE	QFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TPS40140RHHTG4	ACTIVE	QFN	RHH	36	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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MECHANICAL DATA

RHH (S−PQFP−N36) PLASTIC QUAD FLATPACK

6,00 A

B

6,00

36
1

PIN 1
INDEX AREA

1,00
0,80

0,08 C

0,20 REF

C

SEATING PLANE

0,05 MAX

1

36

4X 4,00

0,50

36X 0,65
0,45

EXPOSED THERMAL PAD
D

36X 0,30
0,18

⊕ 0,10 Ⓜ C A B

4205094/B 11/04
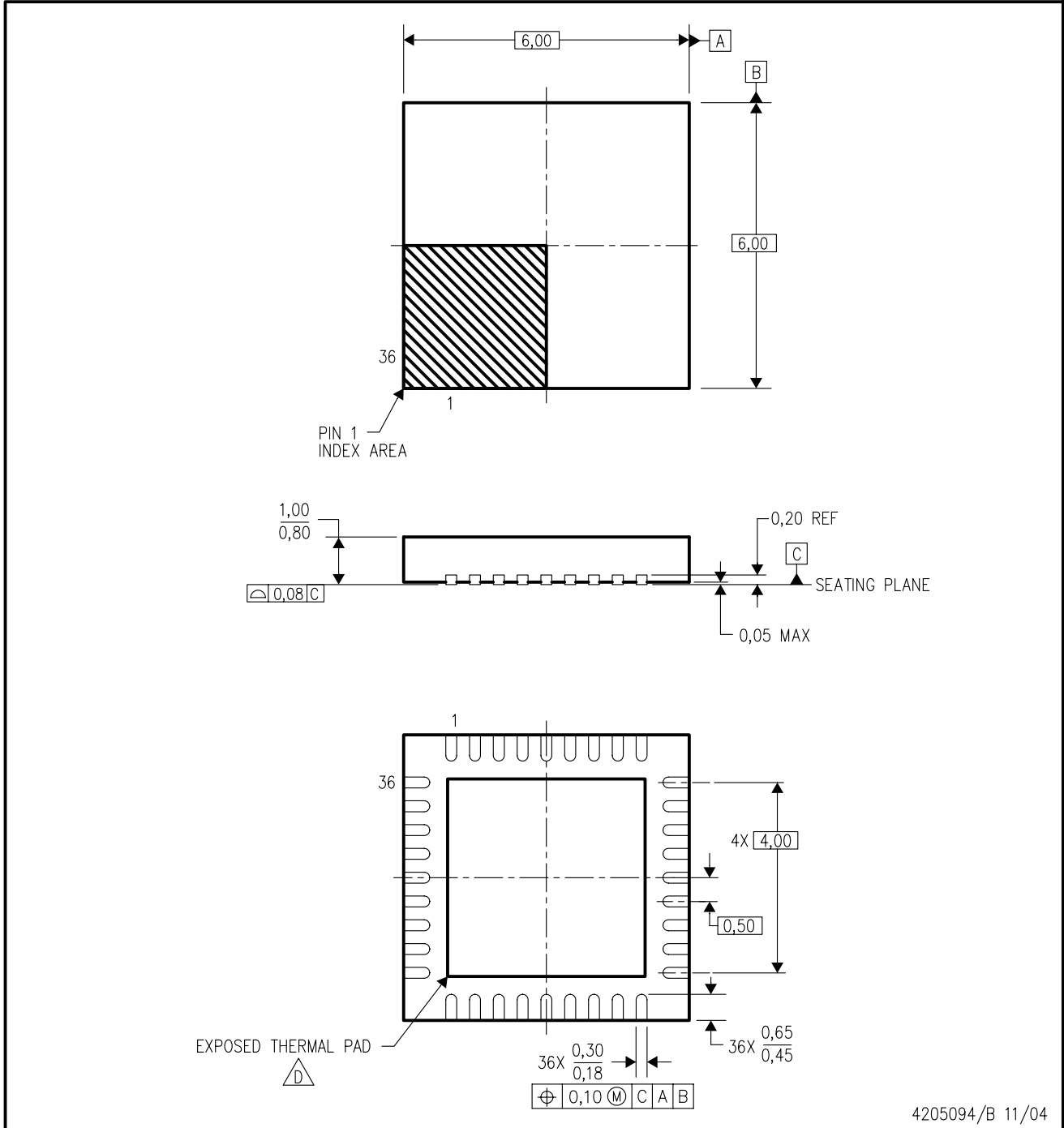
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No−Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO−220.

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THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No−Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
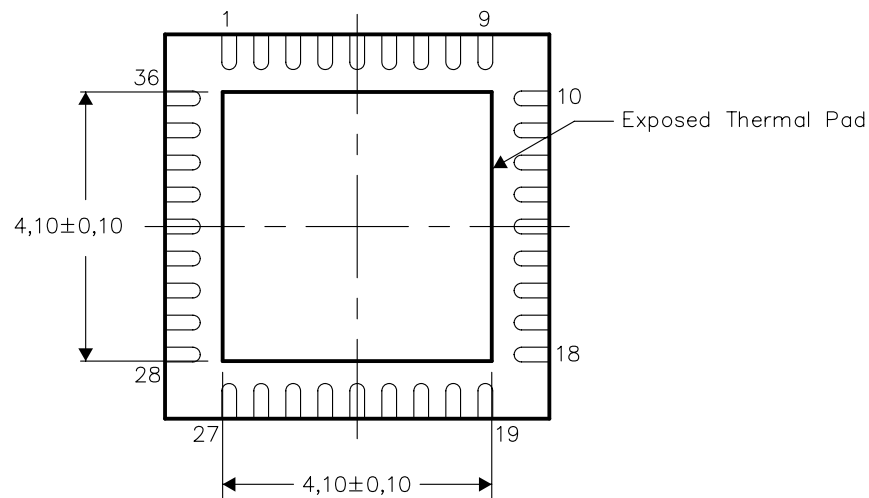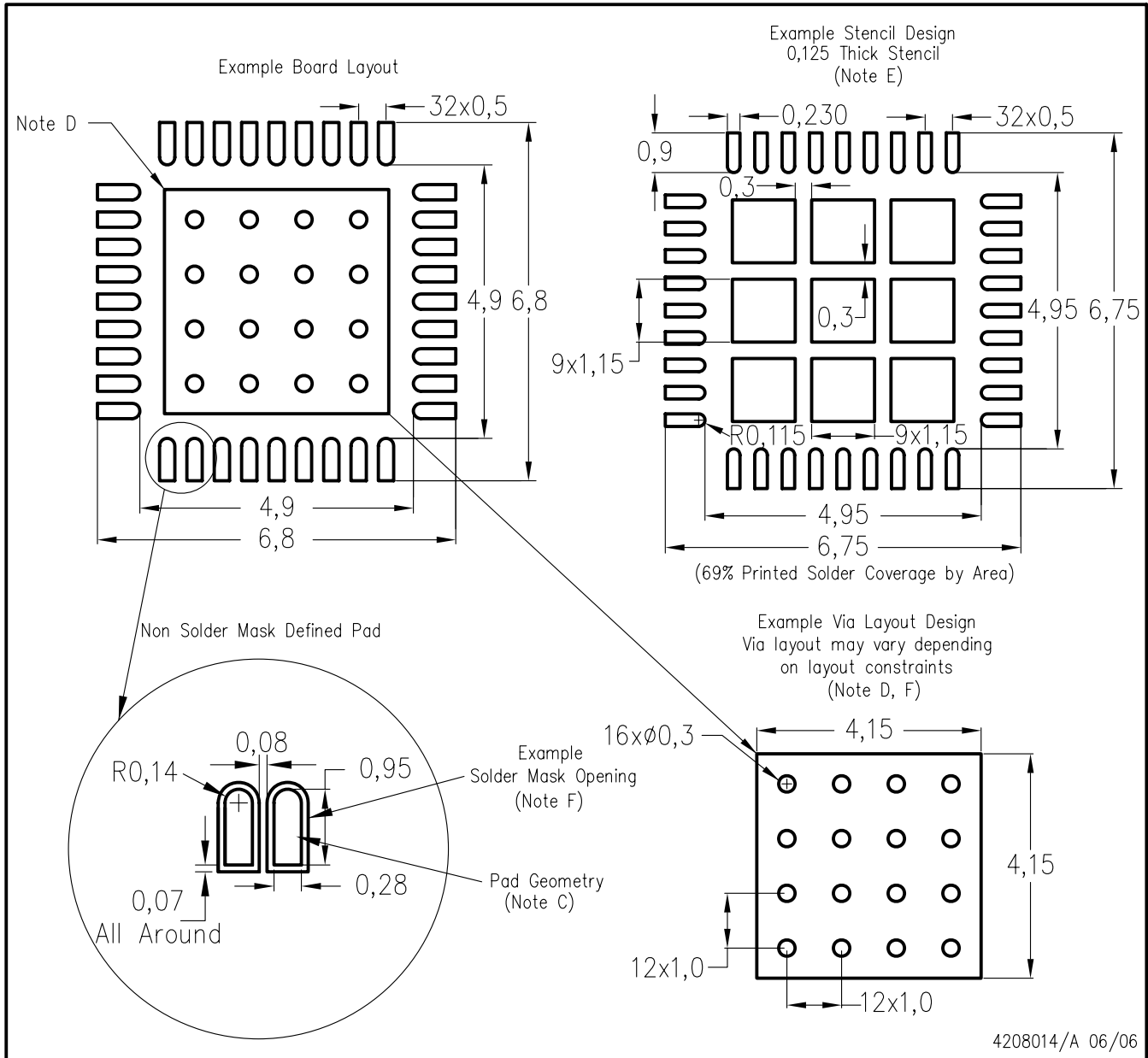

Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHH (S—PQFP—N36)

Example Board Layout

Note D

32x0,5

4,9 6,8

4,9
6,8

Example Stencil Design
0,125 Thick Stencil
(Note E)

0,230   32x0,5

0,9

0,3

0,3

9x1,15

4,95 6,75

R0,115   9x1,15

4,95
6,75

(69% Printed Solder Coverage by Area)

Non Solder Mask Defined Pad

R0,14

0,08

0,95

0,07
All Around

0,28

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

16x⌀0,3   4,15

4,15

12x1,0

12x1,0

4208014/A 06/06

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC—7351 is recommended for alternate designs.
         D.   This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack
              Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
              for specific thermal information, via requirements, and recommended board layout. These documents are available at
              www.ti.com <http://www.ti.com>.
         E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
         F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
              recommendations for vias placed in the thermal pad.

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