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**TPS40200-EP**

# WIDE-INPUT-RANGE NONSYNCHRONOUS VOLTAGE-MODE CONTROLLER

## FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** [1]
- **Input Voltage Range 4.5 V to 52 V**
- **Output Voltage (700 mV to 87% $V_{in}$)**
- **200-mA Internal P-Channel FET Driver**
- **Voltage Feed-Forward Compensation**
- **Undervoltage Lockout**

[1] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Programmable Fixed-Frequency (35 kHz to 500 kHz) Operation**
- **Programmable Short-Circuit Protection**
- **Hiccup Overcurrent Fault Recovery**
- **Programmable Closed-Loop Soft Start**
- **700-mV 1% Reference Voltage**
- **External Synchronization**
- **Small 8-Pin Small-Outline Integrated Circuit (SOIC) (D) Package**

## APPLICATIONS

- **Industrial Control**
- **Distributed Power Systems**
- **DSL/Cable Modems**
- **Scanners**
- **Telecom**

## DESCRIPTION

The TPS40200 is a flexible nonsynchronous controller with a built-in 200-mA driver for P-channel FETs. The circuit operates with inputs up to 52 V, with a power-saving feature that turns off driver current once the external FET has been fully turned on. This feature extends the flexibility of the device, allowing it to operate with an input voltage up to 52 V, without dissipating excessive power. The circuit operates with voltage-mode feedback and has feed-forward input-voltage compensation that responds instantly to input-voltage change. The integral 700-mV reference is trimmed to 2%, providing the means to accurately control low voltages. The TPS40200 is available in an 8-pin SOIC, and supports many of the features of more complex controllers. Clock frequency, soft start, and overcurrent limit each are easily programmed by a single, external component. The part has undervoltage lockout, and can be easily synchronized to other controllers or a system clock to satisfy sequencing and/or noise-reduction requirements.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas

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# TPS40200-EP

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
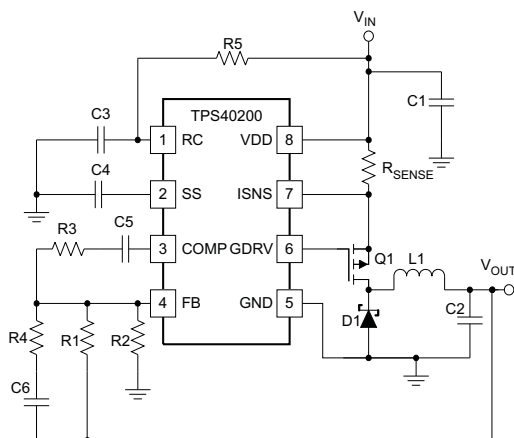
## TYPICAL APPLICATION



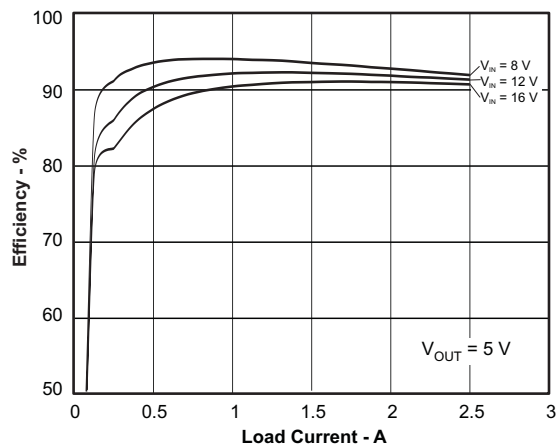**Figure 1. 12-V to 5-V Buck Converter With 94% Efficiency**



**Figure 2. Typical Efficiency of Application Circuit 1 (Described in Application 1)**

## ELECTROSTATIC DISCHARGE (ESD) PROTECTION

|  | MIN | MAX | UNIT |
|---|---|---|---|
| Human-Body Model |  | 1500 | V |
| CDM |  | 1500 | V |

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

|  |  |  | UNIT |
|---|---|---|---|
| Input voltage range | $V_{DD}$, ISNS | 52 | V |
|  | RC, FB | −0.3 to 5.5 |  |
|  | SS | −0.3 to 9 |  |
| Output voltage range | COMP | −0.3 to 9 | V |
|  | GDRV | ($V_{IN}$ − 10) to $V_{IN}$ |  |
| $T_J$ Operating virtual junction temperature range |  | −55 to 150 | °C |
| $T_{stg}$ Storage temperature range |  | −55 to 150 | °C |
| Lead temperature 1,6 mm (1/16 in) from case for 10 s |  | 260 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

|  | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{DD}$   Input voltage | 4.5 | 52 | V |

## ELECTRICAL CHARACTERISTICS

$-55°C < T_A = T_J < 125°C$, $V_{DD} = 12$ V, $f_{OSC} = 100$ kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **Voltage Reference** | | | | | | | | |
| $V_{FB}$ | Feedback voltage | COMP = FB, $T_J = 25°C$ | | | 689 | 696 | 702 | mV |
| | | $4.5$ V $< V_{DD} < 52$ V | $T_J = 25°C$ | | 686 | 696 | 703 | |
| | | | $-40°C < T_J < 125°C$ | | 679 | 696 | 710 | |
| | | | $-55°C < T_J < 125°C$ | | 675 | 696 | 710 | |
| **Gate Driver** | | | | | | | | |
| $I_{src}$ | Gate driver pullup current | | | | 125 | 300 | | mA |
| $I_{snk}$ | Gate driver pulldown current | | | | 200 | 300 | | mA |
| $V_{GATE}$ | Gate driver output voltage | $V_{GATE} = (V_{DD} - V_{GDRV})$, for 12 V $< V_{DD} < 52$ V | | | 6 | 8 | 10 | V |
| **Quiescent Current** | | | | | | | | |
| $I_{qq}$ | Device quiescent current | $F_{OSC} = 300$ kHz, Driver not switching, $4.5$ V $< V_{DD} < 52$ V | | | | 1.5 | 3 | mA |
| **Undervoltage Lockout (UVLO)** | | | | | | | | |
| $V_{UVLO(on)}$ | Turnon threshold | | | | 3.8 | 4.25 | 4.5 | V |
| $V_{UVLO(off)}$ | Turnoff threshold | | | | | 4.05 | | |
| $V_{UVLO(HYST)}$ | Hysteresis | | | | 110 | 200 | 275 | mV |
| **Soft Start** | | | | | | | | |
| $R_{SS(chg)}$ | Internal soft-start pullup resistance | | | | 65 | 105 | 170 | kΩ |
| $R_{SS(dchg)}$ | Internal soft-start pulldown resistance | | | | 190 | 305 | 485 | kΩ |
| $V_{SSRST}$ | Soft-start reset threshold | | | | 100 | 150 | 200 | mV |
| **Overcurrent Protection** | | | | | | | | |
| $V_{ILIM}$ | Overcurrent threshold | $4.5$ V $< V_{DD} < 52$ V | $0°C < T_J < 125°C$ | | 65 | 100 | 140 | mV |
| | | | $-40°C < T_J < 125°C$ | | 55 | 100 | 140 | |
| | | | $-55°C < T_J < 125°C$ | | 35 | 100 | 150 | |
| $OC_{DF}$ | Overcurrent duty cycle[1] | | | | | | 2 | % |
| $V_{ILIM(rst)}$ | Overcurrent reset threshold | | | | 100 | 150 | 200 | mV |
| **Oscillator** | | | | | | | | |
| $F_{OSC}$ | Oscillator frequency range[1] | | | | 35 | | 500 | kHz |
| | Oscillator frequency | $R_{RC} = 200$ kΩ, $C_{RC} = 470$ pF | | | 85 | 100 | 115 | |
| | | $R_{RC} = 68.1$ kΩ, $C_{RC} = 470$ pF | | | 255 | 300 | 345 | |
| | Frequency line regulation | 12 V $< V_{DD} < 52$ V | | | $-9$ | | 0 | % |
| | | $4.5$ V $< V_{DD} < 12$ V | | | $-20$ | | 0 | |
| $V_{RMP}$ | Ramp amplitude | $4.5$ V $< V_{DD} < 52$ V | | | | $V_{DD} \div 10$ | | V |
| **Pulse-Width Modulator** | | | | | | | | |
| $t_{MIN}$ | Minimum controllable pulse width | $V_{DD} = 12$ V | | | | 200 | 500 | ns |
| | | $V_{DD} = 30$ V | | | | 100 | 200 | |
| $D_{MAX}$ | Maximum duty cycle | $F_{OSC} = 100$ kHz, $C_L = 470$ pF | | | 93 | 95 | | % |
| | | $F_{OSC} = 300$ kHz, $C_L = 470$ pF | | | 87 | 93 | | |
| $K_{PWM}$ | Modulator and power-stage dc gain | | | | 8 | 10 | 12 | V/V |
| **Error Amplifier** | | | | | | | | |
| $I_{IB}$ | Input bias current | | | | | 100 | 250 | nA |
| AOL | Open-loop gain[1] | | | | 60 | 80 | | dB |
| GBWP | Unity gain bandwidth[1] | | | | 1.5 | 3 | | MHz |
| $I_{COMP(src)}$ | Output source current | $V_{FB} = 0.6$ V, COMP = 1 V | | | 100 | 250 | | µA |

(1) By design only. Not tested in production.

# TPS40200-EP

## ELECTRICAL CHARACTERISTICS (continued)

$-55°C < T_A = T_J < 125°C$, $V_{DD} = 12$ V, $f_{OSC} = 100$ kHz (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{COMP(snk)}$ | Output sink current | $V_{FB} = 1.2$ V, COMP = 1 V | 1.0 | 2.5 | | mA |

## THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $\theta_{JC}$ | Thermal resistance, junction to case | (1) | 49 | °C/W |
| $\theta_{JA}$ | Thermal resistance, junction to ambient | (1)HIGH-K | 97.5 | °C/W |
| $\theta_{JA}$ | Thermal resistance, junction to ambient | (1)LOW-K | 176 | °C/W |

(1)  TI uses test boards designed to JESD 51-3 and JESD 51-7 for thermal-impedance measurements. The parameters outlined in these standards also are used to set up thermal models.

### ORDERING INFORMATION

| $T_A$ | OUTPUT VOLTAGE | PACKAGE | ORDERABLE PART NUMBER | MEDIUM | QUANTITY |
|---|---|---|---|---|---|
| −55°C to 125°C | Adjustable | SOIC – D | TPS40200MDREP | Tape and reel | 2500/reel |

### DEVICE INFORMATION

#### Functional Block Diagram



D PACKAGE
(TOP VIEW)

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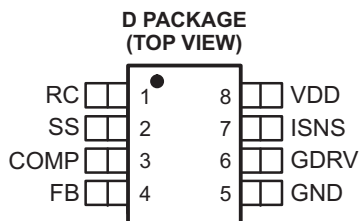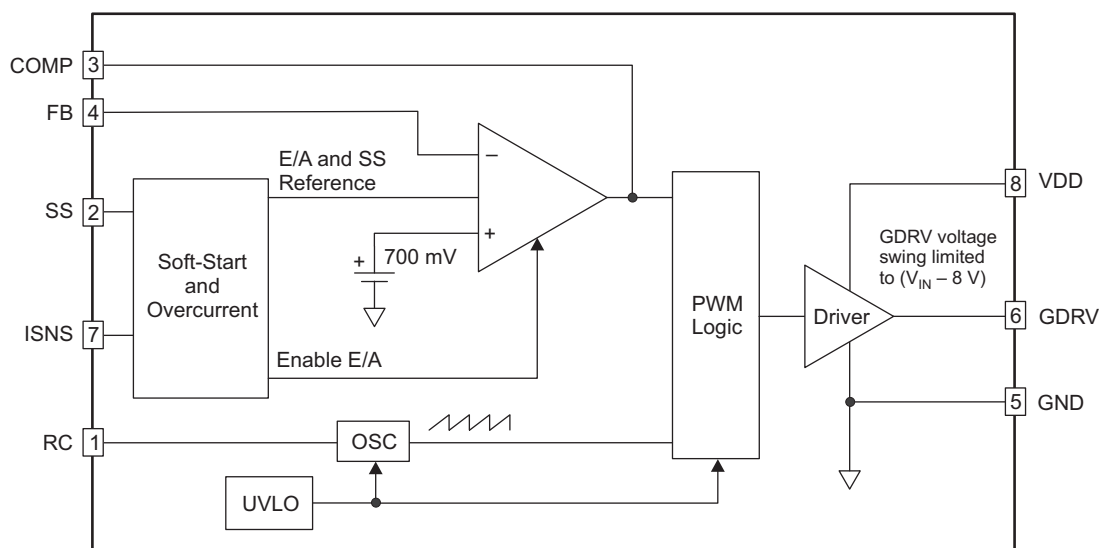
## DEVICE INFORMATION (continued)

### TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| RC | 1 | I | Switching frequency-setting RC network. Connect capacitor from RC pin to GND pin and resistor from $V_{IN}$ pin to RC pin. The device may be synchronized to an external clock by connecting an open-drain output to this pin and pulling it to GND. The pulse width for synchronization should not be excessive. |
| SS | 2 | I | Soft-start programming pin. Connect capacitor from SS to GND to program soft-start time. Pulling this pin below 150 mV causes the output switching to stop, placing the device in a shutdown state. The pin also functions as a restart timer for overcurrent events. |
| COMP | 3 | O | Compensation. Error amplifier output. Connect control-loop compensation network from COMP to FB. |
| FB | 4 | I | Feedback. Error amplifier inverting input. Connect feedback resistor network center tap to this pin. |
| GND | 5 | | Device ground |
| GDRV | 6 | O | Driver output for external P-channel MOSFET |
| ISNS | 7 | I | Current-sense comparator input. Connect a current sense resistor between ISNS and $V_{DD}$ in order to set desired overcurrent threshold. |
| VDD | 8 | I | System input voltage. Connect local bypass capacitor from $V_{DD}$ to GND. |

## TYPICAL CHARACTERISTICS

**QUIESCENT CURRENT vs TEMPERATURE**
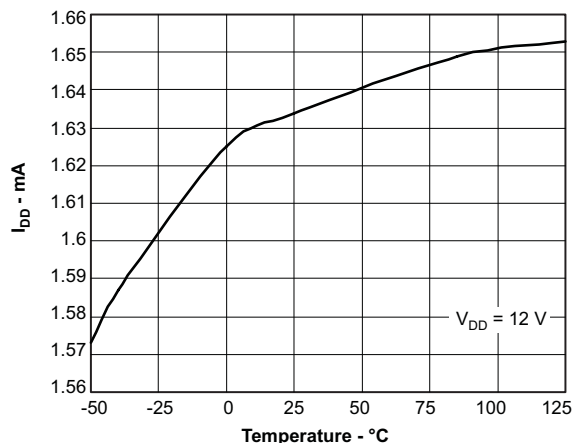


Figure 3.

**QUIESCENT CURRENT vs $V_{DD}$**
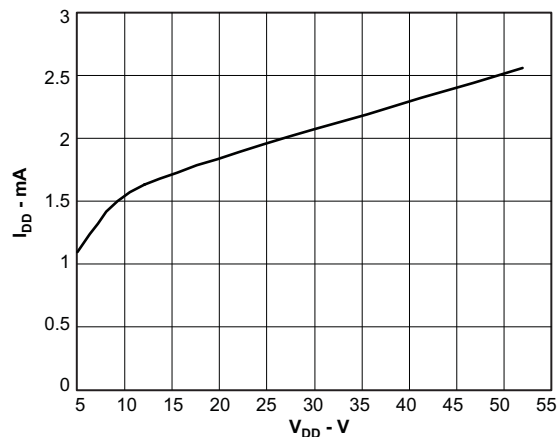


Figure 4.

**SOFT-START THRESHOLD vs TEMPERATURE**
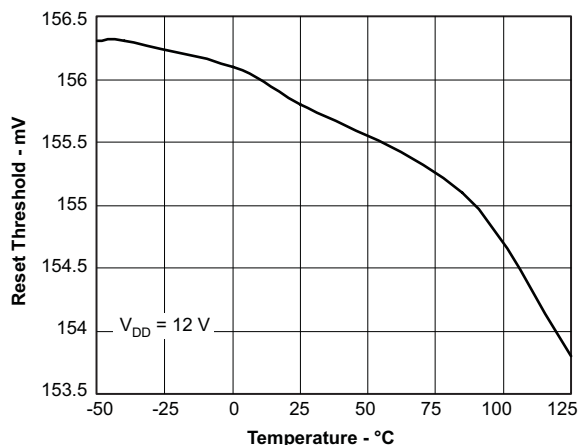


Figure 5.

**UVLO TURNON AND TURNOFF vs TEMPERATURE**
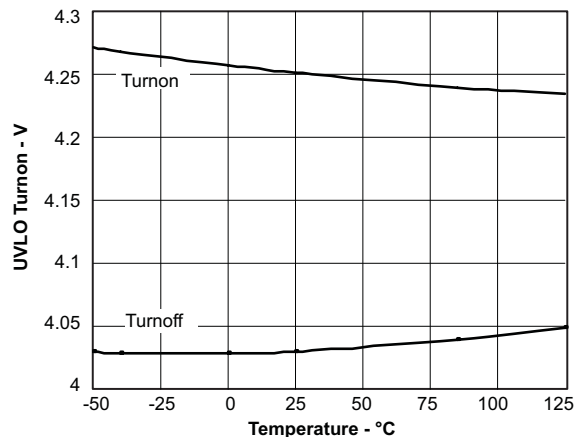


Figure 6.

**TPS40200-EP**
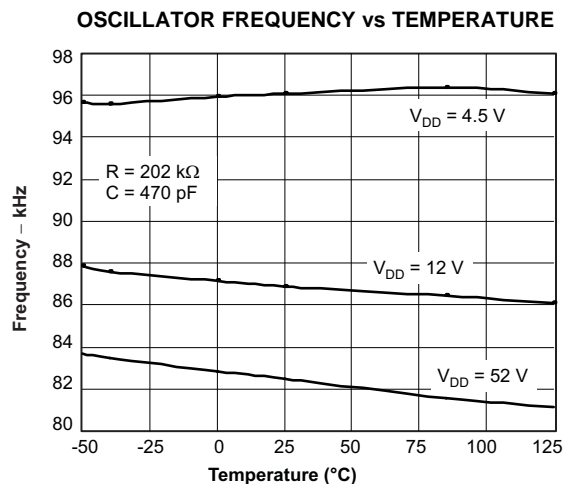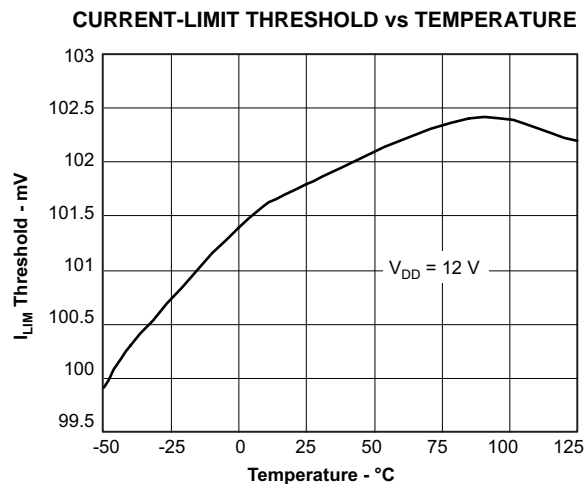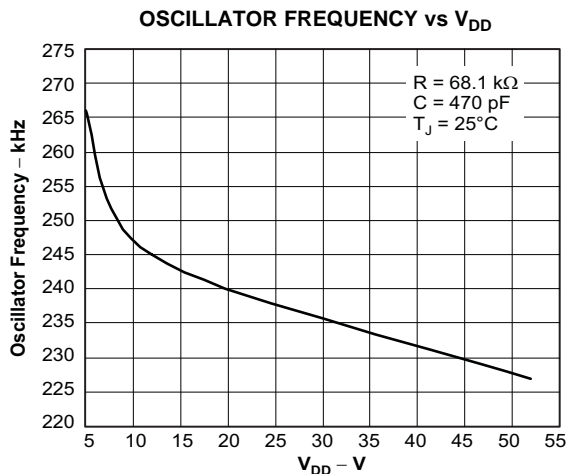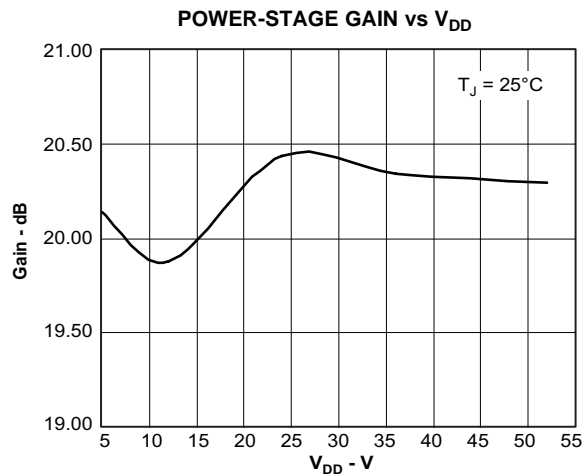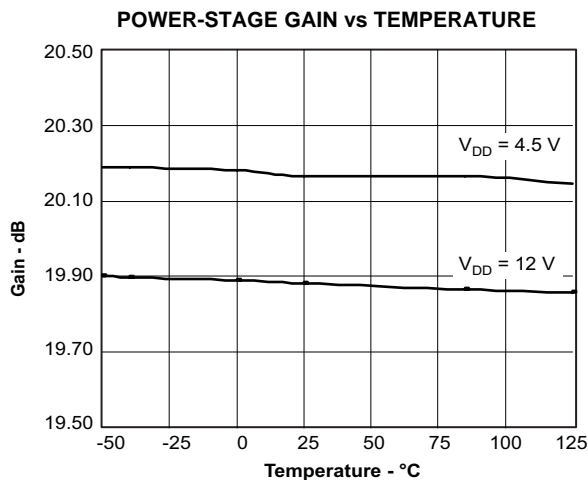
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# TYPICAL CHARACTERISTICS (continued)

OSCILLATOR FREQUENCY vs TEMPERATURE



Figure 7.

CURRENT-LIMIT THRESHOLD vs TEMPERATURE



Figure 8.

OSCILLATOR FREQUENCY vs V_DD



Figure 9.

POWER-STAGE GAIN vs V_DD



Figure 10.

POWER-STAGE GAIN vs TEMPERATURE



Figure 11.

POWER-STAGE GAIN vs TEMPERATURE



Figure 12.

6

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## TYPICAL CHARACTERISTICS (continued)

MODULATOR RAMP AMPLITUDE vs TEMPERATURE



**Figure 13.**

MODULATOR RAMP AMPLITUDE vs TEMPERATURE



**Figure 14.**

MODULATOR RAMP AMPLITUDE vs $V_{DD}$



**Figure 15.**

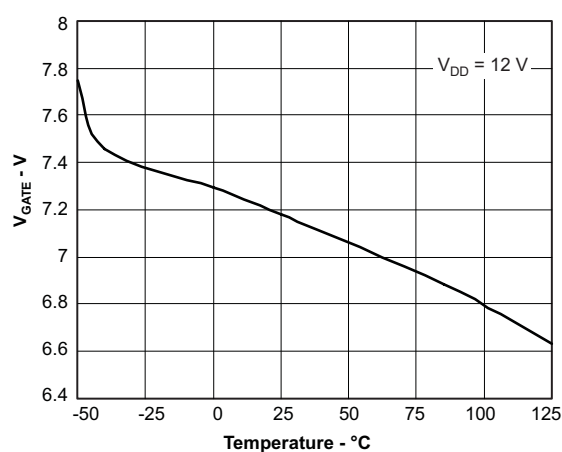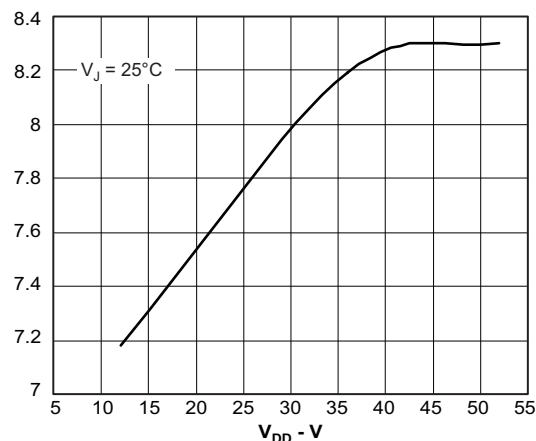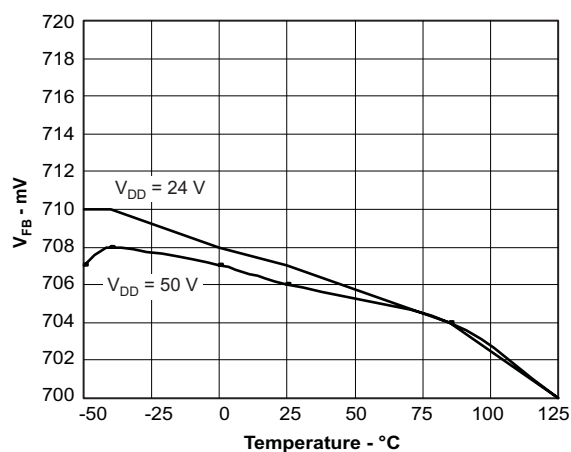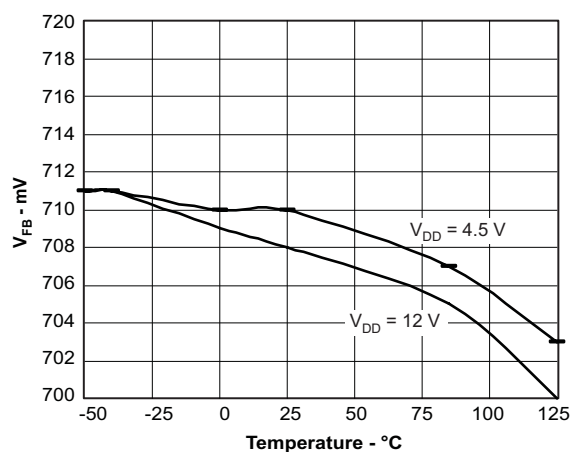FEEDBACK AMPLIFIER INPUT BIAS CURRENT
vs
TEMPERATURE
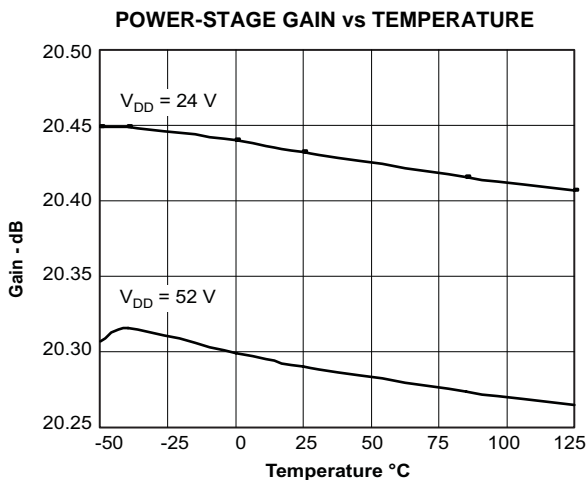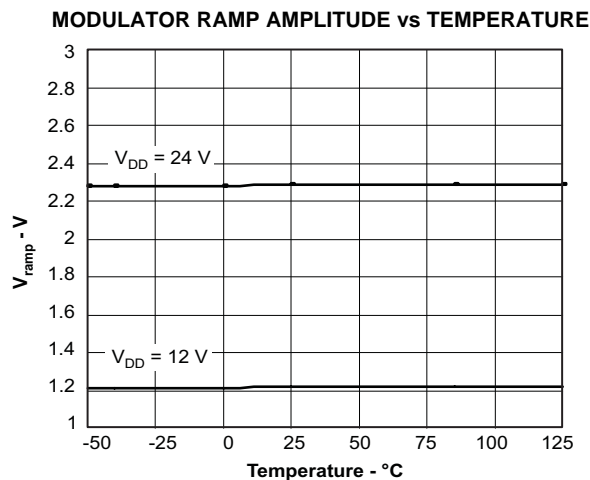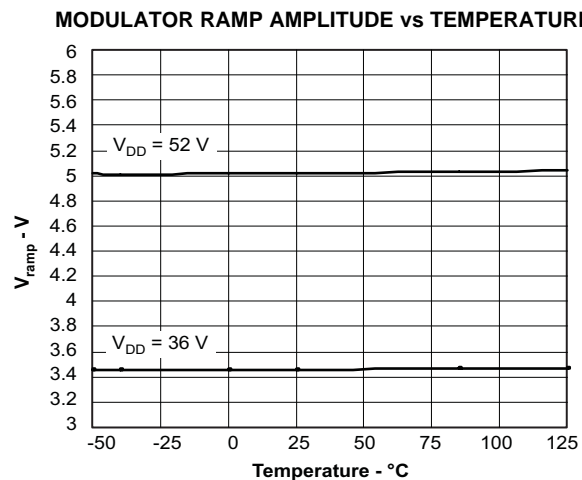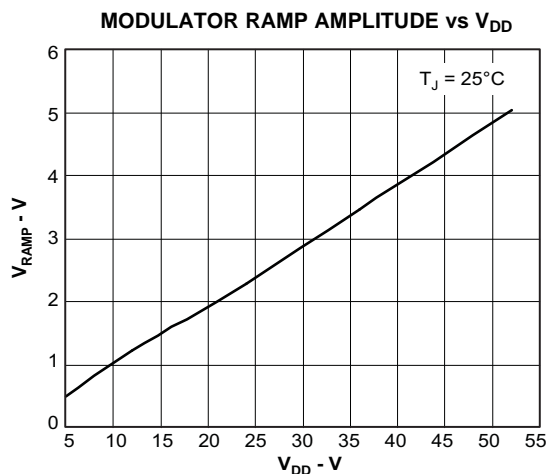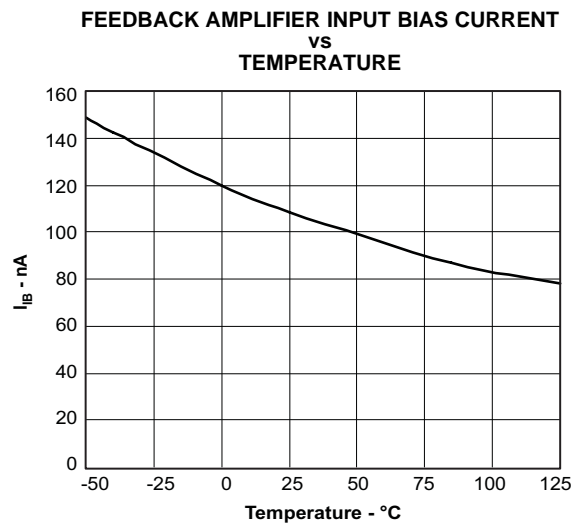


**Figure 16.**

## TYPICAL CHARACTERISTICS (continued)

**COMP SOURCE CURRENT vs TEMPERATURE**
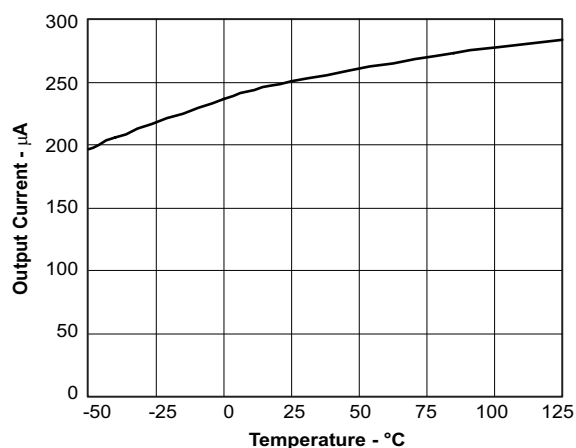


Figure 17.

**COMP SINK CURRENT vs TEMPERATURE**
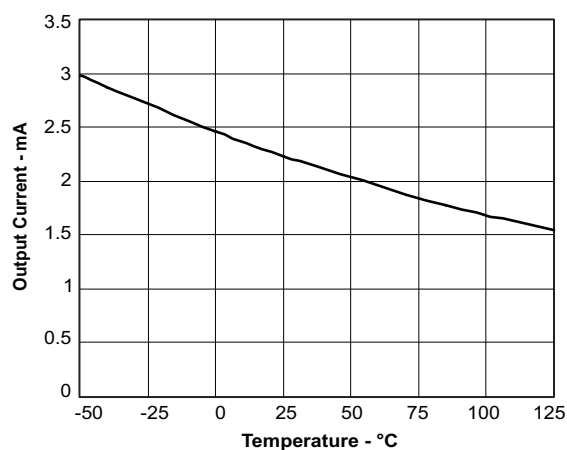


Figure 18.

**GATE DRIVE VOLTAGE vs TEMPERATURE**



Figure 19.

**GATE DRIVE VOLTAGE vs $V_{IN}$**



Figure 20.

**REFERENCE VOLTAGE vs TEMPERATURE**



Figure 21.

**REFERENCE VOLTAGE vs TEMPERATURE**



Figure 22.

**GENERAL INFORMATION**

## Overview

The TPS40200 is a nonsynchronous controller with a built-in 200-mA driver, designed to drive high-speed P-channel FETS up to 500 kHz. Its small size combined with complete functionality makes the part both versatile and easy to use.

The controller uses a low-value current-sensing resistor in series with the input voltage and the power FET source connection to detect switching current. When the voltage drop across this resistor exceeds 100 mV, the part enters a hiccup fault mode at approximately 2% of the operating frequency.

The part uses voltage feedback to an error amplifier that is biased by a precision 700-mV reference. Feed-forward compensation from the input keeps the pulse-width modulator (PWM) gain constant over the full input voltage range, eliminating the need to change frequency compensation for different input voltages.

The part also incorporates a soft-start feature where the output follows a slowly rising soft-start voltage, preventing output-voltage overshoot.

## Programming the Operating Frequency

The operating frequency of the controller is determined by an external resistor, $R_{RC}$, that is connected from the RC pin to VDD and a capacitor attached from the RC pin to ground. This connection, and the two oscillator comparators inside the IC, are shown in Figure 23. The oscillator frequency can be calculated from the following equation:

$$f_{SW} = \frac{1}{R_{RC} \times C_{RC} \times 0.105}$$

(1)

Where:

$f_{SW}$ = Clock frequency

$R_{RC}$ = Timing resistor value (in $\Omega$)

$C_{RC}$ = Timing capacitor value (in F)

$R_{RC}$ must be kept large enough that the current through it does not exceed 750 μA when the internal switch (shown in Figure 23) is discharging the timing capacitor. This condition may be expressed by:

$$\frac{V_{IN}}{R_{RC}} \leq 750 \ \mu A$$

(2)

## Synchronizing the Oscillator

Figure 23 shows the functional diagram of the TPS40200 oscillator. When synchronizing the oscillator to an external clock, RC must be pulled below 150 mV for 20 ns or more. The external clock frequency must be higher than the free-running frequency of the converter as well. When synchronizing the controller, if RC is held low for an excessive amount of time, erratic operation may occur. The maximum amount of time that RC should be held low is 50% of a nominal output pulse, or 10% of the period of the synchronization frequency.

Under circumstances where the input voltage is high and the duty cycle is less than 50%, a Schottky diode connected from RC to an external clock may be used to synchronize the oscillator. The cathode of the diode is connected to RC. The trip point of the oscillator is set by an internal voltage divider to be 1/10 of the input voltage. The clock signal must have an amplitude higher than this trip point. When the clock goes low, it allows the reset current to restart the RC ramp, synchronizing the oscillator to the external clock. This provides a simple, single-component method for clock synchronization.
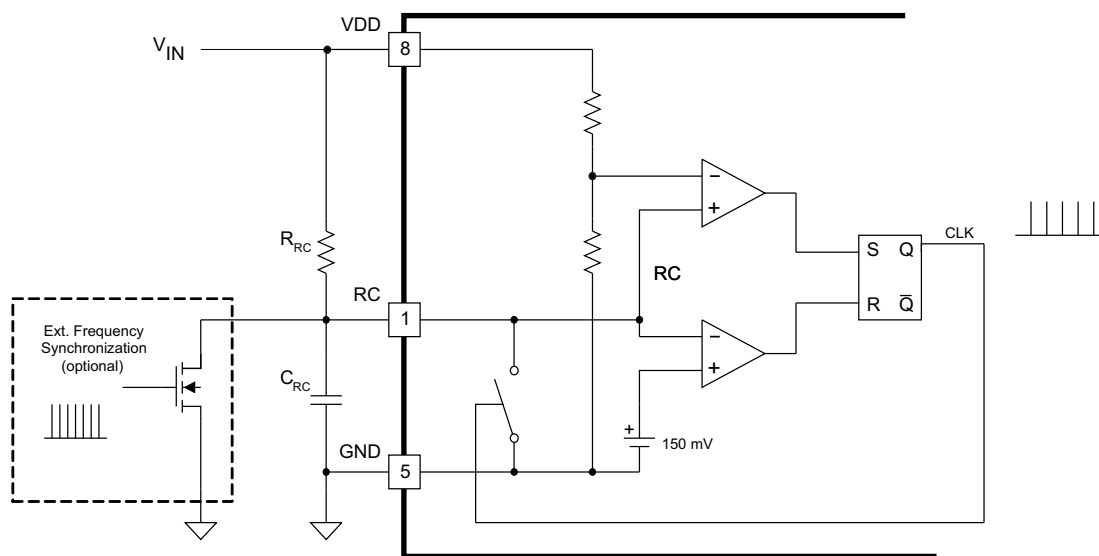
## GENERAL INFORMATION (continued)



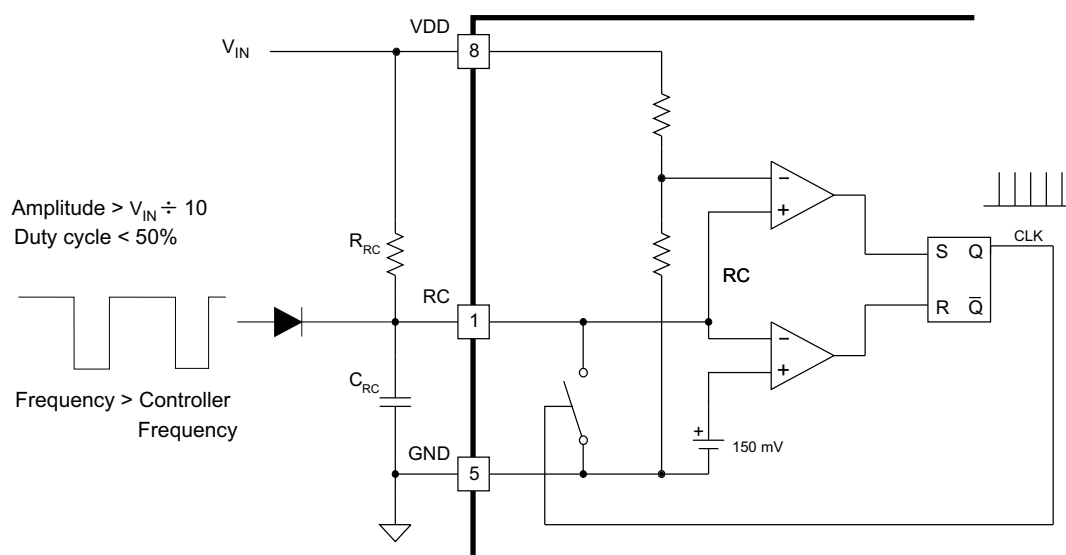**Figure 23. Oscillator Functional Diagram**



**Figure 24. Diode-Connected Synchronization**

## GENERAL INFORMATION (continued)

### Current-Limit Resistor Selection

As shown in Figure 27, a resistor in series with the power MOSFET sets the overcurrent protection level. Use a low-inductance resistor to avoid problems with ringing signals and nuisance tripping. When the FET is on and the controller senses 100 mV or more drop from the VDD pin to the ISNS pin, an overcurrent condition is declared. When this happens, the FET is turned off and, as shown in Figure 28, the soft-start capacitor is discharged. When the soft-start capacitor reaches a level below 150 mV, the converter clears the overcurrent condition flag and attempts to restart. If the condition that caused the overcurrent event to occur is still present on the output of the converter (see Figure 27), another overcurrent condition is declared and the process repeats indefinitely. Figure 27 shows the soft-start capacitor voltage during an extended output fault condition. The overall duty cycle of current conduction during a persistent fault is approximately 2%.
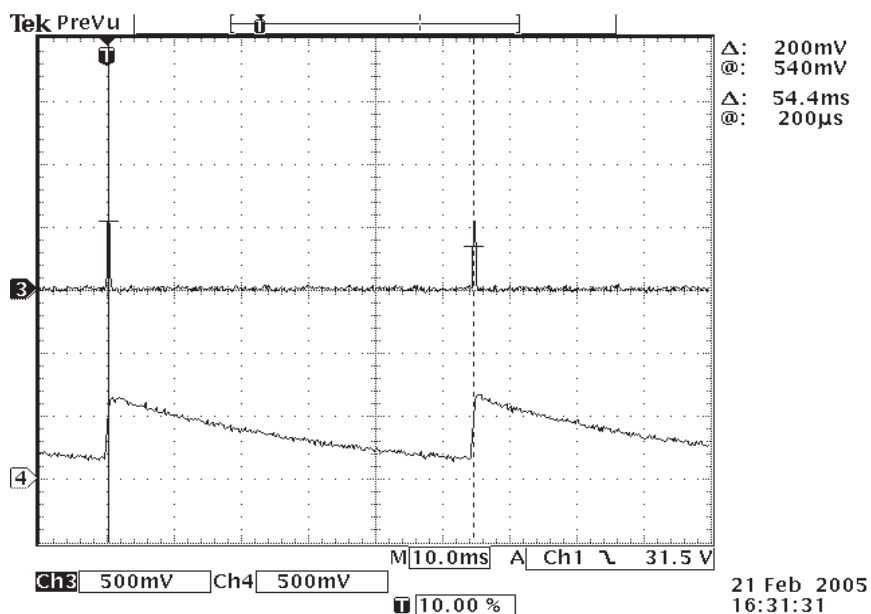


**Figure 25. Typical Soft-Start Capacitor and $V_{OUT}$ During Overcurrent**

## GENERAL INFORMATION (continued)
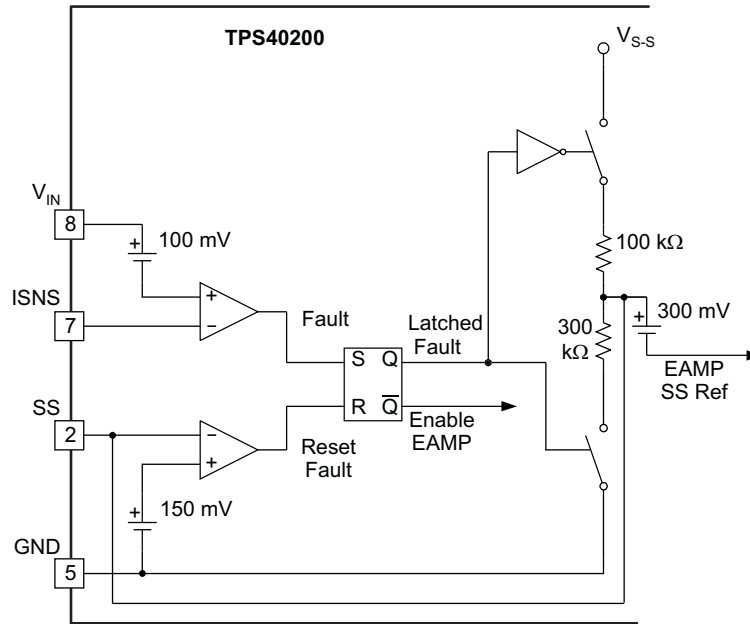


**Figure 26. Current-Limit Reset**

If necessary, a small R-C filter can be added to the current-sensing network to reduce nuisance tripping due to noise pickup. This filter also can be used to trim the overcurrent trip point to a higher level with the addition of a single resistor. See Figure 27. The nominal overcurrent trip point using the circuit of Figure 27 is described as:

$$I_{OC} = \frac{V_{ILIM}}{R_{ILIM}} \times \frac{R_{F1} + R_{F2}}{R_{F2}}$$

(3)

Where:

$I_{OC}$ = Overcurrent trip point, peak current in the inductor

$V_{ILIM}$ = Overcurrent threshold voltage for the TPS40200, typically 100 mV

$R_{ILIM}$ = Value of the current sense resistor (in $\Omega$)

$R_{F1}$ and $R_{F2}$ = Values of the scaling resistors (in $\Omega$)

The value of the capacitor is determined by the nominal pulse width of the converter and the values of the scaling resistors $R_{F1}$ and $R_{F2}$. It is best not to have the time constant of the filter longer than the nominal pulse width of the converter, otherwise a substantial increase in the overcurrent trip point occurs. Using this constraint, the capacitor value may be bounded by: .

$$C_f \leq \frac{V_O}{V_{IN} \times f_{SW}} \div \frac{R_{f1} \times R_{f2}}{R_{f1} + R_{f2}}$$

(4)

Where:

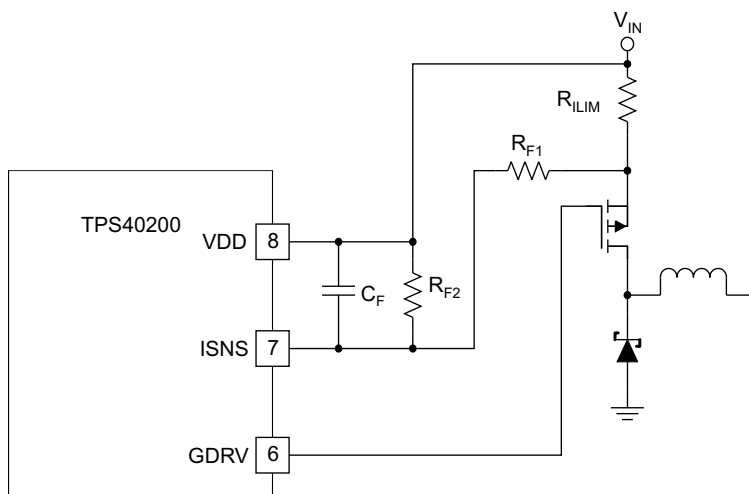$C_f$ = Value of the current-limit filter capacitor (in F)

$V_O$ = Output voltage of the converter

$V_{IN}$ = Input voltage to the converter

$f_{SW}$ = Converter switching frequency

$R_{f1}$ and $R_{f2}$ = Values of the scaling resistors (in $\Omega$)

## GENERAL INFORMATION (continued)



NOTE: The current-limit resistor and its associated circuitry can be eliminated and pins 7 and 8 shorted. However, the result of this may result in damage to the part or PC board in the event of an overcurrent event.

**Figure 27. Current-Limit Adjustment**

## GENERAL INFORMATION (continued)

### MOSFET Gate Drive

The output driver sinking current is approximately 200 mA and is designed to drive P-channel power FETs. When the driver pulls the gate charge of the FET, it is controlling to –8 V, the drive current folds back to a low level so that high power dissipation only occurs during the turnon period of the FET. This feature is particularly valuable when turning on a FET at high input voltages, where leaving the gate drive current on would otherwise cause unacceptable power dissipation.

### Undervoltage Lockout (UVLO) Protection

UVLO protection ensures proper startup of the device only when the input voltage has exceeded minimum operating voltage. Undervoltage protection incorporates hysteresis, which eliminates hiccup starting in cases where input supply impedance is high.
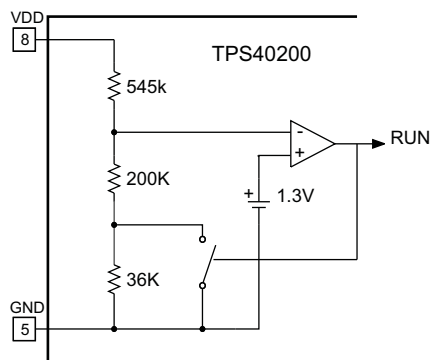


**Figure 28. Undervoltage Lockout**

Undervoltage protection ensures proper startup of the device only when the input voltage has exceeded minimum operating voltage. The UVLO level is measured at the VDD pin with respect to GND. Startup voltage is typically 4.3 V, with approximately 200 mV of hysteresis. The part shuts off at a nominal 4.1 V. As shown in Figure 28, when the input VDD voltage rises to 4.3 V , the 1.3-V comparator's threshold voltage is exceeded and a RUN signal occurs. Feedback from the output closes the switch and shunts the 200-kΩ resistor so that an approximate 200-mV lower voltage, or 4.1 V, is required before the part shuts down.

## GENERAL INFORMATION (continued)

### Programming the Soft-Start Time

An external capacitor, $C_{SS}$, connected from the soft-start (SS) pin to ground controls the TPS40200 soft-start interval. An internal charging resistor connected to VDD produces a rising reference voltage, which is connected though a 700-mV offset to the reference input of the TPS40200 error amplifier. When the soft-start capacitor voltage ($V_{CSS}$) is below 150 mV, there is no switching activity. When $V_{CSS}$ rises above the 700-mV offset, the error amplifier starts to follow $V_{SST}$ – 700 mV, and uses this rising voltage as a reference. When $V_{CSS}$ reaches 1.4 V, the internal reference takes over, and further increases have no effect. An advantage of initiating a slow start in this fashion is that the controller cannot overshoot because its output follows a scaled version of the controller's reference voltage. A conceptual drawing of the circuit that produces these results is shown in Figure 29. A consequence of the 700-mV offset is that the controller does not start switching until the $V_{CSS}$ has charged up to 700 mV. The output remains at 0 V during the resulting delay. When $V_{CCS}$ exceeds the 700-mV offset, the TPS40200 output follows the soft-start time constant. Once above 1.4 V, the 700-mV internal reference takes over, and normal operation begins.
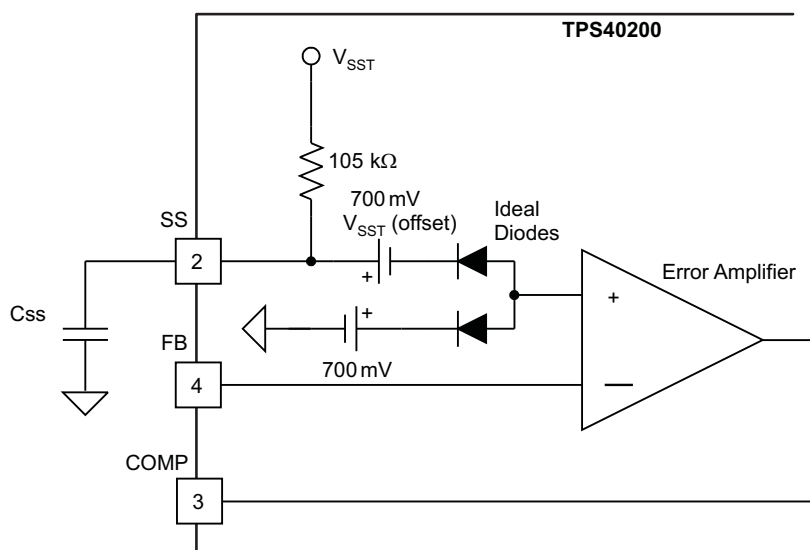


**Figure 29. Soft-Start Circuit**

The slow-start time should be more (slower) than the time constant of the output LC filter. This time constraint may be expressed as:

$$t_S \geq 2\pi \times \sqrt{L_O \times C_O}$$

(5)

The calculation of the soft-start interval is simply the time it takes the RC network to exponentially charge from 0 V to 1.4 V. An internal 105-kΩ charging resistor is connected from the SS pin to $V_{SST}$. For applications where the voltage is above 8 V, an internal regulator clamps the maximum charging voltage to 8 V.

The result of this is a formula for the start-up time, as given by:

$$t_{SS} = R_c \times C_{SS} \times \ln\left(\frac{V_{SST}}{V_{SST} - 1.4}\right)$$

(6)

Where:

$t_{SS}$ = Required soft-start time (in seconds)

$C_{SS}$ = Soft-start capacitor value (in F)

$R_c$ = Internal soft-start charging resistor (105 kΩ nominal)

$V_{SST}$ = Input voltage up to a maximum of 8 V

## GENERAL INFORMATION (continued)

### Voltage Setting and Modulator Gain

Since the input current to the error amplifier is negligible, the feedback impedance can be selected over a wide range. Knowing that the reference voltage is 708 mV, pick a convenient value for R1 and then calculate the value of R2 from the following formula:

$$V_{OUT} = 0.708 \left( 1 + \frac{R_2}{R_1} \right)$$

(7)
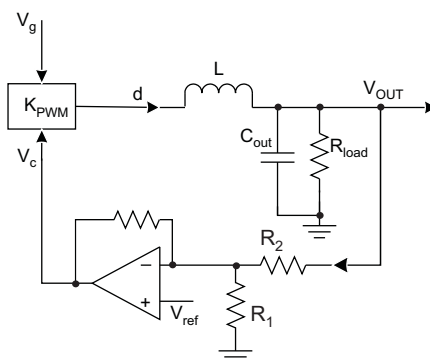


**Figure 30. System Gain Elements**

The error amplifier has a DC open-loop gain of at least 60 dB, with a minimum of a 1.5-MHz gain bandwidth product, which gives the user flexibility with respect to the type of feedback compensation used for this particular application. The gain selected by the user at the crossover frequency is set to provide an overall unity gain for the system. The crossover frequency should be selected so that the error amplifier open-loop gain is high with respect to the required closed-loop gain. This ensures that the amplifier response is determined by the passive feedback elements.

# EXAMPLE APPLICATIONS

## Application 1: Buck Regulator, 8-V to 12-V Input, 3.3 V or 5 V at 2.5-A Output

### Overview

The buck regulator design shown in Figure 31 illustrates the use of the TPS40200. It delivers 2.5 A at either 3.3 V or 5 V as selected by a single feedback resistor. It achieves approximately 90% efficiency at 3.3 V and 94% at 5 V. A discussion of design tradeoffs and methodology is included to serve as a guide to the successful design of forward converters using the TPS40200.

The Bill of Materials (BOM) for this application is given in Table 2. The efficiency and load regulation from boards built from this design are shown in Figure 32 and Figure 33. Gerber files and additional application information are available from the factory.
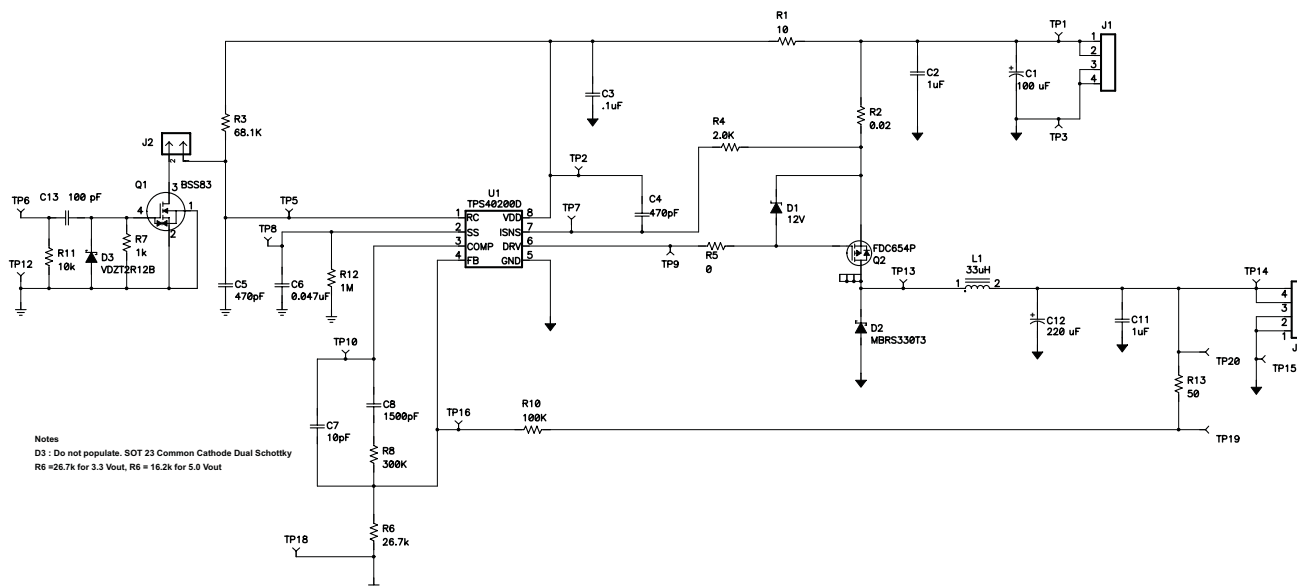


**Figure 31.  8-V to 16-V V$_{IN}$ Step-Down Buck Converter**
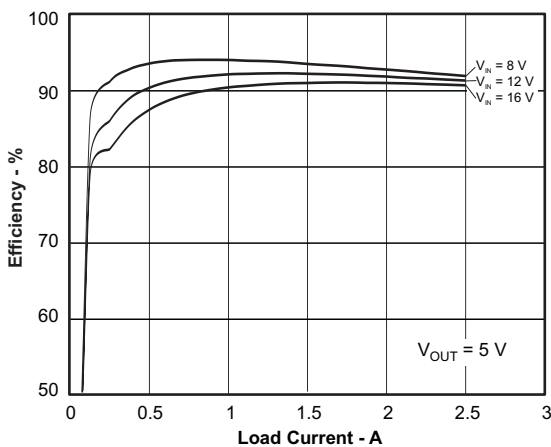


**Figure 32. Full-Load Efficiency at 5-V V$_{OUT}$**
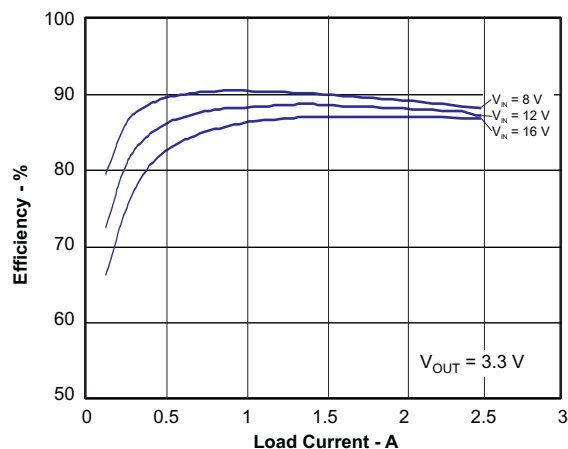


**Figure 33. Full-Load Efficiency at 3.3-V V$_{OUT}$**

# EXAMPLE APPLICATIONS  (continued)

## Component Selection

**Table 1. Design Parameters**

| SYMBOL | PARAMETER | TEST CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | | 8 | 12 | 16 | V |
| $V_{OUT}$ | Output voltage | $I_{OUT}$ at 2.5 A | 3.200 | 3.3 | 3.400[1] | V |
| | Line regulation | ±0.2% $V_{OUT}$ | 3.293 | 3.3 | 3.307 | V |
| | Load regulation | ±0.2% $V_{OUT}$ | 3.293 | 3.3 | 3.307 | V |
| $V_{OUT}$ | Output voltage | $I_{OUT}$ at 2.5 A | 4.85 | 5 | 5.150[1] | V |
| | Line regulation | ±0.2% $V_{OUT}$ | 4.990 | 5 | 5.010 | V |
| | Load regulation | ±0.2% $V_{OUT}$ | 4.990 | 5 | 5.010 | V |
| $V_{RIPPLE}$ | Output ripple voltage | At maximum output current | | 60 | | mV |
| $V_{OVER}$ | Output overshoot | For 2.5-A load transient from 2.5 A to 0.25 A | | 100 | | mV |
| $V_{UNDER}$ | Output undershoot | For 2.5-A load transient from 0.25 A to 2.5 A | | 60 | | mV |
| $I_{OUT}$ | Output current | | 0.125 | | 2.5 | A |
| $I_{SCP}$ | Short-circuit current trip point | | 3.75 | | 5.00 | A |
| | Efficiency | At nominal input voltage and maximum output current | | 90 | | % |
| $F_S$ | Switching frequency | | | 300 | | kHz |

(1)  Set-point accuracy is dependent on external resistor tolerance and the IC reference voltage. Line and load regulation values are referenced to the nominal design output voltage.

### *FET Selection Criteria*

- The maximum input voltage for this application is 16 V. Switching the inductor causes overshoot voltages that can equal the input voltage. Since the $R_{DSON}$ of the FET rises with breakdown voltage, select a FET with as low a breakdown voltage as possible. In this case, a 30-V FET was selected.

- The selection of a power FET's size requires knowing both the switching losses and dc losses in the application. AC losses are all frequency dependent and directly related to device capacitances and device size. Conversely, dc losses are inversely related to device size. The result is an optimum where the two types of losses are equal. Since device size is proportional to $R_{DSON}$, a starting point is to select a device with an $R_{DSON}$ that results in a small loss of power relative to package thermal capability and overall efficiency objectives.

- In this application, the efficiency target is 90% and the output power 8.25 W. This gives a total power-loss budget of 0.916 W. Total FET losses must be small, relative to this number.

The dc conduction loss in the FET is given by:

$$P_{DC} = I_{rms}^2 \times R_{DSON} \tag{8}$$

The rms current is given by:

$$I_{rms} = \left[ D \times \left( I_{OUT}^2 + \frac{\Delta I_{pp}^2}{12} \right) \right]^{\frac{1}{2}} \tag{9}$$

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Where:

$$\Delta I_{pp} = \Delta V \times D \times \frac{t_S}{L_I}$$

$$\Delta V = V_{IN} - V_{OUT} - (DCR + R_{DSON}) \times I_{OUT}$$

$R_{DSON}$ = FET on-state resistance

DCR = Inductor dc resistance

D = Duty cycle

$t_S$ = Reciprocal of the switching frequency

Using the values in this example, the dc power loss is 129 mW. The remaining FET losses are:
- $P_{SW}$ – Power dissipated while switching the FET on and off
- $P_{gate}$ – Power dissipated driving the FET gate capacitance
- $P_{COSS}$ – Power switching the FET output capacitance

The total power dissipated by the FET is the sum of these contributions:

$P_{FET} = P_{SW} + P_{gate} + P_{COSS} + P_{RDSON}$

The P-channel FET used in this application is an FDC654P, with the following characteristics:

| | |
|---|---|
| $t_{rise} = 13 \times 10^{-9}$ | $C_{OSS} = 83 \times 10^{-12}$ |
| $t_{fall} = 6 \times 10^{-9}$ | $Q_g = 9$ nC |
| $R_{DSON} = 0.1\ \Omega$ | $V_{gate} = 1.9$ V |
| $Q_{gd} = 1.2 \times 10^{-9}$ | $Q_{gs} = 1.0 \times 10^{-9}$ |

Using these device characteristics and the following formulas produces:

$$P_{SW} = \frac{f_S}{2} \times \left( V_{IN} \times I_{pk} \times t_{CHON} \right) + \frac{f_S}{2} \left( V_{IN} \times I_{pk} \times t_{CHOFF} \right) = 10 \text{ mW}$$

(10)

Where:

$$t_{CHON} = \frac{Q_{GD} \times R_G}{V_{IN} - V_{TH}}$$

and

$$t_{CHOFF} = \frac{Q_{GD} \times R_G}{V_{IN}}$$

are the switching times for the power FET.

$$P_{GATE} = Q_G \times V_{GATE} \times f_S = 22 \text{ mW}$$

$$P_{COSS} = \frac{C_{OSS} \times V_{IN\_MAX}^2 \times f_S}{2} = 2 \text{ mW}$$

$I_G = Q_G \times f_S = 2.7$ mA is the gate current

The sum of the switching losses is 34 mW and is comparable to the 129-mW dc losses. At added expense, a slightly larger FET would be better because the dc loss would drop and the ac losses would increase, with both moving toward the optimum point of equal losses.

**Rectifier Selection Criteria**

- Rectifier breakdown voltage

  The rectifier has to withstand the maximum input voltage which, in this case, is 16 V. To allow for switching transients that can approach the switching voltage, a 30-V rectifier was selected.

- Diode size

  The importance of power losses from the Schottky rectifier (D2) is determined by the duty cycle. For a low duty-cycle application, the rectifier is conducting most of the time, and the current that flows through it times its forward drop can be the largest component of loss in the entire controller. In this application, the duty cycle ranges from 20% to 40%, which in the worst case means that the diode is conducting 80% of the time. Where efficiency is of major importance, choose a diode with as low a forward drop as possible. In more cost-sensitive applications, size may be reduced to the point of the thermal limitations of the diode package.

  The device in this application is large, relative to the current required by the application. In a more cost-sensitive application, a smaller diode in a less-expensive package provides a less-efficient, but appropriate, solution.

  The device used has the following characteristics:

  - $V_f$ = 0.3 V at 3 A
  - $C_t$ = 300 pF ($C_t$ = the effective reverse-voltage capacitance of the synchronous rectifier, D2)

  The two components of the losses from the diode D2 are:

$$P_{COND} = V_f \times \left( I_{OUT} + \frac{I_{RIPPLE}}{4} \right) \times (1 - D) = 653 \text{ mW}$$

(11)

Where:

D = Duty cycle

$I_{RIPPLE}$ = Ripple current

$I_{OUT}$ = Output current

$V_F$ = Forward voltage

$P_{COND}$ = Conduction power loss

The switching capacitance of this diode adds an AC loss, given by:

$$P_{SW} = \frac{1}{2} [C \times (V_{IN} + V_f)^2 \times f] = 6.8 \text{ mW}$$

(12)

This additional loss raises the total loss to: 660 mW.

At an output voltage of 3.3 V, the application runs at a nominal duty cycle of 27%, and the diode is conducting 72.5% of the time. As the output voltage is moved up to 5 V, the on time increases to 46%, and the diode is conducting only 54% of the time during each clock cycle. This change in duty cycle proportionately reduces the conduction power losses in the diode. This reduction may be expressed as:

$$660 \left( \frac{0.54}{0.725} \right) = 491 \text{ mW}$$

(13)

for a savings in power of 660 – 491 = 169 mW.

To illustrate the relevance of this power savings, the full-load module efficiency was measured for this application at 3.3 V and 5 V. The 5-V output efficiency is 92% versus 89% for the 3.3-V design. This difference in efficiency represents a 456-mW reduction in losses between the two conditions. This 169-mW power-loss reduction in the rectifier represents 37% of the difference.

**Inductor Selection Criteria**

The TPS40200 P-channel FET driver facilitates switching the power FET at a high frequency. This, in turn, enables the use of smaller, less-expensive inductors as shown in this 300-kHz application. Ferrite, with its good high-frequency properties, is the material of choice. Several manufacturers provide catalogs with inductor saturation currents, inductance values, and LSRs (internal resistance) for their various-sized ferrites.

In this application, the part must deliver a maximum current of 2.5 A. This requires that the output inductor saturation current be above 2.5 A plus one-half the ripple current caused during inductor switching. The value of the inductor determines this ripple current. A low value of inductance has a higher ripple current that contributes to ripple voltage across the resistance of the output capacitors. The advantages of a low inductance are a higher transient response, lower DCR, higher saturation current, and a smaller, less-expensive part. Too low an inductor, however, leads to higher peak currents that ultimately are bounded by the overcurrent limit set to protect the output FET or by output ripple voltage. Fortunately, with low-ESR ceramic capacitors on the output, the resulting ripple voltage for relatively high ripple currents can be small.

For example, a single 1-µF 1206-sized 6.3-V ceramic capacitor has an internal resistance of 2 Ω at 1 MHz. For this 2.5-A application, a 10% ripple current of 0.25 A produces a 50-mV ripple voltage. This ripple voltage may be further reduced by additional parallel capacitors.

The other bound on inductance is the minimum current at which the controller enters discontinuous conduction. At this point, inductor current is zero. The minimum output current for this application is specified at 0.125 A. This average current is one-half the peak current that must develop during a minimum on time. The conditions for minimum on time are high line and low load, using:

$$L_{MAX} = \frac{V_{IN} - V_{OUT}}{I_{PEAK}} \times t_{ON} = 32 \ \mu H$$

(14)

Where:

$V_{IN}$ = 16 V

$V_{OUT}$ = 3.3 V

$I_{PEAK}$ =0.25 A

$t_{ON}$ = 0.686 µs

$t_{ON}$ is given by $\dfrac{1}{300 \ kHz} \times \dfrac{3.3 \ V}{16 \ V}$

The inductor used in the circuit is the closest standard value of 33 µH. This is the maximum inductance that can be used in the converter to deliver the minimum current, while maintaining continuous conduction.

**Output Capacitance**

In order to satisfy the output voltage overshoot and undershoot specifications, there must be enough output capacitance to keep the output voltage within the specified voltage limits during load current steps.

In a situation where a full load of 2.5 A within the specified voltage limits is suddenly removed, the output capacitor must absorb energy stored in the output inductor. This condition may be described by realizing that the energy stored in the inductor must be suddenly absorbed by the output capacitance. This energy relationship is written as:

$$\frac{1}{2} \times L_O I_O{}^2 \leq \frac{1}{2} \times [C_O(V_{OS}{}^2 - V_O{}^2)]$$

(15)

Where:

$V_{OS}$ = Allowed overshoot voltage above the output voltage

$L_O$ = Inductance

$I_O$ = Output current

$C_O$ = Output capacitance

$V_O$ = Output voltage

In this application, the worst-case load step is 2.25 A and the allowed overshoot is 100 mV. With a 33-µH output inductor, this implies an output capacitance of 249 µF for a 3.3-V output and 165 µF for a 5-V output.

When the load increases from minimum to full load, the output capacitor must deliver current to the load. The worst case is for a minimum on time that occurs at 16 V in and 3.3 V out and minimum load. This corresponds to an off time of (1 – 0.2) times the period 3.3 µs, and is the worst-case time before the inductor can start supplying current. This situation may be represented by:

$$\Delta V_O < \Delta I_O \times \frac{t_{OFFMAX}}{C_O}$$

(16)

Where:

$\Delta V_O$ = Undershoot specification of 60 mV

$\Delta I_O$ = Load current step

$t_{OFFMAX}$ = Maximum off time

This condition produces a requirement of 100 µf for the output capacitance. The larger of these two requirements becomes the minimum value of output capacitance.

The ripple current develops a voltage across the ESR of the output capacitance, so another requirement on this component is that its ESR be small relative to the ripple voltage specification.

**Switching Frequency**

The TPS40200 has a built-in, 8-V, 200-mA, P-channel FET driver output that facilitates using P-channel switching FETs. A clock frequency of 300 kHz was chosen as a switching frequency which represents a compromise between a high frequency that allows the use of smaller capacitors and inductors, but one that is not so high as to cause excessive transistor switching losses. As previously discussed, an optimum frequency can be selected by picking a value where the dc and switching losses are equal.

The frequency is set by using the design formula given in the FET Selection Criteria section.

$$R_{RC} \times C_{RC} = \frac{1}{0.105 \times f_{SW}}$$

(17)

Where:

$R_{RC}$ = Timing resistor value (in ohms), or $R_{RC}$ = 68.1 $\Omega$

$C_{RC}$ = Timing capacitor value (in F), or C5 = 470 pF

$f_{SW}$ = Desired switching frequency (in Hz) which, in this case, calculates to 297 kHz

At a worst case of 16 V, the timing resistor draws about 250 μA, which is well below the 750 μA maximum that the circuit can pull down.

**Programming the Overcurrent Threshold Level**

The current limit in the TSP40200 is triggered by a comparator with a 100-mV offset, whose inputs are connected across a current-sense resistor between $V_{CC}$ and the source of the high-side switching FET. When current in this resistor develops more than 100 mV, the comparator trips and terminates the output gate drive.

In this application, the current-limit resistor is set by the peak output-stage current, which consists of the maximum load current plus one-half the ripple current (in this case, 2.5 + 0.125 = 2.625 A). To accommodate tolerances, a 25% margin is added, giving a 3.25-A peak current. Using the equation below then yields a value for $R_{ILIM}$ of 0.30 $\Omega$.

Current sensing in a switching environment requires attention to both circuit-board traces and noise pickup. In Figure 34, a small RC filter has been added to the circuit to prevent switching noise from tripping the current-sense comparator. The requirements of this filter are board dependent, but with the layout used in this application, no spurious overcurrent was observed.

$$ILIM = \frac{0.1}{R_{ILIM}}$$
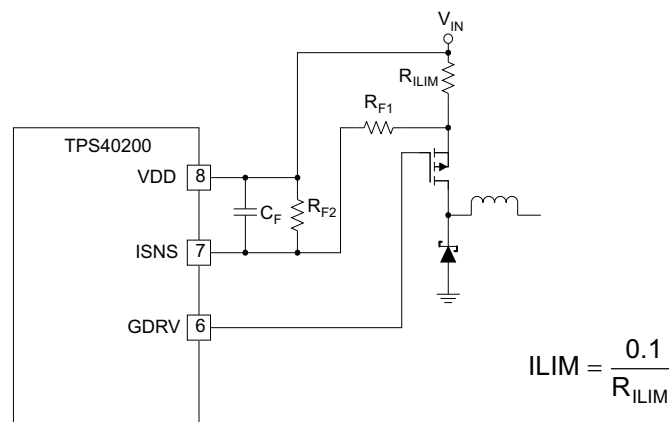
**Figure 34. Overcurrent Trip Circuit for $R_{F2}$ Open**

## Soft-Start Capacitor

The soft-start interval is given (in pF) by:

$$C_{SS} = \frac{t_{SS}}{R \times \ln\left(\dfrac{V_{SST}}{V_{SST} - 1.4}\right)} \times 10^3$$

(18)

Where:

R = Internal 105-kΩ charging resistor

$V_{CC}$ = Input voltage up to 8 V, where the charging voltage is internally clamped to 8 V maximum

$V_{OS}$ = 700 mV and, because the input voltage is 12 V, $V_{SST}$ = 8 V

The oscilloscope output (see Figure 35) shows the expected delay at the output (middle trace) until the soft-start node (bottom trace) reaches 700 mV. At this point, the output rises following the exponential rise of the soft-start capacitor voltage until the soft-start capacitor reaches 1.4 V and the internal 700-mV reference takes over. This total time is approximately 1 ms, which agrees with the calculated value of 0.95 ms where the soft-start capacitance is 0.047 µF.
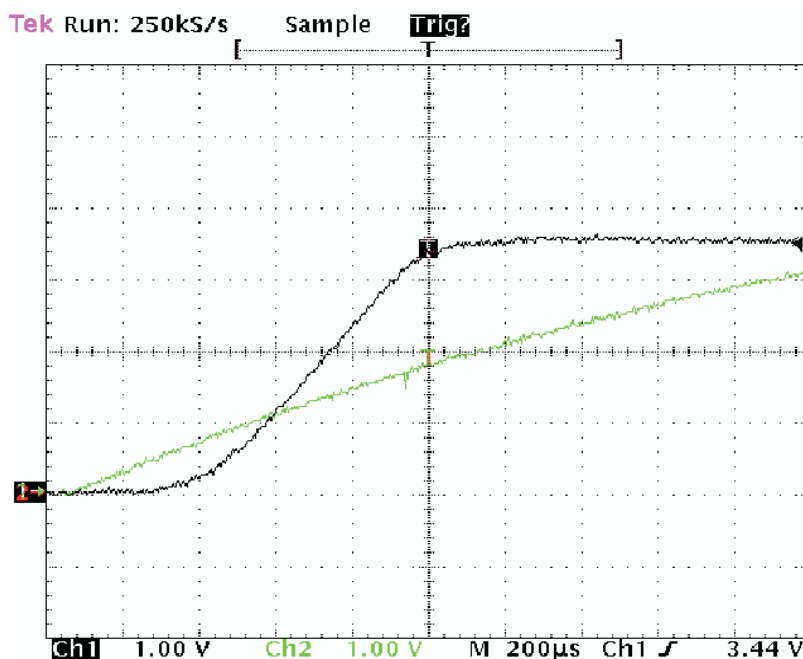


A.    Channel 1 is the output voltage rising to 3.3 V.

B.    Channel 2 is the soft-start (SS) pin.

**Figure 35. Soft Start Showing Output Delay and Controlled Rise to Programmed Output Voltage**

**Frequency Compensation**

The four elements that determine the system overall response are discussed in the following paragraphs. The gain of the error amplifier ($K_{EA}$) is the first of three elements. Its output develops a control voltage, which is the input to the PWM.

The TPS40200 has a unique modulator that scales the peak-to-peak amplitude of the PWM ramp to be 0.1 times the value of the input voltage. Since modulator gain is given by $V_{IN}$ divided by $V_{RAMP}$, the modulator gain is 10 and is constant at 10 (20 dB) over the entire specified input voltage range.

The last two elements that affect system gain are the transfer characteristic of the output LC filter and the feedback network from the output to the input to the error amplifier.

These four elements may be expressed by the following expression that represents the system transfer function (see Figure 36).

$$T_{V(S)} = K_{FB} \times K_{EA}(S) \times K_{PWM} \times X_{LC}(S)$$

(19)

Where:

$K_{FB}$ = Output voltage setting divider

$K_{EA}$ = Error amplifier feedback

$K_{PWM}$ = Modulator gain

$X_{LC}$ = Filter transfer function
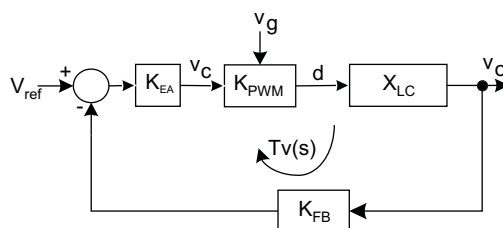


**Figure 36. Control Loop**

Figure 37 shows the feedback network used in this application. This is a type-2 compensation network, which gives a combination of good transient response and phase boost for good stability. This type of compensation has a pole at the origin, causing a –20-dB/decade (–1) slope, followed by a zero that causes a region of flat gain, followed by a final pole that returns the gain slope to –1. The Bode plot in Figure 38 shows the effect of these poles and zeros.

The procedure for setting up the compensation network is as follows:

1. Determine the break frequency of the output capacitor.
2. Select a zero frequency well below this break frequency.
3. From the gain bandwidth of the error amplifier, select a crossover frequency where the amplifier gain is large, relative to expected closed-loop gain.
4. Select a second zero well above the crossover frequency, which returns the gain slope to a –1 slope.
5. Calculate the required gain for the amplifier at crossover

Be prepared to iterate this procedure to optimize the pole and zero locations as needed.
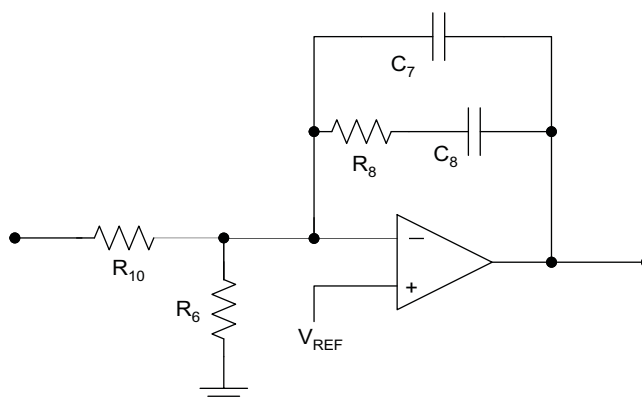


**Figure 37. Error Amplifier Feedback Elements**

The frequency response of this converter is largely determined by two poles that arise from the LC output filter and a higher-frequency zero caused by the ESR of the output capacitance. The poles from the output filter cause a 40-dB/decade rolloff with a phase shift approaching 180°, followed by the output capacitor zero that reduced the rolloff to –20 dB and gives a phase boost back toward 90°. In other nomenclature, this is a –2 slope followed by a –1 slope. The two zeros in the compensation network act to cancel the double pole from the output filter The compensation network's two poles produce a region where the error amplifier is flat and can be set to a gain, such that the overall gain of the system is 0 dB. This region is set so that it brackets the system crossover frequency.
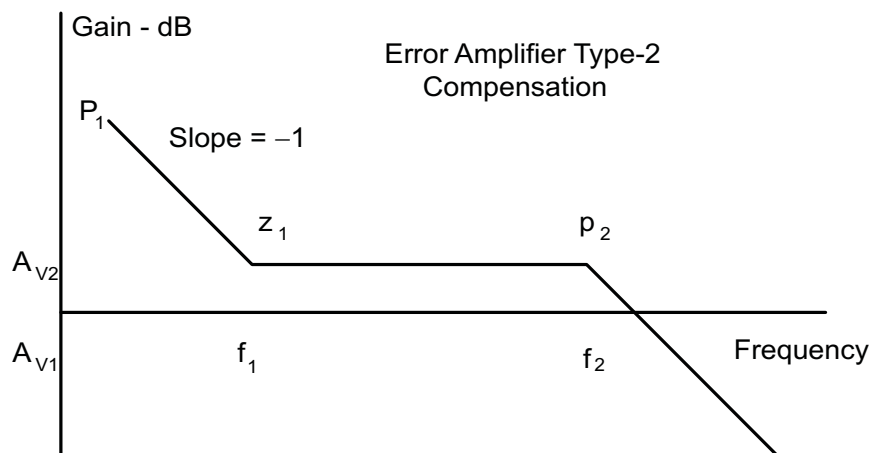


**Figure 38. Error Amplifier Bode Plot**

In order to properly compensate this system, it is necessary to know the frequencies of its poles and zeros.

### Step 1

The break frequency of the output capacitor is given by:

$$F_{esr} = \frac{1}{2\pi R_{esr}C}$$

(20)

Where:

    L = 33 μH
    C = 221 μF

Because of the ESR of the output capacitor, this output filter has a single-pole response above the 1.8-kHz break frequency of the output capacitor and its ESR. This simplifies compensation since the system becomes essentially a single-pole system.

### Step 2

The first zero is place well below the 1.8-kHz break frequency of the output capacitor and its ESR. Phase boost from this zero is shown in Figure 39.

$$f_{Z1} = \frac{1}{2\pi R_8 C_8}$$

(21)

Where:

    R8 = 100 kΩ
    C8 = 1500 pF
    $F_{Z1}$ = 354 Hz

### Step 3

From a minimum gain bandwidth product of 1.5 MHz, and knowing it has a 20-dB/decade rolloff, the gain of the error amplifier is 33 dB at 35 kHz. This approximate frequency is chosen for a crossover frequency to keep the amplifier gain contribution to the overall system gain small.

### Step 4

The second zero is placed well above the 35-kHz crossover frequency.

$$f_{P3} = \frac{1}{2\pi \times C_7 \times C_8 \times R_8} \times (C_7 + C_8)$$

(22)

Where:

    $R_8$ = 300 kΩ
    $C_7$ = 10 pF
    $C_8$ = 1500 pF
    $f_{P3}$ = 53 kHz

### Step 5

Calculate the three other gain elements of the system to determine the gain required by the error amplifier at 35-kHz to make the overall gain 0 dB:

$$T_{V(S)} = K_{FB} \times K_{EA}(S) \times K_{PWM} \times X_{LC}(S)$$

(23)

Where:

$K_{FB}$ = Output voltage setting divider

$K_{EA}$ = Error amplifier feedback

$K_{PWM}$ = Modulator gain

$X_{LC}$ = Filter transfer function

The output filter transfer characteristic is given by the following:

$$X_{LC}(S) = \frac{Z_{OUT}(S)}{Z_{OUT}(S) + Z(S) + R_{SW} \times D + R_{SR} \times (1-D)}$$

(24)

Where:

$Z_{OUT}$ = Parallel combination of output capacitor(s) and the load

$Z_{OUT}$ and $Z_I$ should include parasitic R and L.

Evaluating the response at 35-kHz gives the following:

- The full current output load at 3.3 V is 1.32 $\Omega$, and is in parallel with the 0.4-$\Omega$ ESR of the output capacitor.
- Including the 400 m$\Omega$ of ESR, the capacitive impedance is 14 m$\Omega$, and $Z_{OUT}$ = 414 m$\Omega$.
- The impedance of the inductor is $Z_I$ = 1.659 $\Omega$.
- $X_{LC(S)}$ = 0.033, or –29.6 dB

The feedback network has a gain to the error amplifier given by:

$$K_{fb} = \frac{R_{10}}{R_6}$$

(25)

Where:

R6 = 26.7 k$\Omega$

Using the values in this application, $K_{fb}$ = 11.4 dB.

The modulator has a gain of 10 that is flat to well beyond 35 kHz, so $K_{PWM}$ = 20 dB.

The amplifier gain, including the feedback gain, $K_{fb}$, can be approximated by this expression:

$$\frac{V_O}{V_{IN}}(S) = \frac{-Av_{OL}}{1 + \dfrac{Z_I(S)}{R_6} + \dfrac{R_{10}}{Z_f(S)} \times (1 + Av_{OL})}$$

(26)

Where:

$Z_I$ = $R_{10}$

$Z_f$ = Parallel combination of $C_7$ in parallel with the sum of $R_8$ and the impedance of $C_8$

The gain required to achieve 0-dB system gain is simply the sum of the other three gains: –(–29.6 + 11.4 + 20) = 1.8 dB. With an open-loop gain of 33 dB, the closed-loop gain of the amplifier is 0.8, or –1.66 dB, which gives a 0.13-dB gain at 35 kHz.

Figure 39 shows the result of the compensation. The crossover frequency is 35 kHz, and the phase margin is 45°. The response of the system is dominated by the ESR of the output capacitor and is exploited to produce an essentially single-pole system with simple compensation.
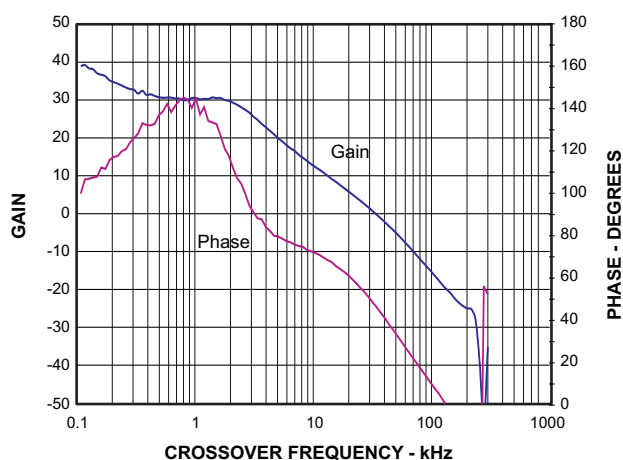
**Figure 39. Overall System Gain and Phase Response**

Figure 39 also shows the phase boost that gives the system a crossover phase margin of 47°.

The Bill of Materials (BOM) for this application is given in Table 2. The efficiency and load regulation from boards built from this design are shown in Figure 44 and Figure 45. Gerber PC layout files and additional application information are available from the factory.

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# TPS40200-EP

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## Table 2. Bill of Materials, Buck Regulator, 12 V to 3.3 V and 5 V

| REF. DES. | VALUE | DESCRIPTION | SIZE | MFR. | PART NUMBER |
|---|---|---|---|---|---|
| C1 | 100 μF | Capacitor, Aluminum, SM, 25-V, 0.3 Ω | 8 x 10 mm | Sanyo | 20SVP100M |
| C12 | 220 μF | Capacitor, Aluminum, SM, 6.3-V, 0.4 Ω | 8 x 6.2 mm | Panasonic | EEVFC0J221P |
| C13 | 100 pF | Capacitor, Ceramic, 50V, [COG], [20%] | 603 | muRata | Std. |
| C3 | 0.1 pF | Capacitor, Ceramic, 50V, [X7R], [20%] | 603 | muRata | Std. |
| C2, C11 | 1 μF | Capacitor, Ceramic, 50V, [X7R], [20%] | 603 | muRata | Std. |
| C4, C5 | 470 pF | Capacitor, Ceramic, 50V, [X7R], [20%] | 603 | muRata | Std. |
| C6 | 0.047 μF | Capacitor, Ceramic, 50V, [X7R], [20%] | 603 | muRata | Std. |
| C7 | 10 pF | Capacitor, Ceramic, 50V, [COG], [20%] | 603 | muRata | Std. |
| C8 | 1500 pF | Capacitor, Ceramic, 50V, [X7R], [20%] | 603 | muRata | Std. |
| D1 | 12 V | Diode, Zener, 12-V, 350-mW | SOT23 | Diodes, Inc. | BZX84C12T |
| D2 | | Diode, Schottky, 30-A, 30-V | SMC | On Semi | MBRS330T3 |
| D3 | 12 V | Diode Zener 12-V 5 mA | VMD2 | Rohm | VDZT2R12B |
| J1,J3 | | Terminal Block 4-Pin 15-Amp 5.1-mm | 0.8 x 0.35 | OST | ED2227 |
| J2 | | Header, 2-pin, 100-mil spacing, (36-pin strip) | 0.100 x 2 | Sullins | PTC36SAAN |
| L1 | 33 μH | Inductor, SMT, 3.2 A, .039 Ω | 12.5 x 12.5 mm | TDK | SLF12575T330M3R2PF |
| PCB | | 2 Layer PCB 2 Ounce Cu | 1.4 x 2.12 x 0.062 | | HPA164 |
| Q1 | | Trans, N-Chan Enhancement Switching, 50 mA | SOT-143B | Phillips | BSS83 |
| Q2 | | MOSFET, P-ch, 30-V, 3.6-A, 75-mΩ | SuperSOT-6 | Fairchild | FDC654P |
| U1 | | IC, Low Cost Non-Sync Buck Controller | SO-8 | TI | TPS40200D |
| R1 | 10 Ω | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R10 | 100 kΩ | Resistor, Chip, , 1/16W, 1% | 603 | Std. | Std. |
| R11 | 10 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R12 | 1 MΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R13 | 49.9 Ω | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R2 | 0.02 Ω | Resistor, Chip, W, 5% | 2010 | Std. | Std. |
| R3 | 68.1 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R4 | 2.0 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R5 | 0 Ω | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R6 | 26.7 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R7 | 1.0 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |
| R8 | 300 kΩ | Resistor, Chip, 1/16 W, 1% | 603 | Std. | Std. |

## PC Board Plots

Figure 40 through Figure 42 show the design of the TPS40200EVM-001 printed circuit board. The design uses 2-layer, 2-oz copper and is 1.4-in × 2.3-in in size. All components are mounted on the top side to allow the user to easily view, probe, and evaluate the TPS40200 control IC in a practical application. Moving components to both sides of the PCB or using additional internal layers can offer additional size reduction for space-constrained applications.

30    Submit Documentation Feedback
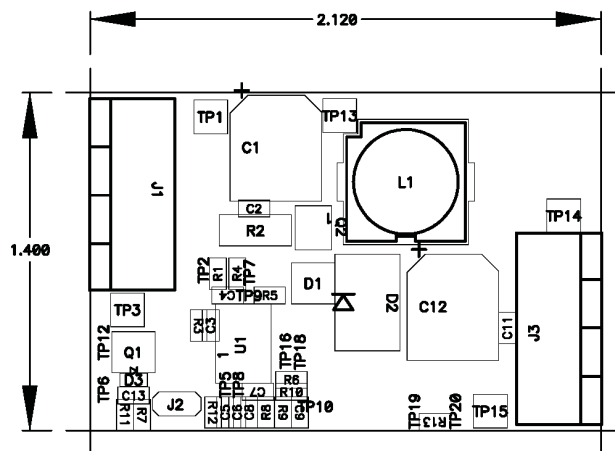
**Figure 40. TPS40200EVM-001 Component Placement (Viewed From Top)**
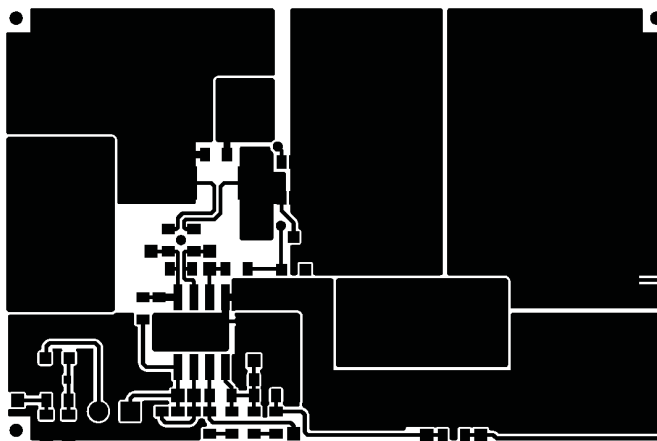


**Figure 41.  TPS40200EVM001 Top Copper (Viewed From Top)**
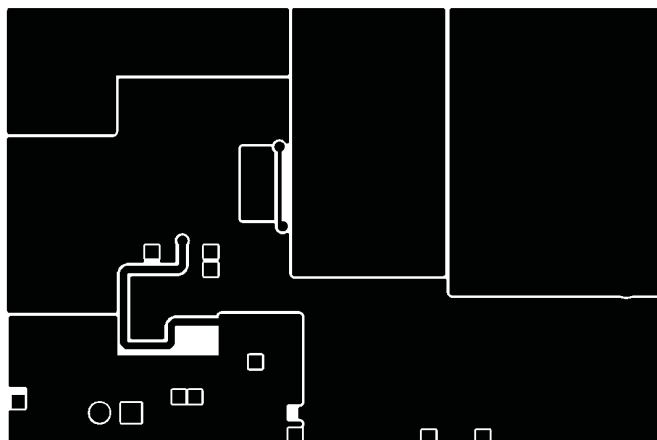


**Figure 42. TPS40200EVM-001 Bottom Copper (X-Ray View From Top)**

## Application 2: 18-V to 50-V Input, 16 V at 1-A Output

This is an example of using the TPS40200 in a higher-voltage application. The output voltage is 16 V at 1 A, with an 18-V to 50-V input. Module boards built to this schematic, and a test report, are available from the factory. The following shows some of the test results.

### Test Results

Figure 44 and Figure 45 show some of the performance obtained from this application. Further information and support material is available from the factory.
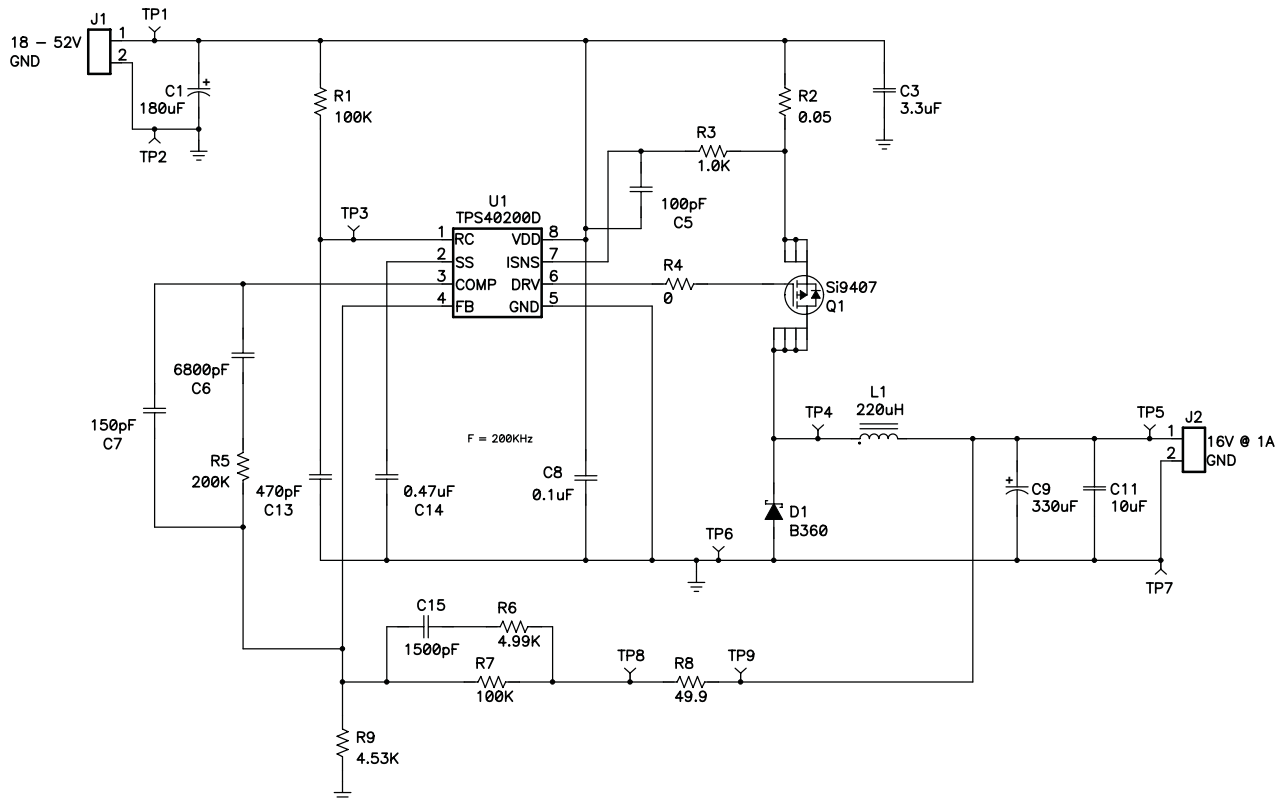


**Figure 43. Buck Converter (V$_{IN}$ = 18 V to 50 V; V$_{OUT}$ = 16 V at 1 A)**
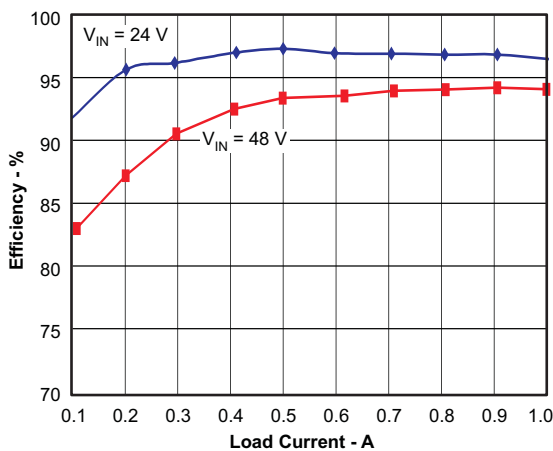


**Figure 44. Efficiency vs Load**
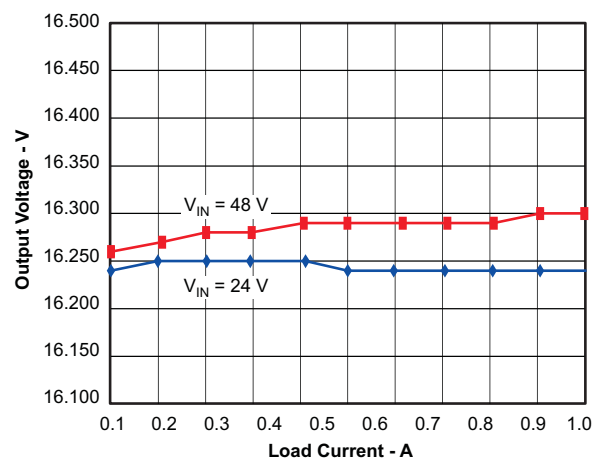


**Figure 45. Load Regulation, Two Input Voltage Extremes**

## Application 3: Wide Input Voltage LED Constant-Current Driver

This application uses the TPS40200 as a buck controller that drives a string of LED diodes. The feedback point for this circuit is a sense resistor in series with this string. The low 0.7-V reference minimizes power wasted in this resistor, and maintains the LED current at a value given by $0.7/R_{SENSE}$. As the input voltage is varied, the duty cycle changes to maintain the LED current at a constant value so that the light intensity does not change with large input voltage variations.
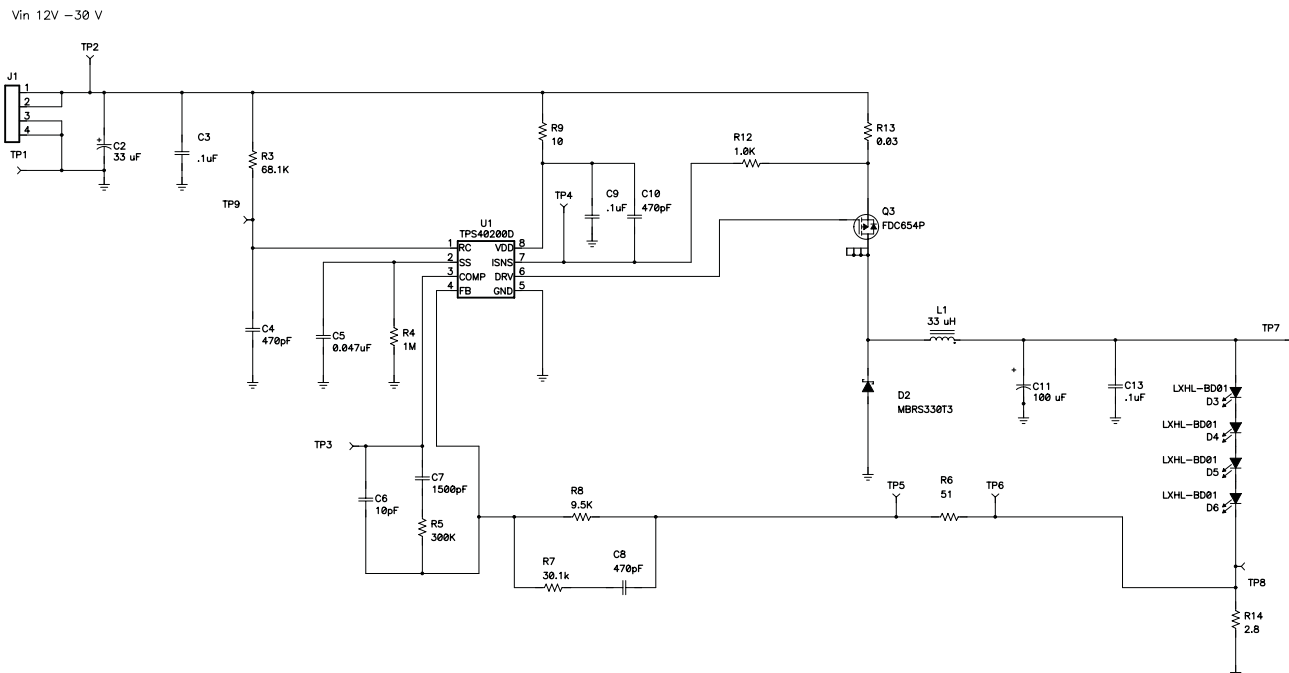
**Figure 46. Wide Input Voltage-Range LED Driver**
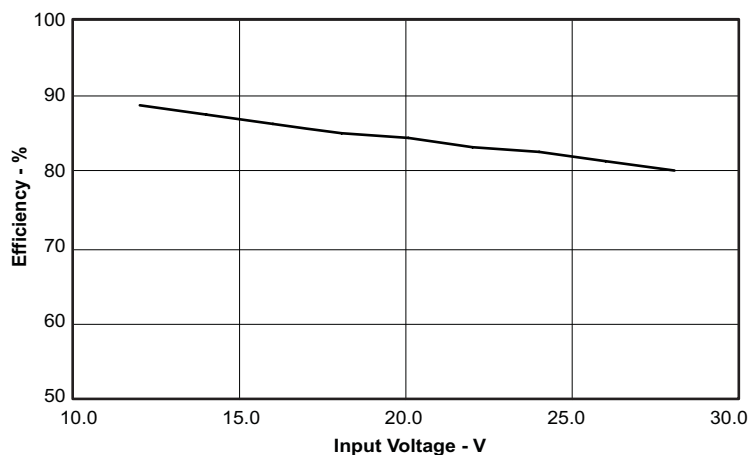
**Figure 47. Efficiency vs Input Voltage**

## DESIGN REFERENCES
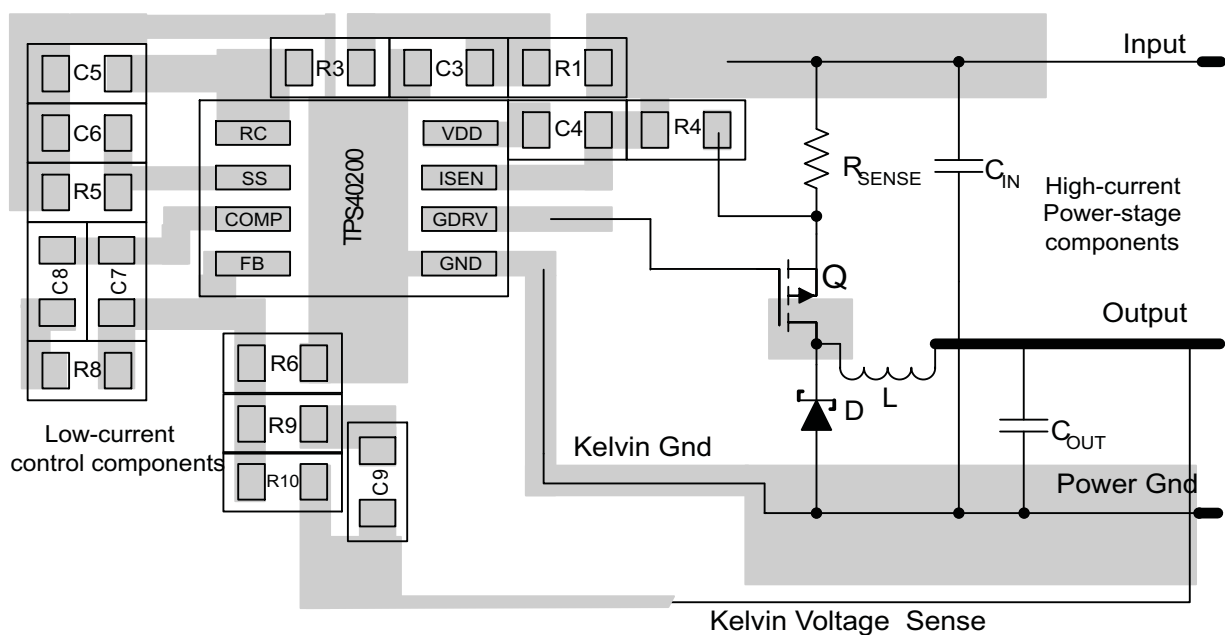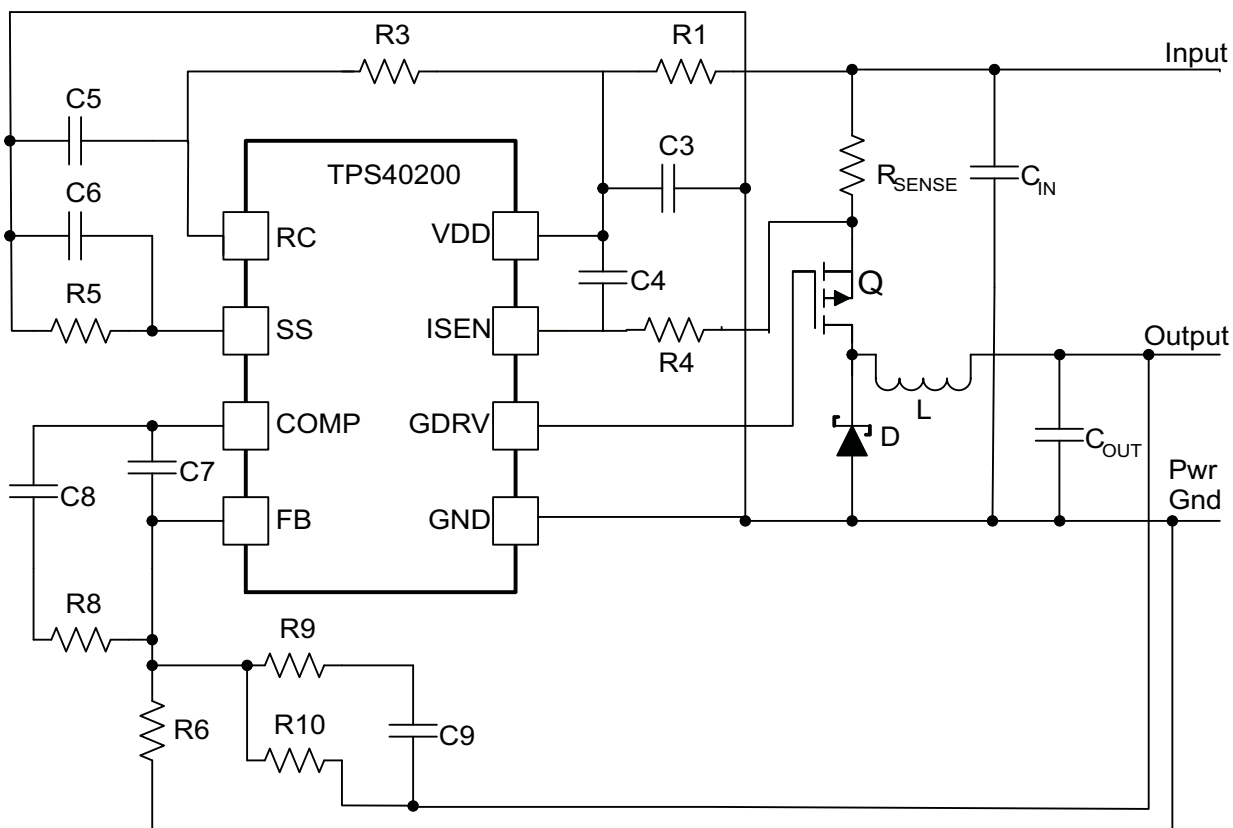


**Figure 48. PC Board Layout Recommendations**

## DESIGN REFERENCES (continued)

**Layout Hints**

- AC current loops must be kept as short as possible. For the maximum effectiveness from C1, place it near the VDD pin of the controller and design the input ac loop consisting of C1-$R_{SENSE}$-Q1-D1 to be as short as possible. Excessive high-frequency noise on VDD during switching degrades overall regulation as the load increases.

- Output loop A (D1-L1-C2) also should be kept as small as possible. Otherwise, the application's output noise performance is degraded.

- It is recommended that traces carrying large ac currents NOT be connected through a ground plane. Instead, use PCB traces on the top layer to conduct the ac current and use the ground plane as a noise shield. Split the ground plane as necessary to keep noise away from the TPS40200 and noise-sensitive areas, such as feedback resistors, R6 and R10.

- Keep the SW node as physically small as possible to minimize parasitic capacitance and to minimize radiated emissions

- For good output voltage regulation, Kelvin connections should be brought from the load to R6 and R10.

- The trace from the R6-R10 junction to the TPS40200 should be short and kept away from any noise source, such as the SW node.

- The gate drive trace should be as close to the power FET gate as possible.

## DESIGN REFERENCES (continued)

The TPS40200 is encapsulated in a standard plastic SOIC-8 package. The typical PC-board layout for this package is shown in Figure 49.
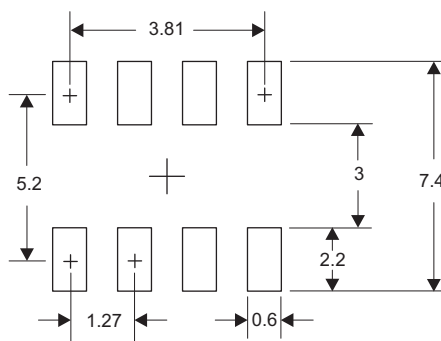


Dimensions are in millimeters

**Figure 49. Suggested SOIC-8 PC-Board Footprint**

### Related Parts

- TPS4007/9 Low Input Synchronous Buck Controller
- TL5001 Wide Input Range Controller

### Reference Documents

- *Under the Hood of Low Voltage DC/DC Converters*, SEM1500 Topic 5, 2002 Seminar Series
- *Understanding Buck Power Stages in Switchmode Power Supplies*, SLVA057, March 1999
- *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, SEM 1400, 2001 Seminar Series
- *Designing Stable Control Loops*, SEM 1400, 2001 Seminar Series
- Power.TI.com
- TPS40K designer software. This simple design tool supports the TPS40xxx family of controllers. To order a CD from the Product Information Center, request SLU015-TPS40k/SWIFT CD-ROM.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TPS40200MDREP | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| V62/07618-01XE | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check
http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# D (R−PDSO−G8)  PLASTIC SMALL−OUTLINE PACKAGE



0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)
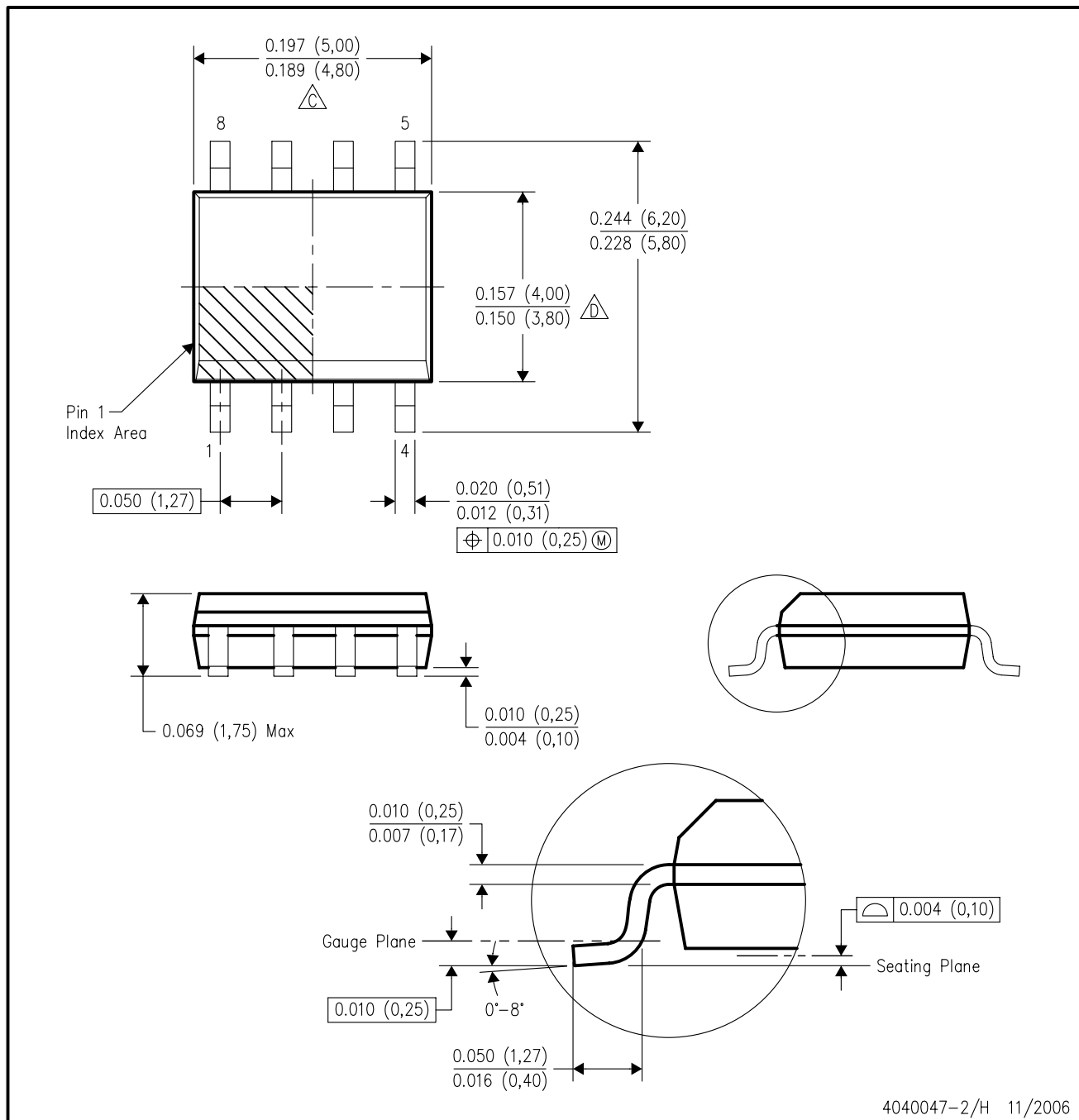
4040047−2/H  11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS−012 variation AA.

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