TPS60120, TPS60121, TPS60122, TPS60123, TPS60124, TPS60125
REGULATED 200-mA HIGH EFFICIENCY CHARGE PUMP DC/DC CONVERTERS

SLVS257B – NOVEMBER 1999 – REVISED AUGUST 2000

features

- High Average Efficiency Over Input Voltage Range Because of Special Switching Topology
- Minimum 200-mA Output Current From an Input Voltage Range of 1.8-V to 3.6-V
- Regulated 3.3-V or 3-V ±4% Output Voltage
- No Inductors Required, Low EMI
- Only Four External Components Required
- 55-μA Quiescent Supply Current
- 0.05-μA Shutdown Current
- Load Disconnected in Shutdown
- Integrated Low Battery and Power Good Detectors
- Evaluation Module Available (TPS60120EVM-142)

applications

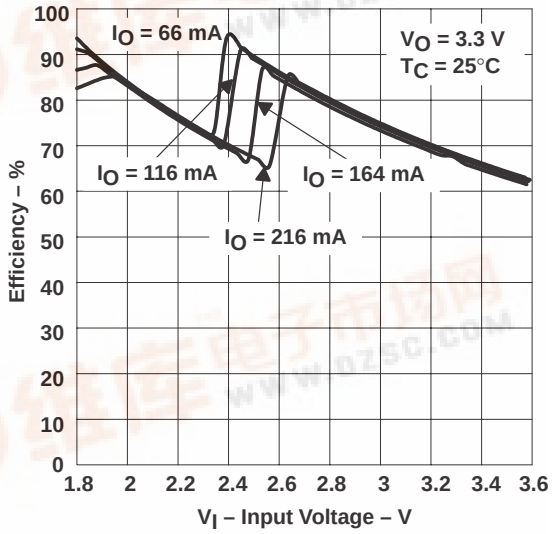
- Applications Powered by Two Battery Cells
- Portable Instruments
- Battery-Powered Microprocessor Systems
- Miniature Equipment
- Backup-Battery Boost Converters
- PDAs, Organizers, Laptops
- MP-3 Portable Audio Players
- Handheld Instrumentation
- Medical Instruments (e.g., Glucose Meters)
- Cordless Phones

description

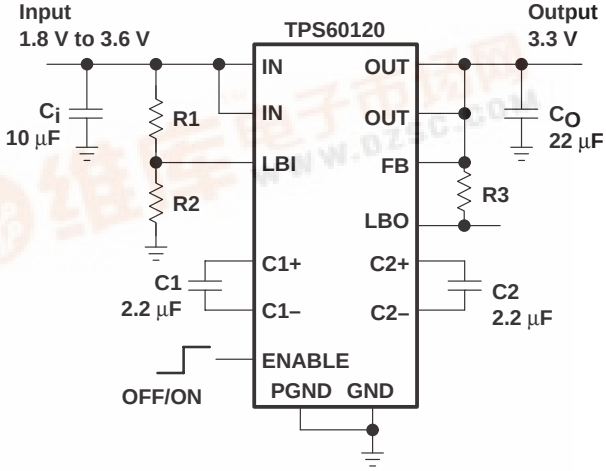
The TPS6012x step-up, regulated charge pumps generate a 3.3-V or 3-V ±4% output voltage from a 1.8-V to 3.6-V input voltage (two alkaline, NiCd, or NiMH batteries). They can deliver an output current of at least 200 mA (100 mA for the TPS60122 and TPS60123), all from a 2-V input. Four external capacitors are needed to build a complete high efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between a 1.5x or doubler conversion mode. From a 2-V input, all ICs can start with full load current.

The devices feature the power-saving pulse-skip mode to extend battery life at light loads. TPS60120, TPS60122, and TPS60124 include a low battery comparator. TPS60121, TPS60123, and TPS60125 feature a power-good output. The logic shutdown function reduces the supply current to a maximum of 1 μA and disconnects the load from the input. Special current-control circuitry prevents excessive current from being drawn from the battery during start-up. This dc/dc converter requires no inductors, therefore EMI is of low concern. It is available in the small, thermally enhanced 20-pin PowerPAD™ package (PWP).

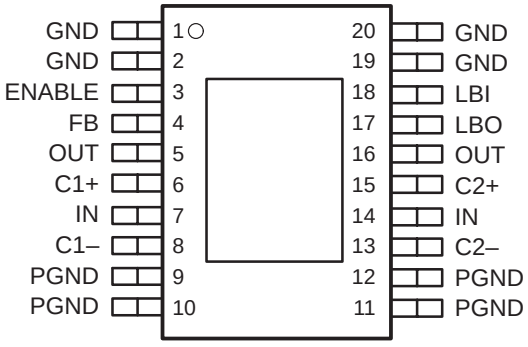
efficiency (TPS60120, TPS60121)



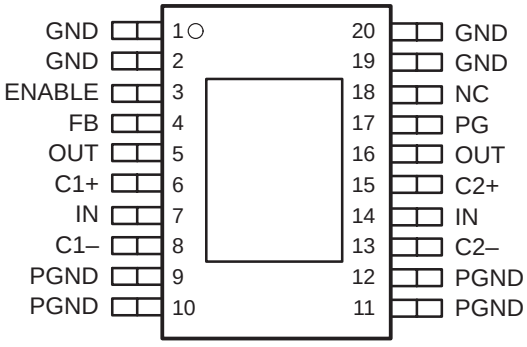
typical operating circuit

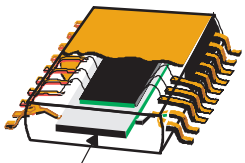


PWP PACKAGE
(TPS60120, TPS60122, TPS60124)
(TOP VIEW)



PWP PACKAGE
(TPS60121, TPS60123, TPS60125)
(TOP VIEW)





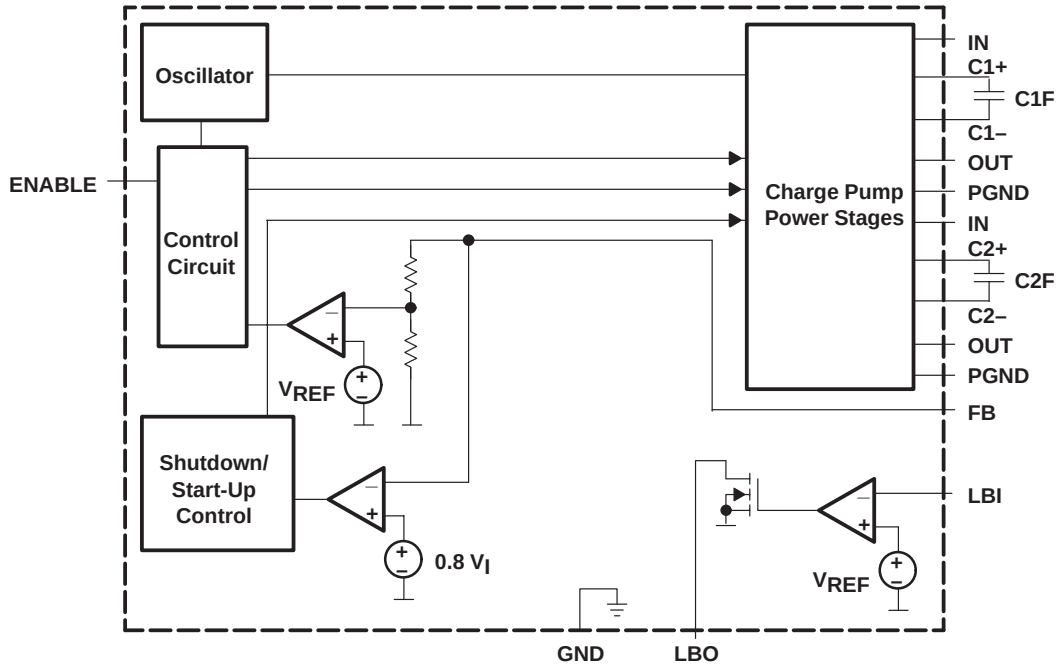
AVAILABLE OPTIONS

T_A	PART NUMBER†	PACKAGE		DEVICE FEATURES	
–40°C to 85°C	TPS60120PWP	PWP	20-Pin thermally enhanced TSSOP	2-Cell to 3.3 V, 200 mA	Low battery detector
	TPS60121PWP				Power good detector
	TPS60122PWP			2-Cell to 3.3 V, 100 mA	Low battery detector
	TPS60123PWP				Power good detector
	TPS60124PWP			2-Cell to 3 V, 200 mA	Low battery detector
	TPS60125PWP				Power good detector

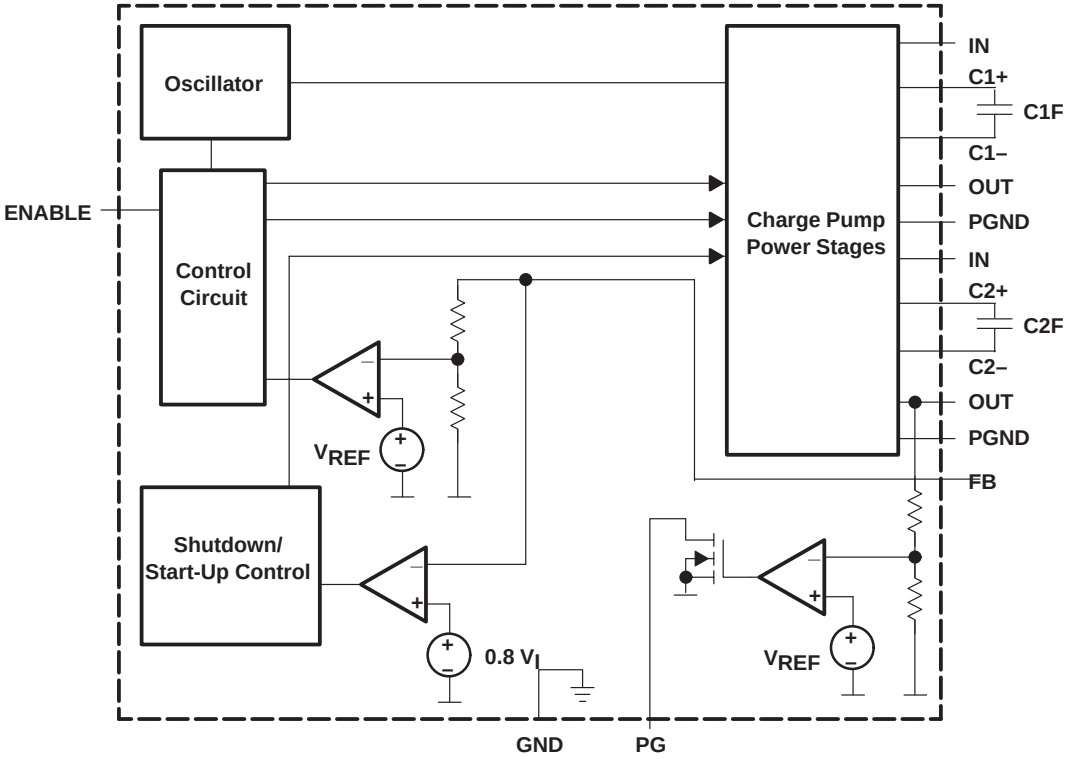
† The PWP package is available taped and reeled. Add R suffix to device type (e.g. TPS60120PWPR) to order quantities of 2000 devices per reel.

functional block diagram

TPS60120, TPS60122, TPS60124



TPS60121, TPS60123, TPS60125



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	6		Positive terminal of the flying capacitor C1
C1–	8		Negative terminal of the flying capacitor C1
C2+	15		Positive terminal of the flying capacitor C2
C2–	13		Negative terminal of the flying capacitor C2
ENABLE	3	I	ENABLE input. Connect ENABLE to IN for normal operation. When ENABLE is a logic low, the device turns off and the supply current decreases to 0.05 μA. The output is disconnected from the input when the device is placed in shutdown.
FB	4	I	Feedback input. Connect FB to OUT as close to the load as possible to achieve best regulation. Resistive divider is on the chip to match the internal reference voltage of 1.21 V.
GND	1, 2, 19, 20		Ground. Analog ground for internal reference and control circuitry. Connect to PGND through a short trace.
IN	7,14	I	Supply input. Connect to an input supply in the 1.8-V to 3.6-V range. Bypass IN to PGND with a (C_O/2) μF capacitor. Connect both INs through a short trace.
LBO/PG	17	O	Low battery detector output or power good output. Open drain output of the low battery or power-good comparator. It can sink 1 mA. A 100-kΩ to 1-MΩ pullup is recommended. Leave terminal unconnected if not used.
LBI/NC	18	I	Low battery detector input (TPS60120/TPS60122/TPS60124 only). The input is compared to the internal 1.21-V reference voltage. Connect terminal to ground if the low-battery detector function is not used. On the TPS60121, TPS60123, and TPS60125, this terminal is not connected.
OUT	5, 16	O	Regulated power output. Connect both OUT terminals through a short trace and bypass OUT to GND with the output filter capacitor C_O.
PGND	9–12		Power ground. Charge-pump current flows through this pin. Connect all PGND pins together.

detailed description

operating principle

The TPS6012x charge pumps provide a regulated 3.3-V or 3-V output from a 1.8-V to 3.6-V input. They are designed for a maximum load current of at least 200 mA or 100 mA, respectively. Designed specifically for space-critical, battery-powered applications, the complete charge pump circuit requires only four external capacitors. The circuit is optimized for efficiency over a wide input voltage range.

The TPS6012x charge pumps consist of an oscillator, a 1.21-V bandgap reference, an internal resistive feedback circuit, an error amplifier, high current MOSFET switches, a shutdown/start-up circuit, a low-battery or power-good comparator, and a control circuit (see the functional block diagram).

The device consists of two single-ended charge pumps. The power stages of the charge pump are automatically configured to amplify the input voltage with a conversion factor of 1.5 or 2. The conversion ratio depends on input voltage and output current. With input voltages lower than approximately 2.4 V, the convertor will run in a voltage doubler mode with a gain of two. With a higher input voltage, the converter operates with a gain of 1.5. This assures high efficiency over the wide input voltage range of a two-cell battery stack and is further described in the *adaptive mode switching* section.

adaptive mode switching

The ON-resistance of the MOSFETs that are in the charge path of the flying capacitors is regulated when the charge pump operates in voltage doubler-mode. It is changed depending on the output voltage that is fed back into the control loop. This way, the time-constant during the charging phase can be modified and increased versus a time-constant for fully switched-on MOSFETs. The ON-resistance of both switches and the capacitance of the flying capacitor define the time constant. The MOSFET switches in the discharge path of the charge pump are always fully switched on to their minimum $r_{DS(on)}$. With the time-constant during charge phase being larger than the time constant in discharge phase, the voltage on the flying capacitors stabilizes to the lowest possible value necessary to get a stable V_O.

adaptive mode switching (continued)

The voltage on the flying capacitors is measured and compared with the supply voltage (V_I). If the voltage across the flying capacitors is smaller than half of the supply voltage, then the charge pump switches into the 1.5x conversion-mode. The charge pump switches back from a 1.5x conversion-mode to a voltage doubler mode if the load current in 1.5x conversion-mode can no longer be delivered.

With this control mode the device runs in doubler-mode at low V_I and in 1.5x conversion-mode at high V_I to optimize the efficiency. The most desirable doubler mode is automatically selected depending on both V_I and I_L. This means that at light loads the device selects the 1.5x conversion-mode already at smaller supply voltages than at heavy loads.

The TPS6012x output voltage is regulated using the *ACTIVE-CYCLE* regulation. An active cycle controlled charge pump utilizes two methods to control the output voltage. At high load currents it varies the on resistances of the internal switches and keeps the ratio ON/OFF time (=frequency) constant. That means the charge pump runs at a fixed frequency. It also keeps the output voltage ripple as low as in linear-mode. At light loads the internal resistance and also the amount of energy transferred per pulse is fixed and the charge pump regulates the voltage by means of a variable ratio of ON-to-OFF time. In this operating point, it runs like a skip mode controlled charge pump with a very high internal resistance, which also enables a low ripple in this operation mode. Since the charge pump does effectively switch at lower frequencies at light loads, it achieves a low quiescent current.

pulse-skip mode

In pulse-skip mode the error amplifier disables switching of the power stages when it detects an output higher than the nominal output voltage. The oscillator halts and the IC then skips switching cycles until the output voltage drops below the nominal output voltage. Then the error amplifier reactivates the oscillator and starts switching the power stages again. The pulse-skip regulation mode minimizes operating current because it does not switch continuously and deactivates all functions except bandgap reference, error amplifier, and low-battery/power-good comparator when the output is higher than the nominal output voltage. When switching is disabled from the error amplifier, the load is also isolated from the input. In pulse-skip mode, a special current control circuitry limits the peak current. This assures moderate output voltage ripple and also prevents the device from drawing excessive current spikes out of the battery.

start-up procedure

During start-up, i.e., when ENABLE is set from logic low to logic high, the output capacitor is charged up with a limited current until the output voltage (V_O) reaches $0.8 \times V_I$. When the start-up comparator detects this voltage limit, the IC begins switching. This start-up charging of the output capacitor ensures a short start-up time and eliminates the need of a Schottky diode between IN and OUT. The IC starts into a maximum load resistance of $V_{O(nom)}/I_{O(max)}$.

shutdown

Driving ENABLE low places the device in shutdown mode. This disables all switches, the oscillator, and control logic. The device typically draws 0.05 μA (1 μA max) of supply current in this mode. Leakage current drawn from the output is as low as 1 μA max. The device exits shutdown once ENABLE is set to a high level. The typical no-load shutdown exit time is 10 μs. When the device is in shutdown, the load is isolated from the input.

undervoltage lockout and short-circuit current limit

The TPS6012x devices have an undervoltage lockout feature that deactivates the device and places it in shutdown mode when the input voltage falls below the typical threshold voltage of 1.6 V. During a short-circuit condition at the output, the current is limited to 115 mA.

low-battery detector (TPS60120, TPS60122, TPS60124)

The internal low-battery comparator trips at 1.21 V ±5% when the voltage on LBI ramps down. The battery voltage at which the comparator initiates a low battery warning at the LBO output can easily be programmed with a resistive divider as shown in Figure 1. The sum of resistors R1 and R2 is recommended to be in the 100-kΩ to 1-MΩ range.

LBO is an open drain output. An external pullup resistor to OUT, in the 100-kΩ to 1-MΩ range, is recommended. During start-up, the LBO output signal is invalid for the first 500 μs. LBO is high impedance when the device is disabled.

If the low-battery comparator function is not used, connect LBI to ground and leave LBO unconnected.

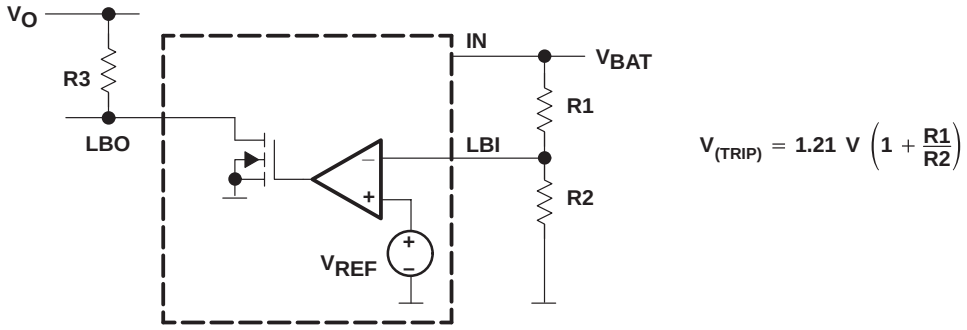


Figure 1. Programming of the Low-Battery Comparator Trip Voltage

Formulas to calculate the resistive divider for low battery detection, with V_{LBI} = 1.15 V – 1.27 V:

$$R2 = 1\ M\Omega \times \frac{V_{LBI}}{V_{Bat}}$$

$$R1 = 1\ M\Omega - R2$$

Formulas to calculate the minimum and maximum battery voltage that triggers the low battery detector:

$$V_{Bat(min)} = V_{LBI(min)} \times \frac{R1_{(min)} + R2_{(max)}}{R2_{(max)}}$$

$$V_{Bat(max)} = V_{LBI(max)} \times \frac{R1_{(max)} + R2_{(min)}}{R2_{(min)}}$$

Table 1. Recommended Values for the Resistive Divider From the E96 Series (±1%), V_{LBI} = 1.15 V – 1.27 V

V_{BAT}/V	R1/kΩ	R2/kΩ	$V_{BAT\ (MIN)}$/V		$V_{BAT(MAX)}$/V	
1.8	357	732	1.700	–5.66%	1.902	5.67%
1.9	365	634	1.799	–5.32%	2.016	6.11%
2.0	412	634	1.883	–5.86%	2.112	5.6%
2.1	432	590	1.975	–5.95%	2.219	5.67%
2.2	442	536	2.080	–5.45%	2.338	6.27%

Using ±1% accurate resistors, the total accuracy of the trip voltage is about ±6%, considering the ±4% accuracy the integrated voltage reference adds and considering that not every calculated resistor value is available.

low-battery detector (TPS60120, TPS60122, TPS60124) (continued)

A 100-nF bypass capacitor should be connected in parallel to R2 if large line transients are expected. These voltage drops can inadvertently trigger the low-battery comparator and produce a wrong low-battery warning signal at the LBO terminal.

power-good detector (TPS60121, TPS60123, TPS60125)

The PG terminal is an open-drain output that is pulled low when the output is out of regulation. When the output voltage rises to about 90% of its nominal voltage, the power-good output is released. PG is high impedance when the device is disabled. A pullup resistor must be connected between PG and OUT. The pullup resistor should be in the 100-kΩ to 1-MΩ range. If the power-good function is not used, then PG should remain unconnected.

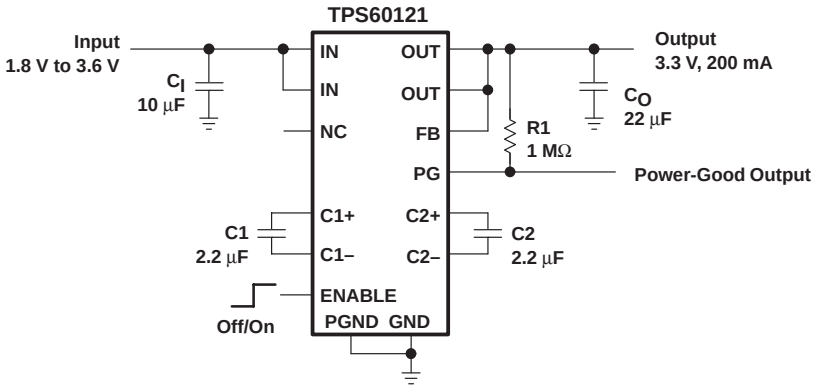


Figure 2. Typical Operating Circuit Using Power-Good Comparator

absolute maximum ratings (see Note 1)†

Input voltage range, V_I (IN, OUT, ENABLE, FB, LBI, LBO/PG) . . . . . –0.3 V to 5.5 V
Differential input voltage, V_{ID} (C1+, C2+ to GND) . . . . . –0.3 V to (V_O + 0.3 V)
Differential input voltage, V_{ID} (C1–, C2– to GND) . . . . . –0.3 V to (V_I + 0.3 V)
Continuous total power dissipation . . . . . See dissipation rating table
Continuous output current TPS60120, TPS60121, TPS60124, TPS60125 . . . . . 300 mA
Continuous output current TPS60122, TPS60123 . . . . . 150 mA
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s . . . . . 260°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: $V_{(ENABLE)}$, $V_{(LBI)}$, and $V_{(LBO/PG)}$ can exceed V_I up to the maximum rated voltage without increasing the leakage current drawn by these inputs.

DISSIPATION RATING TABLE 1 FREE-AIR TEMPERATURE (see Figure 3)

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
PWP	700 mW	5.6 mW/°C	448 mW	364 mW

DISSIPATION RATING TABLE 2 FREE-AIR TEMPERATURE (see Figure 4)

PACKAGE	$T_C \le 62.5°C$ POWER RATING	DERATING FACTOR ABOVE $T_C = 62.5°C$	$T_C = 70°C$ POWER RATING	$T_C = 85°C$ POWER RATING
PWP	25 mW	285.7 mW/°C	22.9 mW	18.5 mW

DISSIPATION DERATING CURVE† vs FREE-AIR TEMPERATURE

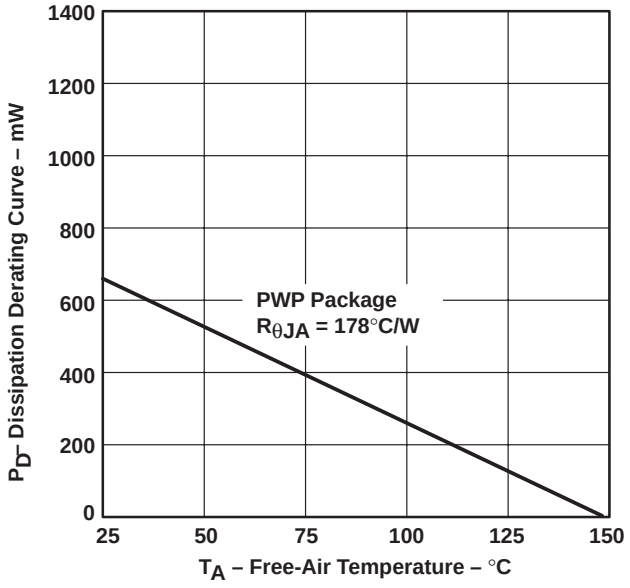


Figure 3

MAXIMUM CONTINUOUS DISSIPATION† vs CASE TEMPERATURE

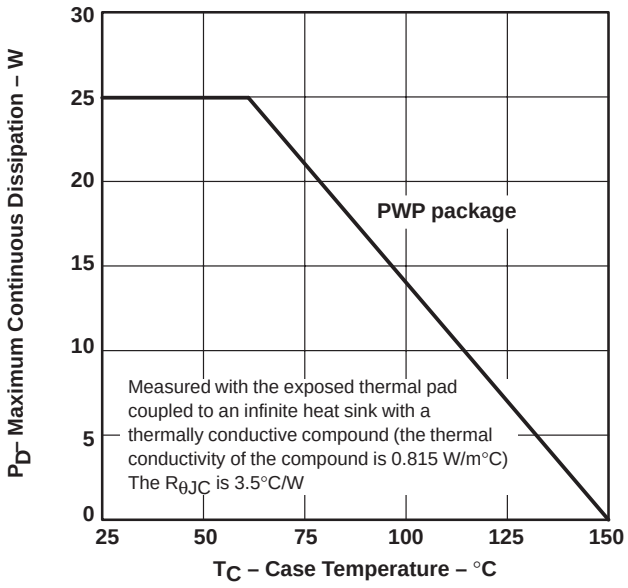


Figure 4

† Dissipation rating tables and figures are provided for maintenance of junction temperature at or below absolute maximum temperature of 150°C. It is recommended not to exceed a junction temperature of 125°C.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	1.8	3.6	V
Operating junction temperature, T_J		125	°C

electrical characteristics at C_I = 10 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 22 μF, T_C = –40°C to 85°C, V_I = 2 V, V_{FB} = V_O and $V_{(ENABLE)}$ = V_I (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(min)}$	Minimum start-up voltage		I_O = 0	1.8			V
			I_O = $I_{O(max)}$	2			
$V_{(UVLO)}$	Input undervoltage lockout threshold		T_C = 25°C		1.6	1.8	V
$I_{O(MAX)}$	Maximum continuous output current	TPS60120, TPS60121, TPS60124, TPS60125		200			mA
		TPS60122, TPS60123		100			mA
V_O	Output voltage	TPS60120, TPS60121, TPS60122, TPS60123	1.8 V < V_I < 2 V, 0 < I_O < $I_{O(MAX)}$/2, T_C = 0°C to 70°C	3.17		3.43	V
			2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.43	
			3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	3.17		3.47	
		TPS60124, TPS60125	1.8 V < V_I < 2 V, 0 < I_O < $I_{O(MAX)}$/2, T_C = 0°C to 70°C	2.88		3.12	
			2 V < V_I < 3.3 V, 0 < I_O < $I_{O(MAX)}$	2.88		3.12	
			3.3 V < V_I < 3.6 V, 0 < I_O < $I_{O(MAX)}$	2.88		3.3	
$I_{lkg(OUT)}$	Output leakage current		V_I = 2.4 V, $V_{(ENABLE)}$ = 0 V			1	μA
I_Q	Quiescent current (no-load input current)		V_I = 2.4 V		55	90	μA
$I_{Q(SDN)}$	Shutdown supply current		V_I = 2.4 V, $V_{(ENABLE)}$ = 0 V		0.05	1	μA
$f_{OSC(INT)}$	Internal switching frequency		V_I = 2.4 V	210	320	450	kHz
V_{IL}	Enable input voltage low		V_I = 1.8 V			0.3 x V_I	V
V_{IH}	Enable input voltage high		V_I = 3.6 V	0.7 x V_I			V
$I_{lkg(ENABLE)}$	Enable input leakage current		$V_{(ENABLE)}$ = V_{GND} or V_I		0.01	0.1	μA
	Output load regulation		V_I = 2.4 V, 1 mA < I_O < $I_{O(MAX)}$ T_C = 25°C		0.003%		/mA
	Output line regulation		2 V < V_I < 3.3 V, I_O = 100 mA, T_C = 25°C		0.3%		/V
	Short circuit current limit		V_I < 2.4 V, V_O = 0 V, T_C = 25°C		115		mA
$V_{(LBITRIP)}$	Low battery trip voltage	TPS60120, TPS60122, TPS60124	V_I = 1.8 V to 2.2 V, Hysteresis 0.8% for rising LBI, T_C = 0°C to 70°C	1.15	1.21	1.27	V
$I_{I(LBI)}$	LBI input current	TPS60120, TPS60122, TPS60124	$V_{(LBI)}$ = 1.3 V			100	nA
$V_{O(LBO)}$	LBO output voltage low (see Note 2)	TPS60120, TPS60122, TPS60124	$V_{(LBI)}$ = 0 V, $I_{(LBO,SINK)}$ = 1 mA			0.4	V
$I_{lkg(LBO)}$	LBO leakage current	TPS60120, TPS60122, TPS60124	$V_{(LBI)}$ = 1.3 V, $V_{(LBO)}$ = 3.3 V		0.01	0.1	μA

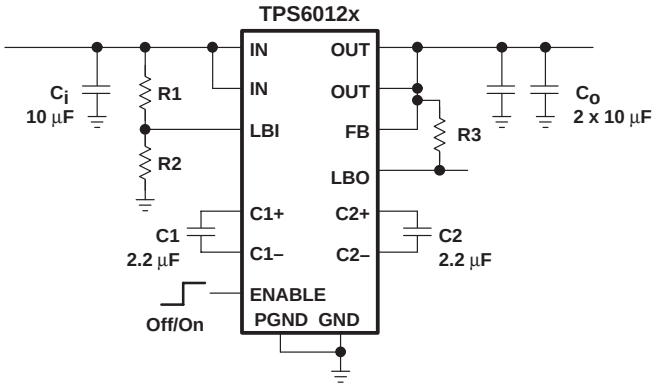
NOTE 2: During start-up the LBO and PG output signal is invalid for the first 500 μs.

electrical characteristics at C_I = 10 μF, C_{1F} = C_{2F} = 2.2 μF, C_O = 22 μF, T_C = –40°C to 85°C, V_I = 2 V, V_{FB} = V_O and $V_{(ENABLE)}$ = V_I (unless otherwise noted) (continued)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PGTRIP)}$	Power-good trip voltage	TPS60121, TPS60123, TPS60125	T_C = 0°C to 70°C	0.86 × V_O	0.90 × V_O	0.94 × V_O	V
$V_{hys(PG)}$	Power-good trip voltage hysteresis	TPS60121, TPS60123, TPS60125	V_O ramping negative, T_{CA} = 0°C to 70°C		0.8%		
$V_{O(PG)}$	Power-good output voltage low (see Note 2)	TPS60121, TPS60123, TPS60125	V_O = 0 V, $I_{(PG,SINK)}$ = 1 mA			0.4	V
$I_{lkg(PG)}$	Power-good leakage current	TPS60121, TPS60123, TPS60125	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	μA

NOTE 2: During start-up the LBO and PG output signal is invalid for the first 500 μs.

PARAMETER MEASUREMENT INFORMATION



Used capacitor types:
C_i: Ceramic, X7R
C_O: Ceramic, X7R
C1, C2: Ceramic, X7R

Figure 5. Circuit Used For Typical Characteristics Measurements

TYPICAL CHARACTERISTICS

Table of Graphs

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η	Efficiency	vs Output Current (TPS60120, TPS60122, and TPS60124)	6, 7, 8
		vs Input Voltage (TPS60120, TPS60122, and TPS60124)	9, 10, 11
I	Supply Current	vs Input Voltage	12
V_O	Output Voltage	vs Output Current (TPS60120, TPS60122, and TPS60124)	13, 14, 15
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V_{PP}	Output Voltage Ripple Amplitude	vs Input Voltage	22
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TYPICAL CHARACTERISTICS

TPS60120
EFFICIENCY
vs
OUTPUT CURRENT

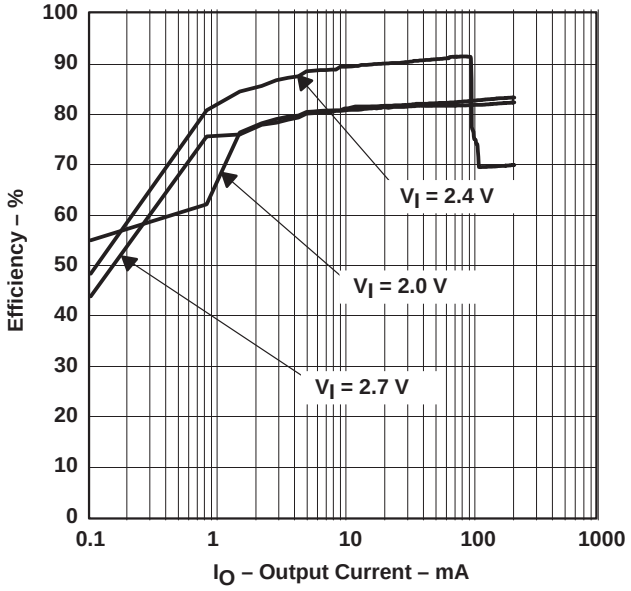


Figure 6

TPS60122
EFFICIENCY
vs
OUTPUT CURRENT

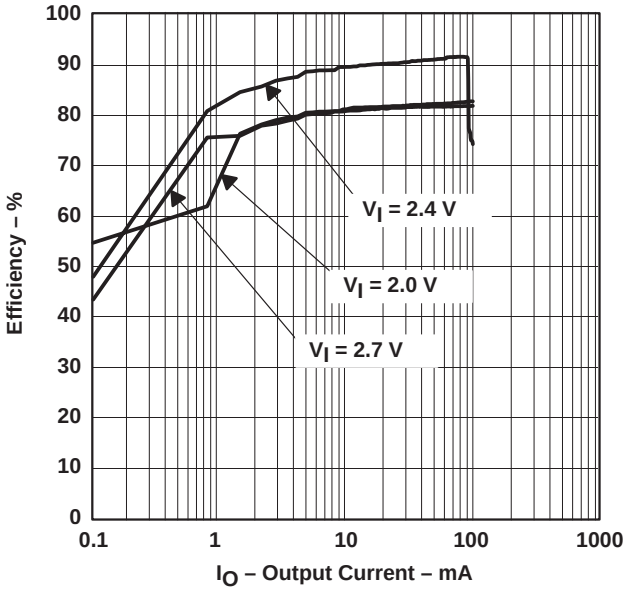


Figure 7

TPS60124
EFFICIENCY
vs
OUTPUT CURRENT

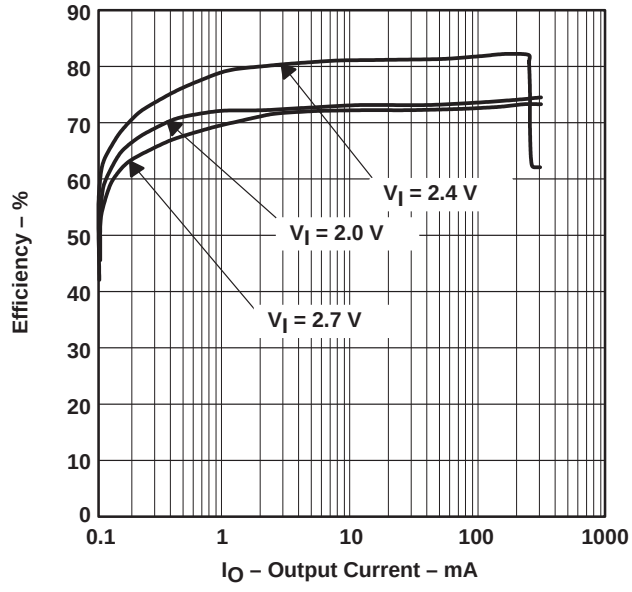


Figure 8

TPS60120
EFFICIENCY
vs
INPUT VOLTAGE

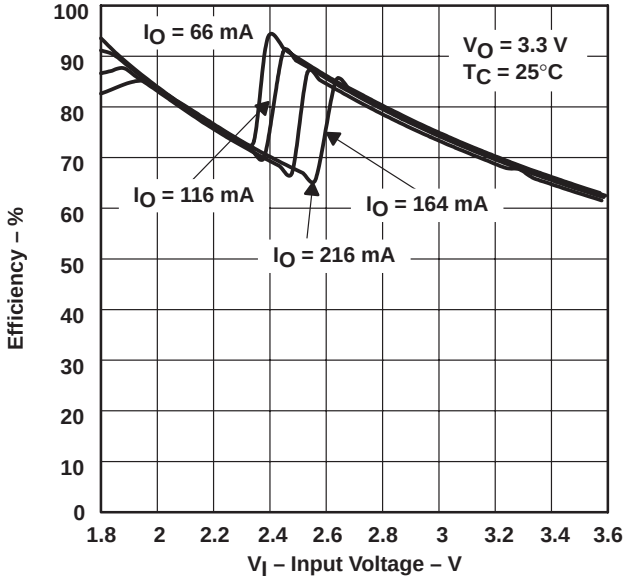


Figure 9

TYPICAL CHARACTERISTICS

TPS60122
EFFICIENCY
vs
INPUT VOLTAGE

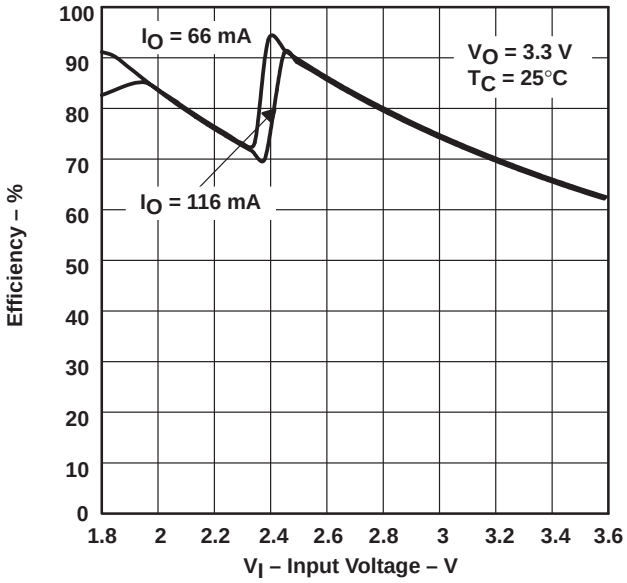


Figure 10

TPS60124
EFFICIENCY
vs
INPUT VOLTAGE

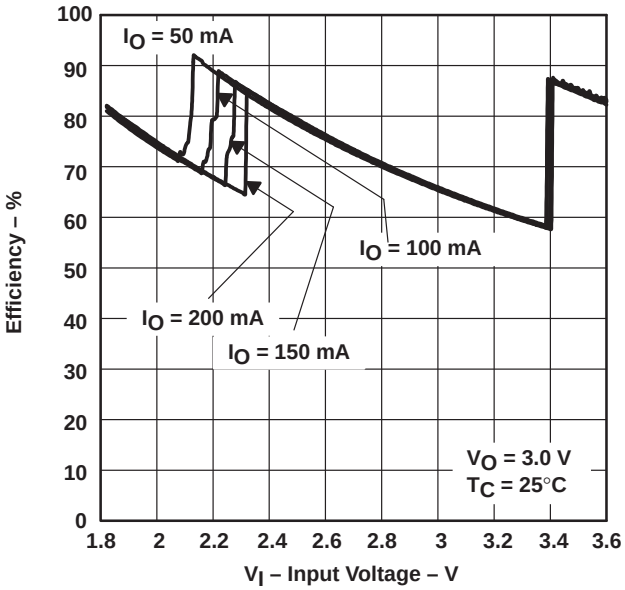


Figure 11

SUPPLY CURRENT
vs
INPUT VOLTAGE

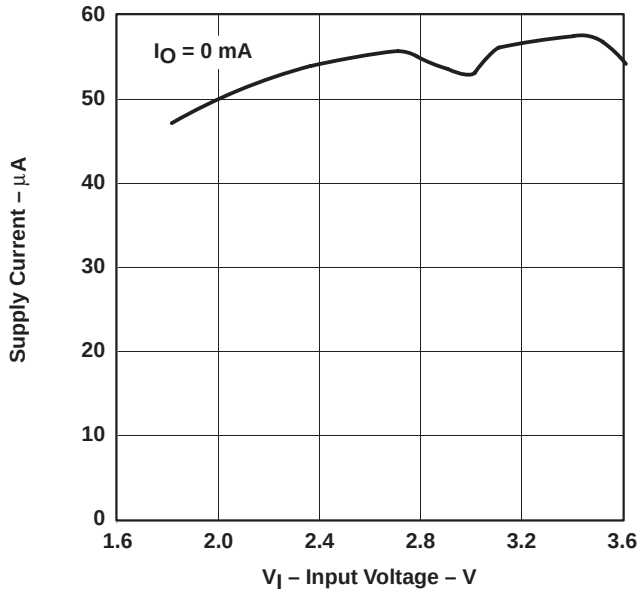


Figure 12

TPS60120
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

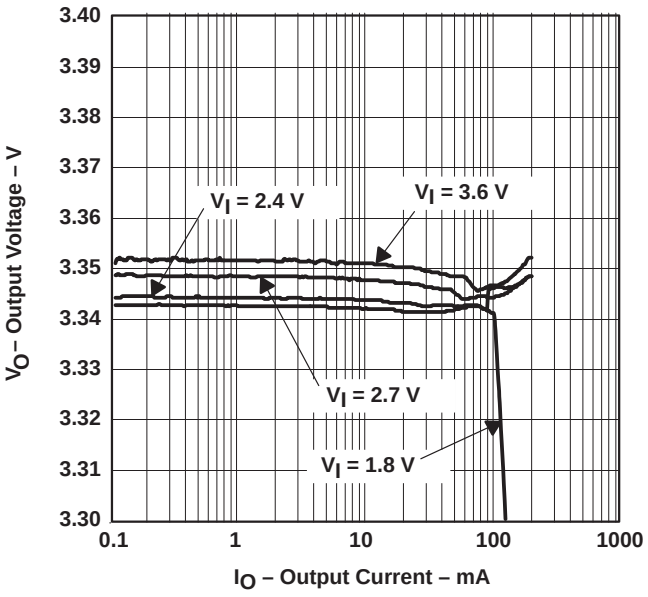


Figure 13

TYPICAL CHARACTERISTICS

TPS60122
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

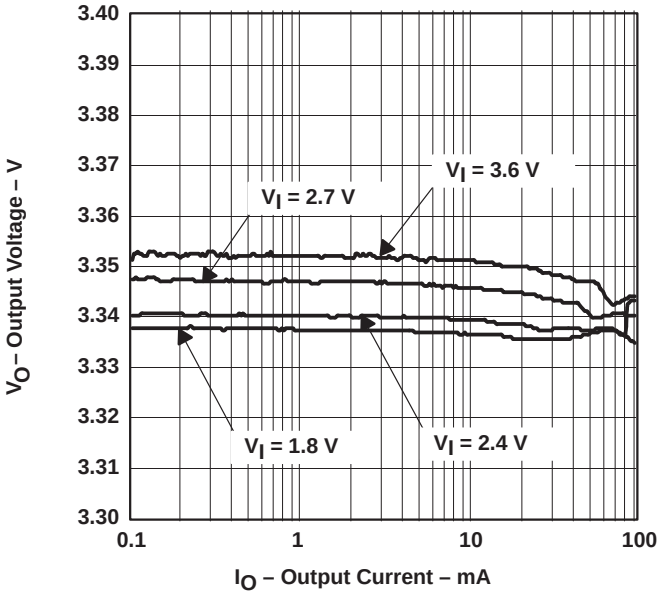


Figure 14

TPS60124
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

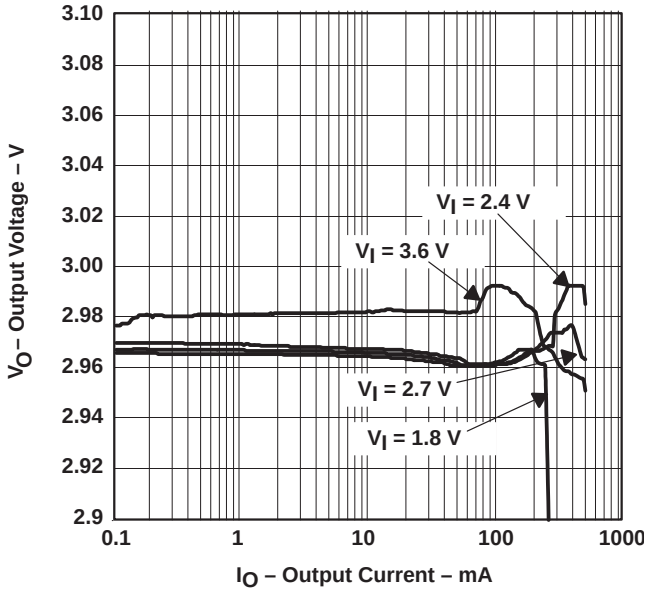


Figure 15

TPS60120
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

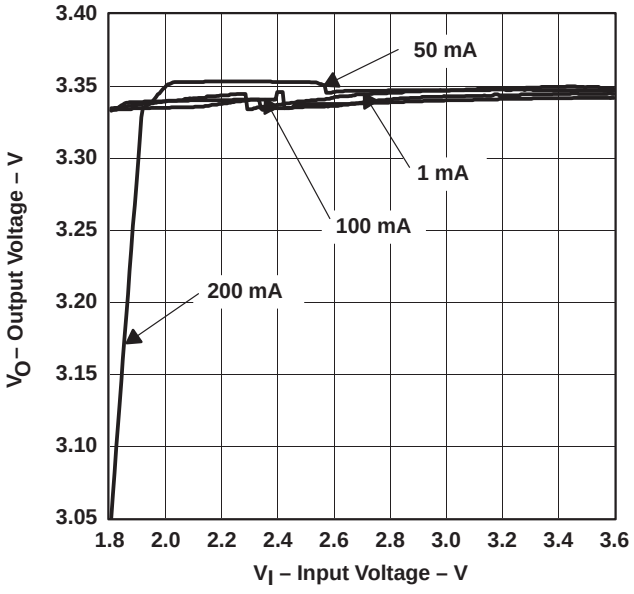


Figure 16

TPS60122
OUTPUT VOLTAGE
vs
INPUT VOLTAGE

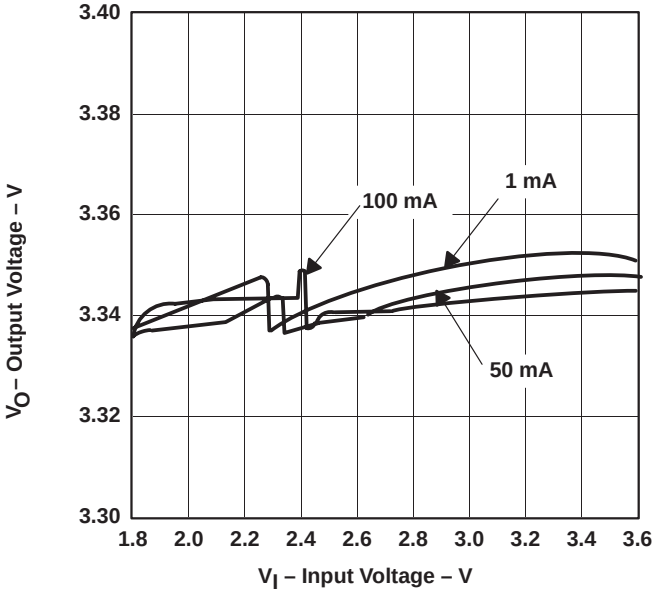


Figure 17

TYPICAL CHARACTERISTICS

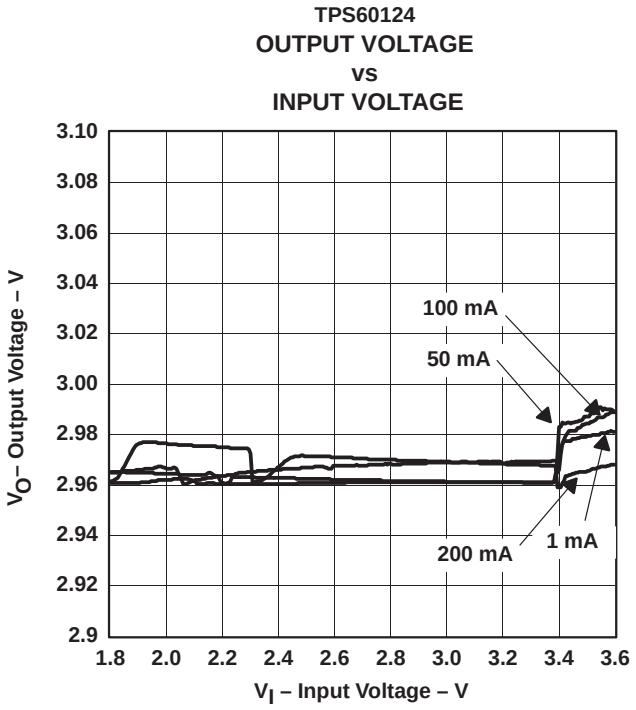


Figure 18

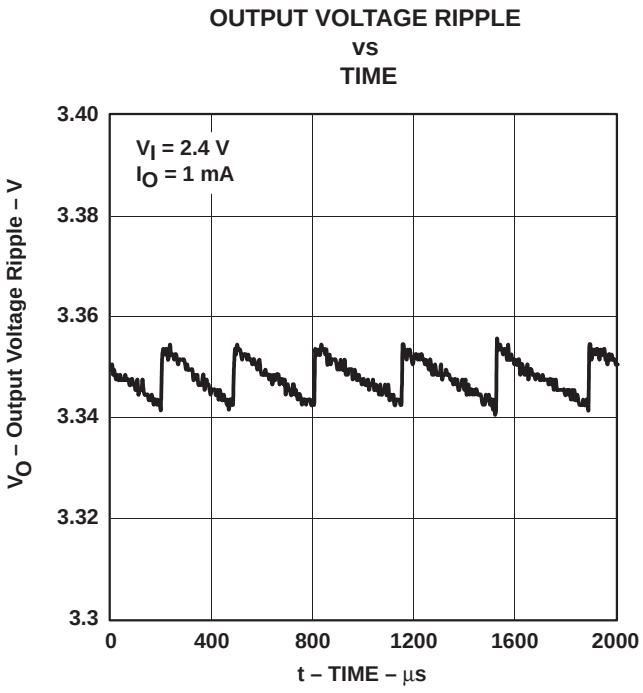


Figure 19

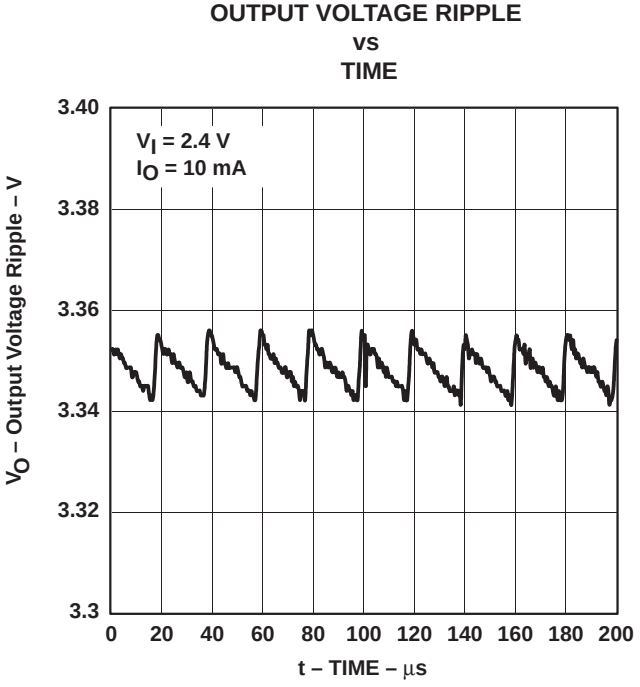


Figure 20

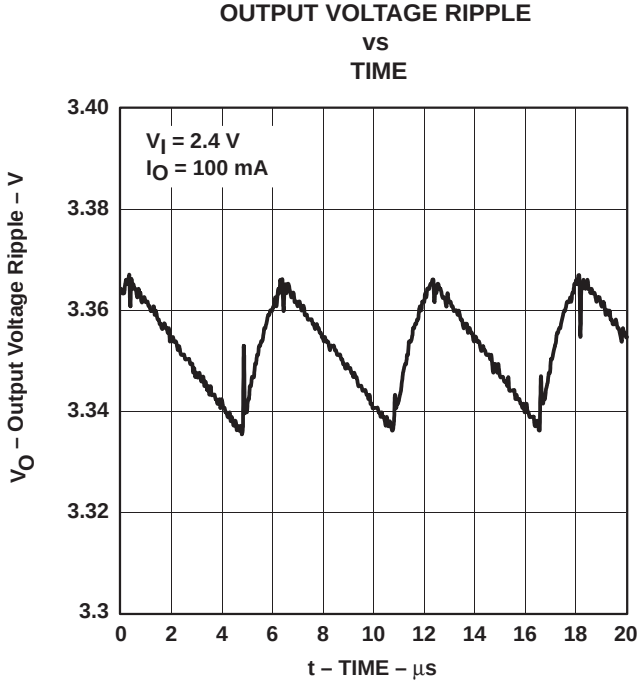


Figure 21

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE RIPPLE AMPLITUDE vs INPUT VOLTAGE

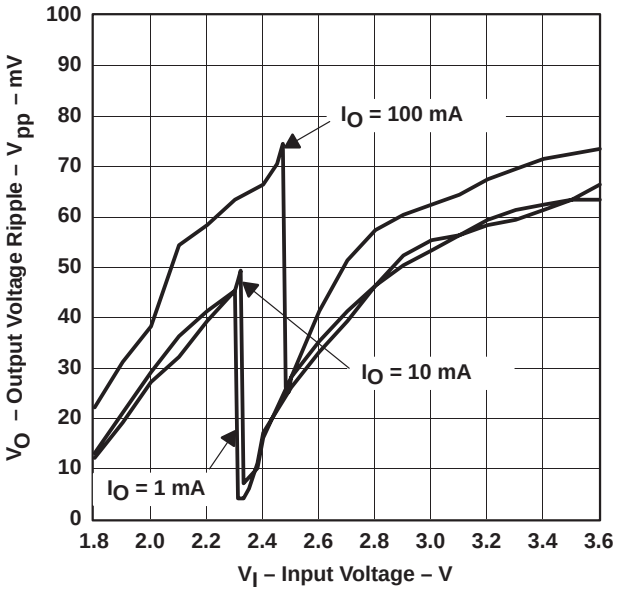


Figure 22

OSCILLATOR FREQUENCY vs INPUT VOLTAGE

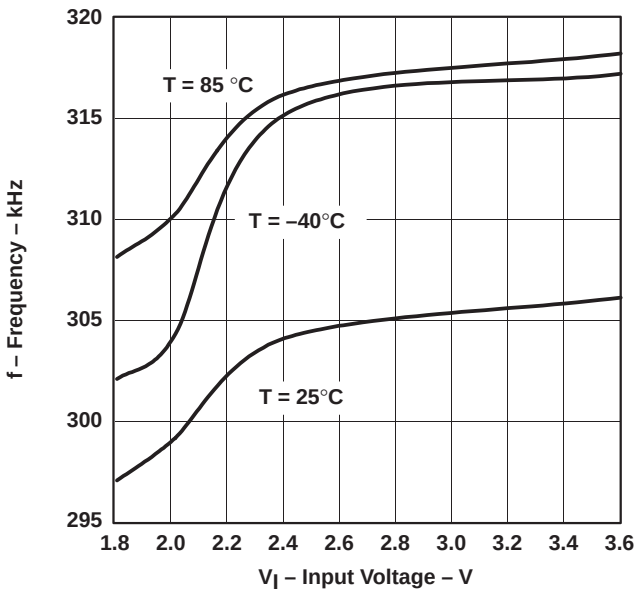


Figure 23

TPS60120 LOAD TRANSIENT RESPONSE

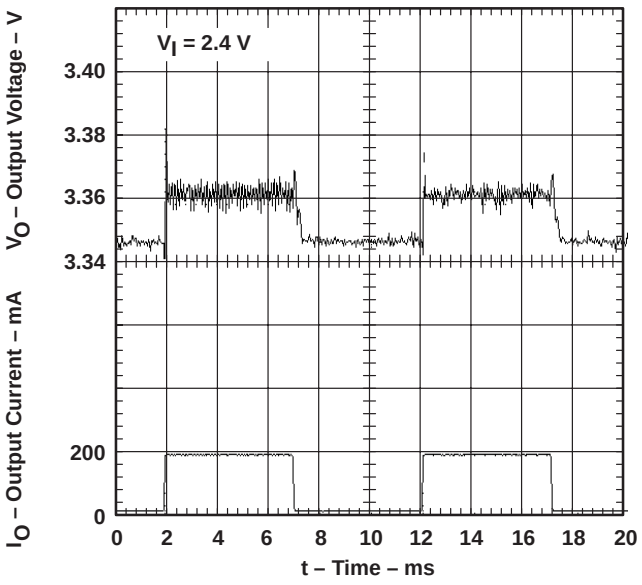


Figure 24

TPS60120 LINE TRANSIENT RESPONSE

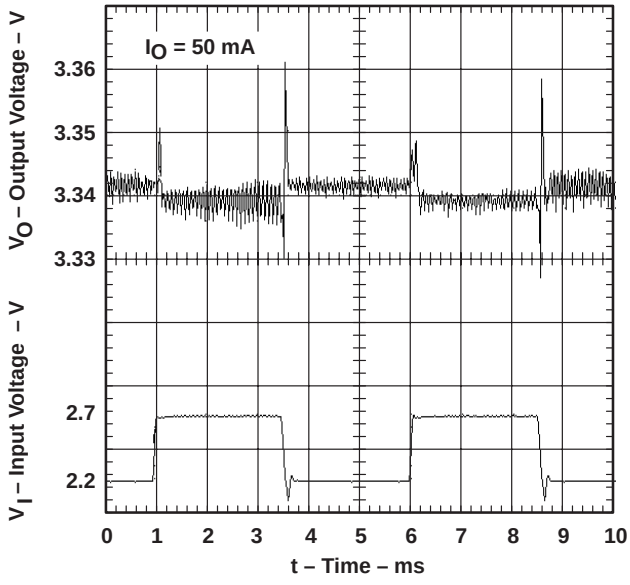


Figure 25

TYPICAL CHARACTERISTICS

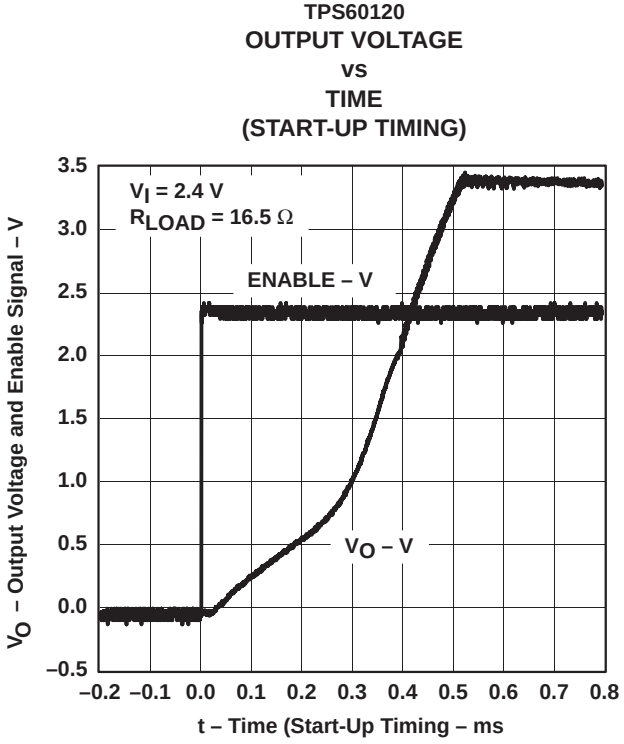


Figure 26

APPLICATION INFORMATION

capacitor selection

The TPS6012x charge pumps require only four external capacitors as shown in the basic application circuit. Their values and types are closely linked to the output current and output noise/ripple requirements. For lowest noise and ripple, low ESR (<0.1 Ω) capacitors should be used for input and output capacitors.

The input capacitor improves system efficiency by reducing the input impedance. It also stabilizes the input current of the power source. The input capacitor should be chosen according to the power supply used and the distance from the power source to the converter IC. The input capacitor also has an impact on the output ripple requirements. The lower the ESR of the input capacitor C_i, the lower is the output ripple. C_i is recommended to be about two to four times as large as $C_{(xF)}$.

The output capacitor (C_O) can be selected from 5-times to 50-times larger than $C_{(xF)}$, depending on the ripple tolerance. The larger C_O and the lower its ESR, the lower will be the output voltage ripple. C_i and C_O can be either ceramic or low-ESR tantalum; aluminum capacitors are not recommended.

APPLICATION INFORMATION

capacitor selection (continued)

Generally, the flying capacitors $C_{(xF)}$ will be the smallest. Only ceramic capacitors are recommended because they are low ESR and because they retain their capacitance at the switching frequency. Because the device regulates the output voltage with the pulse-skip technique, a larger flying capacitor will lead to a higher output voltage ripple if the size of the output capacitor is not increased. Be aware that, depending on the material used to manufacture them, ceramic capacitors might lose their capacitance over temperature and voltage. Ceramic capacitors of type X7R or X5R material will keep their capacitance over temperature and voltage, whereas Z5U or Y5V-type capacitors will decrease in capacitance. Table 2 lists recommended capacitor values.

Table 2. Recommended Capacitor Values

PART	V_I (V)	I_O (mA)	C_i (μF)		$C_{(xF)}$ (μF)	C_O (μF)		V_{PP}TYP (mV)
			TANTALUM	CERAMIC (X7R)	CERAMIC (X7R)	TANTALUM	CERAMIC (X7R)	
TPS60120 TPS60121 TPS60124 TPS60125	2.4	150	4.7	4.7	2.2	22	4.7	65
							22	40
		200	10	4.7	2.2	22	4.7	80
				10			22	35
TPS60122 TPS60123	2.4	50		2.2	1		10	70
		100		4.7				80

The TPS6012x devices are charge pumps that regulate the output voltage using the pulse-skip operating mode. The output voltage ripple is therefore dependent on the values and the ESR of the input, output and flying capacitors. The only possibility to reduce the output voltage ripple is to choose the appropriate capacitors. The lowest output voltage ripple can be achieved with ceramic capacitors due to their low ESR and their frequency characteristic.

Ceramic capacitors typically have an ESR that is more than 10 times lower than tantalum capacitors and they retain their capacitance at frequencies more than 10 times higher than tantalum capacitors. Many different tantalum capacitors act as an inductance for frequencies higher than 200 kHz. This behavior increases the output voltage ripple. Therefore, the best choice for a minimized ripple is the ceramic capacitor. For applications that do not need higher performance in output voltage ripple, tantalum capacitors with a low ESR are a possibility for input and output capacitor, but a ceramic capacitor should be connected in parallel. Be aware that the ESR of tantalum capacitors is indirectly proportional to the physical size of the capacitor.

Table 2 is a good starting point for choosing the capacitors. If the output voltage ripple is too high for the application, it can be improved by selecting the appropriate capacitors. The first step is to increase the capacitance at the output. If the ripple is still too high, the second step would be to increase the capacitance at the input.

For the TPS60120, TPS60121, TPS60124, and TPS60125, the smallest board space can be achieved using Sprague's 595D-series tantalum capacitors for input and output. However, with the trend towards high capacitance ceramic capacitors in smaller size packages, these types of capacitors may become more competitive in size. The smallest size for the TPS60122 and TPS60123 can be achieved using the recommended ceramic capacitors.

Tables 3 and 4 lists the manufacturers of recommended capacitors. In most applications surface-mount tantalum capacitors will be the right choice. However, ceramic capacitors provide the lowest output voltage ripple due to their typically lower ESR.

APPLICATION INFORMATION

capacitor selection (continued)

Table 3. Recommended Capacitors

MANUFACTURER	PART NUMBER	CAPACITANCE	CASE SIZE	TYPE
Taiyo Yuden	LMK212BJ105KG–T	1 μF	0805	Ceramic
	LMK212BJ225MG–T	2.2 μF	0805	Ceramic
	LMK316BJ475KL–T	4.7 μF	1206	Ceramic
	LMK325BJ106MN–T	10 μF	1210	Ceramic
	LMK432BJ226MM–T	22 μF	1812	Ceramic
AVX	0805ZC105KAT2A	1 μF	0805	Ceramic
	1206ZC225KAT2A	2.2 μF	1206	Ceramic
	TPSC475035R0600	4.7 μF	Case C	Tantalum
	TPSC106025R0500	10 μF	Case C	Tantalum
	TPSC226016R0375	22 μF	Case C	Tantalum
Sprague	595D106X0016B2T	10 μF	Case B	Tantalum
	595D226X06R3B2T	22 μF	Case B	Tantalum
	595D226X0020C2T	22 μF	Case B	Tantalum
Kemet	T494C156K010AS	10 μF	Case C	Tantalum
	T494C226M010AS	22 μF	Case C	Tantalum

NOTE: Case code compatibility with EIA 535BAAC and CECC30801 molded chips.

Table 4. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET SITE
Taiyo Yuden	X7R/X5R ceramic	http://www.t–yuden.com/
AVX	X7R/X5R ceramic TPS-series tantalum	http://www.avxcorp.com/
Sprague	595D-series tantalum 593D-series tantalum	http://www.vishay.com/
Kemet	T494-series tantalum	http://www.kemet.com/

power dissipation

The power dissipated in the TPS6012x depends on output current and mode of operation (1.5x or doubler voltage conversion mode). It is described by the following:

$P_{DISS} = \left(\frac{1}{\eta} - 1\right) V_O \times I_O$ (Efficiency η mainly depends on V_I and also on I_O. See efficiency graphs.)

P_{DISS} must be less than that allowed by the package rating. See the absolute maximum ratings for 20-pin PWP package power-dissipation limits and deratings.

APPLICATION INFORMATION

board layout

Careful board layout is necessary due to the high transient currents and switching frequency of the converter. All capacitors should be soldered in close proximity to the IC. Connect ground and power ground pins through a short, low-impedance trace. A PCB layout proposal for a two-layer board is given in Figure 27. The bottom layer of the board carries only ground potential for best performance.

An evaluation module for the TPS60120 is available and can be ordered under product code TPS60120EVM–142. The EVM uses the layout shown in Figure 27. The layout also provides improved thermal performance as the exposed leadframe of the PowerPAD package can be soldered to the PCB.

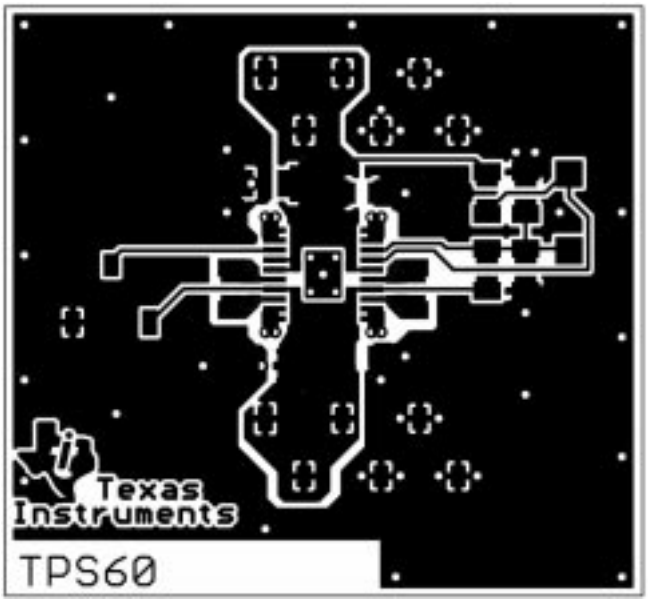


Figure 27. Recommended PCB Layout for TPS6012X

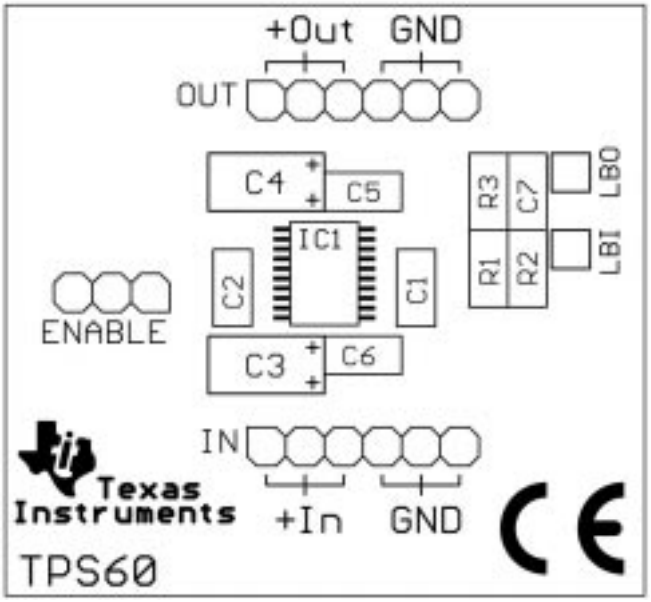


Figure 28. Component Placement

Table 5. Component Identification

IC1	TPS6012x
C1, C2	Flying capacitors
C3, C6	Input capacitors
C4, C5	Output capacitors
C7	Stabilization capacitor for LBI
R1, R2	Resistive divider for LBI
R3	Pullup resistor for LBO

The best performance of the converter is achieved with the additional bypass capacitors C5 and C6 at input and output. Capacitor C7 should be included if the large line transients are expected. The capacitors are not required. They can be omitted in most applications.

APPLICATION INFORMATION

application proposals

paralleling of two TPS6012x to deliver 400-mA total output current

Two TPS6012x devices can be connected in parallel to yield higher load currents. The circuit of Figure 29 can deliver up to 400 mA at an output voltage of 3.3 V. The devices can share the output capacitors, but each one requires its own transfer capacitors and input capacitor. If both a TPS60120 and a TPS60121 are used, it is possible to monitor the battery voltage with the TPS60120 using the low-battery comparator function and to supervise the output voltage with the TPS60121 using the power-good comparator. Make the layout of the charge pumps as similar as possible, and position the output capacitor the same distance from both devices.

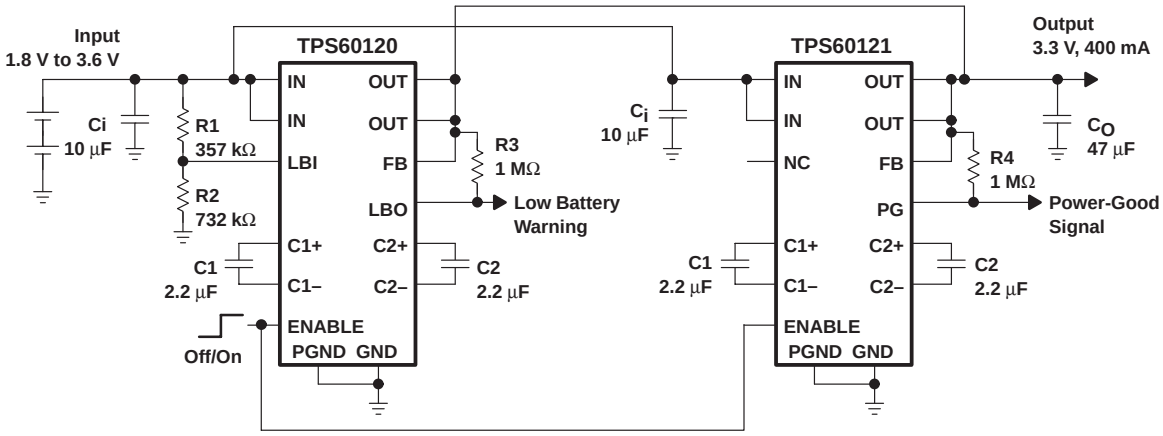


Figure 29. Paralleling of Two TPS6012x Charge Pumps

APPLICATION INFORMATION

TPS6012x operated with ultralow quiescent current

Because the output of the TPS6012x is isolated from the input when the devices are disabled, and because the internal resistive divider is disconnected in shutdown, an ultralow quiescent current mode can be implemented. In this mode, the output voltage is sustained because the converter is periodically enabled to refresh the output capacitor. The necessary external control signal that is applied to the ENABLE pin is generated from a microcontroller like the ultralow power microcontroller MSP430. For a necessary supply current for the system of 1 mA and a minimum supply voltage of 3 V with a 22-µF output capacitor, the refresh has to be done after a maximum of 3.5 ms. Longer refresh periods can be achieved with a larger output capacitor.

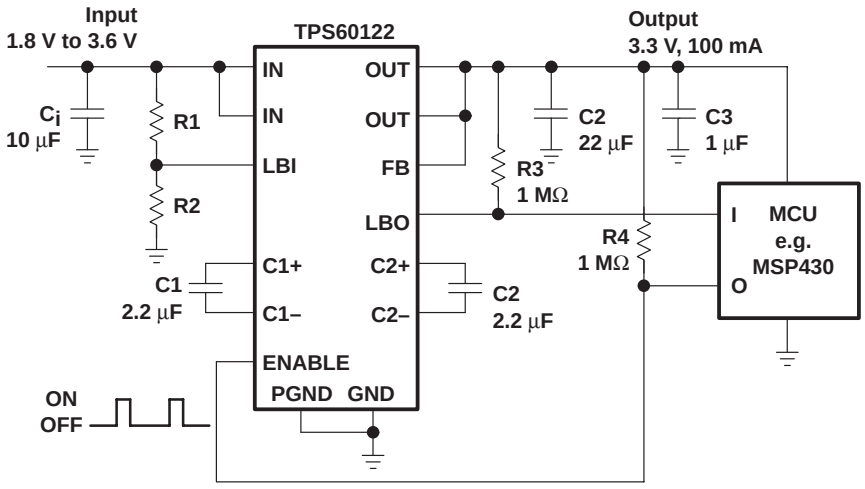


Figure 30. TPS60122 in UltraLow Quiescent Current Mode

regulated discharge of the output capacitors after disabling of the TPS6012x

During shutdown of the charge pump TPS6012x, the output is isolated from the input. Therefore, the discharging of the output capacitor depends on the load and on the leakage current of the capacitor. In certain applications it is necessary to completely remove the supply voltage from the load in shutdown mode. That means the output capacitor of the charge pump has to be actively discharged when the charge pump is disabled. Figure 31 shows one solution to this problem.

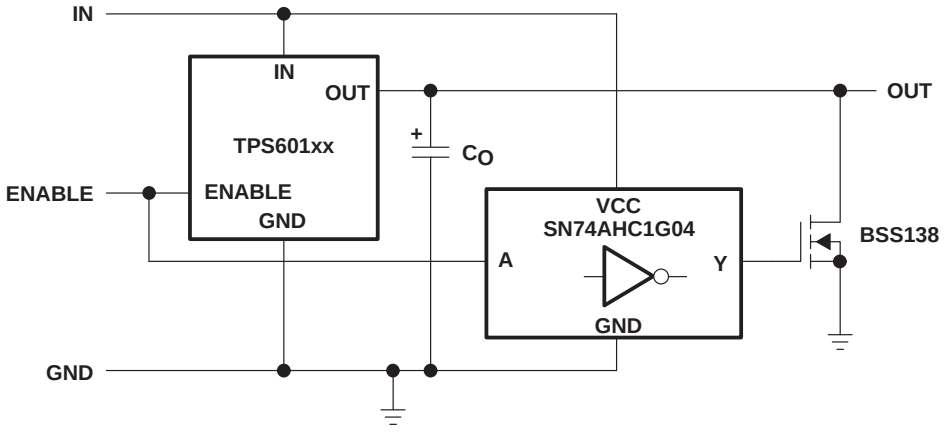


Figure 31. Block Diagram of the Regulated Discharge of the Output Capacitor

APPLICATION INFORMATION

related information

application reports

For more application information see:

- PowerPAD™ Application Report, Literature Number SLMA002
- *TPS6010x/TPS6011x Charge Pump Application Report*, Literature Number SLVA070
- Designer Note Page: Powering the TMS320C5420 Using the TPS60100, TPS76918, and the TPS3305-18, Literature Number SLVA082.

device family products

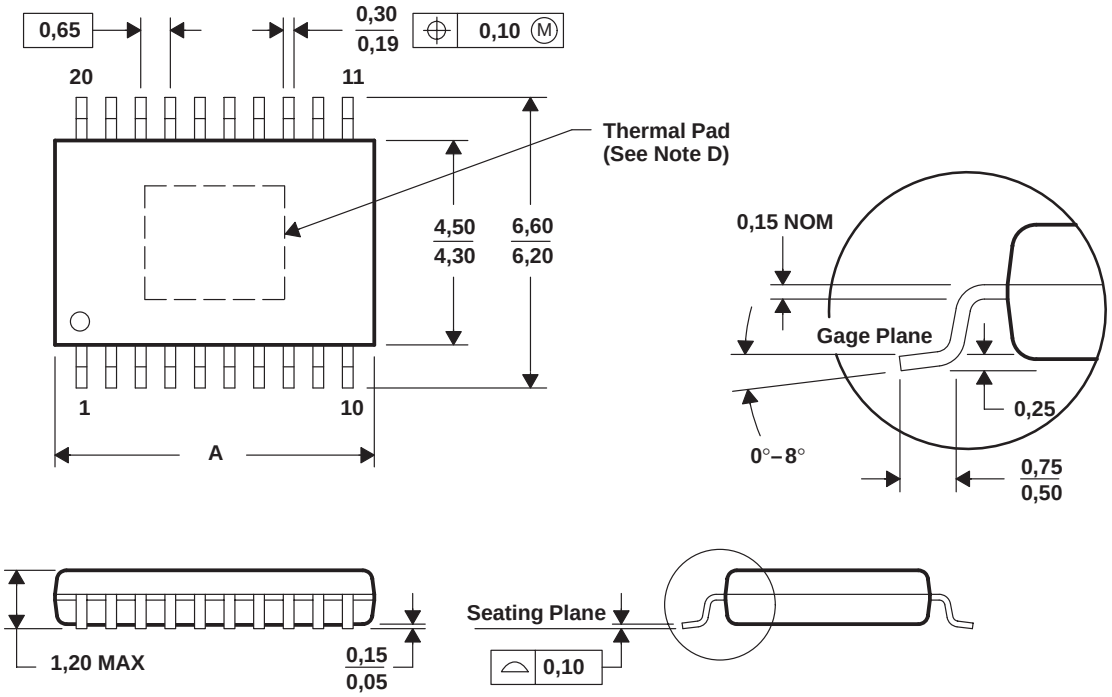
Other devices in this family are:

PART NUMBER	DATASHEET LITERATURE CODE	DESCRIPTION
TPS60100	SLVS213B	Regulated 3.3-V, 200-mA low-noise charge pump dc-dc converter
TPS60101	SLVS214A	Regulated 3.3-V, 100-mA low-noise charge pump dc-dc converter
TPS60110	SLVS215A	Regulated 5-V, 300-mA low-noise charge pump dc-dc converter
TPS60111	SLVS216A	Regulated 5-V, 150-mA low-noise charge pump dc-dc converter
TPS60130	SLVS258	Regulated 5-V, 300-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60131	SLVS258	Regulated 5-V, 300-mA high efficiency charge pump dc-dc converter with power-good comparator
TPS60132	SLVS258	Regulated 5-V, 150-mA high efficiency charge pump dc-dc converter with low-battery comparator
TPS60133	SLVS258	Regulated 5-V, 150-mA high efficiency charge pump dc-dc converter with power-good comparator

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



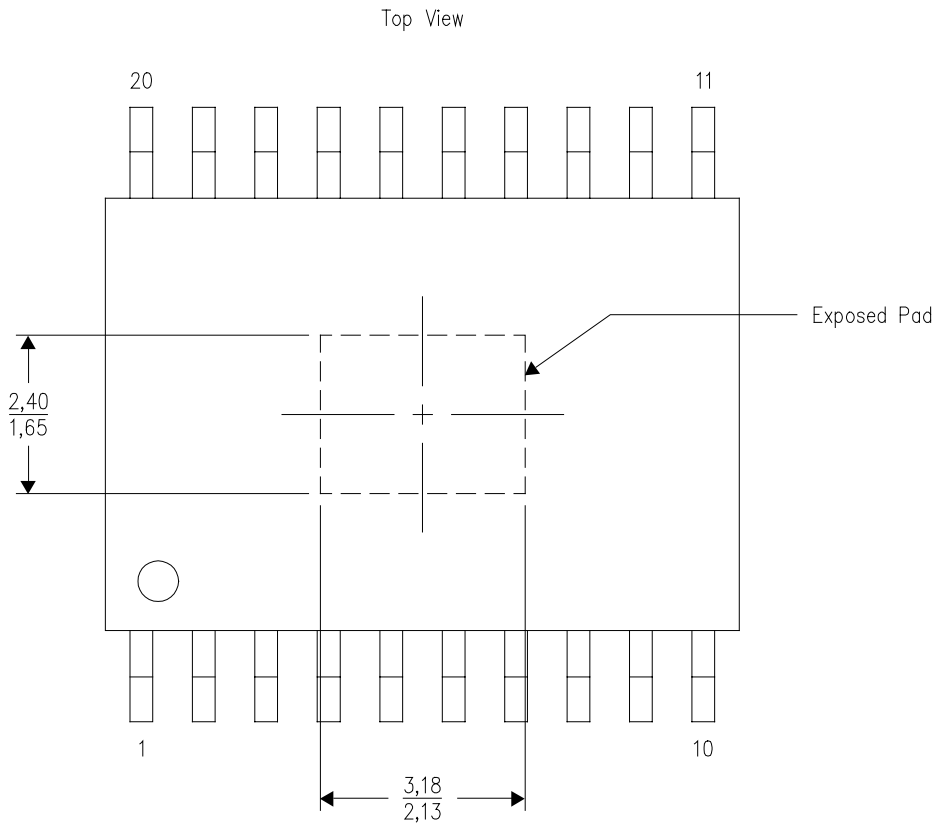
DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments Incorporated.

PWP (R-PDSO-G20) **PowerPAD™ PLASTIC SMALL-OUTLINE**



06/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS60120PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:

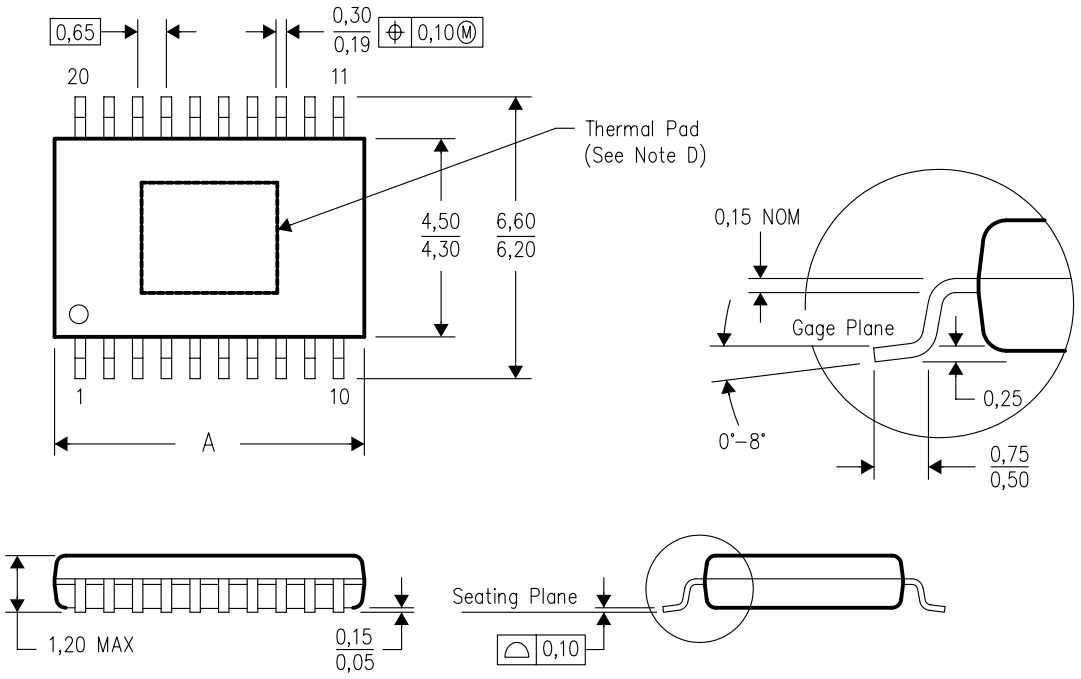
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

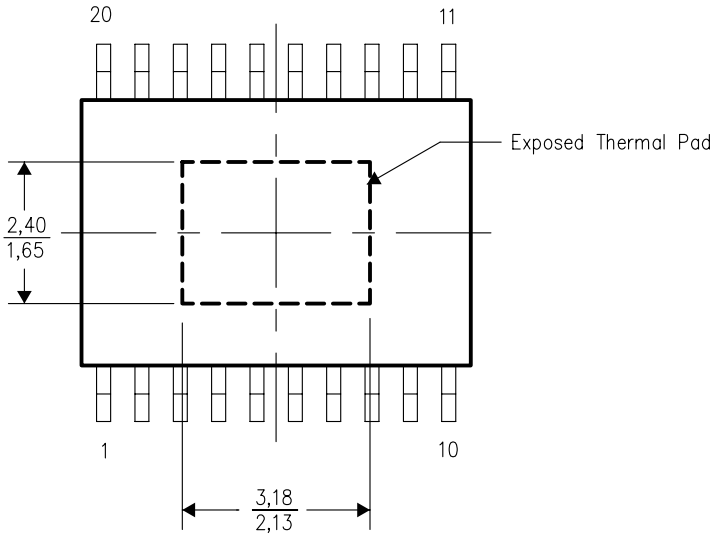
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

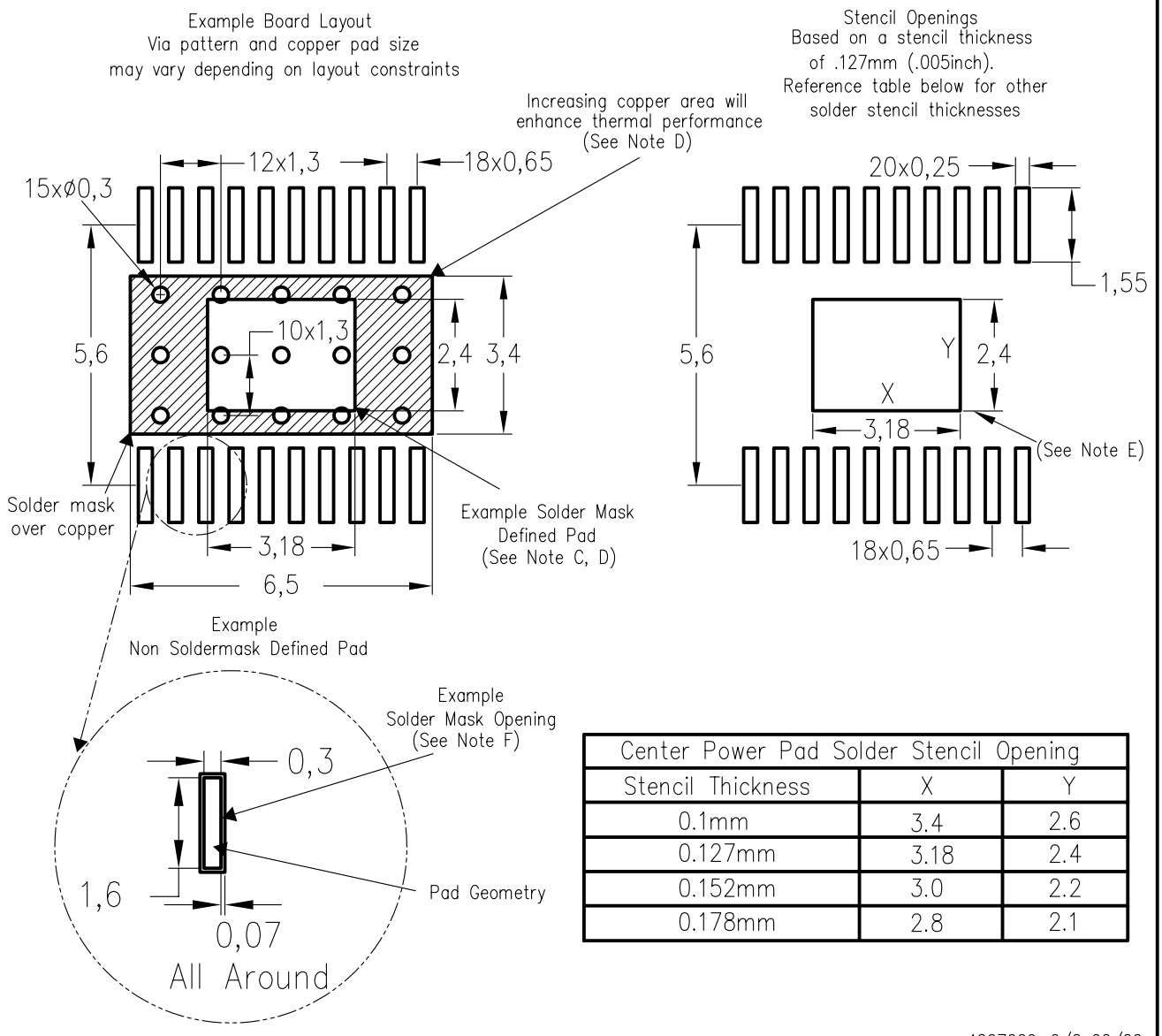


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.18	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS60120PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60120PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60121PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60122PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60123PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60124PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS60125PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
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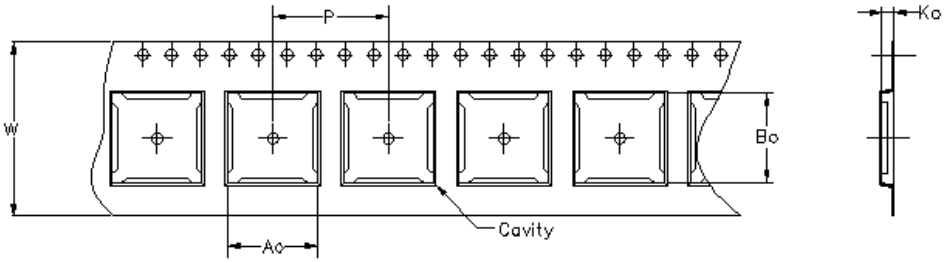
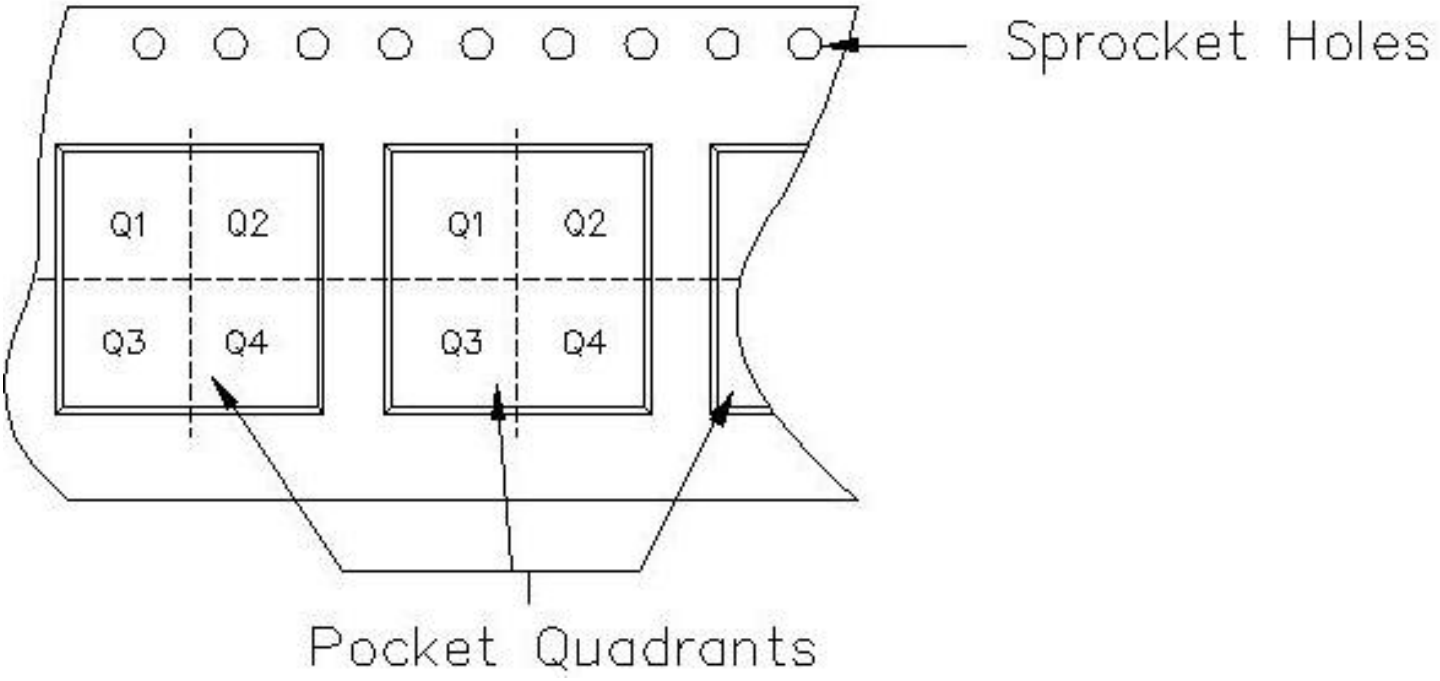
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



Carrier tape design is defined largely by the component lentgh, width, and thickness.

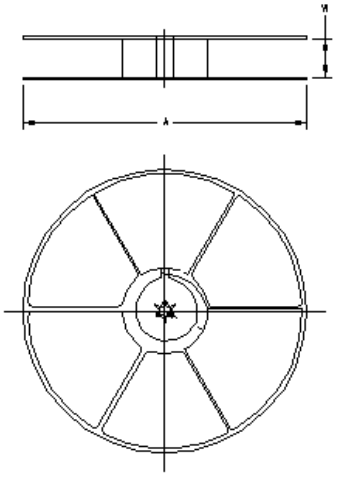
Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

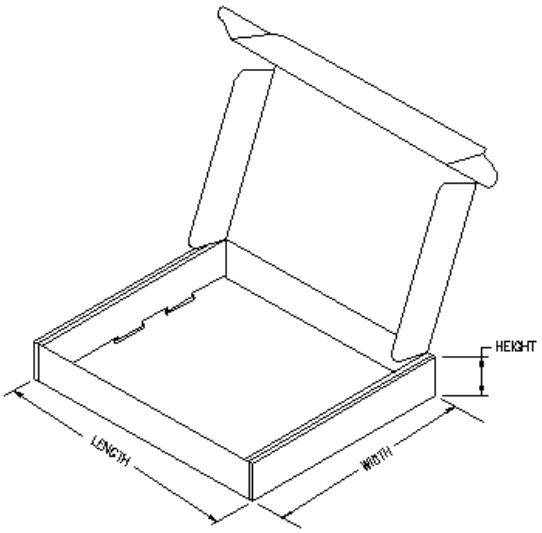
PACKAGE MATERIALS INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60120PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1
TPS60121PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1
TPS60122PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1
TPS60123PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1
TPS60124PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1
TPS60125PWPR	PWP	20	TAI	330	16	6.95	7.1	1.6	8	16	Q1



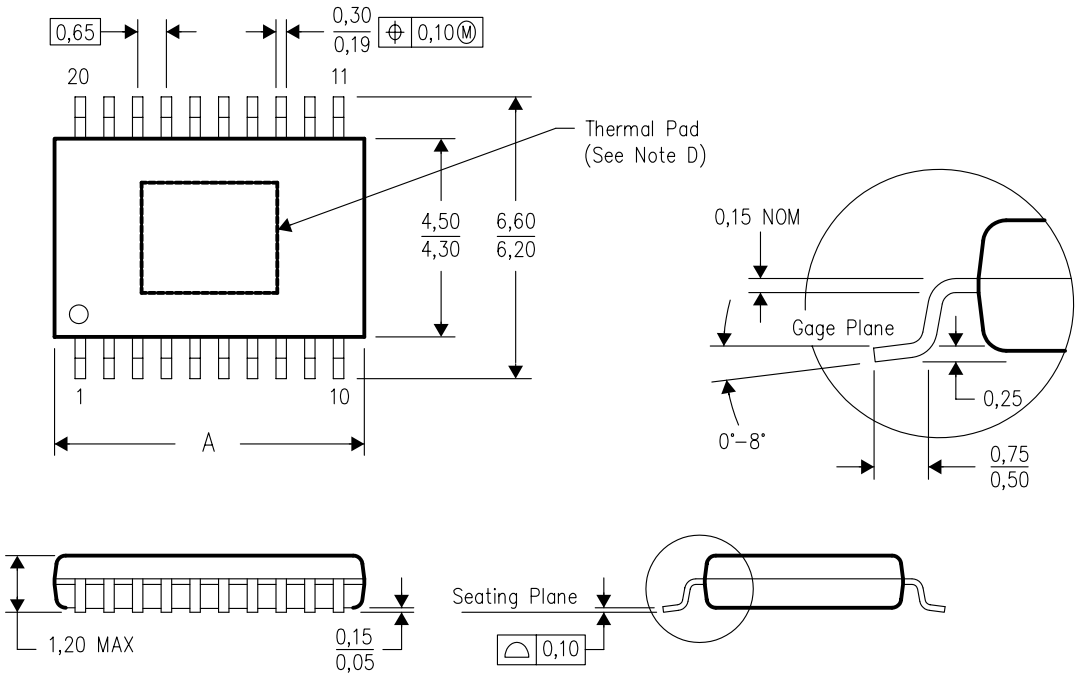
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TPS60120PWPR	PWP	20	TAI	346.0	346.0	33.0
TPS60121PWPR	PWP	20	TAI	346.0	346.0	33.0
TPS60122PWPR	PWP	20	TAI	346.0	346.0	33.0
TPS60123PWPR	PWP	20	TAI	346.0	346.0	33.0
TPS60124PWPR	PWP	20	TAI	346.0	346.0	33.0
TPS60125PWPR	PWP	20	TAI	346.0	346.0	33.0


HEIGHT
LENGTH
WIDTH

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

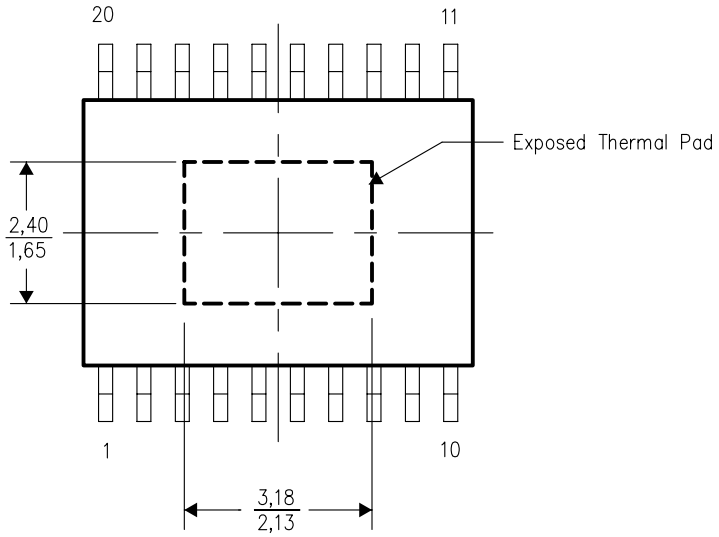
PowerPAD is a trademark of Texas Instruments.

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

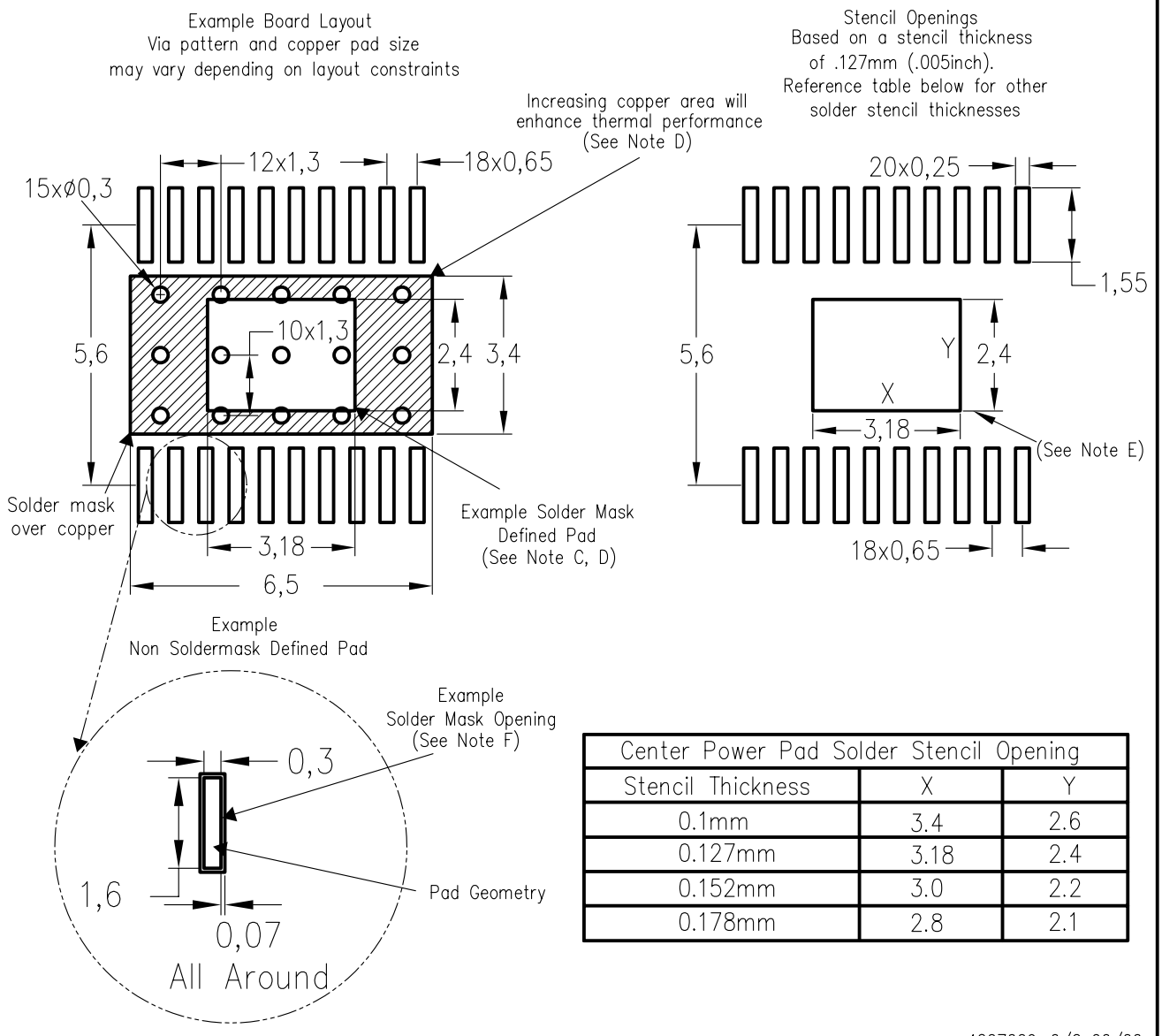


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.4	2.6
0.127mm	3.18	2.4
0.152mm	3.0	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
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E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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		Wireless	www.ti.com/wireless

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