

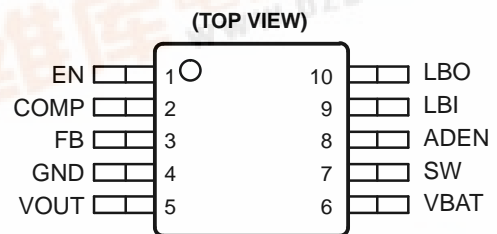


HIGH-EFFICIENCY, 1-CELL AND 2-CELL BOOST CONVERTERS

FEATURES

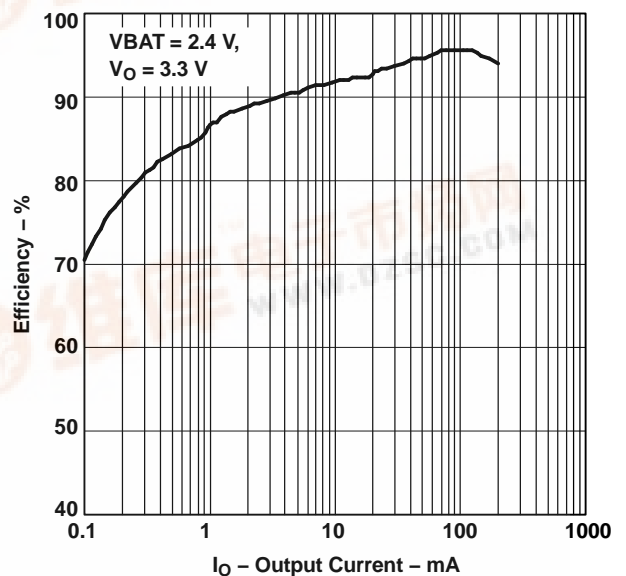
- **Integrated Synchronous Rectifier for Highest Power Conversion Efficiency (>95%)**
- **Start-Up Into Full Load With Supply Voltages as Low as 0.9 V, Operating Down to 0.8 V**
- **200-mA Output Current From 0.9-V Supply**
- **Powersave-Mode for Improved Efficiency at Low Output Currents**
- **Autodischarge Allows to Discharge Output Capacitor During Shutdown**
- **Device Quiescent Current Less Than 50 μ A**
- **Ease-of-Use Through Isolation of Load From Battery During Shutdown of Converter**
- **Integrated Antiringing Switch Across Inductor**
- **Integrated Low Battery Comparator**
- **Micro-Small 10-Pin MSOP Package**
- **Applications Include All Single- or Dual-Cell Battery Operated Products Like Internet Audio Players, Pager, Portable Medical Diagnostic Equipment, Remote Control, Wireless Headsets**
- **EVM Available (TPS6101xEVM-157)**

An autodischarge function allows discharging the output capacitor during shutdown mode. This is especially useful when a microcontroller or memory is supplied, where residual voltage across the output capacitor can cause malfunction of the applications. When programming the ADEN-pin, the autodischarge function can be disabled. A low-EMI mode is implemented to reduce interference and radiated electromagnetic energy when the converter enters the discontinuous conduction mode. The device is packaged in the micro-small space saving 10-pin MSOP package.




ACTUAL SIZE
(3,05mm x 4,98mm)

EFFICIENCY VS OUTPUT CURRENT



DESCRIPTION

The TPS6101x devices are boost converters intended for systems that are typically operated from a single- or dual-cell nickel-cadmium (NiCd), nickel-metal hydride (NiMH), or alkaline battery. The converter output voltage can be adjusted from 1.5 V to a maximum of 3.3 V, by an external resistor divider or, is fixed internally on the chip. The devices provide an output current of 200 mA with a supply voltage of only 0.9 V. The converter starts up into a full load with a supply voltage of only 0.9 V and stays in operation with supply voltages down to 0.8 V.

The converter is based on a fixed frequency, current mode, pulse-width-modulation (PWM) controller that goes automatically into power save mode at light load. It uses a built-in synchronous rectifier, so, no external Schottky diode is required and the system efficiency is improved. The current through the switch is limited to a maximum value of 1300 mA. The converter can be disabled to minimize battery drain. During shutdown, the load is completely isolated from the battery.



TPS61010, TPS61011
TPS61012, TPS61013
TPS61014, TPS61015, TPS61016

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

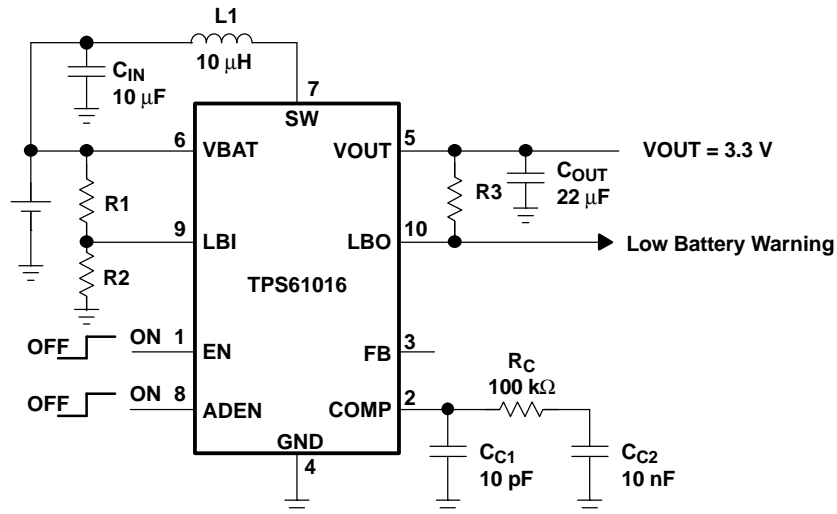


Figure 1. Typical Application Circuit for Fixed Output Voltage Option

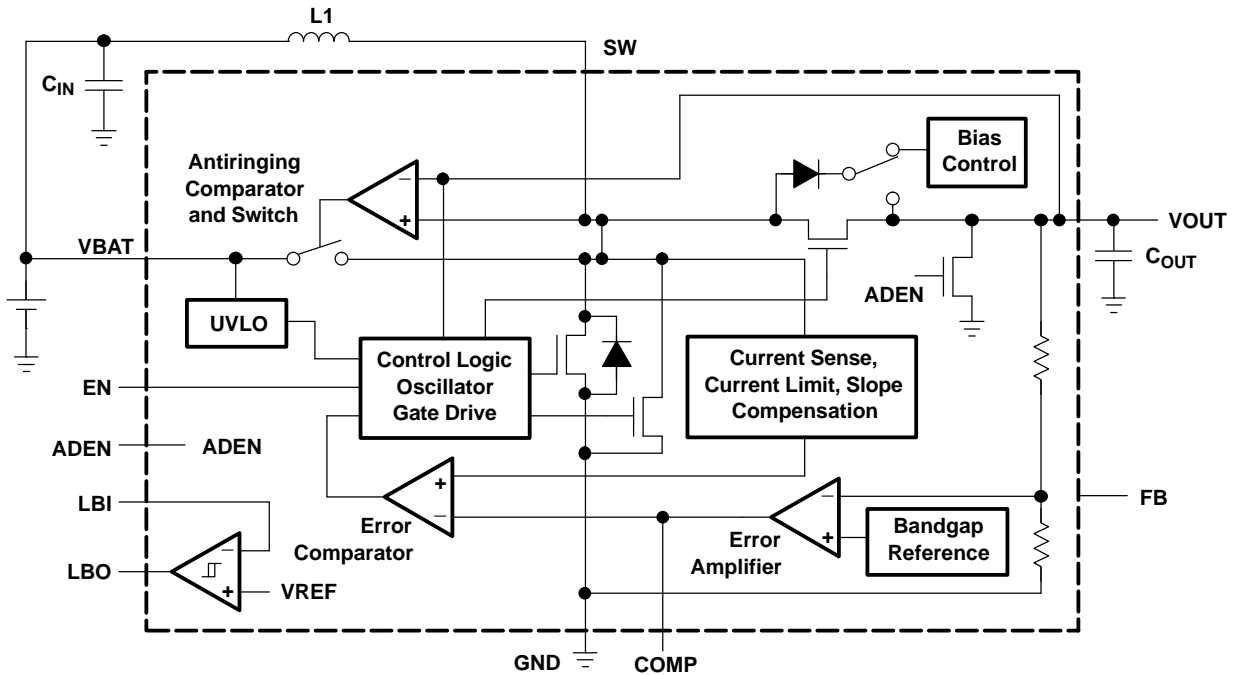
AVAILABLE OUTPUT VOLTAGE OPTIONS

| T _A | OUTPUT VOLTAGE | PART NUMBER (1) | MARKING DGS PACKAGE |
|----------------|--------------------------------|-----------------|---------------------|
| -40°C to 85°C | Adjustable from 1.5 V to 3.3 V | TPS61010DGS | AIP |
| | 1.5 V | TPS61011DGS | AIQ |
| | 1.8 V | TPS61012DGS | AIR |
| | 2.5 V | TPS61013DGS | AIS |
| | 2.8 V | TPS61014DGS | AIT |
| | 3.0 V | TPS61015DGS | AIU |
| | 3.3 V | TPS61016DGS | AIV |

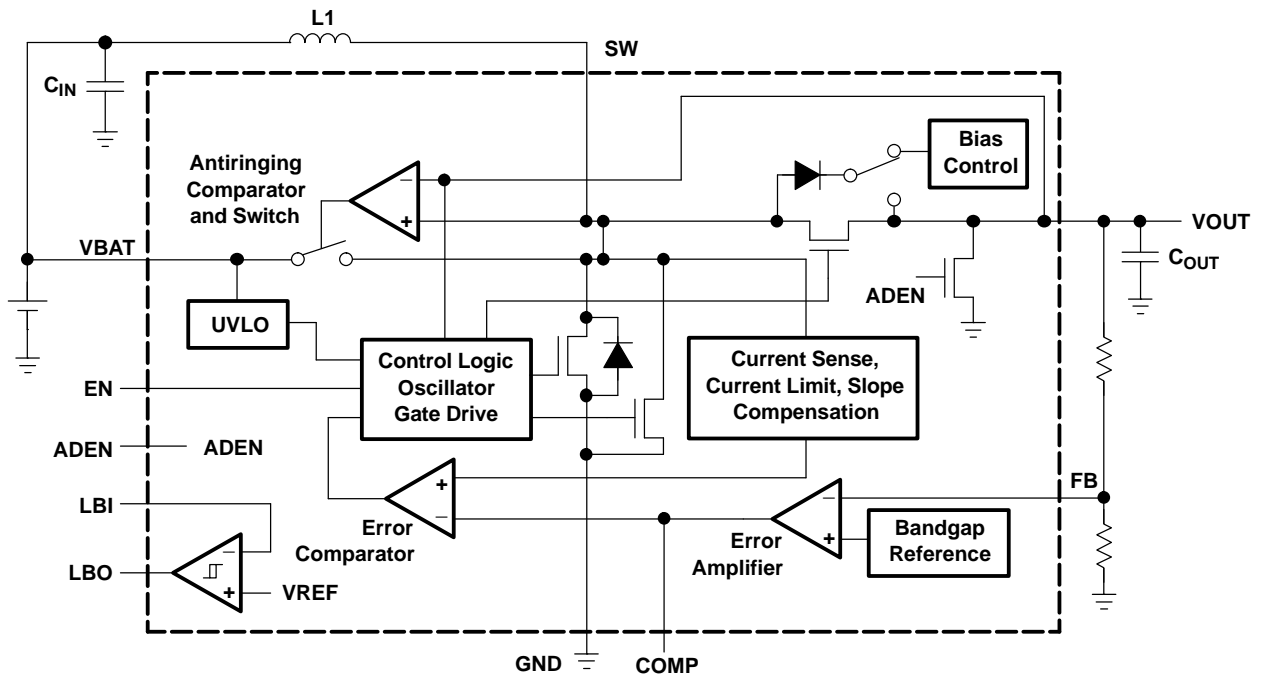
(1) The DGS package is available taped and reeled. Add R suffix to device type (e.g. TPS61010DGSR) to order quantities of 3000 devices per reel.

FUNCTIONAL BLOCK DIAGRAMS

fixed output voltage versions TPS61011 to TPS61016



adjustable output voltage version TPS61010



TPS61010, TPS61011
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Terminal Functions

| terminal name | no. | I/O | description |
|---------------|-----|-----|---|
| ADEN | 8 | I | Autodischarge input. The autodischarge function is enabled if this pin is connected to VBAT, it is disabled if ADEN is tied to GND. |
| COMP | 2 | I | Compensation of error amplifier. Connect an R/C/C network to set frequency response of control loop. |
| EN | 1 | I | Chip-enable input. The converter is switched on if this pin is set high, it is switched off if this pin is connected to GND. |
| FB | 3 | I | Feedback input for adjustable output voltage version TPS61010. Output voltage is programmed depending on the output voltage divider connected there. For the fixed output voltage versions, leave FB-pin unconnected. |
| GND | 4 | | Ground |
| LBI | 9 | I | Low-battery detector input. A low battery warning is generated at LBO when the voltage on LBI drops below the threshold of 500 mV. Connect LBI to GND or VBAT if the low-battery detector function is not used. Do not leave this pin floating. |
| LBO | 10 | O | Open-drain low-battery detector output. This pin is pulled low if the voltage on LBI drops below the threshold of 500 mV. A pullup resistor must be connected between LBO and VOUT. |
| SW | 7 | I | Switch input pin. The inductor is connected to this pin. |
| VOUT | 5 | O | Output voltage. Internal resistor divider sets regulated output voltage in fixed output voltage versions. |
| VBAT | 6 | I | Supply pin |

DETAILED DESCRIPTION

Controller Circuit

The device is based on a current-mode control topology using a constant frequency pulse-width modulator to regulate the output voltage. The controller limits the current through the power switch on a pulse by pulse basis. The current-sensing circuit is integrated in the device, therefore, no additional components are required. Due to the nature of the boost converter topology used here, the peak switch current is the same as the peak inductor current, which will be limited by the integrated current limiting circuits under normal operating conditions.

The control loop must be externally compensated with an R-C-C network connected to the COMP-pin.

Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. There is no additional Schottky diode required. Because the device uses a integrated low $r_{DS(on)}$ PMOS switch for rectification, the power conversion efficiency reaches 95%.

A special circuit is applied to disconnect the load from the input during shutdown of the converter. In conventional synchronous rectifier circuits, the backgate diode of the high-side PMOS is forward biased in shutdown and allows current flowing from the battery to the output. This device, however, uses a special circuit to disconnect the backgate diode of the high-side PMOS and so, disconnects the output circuitry from the source when the regulator is not enabled (EN = low).

The benefit of this feature for the system design engineer, is that the battery is not depleted during shutdown of the converter. So, no additional effort has to be made by the system designer to ensure disconnection of the battery from the output of the converter. Therefore, design performance will be increased without additional costs and board space.

Power-Save Mode

The TPS61010 is designed for high efficiency over a wide output current range. Even at light loads, the efficiency stays high because the switching losses of the converter are minimized by effectively reducing the switching frequency. The controller enters a powersave-mode if certain conditions are met. In this mode, the controller only switches on the transistor if the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses, and goes again into powersave-mode once the output voltage exceeds a set threshold voltage.

DETAILED DESCRIPTION (continued)

Device Enable

The device is shut down when EN is set to GND. In this mode, the regulator stops switching, all internal control circuitry including the low-battery comparator, is switched off, and the load is disconnected from the input (as described above in the synchronous rectifier section). This also means that the output voltage may drop below the input voltage during shutdown.

The device is put into operation when EN is set high. During start-up of the converter, the duty cycle is limited in order to avoid high peak currents drawn from the battery. The limit is set internally by the current limit circuit and is proportional to the voltage on the COMP-pin.

Under-Voltage Lockout

An under-voltage lockout function prevents the device from starting up if the supply voltage on VBAT is lower than approximately 0.7 V. This under-voltage lockout function is implemented in order to prevent the malfunctioning of the converter. When in operation and the battery is being discharged, the device will automatically enter the shutdown mode if the voltage on VBAT drops below approximately 0.7 V.

Autodischarge

The autodischarge function is useful for applications where the supply voltage of a μC , μP , or memory has to be removed during shutdown in order to ensure a defined state of the system.

The autodischarge function is enabled when the ADEN is set high, and is disabled when the ADEN is set to GND. When the autodischarge function is enabled, the output capacitor will be discharged after the device is shut down by setting EN to GND. The capacitors connected to the output are discharged by an integrated switch of 300 Ω , hence the discharge time depends on the total output capacitance. The residual voltage on VOUT is less than 0.4 V after autodischarge.

Low-Battery Detector Circuit (LBI and LBO)

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO-pin is high impedance. The LBO-pin goes active low when the voltage on the LBI-pin decreases below the set threshold voltage of 500 mV \pm 15 mV, which is equal to the internal reference voltage. The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI-pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI-pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI-threshold.

If the low-battery detection circuit is not used, the LBI-pin should be connected to GND (or to VBAT) and the LBO-pin can be left unconnected. Do not let the LBI-pin float.

Antiringing Switch

The device integrates a circuit that removes the ringing that typically appears on the SW-node when the converter enters the discontinuous current mode. In this case, the current through the inductor ramps to zero and the integrated PMOS switch turns off to prevent a reverse current from the output capacitors back to the battery. Due to remaining energy that is stored in parasitic components of the semiconductors and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage internally to V_{BAT} and therefore, dampens this ringing.

Adjustable Output Voltage

The devices with fixed output voltages are trimmed to operate with an output voltage accuracy of \pm 3%.

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The accuracy of the adjustable version is determined by the accuracy of the internal voltage reference, the controller topology, and the accuracy of the external resistor. The reference voltage has an accuracy of $\pm 4\%$ over line, load, and temperature. The controller switches between fixed frequency and pulse-skip mode, depending on load current. This adds an offset to the output voltage that is equivalent to 1% of V_O . The tolerance of the resistors in the feedback divider determine the total system accuracy.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | UNIT |
|---|-----------------------------------|------------------------------|
| Input voltage range on | VBAT, VOUT, SW, EN, LBI, FB, ADEN | -0.3 V to 3.6 V |
| | SW | -0.3 V to 7 V |
| Voltage range on: LBO, COMP | | 3.6 V |
| Peak current into SW | | 1300 mA |
| Continuous total power dissipation | | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | | -40°C to 85°C |
| Maximum junction temperature, T_J | | 150°C |
| Storage temperature range, T_{stg} | | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10s | | 260°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

| PACKAGE | $T_A < 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ POWER RATING | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|---------------------------------------|
| DGS | 424 mW | 3.4 mW/°C | 271 mW | 220 mW |

RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|-----|-----|------|---------------|
| Supply voltage at VBAT, V_I | 0.8 | | VOUT | V |
| Maximum output current at $V_{IN} = 1.2\text{ V}$, I_O | 100 | | | mA |
| Maximum output current at $V_{IN} = 2.4\text{ V}$, I_O | 200 | | | mA |
| Inductor, L1 | 10 | 33 | | μH |
| Input capacitor, C_I | | 10 | | μF |
| Output capacitor, C_O | 10 | 22 | 47 | μF |
| Operating virtual junction temperature, T_J | -40 | | 125 | °C |

ELECTRICAL CHARACTERISTICS

 over recommended operating free-air temperature range, V_{BAT} = 1.2 V, EN = V_{BAT} (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|------|------|------|------|
| V _I | Minimum input voltage for start-up | R _L = 33 Ω | | 0.85 | 0.9 | V |
| | | R _L = 3 kΩ, T _A = 25 °C | | 0.8 | | |
| | Input voltage once started | I _O = 100 mA | | 0.8 | | |
| V _O | Programmable output voltage range | TPS61010, I _{OUT} = 100 mA | | 1.5 | 3.3 | V |
| | Output voltage | TPS61011, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 1.45 | 1.5 | 1.55 | V |
| | | TPS61012, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 1.74 | 1.8 | 1.86 | V |
| | | TPS61013, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 2.42 | 2.5 | 2.58 | V |
| | | TPS61013, 1.6 V < V _I < V _O , I _O = 0 to 200 mA | 2.42 | 2.5 | 2.58 | V |
| | | TPS61014, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 2.72 | 2.8 | 2.88 | V |
| | | TPS61014, 1.6 V < V _I < V _O , I _O = 0 to 200 mA | 2.72 | 2.8 | 2.88 | V |
| | | TPS61015, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 2.9 | 3.0 | 3.1 | V |
| | | TPS61015, 1.6 V < V _I < V _O , I _O = 0 to 200 mA | 2.9 | 3.0 | 3.1 | V |
| | | TPS61016, 0.8 V < V _I < V _O , I _O = 0 to 100 mA | 3.2 | 3.3 | 3.4 | V |
| TPS61016, 1.6 V < V _I < V _O , I _O = 0 to 200 mA | 3.2 | 3.3 | 3.4 | V | | |
| I _O | Maximum continuous output current | V _I ≥ 0.8 V | | 100 | | mA |
| | | V _I ≥ 1.8 V | | 250 | | |
| I _(SW) | Switch current limit | TPS61011, once started | 0.39 | 0.48 | | A |
| | | TPS61012, once started | 0.54 | 0.56 | | |
| | | TPS61013, once started | 0.85 | 0.93 | | |
| | | TPS61014, once started | 0.95 | 1.01 | | |
| | | TPS61015, once started | 1 | 1.06 | | |
| | | TPS61016, once started | 1.07 | 1.13 | | |
| V _(FB) | Feedback voltage | | 480 | 500 | 520 | mV |
| f | Oscillator frequency | | 420 | 500 | 780 | kHz |
| D | Maximum duty cycle | | | 85% | | |
| r _{DS(on)} | NMOS switch on-resistance | V _O = 1.5 V | | 0.37 | 0.51 | Ω |
| | PMOS switch on-resistance | | | 0.45 | 0.54 | |
| r _{DS(on)} | NMOS switch on-resistance | V _O = 3.3 V | | 0.2 | 0.37 | Ω |
| | PMOS switch on-resistance | | | 0.3 | 0.45 | |
| | Line regulation (1) | V _I = 1.2 V to 1.4 V, I _O = 100 mA | | 0.3 | | %V |
| | Load regulation (1) | V _I = 1.2 V; I _O = 50 mA to 100 mA | | 0.1 | | |
| | Autodischarge switch resistance | | | 300 | 400 | Ω |
| | Residual output voltage after autodischarge | ADEN = V _{BAT} ; EN = GND | | | 0.4 | V |
| V _{IL} | LBI voltage threshold (2) | V _(LBI) voltage decreasing | 480 | 500 | 520 | mV |
| | LBI input hysteresis | | | 10 | | mv |
| | LBI input current | | | 0.01 | 0.03 | |
| V _{OL} | LBO output low voltage | V _(LBI) = 0 V, V _O = 3.3 V, I _(OL) = 10 μA | | 0.04 | 0.2 | V |
| | LBO output leakage current | V _(LBI) = 650 mV, V _(LBO) = V _O | | | 0.03 | μA |
| I _(FB) | FB input bias current (TPS61010 only) | V _(FB) = 500 mV | | 0.01 | 0.03 | |

(1) Line and load regulation is measured as a percentage deviation from the nominal value (i.e., as percentage deviation from the nominal output voltage). For line regulation, x %/V stands for ±x% change of the nominal output voltage per 1-V change on the input/supply voltage. For load regulation, y% stands for ±y% change of the nominal output voltage per the specified current change.

(2) For proper operation the voltage at LBI may not exceed the voltage at V_{BAT}.

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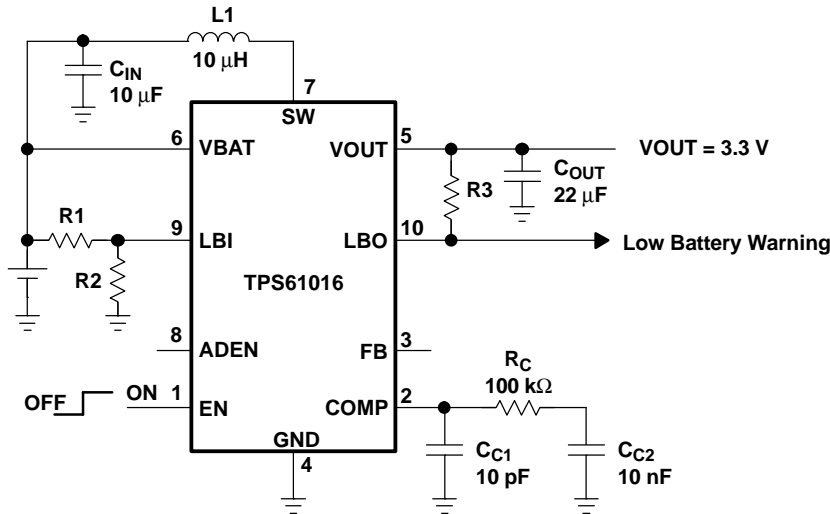
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ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, V_{BAT} = 1.2 V, EN = V_{BAT} (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|------------------|---|--|----------------------|-----|------------------------|------|----|
| V _{IL} | EN and ADEN input low voltage | 0.8 V < V _{BAT} < 3.3 V | | | 0.2 × V _{BAT} | V | |
| V _{IH} | EN and ADEN input high voltage | 0.8 V < V _{BAT} < 3.3 V | | | 0.8 × V _{BAT} | V | |
| | EN and ADEN input current | EN and ADEN = GND or V _{BAT} | | | 0.01 | 0.03 | μA |
| I _q | Quiescent current into pins V _{BAT} /SW and V _{OUT} | I _L = 0 mA, V _{EN} = V _I | V _{BAT} /SW | 31 | 46 | μA | |
| | | | V _O | 5 | 8 | | |
| I _{off} | Shutdown current from power source | V _{EN} = 0 V, ADEN = V _{BAT} , T _A = 25°C | | | 1 | 3 | μA |

PARAMETER MEASUREMENT INFORMATION



List of Components:

- IC1: Only Fixed Output Versions (Unless Otherwise Noted)
- L1: SUMIDA CDRH6D38 – 100
- C_{IN}: X7R/X5R Ceramic
- C_{OUT}: X7R/X5R Ceramic

Figure 2. Circuit Used for Typical Characteristics Measurements

TYPICAL CHARACTERISTICS

Table of Graphs

| | | FIGURE |
|--|--|--------|
| Maximum output current | vs Input voltage for $V_O = 2.5\text{ V}, 3.3\text{ V}$ | 3 |
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| | vs Output current for $V_I = 1.2\text{ V}, V_O = 2.5\text{ V}, L1 = \text{Sumida CDR74}, 10\text{ }\mu\text{H}$ | 6 |
| | vs Output current for $V_{IN} = 1.2\text{ V}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74}, 10\text{ }\mu\text{H}$ | 7 |
| | vs Output current for $V_I = 2.4\text{ V}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74}, 10\text{ }\mu\text{H}$ | 8 |
| | vs Input voltage for $I_O = 10\text{ mA}, I_O = 100\text{ mA}, I_{OUT} = 200\text{ mA}, V_O = 3.3\text{ V}, L1 = \text{Sumida CDR74}, 10\text{ }\mu\text{H}$ | 9 |
| | TPS61016, $V_{BAT} = 1.2\text{ V}, I_O = 100\text{ mA}$ | 10 |
| | Sumida CDRH6D38 - $10\text{ }\mu\text{H}$ | |
| | Sumida CDRH5D18 - $10\text{ }\mu\text{H}$ | |
| | Sumida CDRH74 - $10\text{ }\mu\text{H}$ | |
| | Sumida CDRH74B - $10\text{ }\mu\text{H}$ | |
| | Coilcraft DS 1608C - $10\text{ }\mu\text{H}$ | |
| | Coilcraft DO 1608C - $10\text{ }\mu\text{H}$ | |
| | Coilcraft DO 3308P - $10\text{ }\mu\text{H}$ | |
| | Coilcraft DS 3316 - $10\text{ }\mu\text{H}$ | |
| | Coiltronics UP1B - $10\text{ }\mu\text{H}$ | |
| | Coiltronics UP2B - $10\text{ }\mu\text{H}$ | |
| | Murata LQS66C - $10\text{ }\mu\text{H}$ | |
| Murata LQN6C - $10\text{ }\mu\text{H}$ | | |
| TDK SLF 7045 - $10\text{ }\mu\text{H}$ | | |
| TDK SLF 7032 - $10\text{ }\mu\text{H}$ | | |
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TYPICAL CHARACTERISTICS

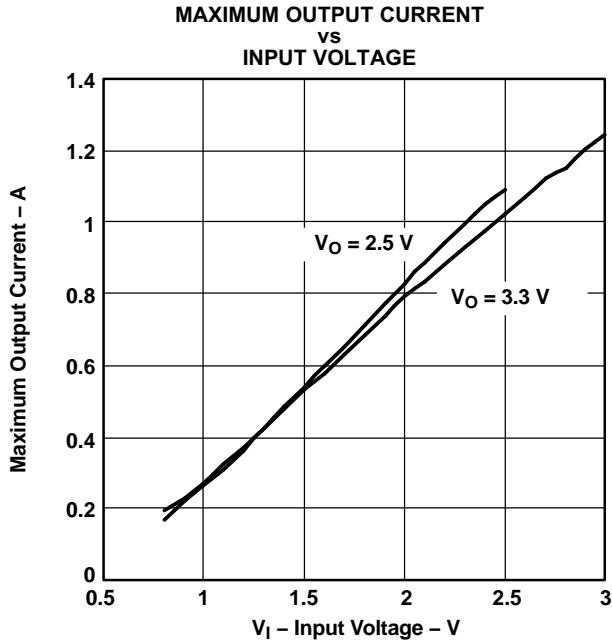


Figure 3.

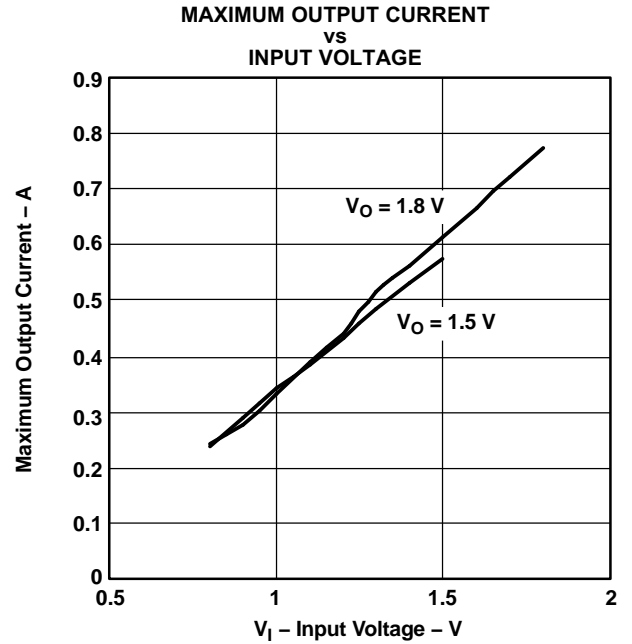


Figure 4.

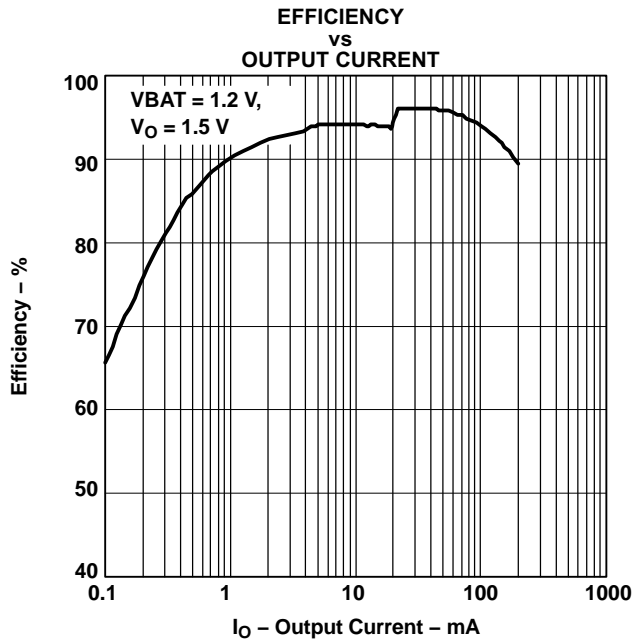


Figure 5.

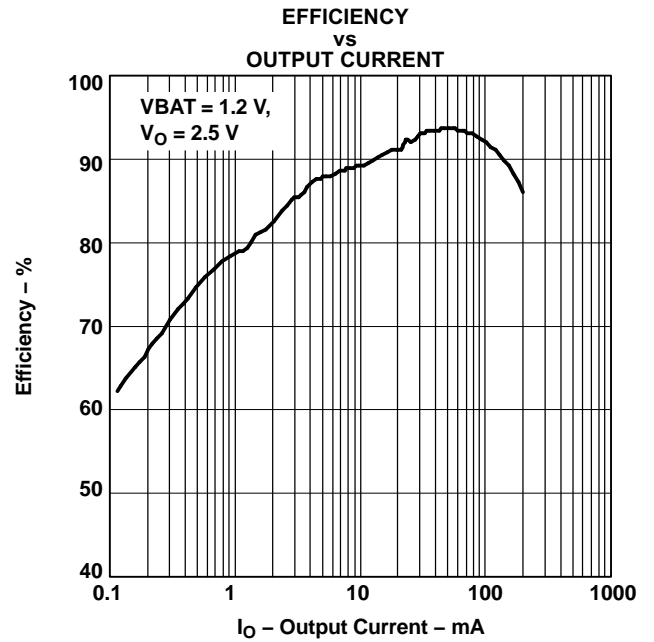


Figure 6.

TYPICAL CHARACTERISTICS (continued)

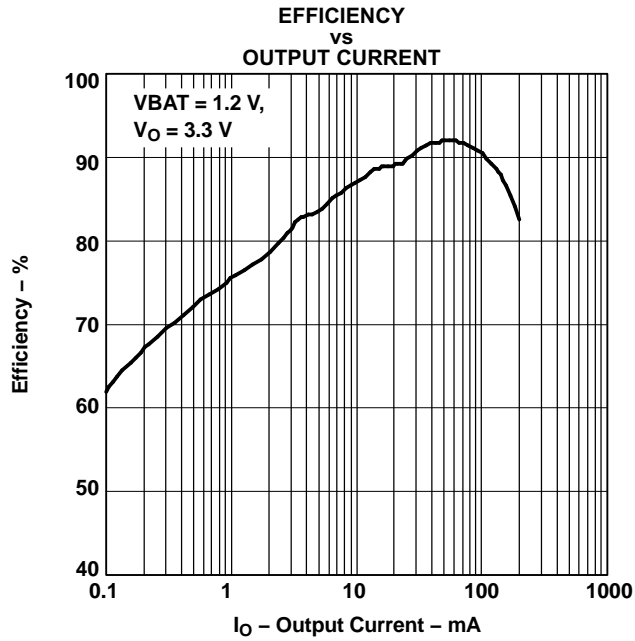


Figure 7.

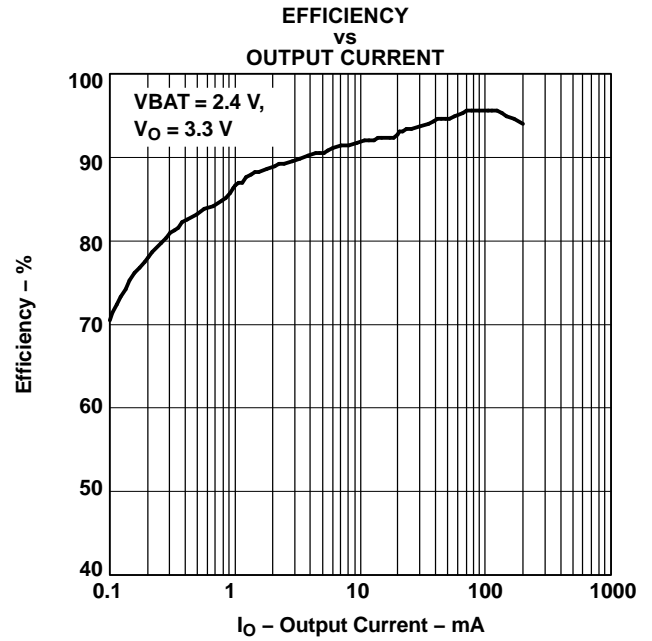


Figure 8.

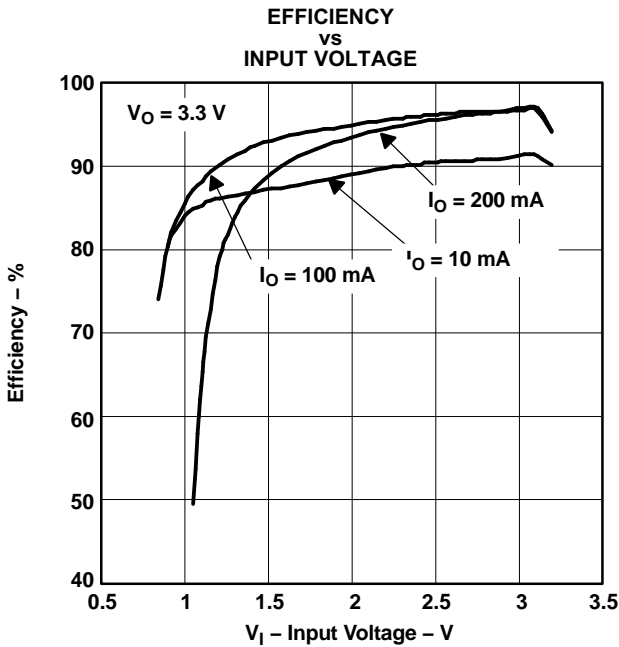
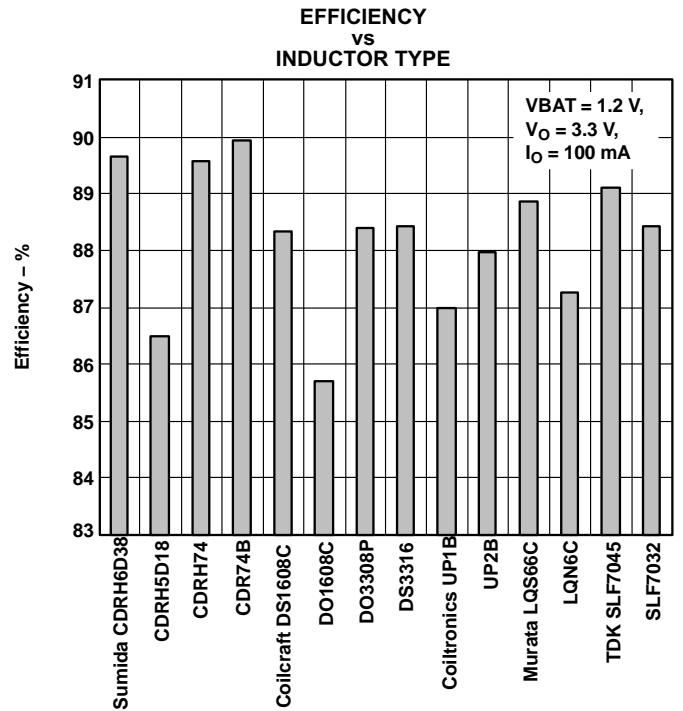


Figure 9.



Inductor Type
Figure 10.

TYPICAL CHARACTERISTICS (continued)

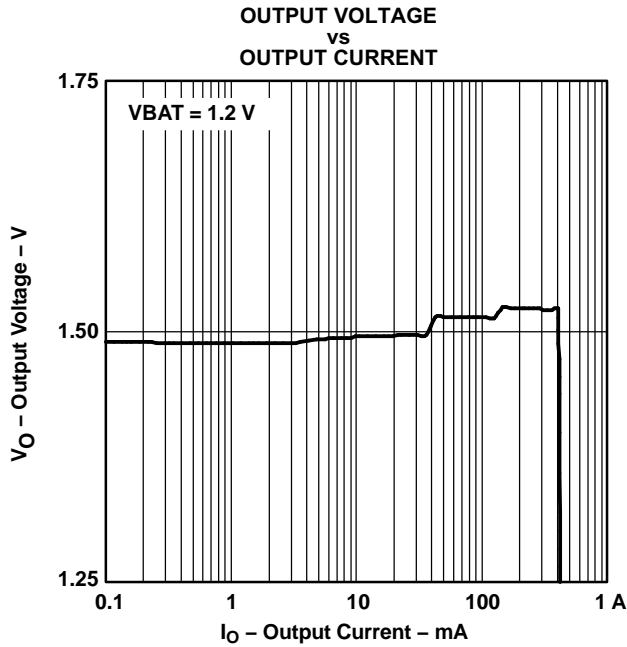


Figure 11.

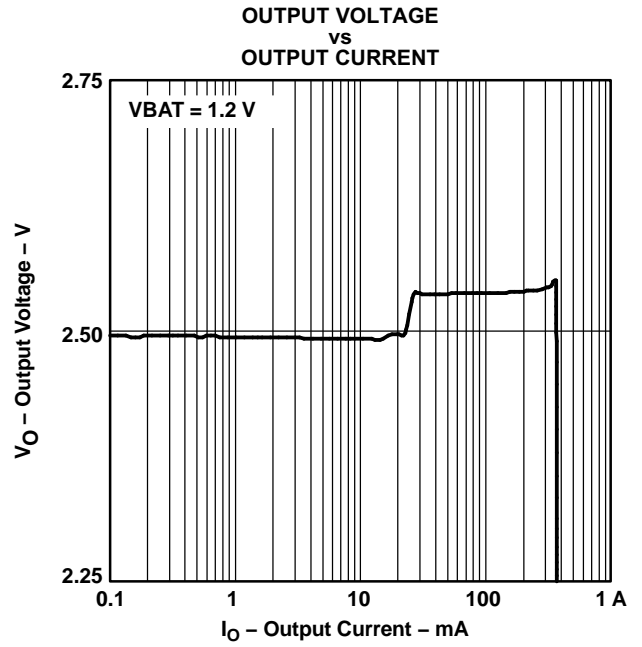


Figure 12.

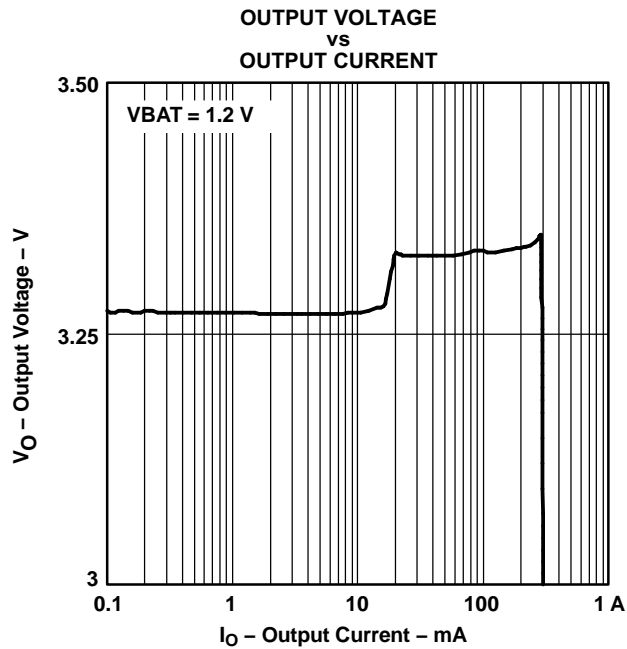


Figure 13.

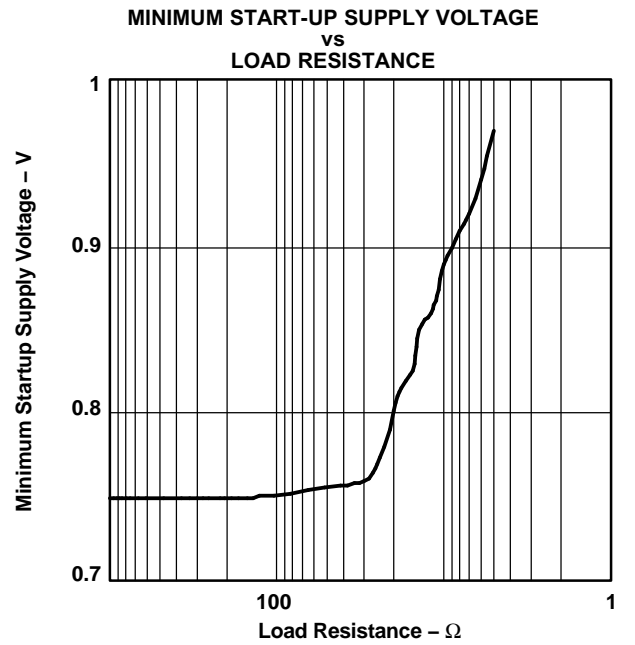


Figure 14.

TYPICAL CHARACTERISTICS (continued)

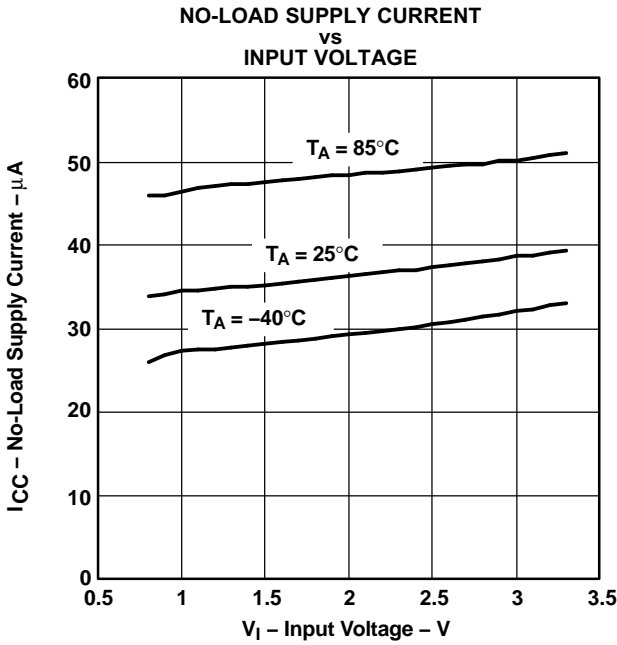


Figure 15.

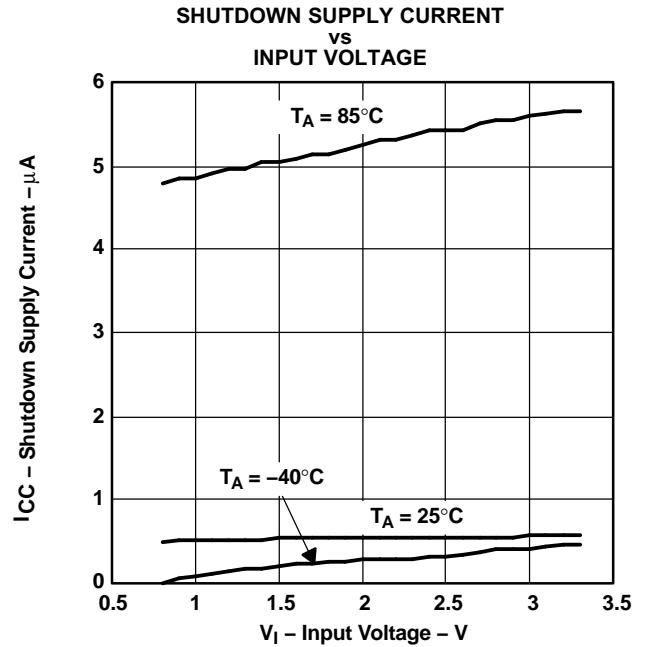


Figure 16.

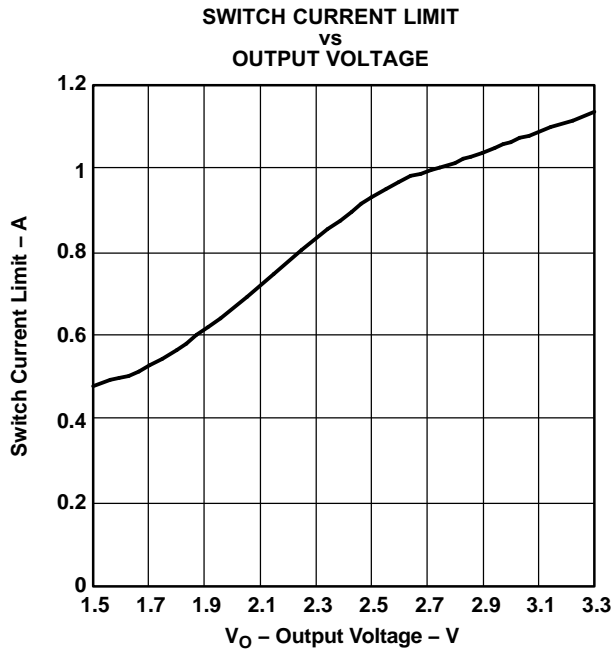


Figure 17.

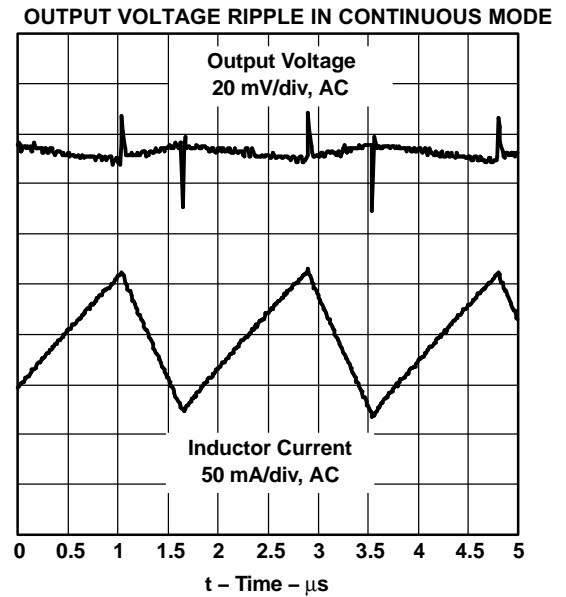


Figure 18.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE RIPPLE IN DISCONTINUOUS MODE

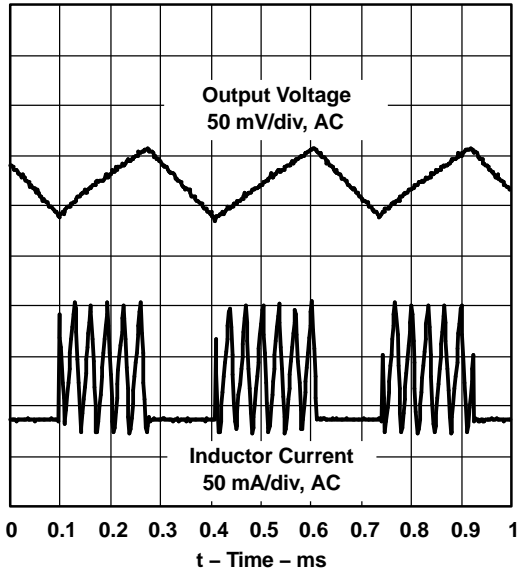


Figure 19.

LOAD TRANSIENT RESPONSE

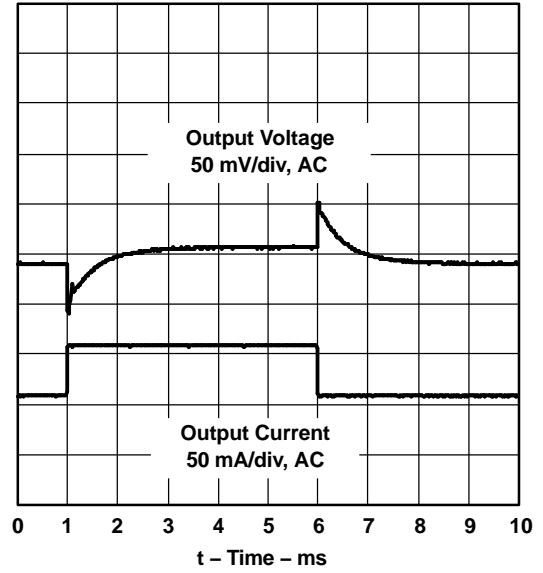


Figure 20.

LINE TRANSIENT RESPONSE

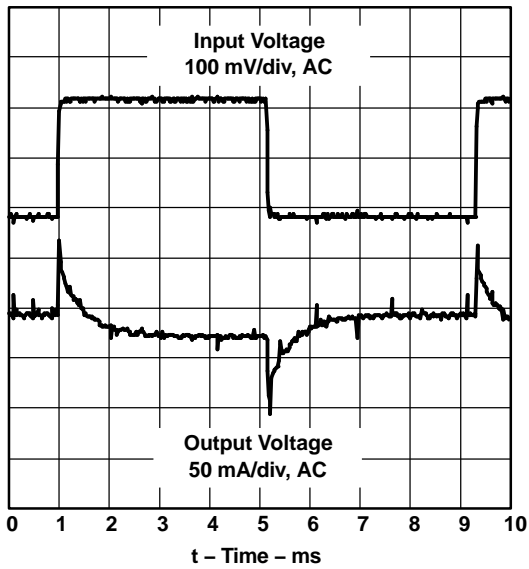


Figure 21.

CONVERTER START-UP TIME AFTER ENABLE

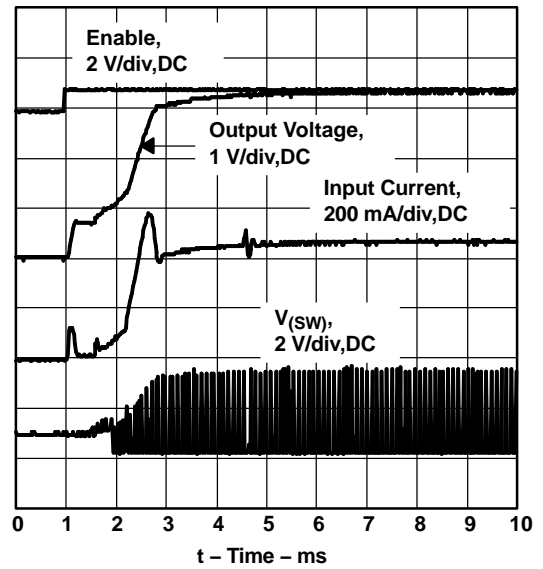


Figure 22.

DESIGN PROCEDURE

The TPS6101x boost converter family is intended for systems that are powered by a single-cell NiCd or NiMH battery with a typical terminal voltage between 0.9 V to 1.6 V. It can also be used in systems that are powered by two-cell NiCd or NiMH batteries with a typical stack voltage between 1.8 V and 3.2 V. Additionally, single- or dual-cell, primary and secondary alkaline battery cells can be the power source in systems where the TPS6101x is used.

Programming the TPS61010 Adjustable Output Voltage Device

The output voltage of the TPS61010 can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV in fixed frequency operation and 485 mV in the power-save operation mode. The maximum allowed value for the output voltage is 3.3 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μ A, and the voltage across R4 is typically 500 mV. Based on those two values, the recommended value for R4 is in the range of 500 k Ω in order to set the divider current at 1 μ A. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using Equation 1.

$$R3 = R4 \times \left(\frac{V_O}{V_{FB}} - 1 \right) = 500 \text{ k}\Omega \times \left(\frac{V_O}{500 \text{ mV}} - 1 \right) \quad (1)$$

If, as an example, an output voltage of 2.5 V is needed, a 2-M Ω resistor should be chosen for R3.

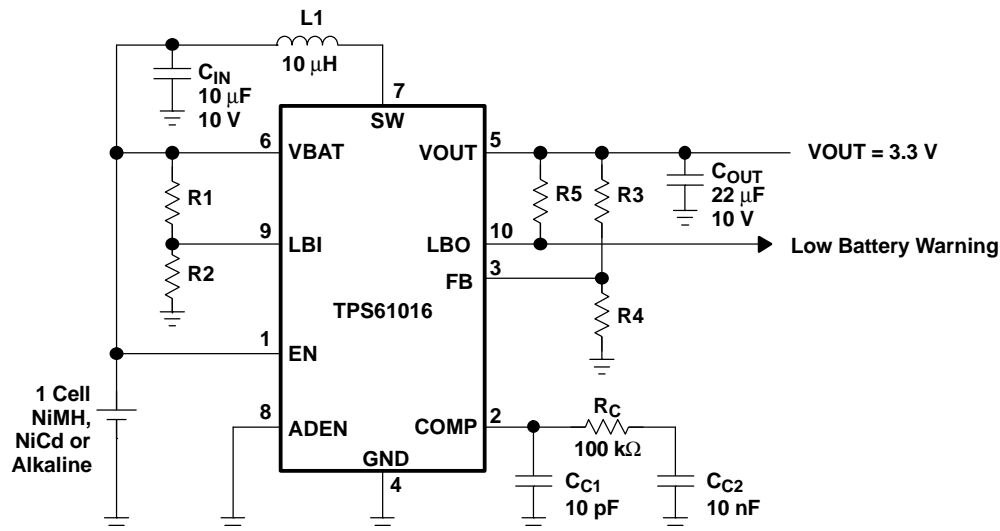


Figure 23. Typical Application Circuit for Adjustable Output Voltage Option

The output voltage of the adjustable output voltage version changes with the output current. Due to device-internal ground shift, which is caused by the high switch current, the internal reference voltage and the voltage on the FB pin increases with increasing output current. Since the output voltage follows the voltage on the FB pin, the output voltage rises as well with a rate of 1 mV per 1-mA output current increase. Additionally, when the converter goes into pulse-skip mode at output currents around 5 mA and lower, the output voltage drops due to the hysteresis of the controller. This hysteresis is about 15 mV, measured on the FB pin.

programming the low battery comparator threshold voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 μ A, the voltage across R2 is equal to the reference voltage that is generated on-chip, which has a value of 500 mV \pm 15 mV. The recommended value for R2 is therefore in the range of 500 k Ω . From that, the value of resistor R1, depending on the desired minimum battery voltage V_{BAT} , can be calculated using Equation 2.

DESIGN PROCEDURE (continued)

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{REF}} - 1 \right) = 500 \text{ k}\Omega \times \left(\frac{V_{BAT}}{500 \text{ mV}} - 1 \right) \quad (2)$$

For example, if the low-battery detection circuit should flag an error condition on the LBO output pin at a battery voltage of 1 V, a resistor in the range of 500 kΩ should be chosen for R1. The output of the low battery comparator is a simple open-drain output that goes active low if the battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ, and should only be pulled up to the V_O. If not used, the LBO pin can be left floating or tied to GND.

inductor selection

A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor is required and a storage capacitor at the output. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS61010's switch is 1100 mA at an output voltage of 3.3 V. The highest peak current through the inductor and the switch depends on the output load, the input (V_{BAT}), and the output voltage (V_O). Estimation of the maximum average inductor current can be done using Equation 3.

$$I_L = I_{OUT} \times \frac{V_O}{V_{BAT} \times 0.8} \quad (3)$$

For example, for an output current of 100 mA at 3.3 V, at least 515-mA of current flows through the inductor at a minimum input voltage of 0.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs.

With those parameters, it is possible to calculate the value for the inductor by using Equation 4.

$$L = \frac{V_{BAT} \times (V_{OUT} - V_{BAT})}{\Delta I_L \times f \times V_{xOUT}} \quad (4)$$

Parameter 7 is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 20% × I_L.

In this example, the desired inductor has the value of 12 μH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care must be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers were tested. All work with the TPS6101x converter within their specified parameters:

Table 1. Recommended Inductors

| VENDOR | RECOMMENDED INDUCTOR SERIES |
|-----------|-----------------------------|
| Sumida | Sumida CDR74B |
| | Sumida CDRH74 |
| | Sumida CDRH5D18 |
| | Sumida CDRH6D38 |
| Coilcraft | Coilcraft DO 1608C |
| | Coilcraft DS 1608C |
| | Coilcraft DS 3316 |
| | Coilcraft DT D03308P |

DESIGN PROCEDURE (continued)

Recommended Inductors (continued)

| VENDOR | RECOMMENDED INDUCTOR SERIES |
|-------------|-----------------------------|
| Coiltronics | Coiltronics UP1B |
| | Coiltronics UP2B |
| Murata | Murata LQS66C |
| | Murata LQN6C |
| TDK | TDK SLF 7045 |
| | TDK SLF 7032 |

capacitor selection

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 5.

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{BAT}})}{f \times \Delta V \times V_{\text{OUT}}} \quad (5)$$

Parameter f is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV, a minimum capacitance of 10 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 6.

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}} \quad (6)$$

An additional ripple of 30 mV is the result of using a tantalum capacitor with a low ESR of 300 m Ω . The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 45 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, like ceramics. For example, a 10- μF ceramic capacitor with an ESR of 50 m Ω is used on the evaluation module (EVM). Tradeoffs must be made between performance and costs of the converter circuit.

A 10- μF input capacitor is recommended to improve transient behavior of the regulator. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel placed close to the IC is recommended.

Compensation of the Control Loop

An R/C/C network must be connected to the COMP pin in order to stabilize the control loop of the converter. Both the pole generated by the inductor L_1 and the zero caused by the ESR and capacitance of the output capacitor must be compensated. The network shown in Figure 5 satisfies these requirements.

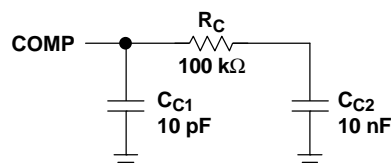


Figure 24. Compensation of Control Loop

Resistor R_C and capacitor C_{C2} depend on the chosen inductance. For a 10- μH inductor, the capacitance of C_{C2} should be chosen to 10 nF, or in other words, if the inductor is **XX** μH , the chosen compensation capacitor should be **XX** nF, the same number value. The value of the compensation resistor is then chosen based on the requirement to have a time constant of 1 ms, for the R/C network R_C and C_{C2} , hence for a 33-nF capacitor, a 33-k Ω resistor should be chosen for R_C .

DESIGN PROCEDURE (continued)

Capacitor C_{C1} depends on the ESR and capacitance value of the output capacitor, and on the value chosen for R_C . Its value is calculated using Equation 7.

$$C_{C1} = \frac{C_{OUT} \times ESR_{COU}}{R_C} \tag{7}$$

For a selected output capacitor of 22 μF with an ESR of 0.2Ω , an R_C of 33 $\text{k}\Omega$, the value of C_{C1} is in the range of 100 pF .

Table 2. Recommended Compensation Components

| INDUCTOR[μH] | OUTPUT CAPACITOR | | RC[k Ω] | CC1[pF] | CC2[nF] |
|---------------------------|------------------------------|-----------------|-----------------|---------|---------|
| | CAPACITANCE[μF] | ESR[Ω] | | | |
| 33 | 22 | 0.2 | 33 | 120 | 33 |
| 22 | 22 | 0.3 | 47 | 150 | 22 |
| 10 | 22 | 0.4 | 100 | 100 | 10 |
| 10 | 10 | 0.1 | 100 | 10 | 10 |

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.

Therefore, use wide and short traces for the main current path as indicated in **bold** in Figure 25. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node as shown in Figure 25 to minimize the effects of ground noise. The compensation circuit and the feedback divider should be placed as close as possible to the IC. To layout the control ground, it is recommended to use short traces as well, separated from the power ground traces. Connect both grounds close to the ground pin of the IC as indicated in the layout diagram in Figure 25. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

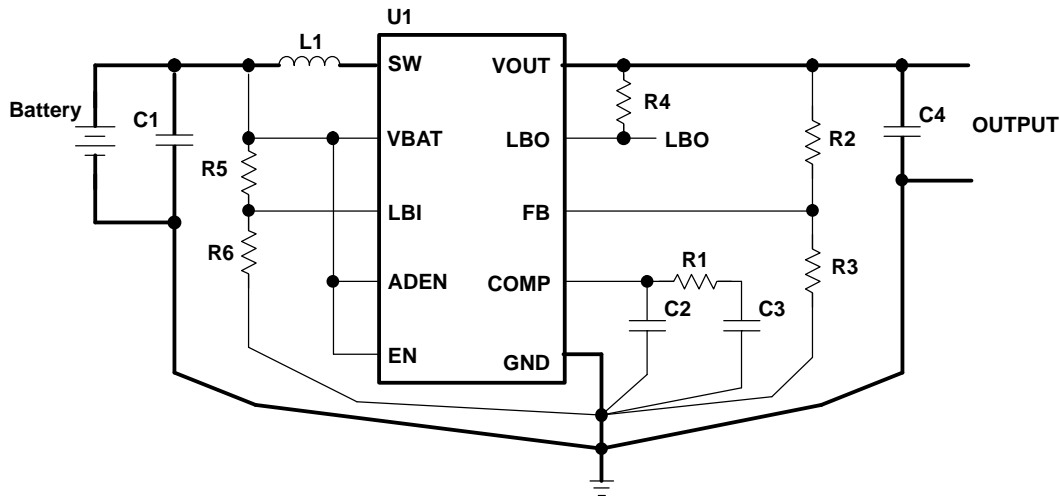


Figure 25. Layout Diagram

APPLICATION INFORMATION

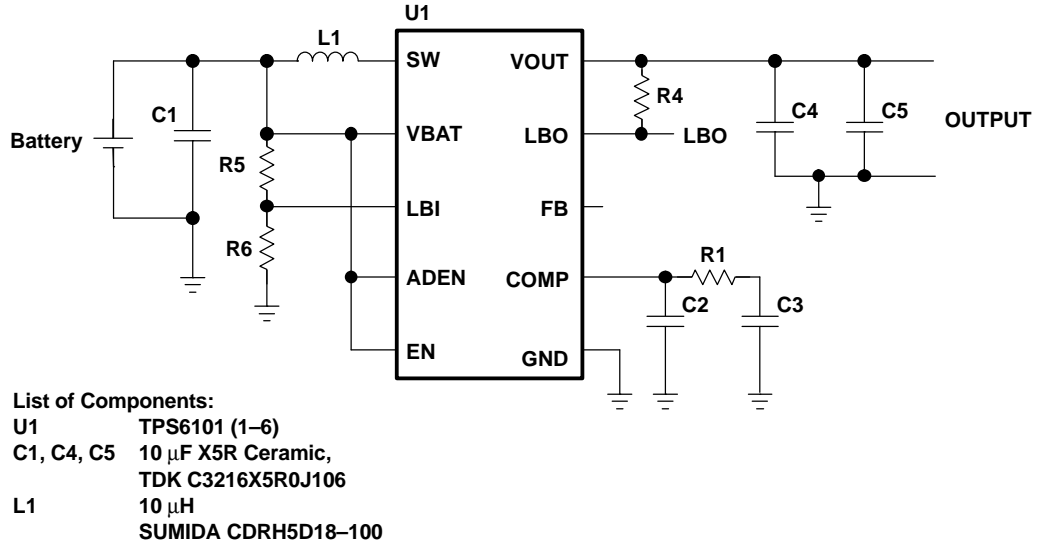


Figure 26. 1,8 mm Maximum Height Power Supply With Single Battery Cell Input Using Low Profile Components

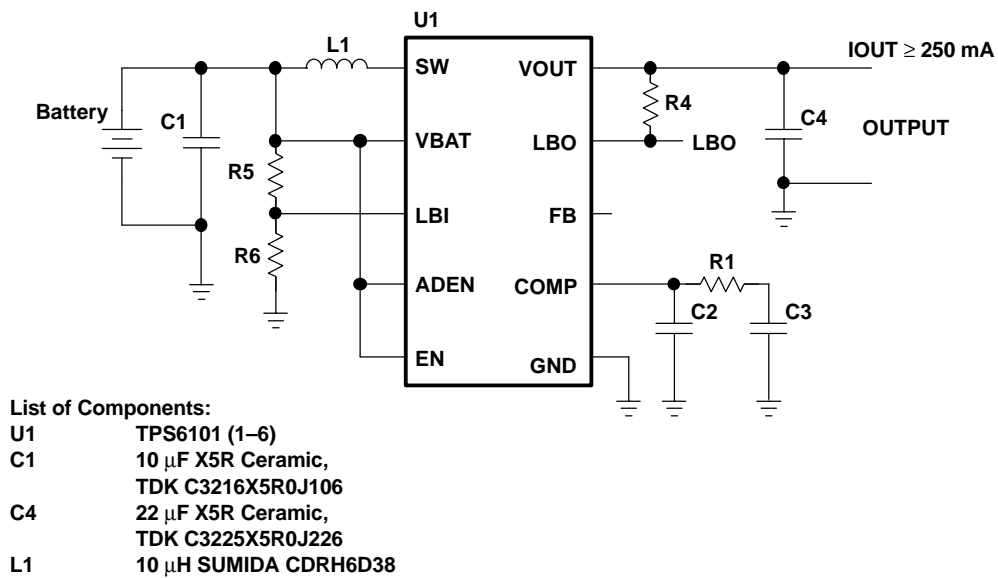
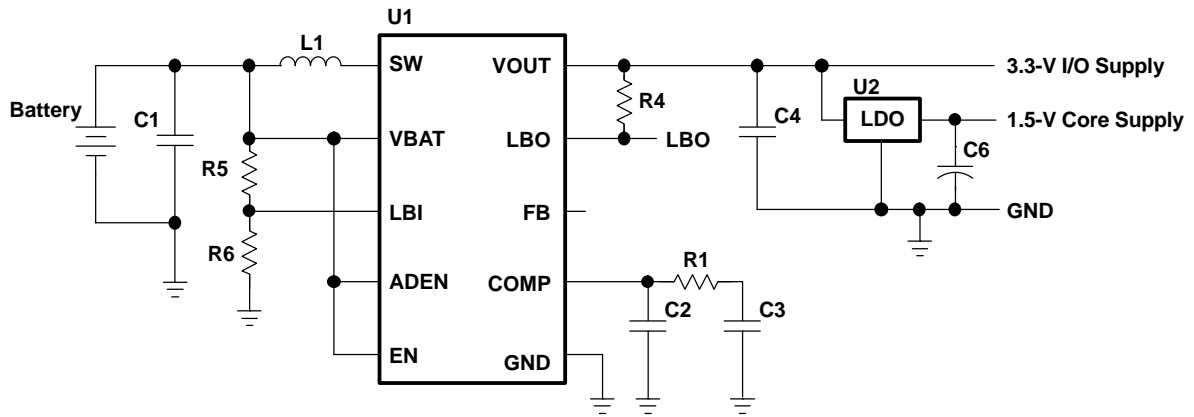


Figure 27. 250-mA Power Supply With Two Battery Cell Input

TPS61010, TPS61011
 TPS61012, TPS61013
 TPS61014, TPS61015, TPS61016

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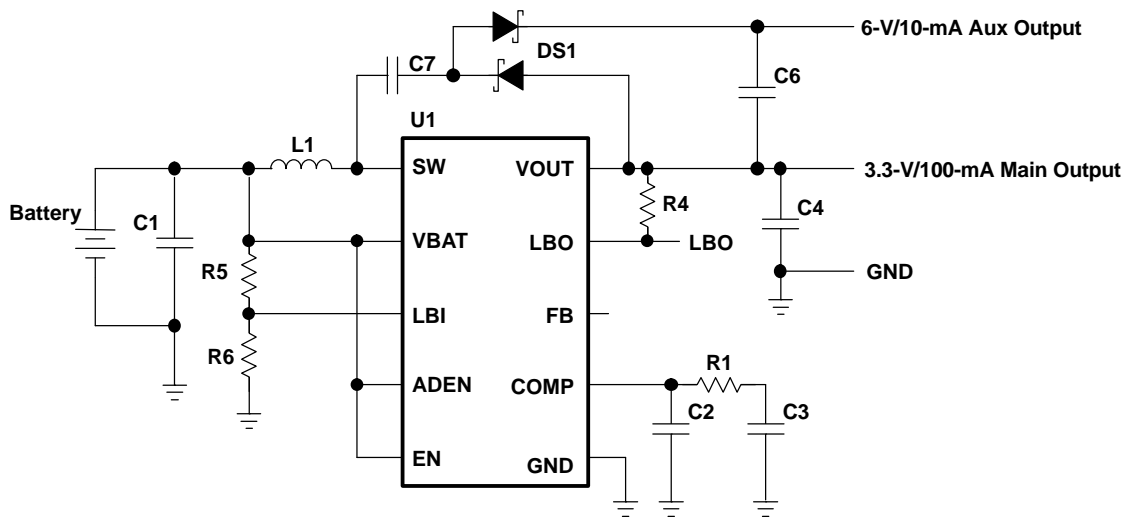
APPLICATION INFORMATION (continued)



List of Components:

- U1 TPS61016
- U2 TPS76915
- C1 10 μ F X5R Ceramic,
TDK C3216X5R0J106
- C4 22 μ F X5R Ceramic,
TDK C3225X5R0J226
- L1 10 μ H SUMIDA CDRH6D38

Figure 28. Dual Output Voltage Power Supply for DSPs

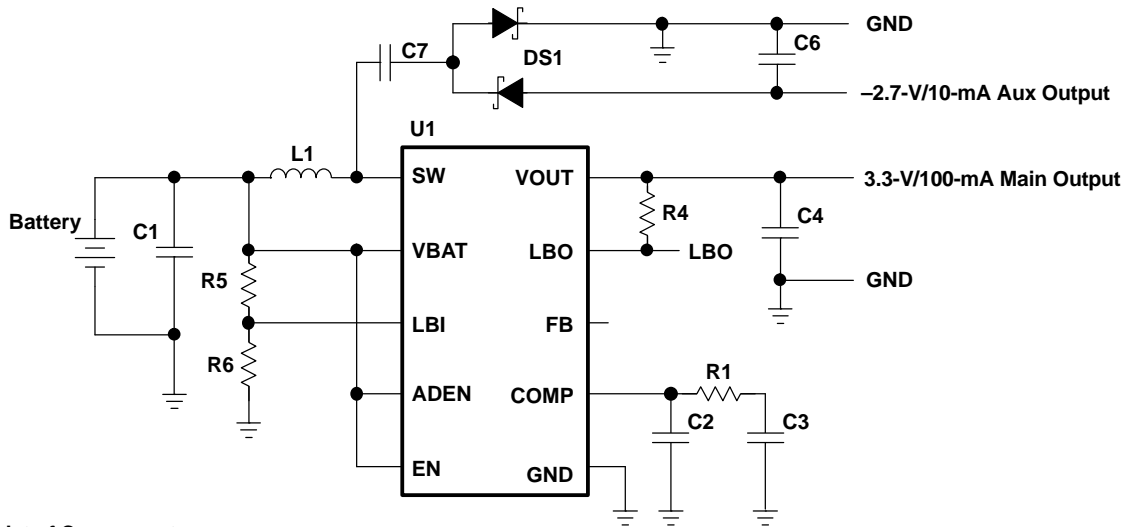


List of Components:

- U1 TPS61016
- DS1 BAT54S
- C1 10 μ F X5R Ceramic,
TDK C3216X5R0J106
- C4 22 μ F X5R Ceramic,
TDK C3225X5R0J226,
- C6 1 μ F X5R Ceramic,
- C7 0.1 μ F X5R Ceramic,
- L1 10 μ H SUMIDA CDRH6D38-100

Figure 29. Power Supply With Auxiliary Positive Output Voltage

APPLICATION INFORMATION (continued)



List of Components:

- U1 TPS61016
- DS1 BAT54S
- C1 10 μ F X5R Ceramic,
TDK C3216X5R0J106
- C4 22 μ F X5R Ceramic,
TDK C3225X5R0J226,
- C6 1 μ F X5R Ceramic,
- C7 0.1 μ F X5R Ceramic,
- L1 10 μ H SUMIDA CDRH6D38-100

Figure 30. Power Supply With Auxiliary Negative Output Voltage

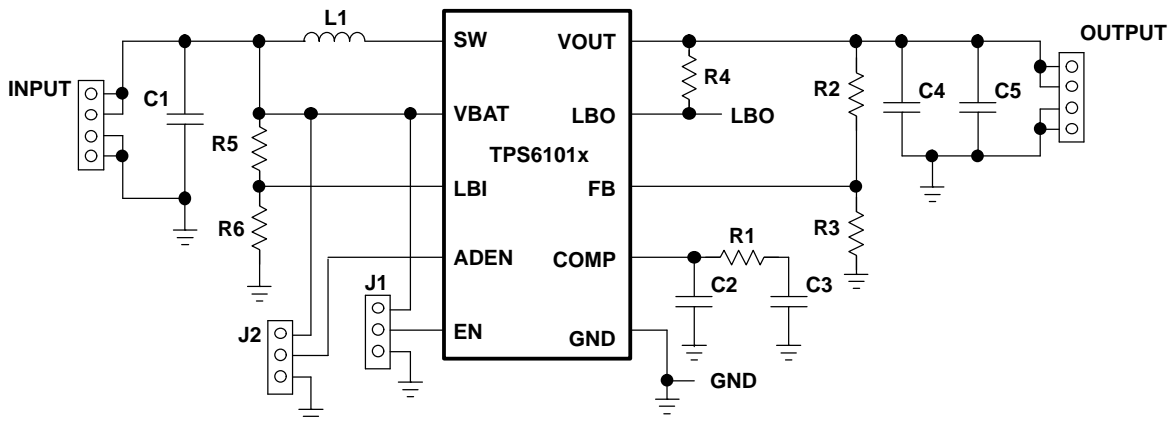


Figure 31. TPS6101x EVM Circuit Diagram

APPLICATION INFORMATION (continued)

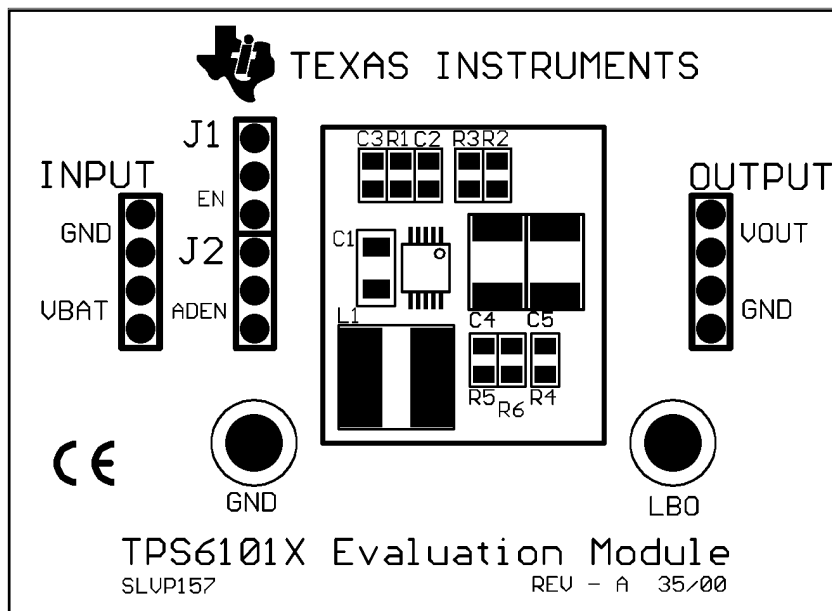


Figure 32. TPS6101x EVM Component Placement (actual size: 55,9 mm x 40,6 mm)

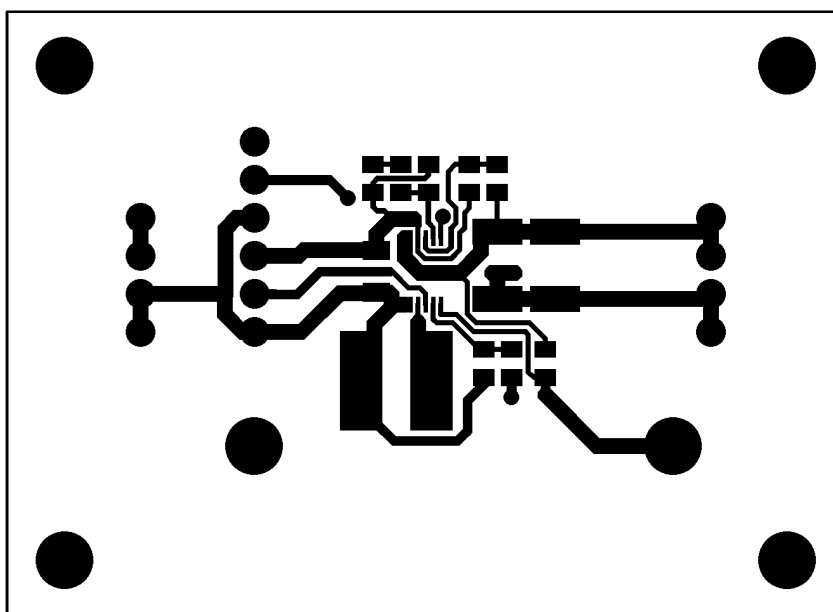
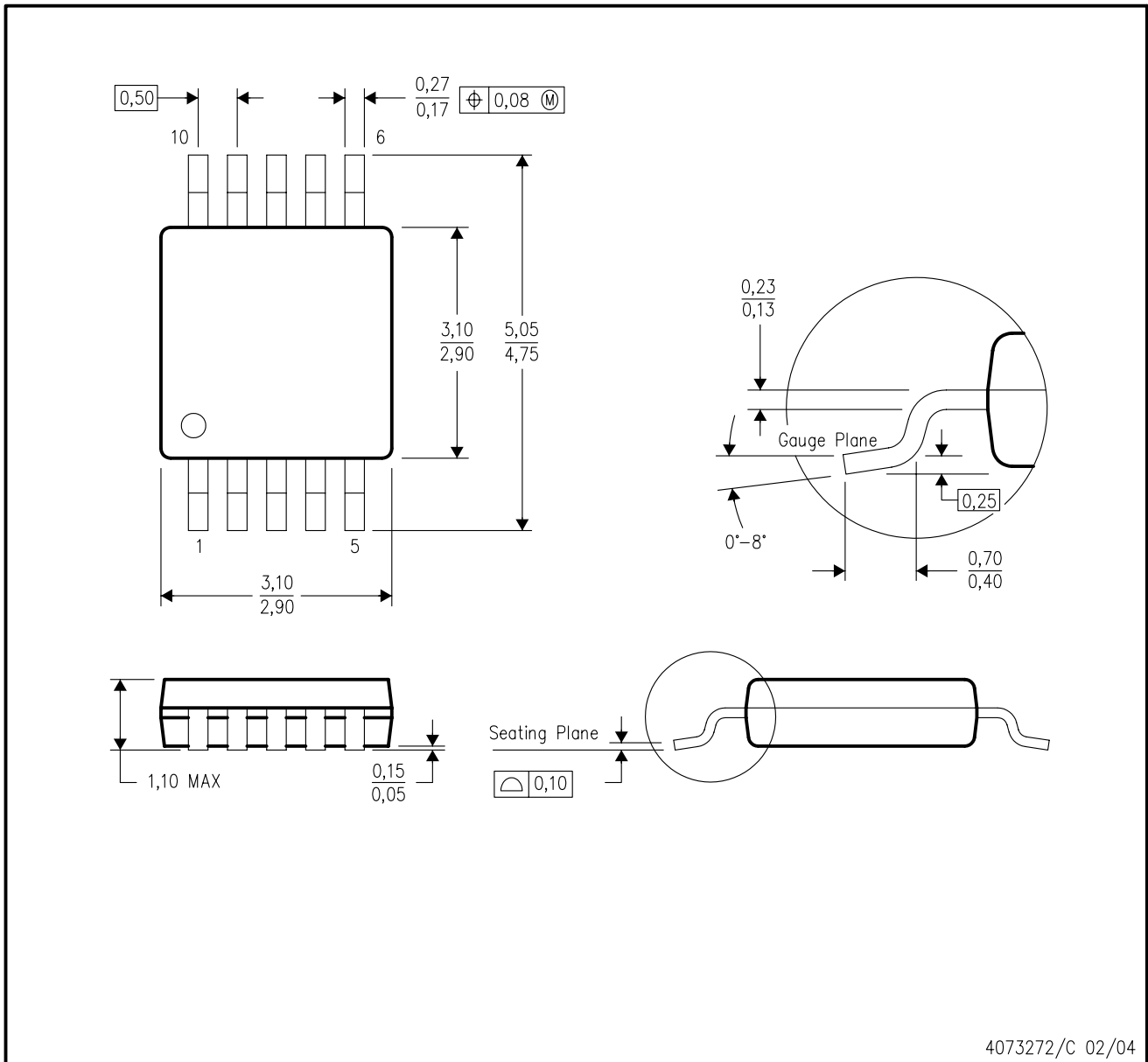


Figure 33. TPS6101x EVM Top Layer Layout (actual size: 55,9 mm x 40,6 mm)

MECHANICAL DATA

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

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