Multi-Standard Fully Integrated 13.56-MHz Radio Frequency Identification (RFID) Analog Front End and Data Framing Reader System

FEATURES

- Completely Integrated Protocol Handling (OSI Model Layer 3 and Below)
- Separate Internal High-PSRR Power Supplies for Analog, Digital, and PA Sections Provides Noise Isolation for Superior Read Range and Reliability
- Dual Receiver Input With AM and PM Demodulation to Minimize Communication Holes (Patent Pending).
- Receiver AM and PM RSSI
- Reader-to-Reader Anti-Collision
- High Integration Reduces Total BOM and Board Area
  - Single External 13.56-MHz Cystal Oscillator
  - MCU-Selectable Clock-Fequency Output of RF, RF/2, or RF/4
  - Adjustable 20-mA, High-PSRR LDO for Powering External MCU
- Easy to Use With High Flexibility
  - Auto-Configured Default Modes for Each Spported ISO Protocol
  - 11 User-Programmable Registers
  - Selectable Receiver Gain and AGC
  - Programmable Output Power (100 mW or 200 mW)
  - Adjustable ASK Modulation Range (8% to 30%)
  - Built-In Receiver Band-Pass Filter With User-Selectable Corner Frequencies
- Wide Operating Voltage Range of 2.7 V to 5.5 V
- Ultralow-Power Modes
  - Power Down < 1 μA
  - Standby 120 μA
  - Active (Rx only) 10 mA
- Parallel 8-Bit or Serial 4-Pin SPI Interface With MCU Using 12-Byte FIFO
- Ultrasmall 32-Pin QFN Package (5 mm × 5 mm)
- Available tools
  - Reference Design/EVM With Development Software
  - Source Code Available for MSP430

APPLICATIONS

- Secure Access Control
- Product Authentication
  - Printer Ink Cartridges
  - Blood Gucose Monitors
- Contactless Payment Systems

DESCRIPTION

The TRF7960/61 is an integrated analog front end and data framing system for a 13.56-MHz RFID reader system. Built-in programming options make it suitable for a wide range of applications both in proximity and vicinity RFID systems.

The reader is configured by selecting the desired protocol in the control registers. Direct access to all control registers allows fine tuning of various reader parameters as needed.

Table 1. PRODUCT SELECTION TABLE

DEVICE	PROTOCOLS					
	ISO14443A/B				ISO15693 ISO18000-3	Tag-it™
	106 kbps	212 kbps	424 kbps	848 kbps		
TRF7960	X	X	X	X	X	X
TRF7961					X	X

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

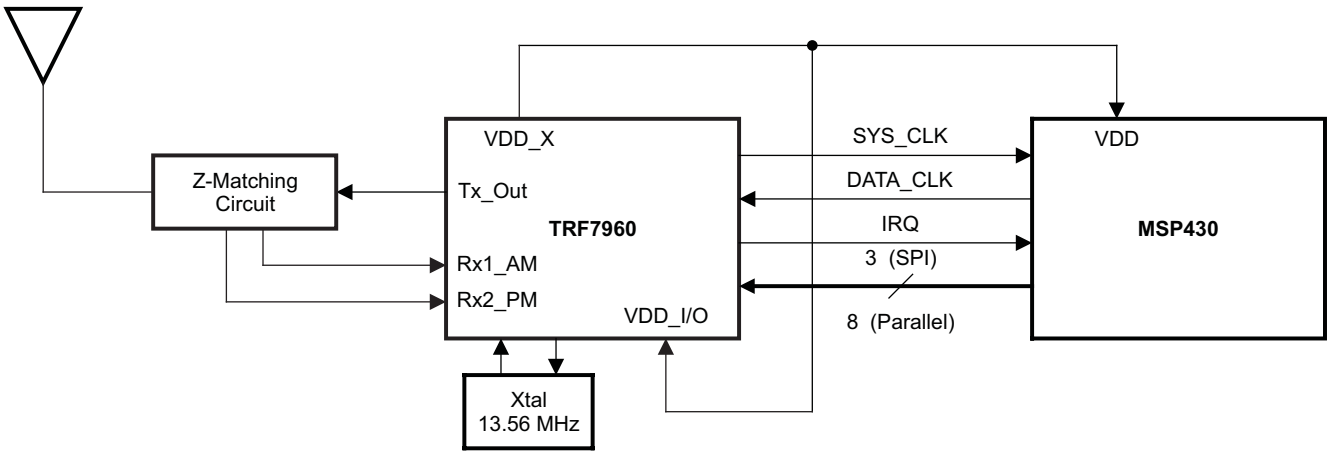


Figure 1. Typical Application

A parallel or serial interface can be used for communication between the MCU and reader. When hardware encoders and decoders are used (accelerators for different standards), transmission and receive functions use a 12-byte FIFO register. For direct transmit or receive functions, the encoders/decoders can be bypassed in order for the MCU to process the data in real time. The transmitter has selectable output-power levels of 100 mW (20 dBm) or 200 mW (23 dBm) into a 50-Ω load (at 5 -V supply) and is capable of ASK or OOK modulation. Integrated voltage regulators ensure power-supply noise rejection for the complete reader system.

Data transmission comprises low-level encoding for ISO15693, modified Miller for ISO14443-A, high-bit-rate systems, Tag-it, and HF-EPC system coding. Included with the data encoding is automatic generation of SOF, EOF, CRC, and/or parity bits.

The receiver system enables AM and PM demodulation using a dual-input architecture. The receiver also includes an automatic gain control option and selectable gain. Also included is a selectable bandwidth to cover a broad range of input subcarrier signal options. The received signal strength for AM and PM modulation is accessible via the RSSI register. The receiver output is selectable between a digitized subcarrier signal and any of eleven integrated subcarrier decoders (two for ISO15693 low bit rate, two for ISO15693 high bit rate, two for ISO14443, three for ISO14443 high bit rates, one for Tag-it, and one for HF-EPC system). Selected decoders also deliver bit stream and a data clock as outputs.

The receiver system also includes a framing system. This system performs the CRC and/or parity check, removes the EOF and SOF settings, and organizes the data in bytes. Framed data is then accessible to the MCU via a 12-byte FIFO register and MCU interface. The framing supports ISO14443 and ISO15693 protocols.

The TRF7960/61 supports data communication levels between 1.8 V–5.5 V for the MCU I/O interface while also providing a data synchronization clock. An auxiliary 20-mA regulator (pin 32) is available for additional system circuits.

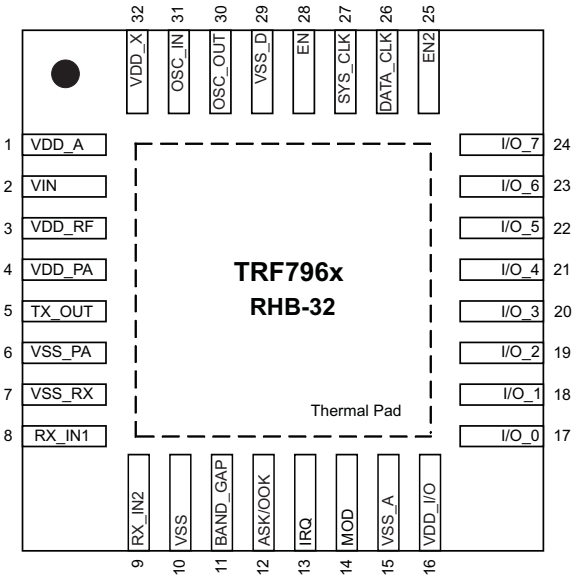


Figure 2. TRF796x Pin Assignments (Top View)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
VIN	Supply voltage		6	V
I_O	Output current		150	mA
	Continuous power dissipation		See Dissipation Rating Table	
T_J	Maximum junction temperature, any condition(2)		140	°C
	Maximum junction temperature, continuous operation, long-term reliability(2)		125	°C
T_{stg}	Storage temperature range		–55 to 150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
	ESDS rating	HBM (human body model)	2	kV
		CDM (charged device model)	500	V
		MM (machine model)	200	

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified are not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

TABLE 5. PACKAGING/ORDERING INFORMATION(1)

PACKAGED DEVICES	PACKAGE TYPE	TRANSPORT MEDIA	QUANTITY
TRF7960RHBT	RHB-32	Tape and reel	250
TRF7960RHBR		Tape and reel	3000
TRF7961RHBT	RHB-32	Tape and reel	250
TRF7961RHBR		Tape and reel	3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

DISSIPATION RATINGS TABLE PER PACKAGE

PACKAGE	θ_{JC} (°C/W)	θ_{JA}(1) (°C/W)	POWER RATING(2)	
			$T_A \leq 25°C$	$T_A = 85°C$
RHB (32)	31	36.4	2.7 W	1.1 W

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
VIN	Supply voltage	2.7	5	5.5	V
T_J	Operating virtual junction temperature range	–40		125	°C
T_A	Operating ambient temperature range	–40	25	110	°C
	Load impedance at TX OUT (pin 5)		10		Ω

PACKAGE OPTION ADDENDUM

4-Apr-2007

PACKAGING INFORMATION

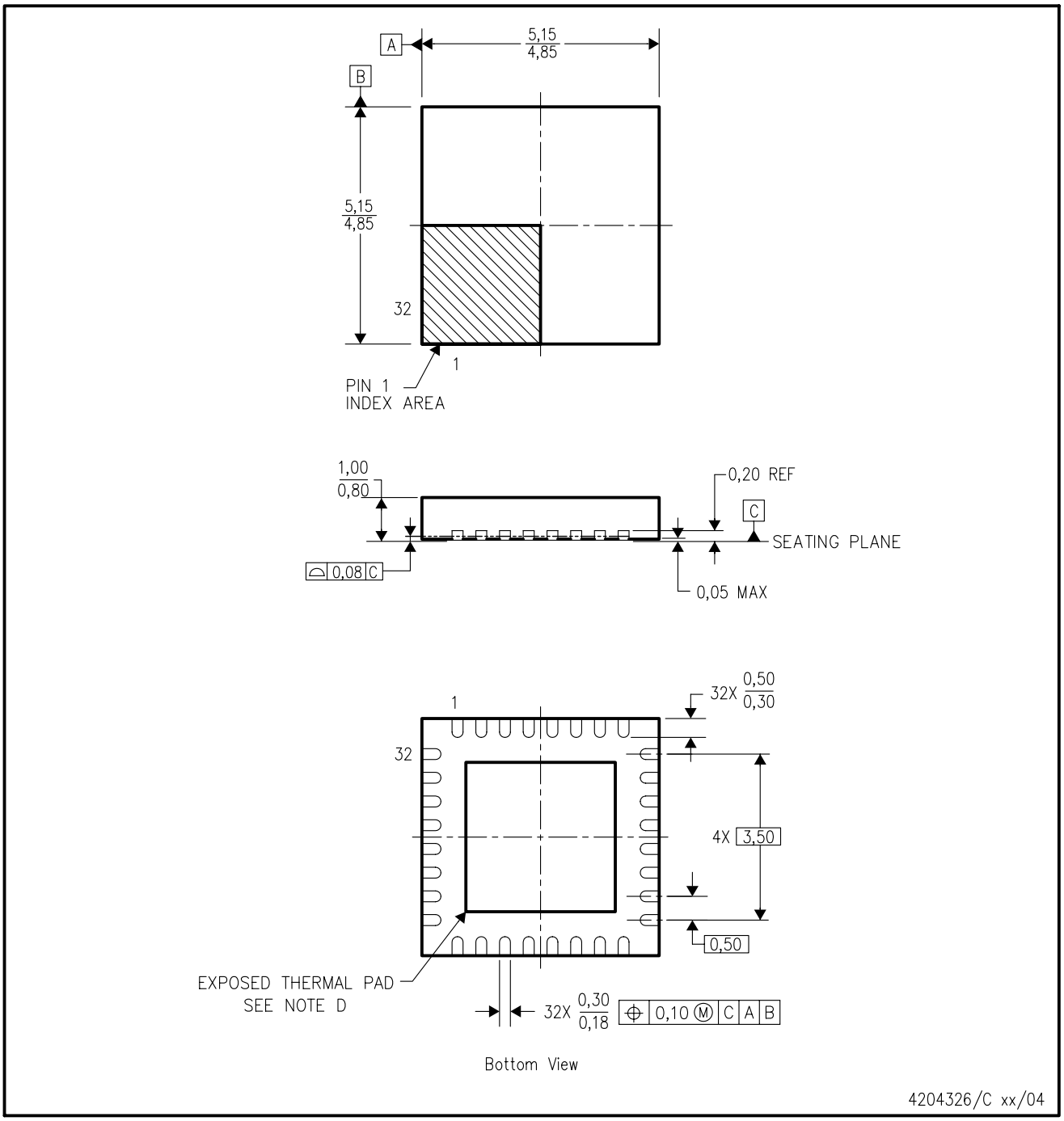
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TRF7960RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7960RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7961RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TRF7961RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

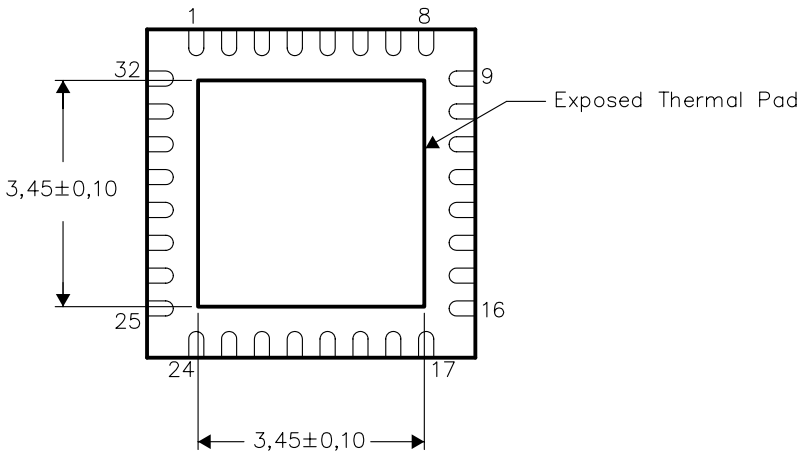
RHB (S–PQFP–N32)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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