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TSB43EA/EB/EC42
TSB43EA/EB/EC43
IEEE Std 1394a-2000
Consumer Electronics Solution
Data Sheet Extract
Rev 1.1

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1 Revision History

Version	Date	Notes
1.0 - Released	April 2008	Initial release
1.1 - Released	July 2008	Modification on operating ambient temperature range(section 4.4)

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2 Overview

The TSB43Ex42/43 is high-performance consumer electronics 1394 link layer and integrated physical layer device designed for digitally interfacing advanced video consumer electronics applications. It supports formatting and transmission of IEC61883 data, including IEC61883-1 (general), IEC61883-2 (SD-DVCR), IEC61883-4 (MPEG2-TS), and IEC61883-7 (ITU-R BO.1294 SystemB-DSS). TSB43Ex42/43 also supports standard 1394 data types, such as asynchronous, asynchronous streams, and PHY packets.

The TSB43EAxx/ECxx version incorporates DTCP (M6) baseline per the DTLA (5C) specification to support transmit and receive of up to two MPEG2 transport streams with encryption and decryption. The TSB43EAxx/ECxx version also includes hardware acceleration for content key generation.

The TSB43EBxx devices are identical to the TSB43EAxx/ECxx devices, except without implementation of the encryption/decryption features. The TSB43EB42xx/43xx devices allow customers that do not require the encryption/decryption features to incorporate the TSB43Ex42/43 function without becoming DTLA licensees.

The TSB43Ex42/43 features an integrated 2-port/3-port PHY. The PHY operates at 100 Mbps, 200 Mbps, or 400 Mbps. They follow all requirements as stated in IEEE Std 1394-1995 and IEEE Std 1394a-2000.

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3 Features

3.1 *1394 Features*

- Integrated 400/200/100-Mbps 2-port/3-port PHY
- Compliant with IEEE Std 1394-1995 and IEEE Std 1394a-2000
- Supports bus manager functions and automatic 1394 self-id verification
- Separate asynchronous acknowledgement (Ack) buffers decrease Ack-tracking burden on external CPU

3.2 *DTCP and AES Encryption Support for MPEG-DVB and DSS (TSB43EA42/43 and TSB43EC42/43 Only)*

- DTCP encryption support on 1394 bus
- AES128 encryption support on HSDI path (TSB43EC42/43 only)
- Support for up to two encrypted/decrypted streams at one time
- Full or restricted AKE performed with hardware assist
- Secure method for loading DTCP and AES128 information using Ex-CPU interface
- Localization support compliant with DTCP draft revision 1.51.

3.3 *Video Interfaces*

- Two configurable high-speed data ports for video data
  - o One port configurable as parallel or serial
  - o One port serial only
- Pass-through modes for HSDI0 and HSDI1
- Packet Insertion – Two insertion buffers per HSDI for PAT, PMT, SIT, and DIT packets
- PID filtering (32 PID filters per HSDI port)

3.4 *External CPU Interfaces*

- Motorola 68K-style 16-bit asynchronous interface
- SRAM-like 16-bit asynchronous interface
- PCI interface (33 MHz) compliant to PCI specification version 3.0 (supports PCI slave and master functions)

3.5 *DMA*

- Higher asynchronous throughput with DMA hardware enhancements (available in PCI mode only)
- Internal DMA controller – Asynchronous, asynchronous Stream TX/RX
  - o General DMA
  - o Auto-response DMA for SBP2 transactions

3.6 *Data Buffers*

- Two 4-KByte isochronous buffers for video data
- Two 2-KByte asynchronous/asynchronous stream transmit buffers
- Two 2-KByte asynchronous/asynchronous stream receive buffers
- One 1-KByte self-ID buffer
- Insertion buffers for MPEG-DVB/DSS packet insertion
- Programmable data/space available indicators for buffer flow control

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3.7 *Hardware Packet Formatting for the Following Standards*

- IEC61883-1 (general)
- IEC61883-2 (SD-DVCR)
- IEC61883-4 (MPEG2-TS)
- IEC61883-7 (ITU-R BO.1294 System B) – DSS
- Generic 61883 mode
- Asynchronous packets
- Asynchronous streams
- PHY packets (including self-IDs)
- MPEG4 supported under IEC61883-4 (no new requirement for MPEG4 over 1394)

3.8 *Additional Features*

- JTAG interface to support post-assembly scan of device I/O – boundary scan
- Unique “binding” method for protecting sensitive data on the circuit board traces at the Ex-CPU interface
- Unique “EMI-AES Binding” method to prevent protected data from being transmitted in the clear.

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4 General Information

4.1 *Disclaimer*

Any operations not described by this data sheet are undefined. TI is not responsible for the results if the user operates TSB43Ex42/43 in a manner not described by this document.

4.2 *Package Size/Ordering information*

Only the devices in the green rows are available for order. Other devices are previews and are scheduled to be released.

Ordering Number	Availability	Number of PHY Ports	5C/Non-5C	Voltage	Package	Package Type
TSB43EA42	**Available**	**2**	**5C only**	**3.3 V/1.5 V**	**MicroStar BGA™ 144**	**ZGU**
TSB43EB42	Preview	2	Non-5C	**3.3 V/1.5 V**	**MicroStar BGA144**	**ZGU**
TSB43EC42	Preview	2	5C + AES	**3.3 V/1.5 V**	**MicroStar BGA 144**	**ZGU**
TSB43EB43	Preview	3	Non-5C	**3.3 V/1.5 V**	**MicroStar BGA 144**	**ZGU**
TSB43EA43	Preview	3	5C only	**3.3 V/1.5 V**	**MicroStar BGA 144**	**ZGU**
TSB43EC43	Preview	3	5C + AES	**3.3 V/1.5 V**	**MicroStar BGA 144**	**ZGU**

4.3 *Operating Voltage*

		MIN	MAX	UNIT
Nominal voltage	1.5 V	1.35	1.65	V
	3.3 V	3	3.6	V

Note: I/Os are not 5-V tolerant (including PCI interface)

4.4 *Operating Temperature*

		MIN	NOM	MAX	UNIT
Operating ambient temperature	**Commercial**	0		70	°C
	Industrial (To be released)	-40		85	°C
Storage temperature		-65		150	°C

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5 Application Diagram

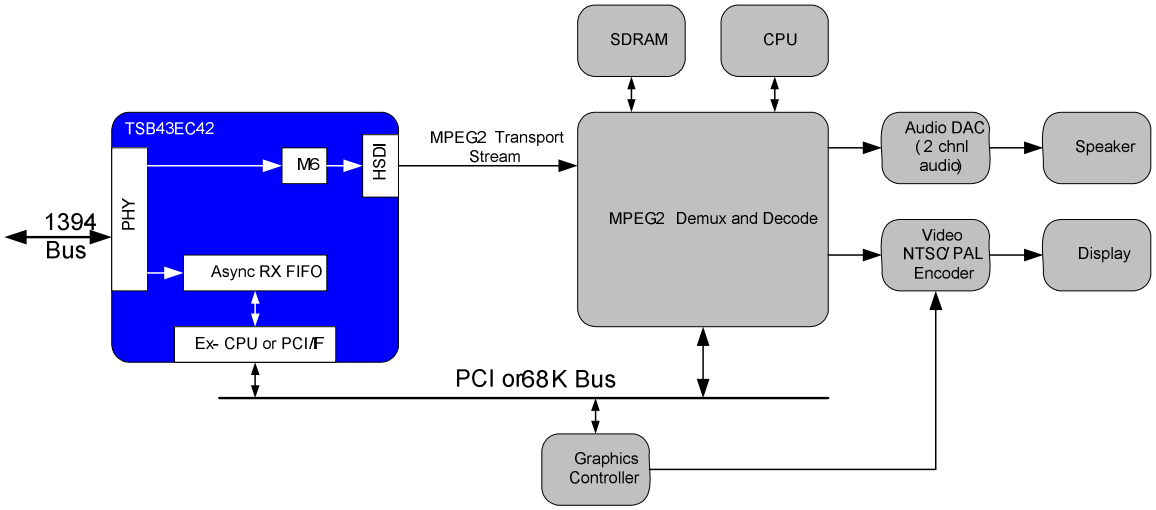

Figure 1. TSB43EC42 in HDTV Application

In the HDTV application, the TSB43EC42/43 receives the MPEG2 transport stream, decrypts it using the M6 cipher, and outputs it to the application over the HSDI port AES encrypted. The MPEG2 demultiplex and decode device separates the audio and video streams, decodes them, and outputs the 2-channel audio to an audio DAC for listening and the video to an NTSC/PAL encoder for display.

The HDTV receives on-screen display (OSD) information from the video source, such as a set top box, using the EIA775 standard. The system processor receives the OSD data through the TSB43EC42/43 asynchronous receive buffer. The system graphics controller controls the OSD and mixes it with the video data for display.

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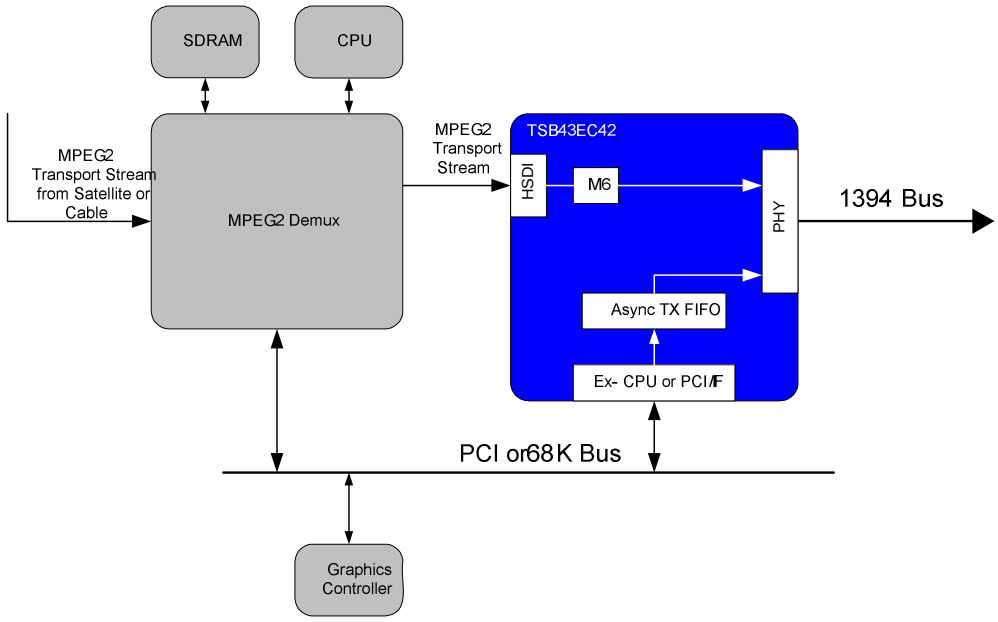

Figure 2. TSB43EC2/43 in STB Application

The set top box receives the MPEG2 transport stream from either satellite or cable sources. The MPEG2 transport stream is input to the TSB43EC42/43 HSDI port in AES encrypted format. The TSB43EC42/43 decrypts the packets received over the HSDI port, performs any PID filtering or packet insertion, encrypt the stream using M6 cipher, and transmit the stream over 1394.

The set top box also creates on-screen display (OSD) graphics to transmit to the sink device. The system inputs the OSD data to the TSB43Ex42/43 asynchronous transmit buffer. The TSB43EC42/43 transmits the OSD using asynchronous packets to the sink device.

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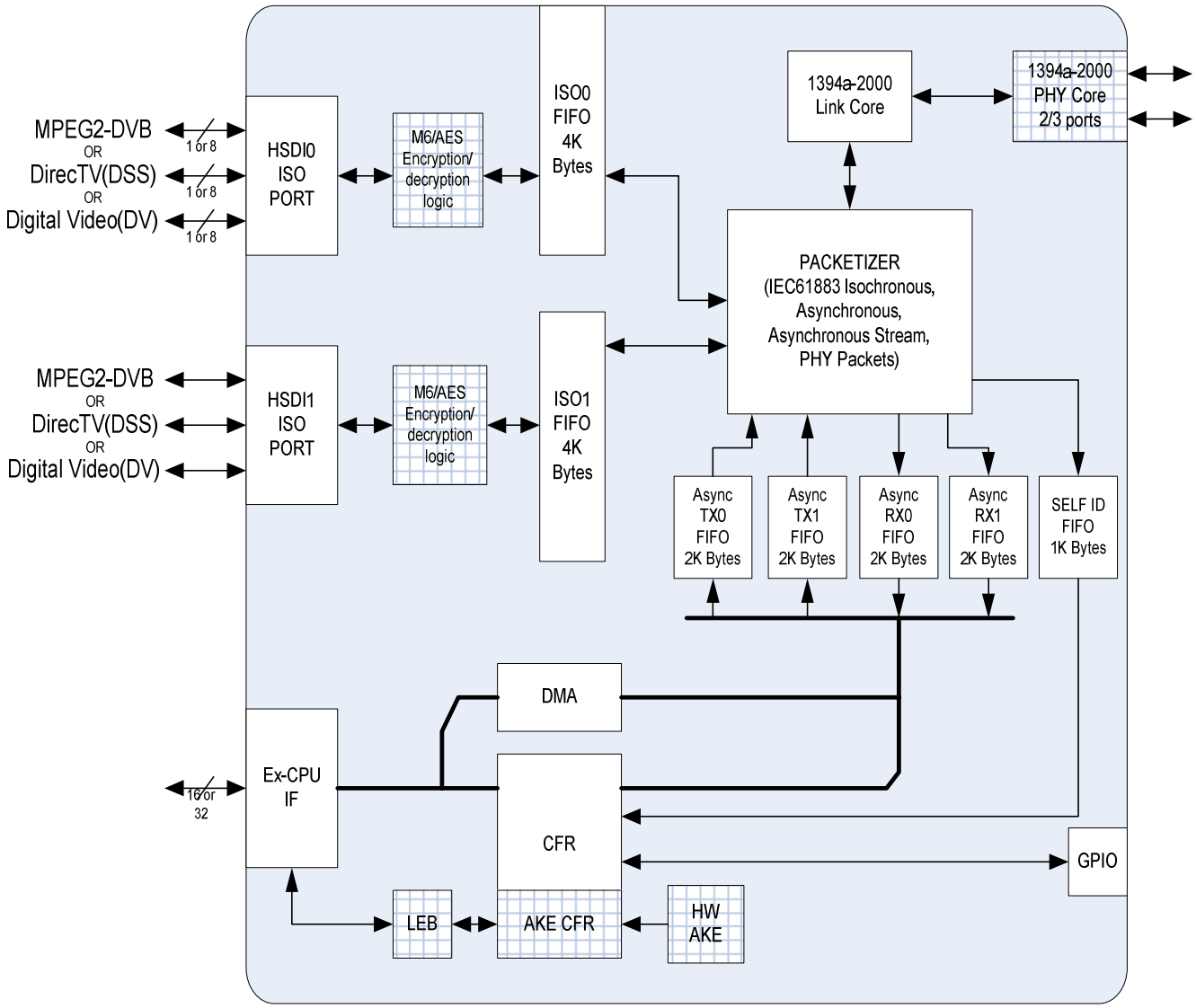
6 Block Diagram



Note: Blocks with the checked and shaded pattern are available only in selected versions of the device.

Figure 3. TSB43EA/EB/EC42, TSB43EA/EB/EC43 Block Diagram

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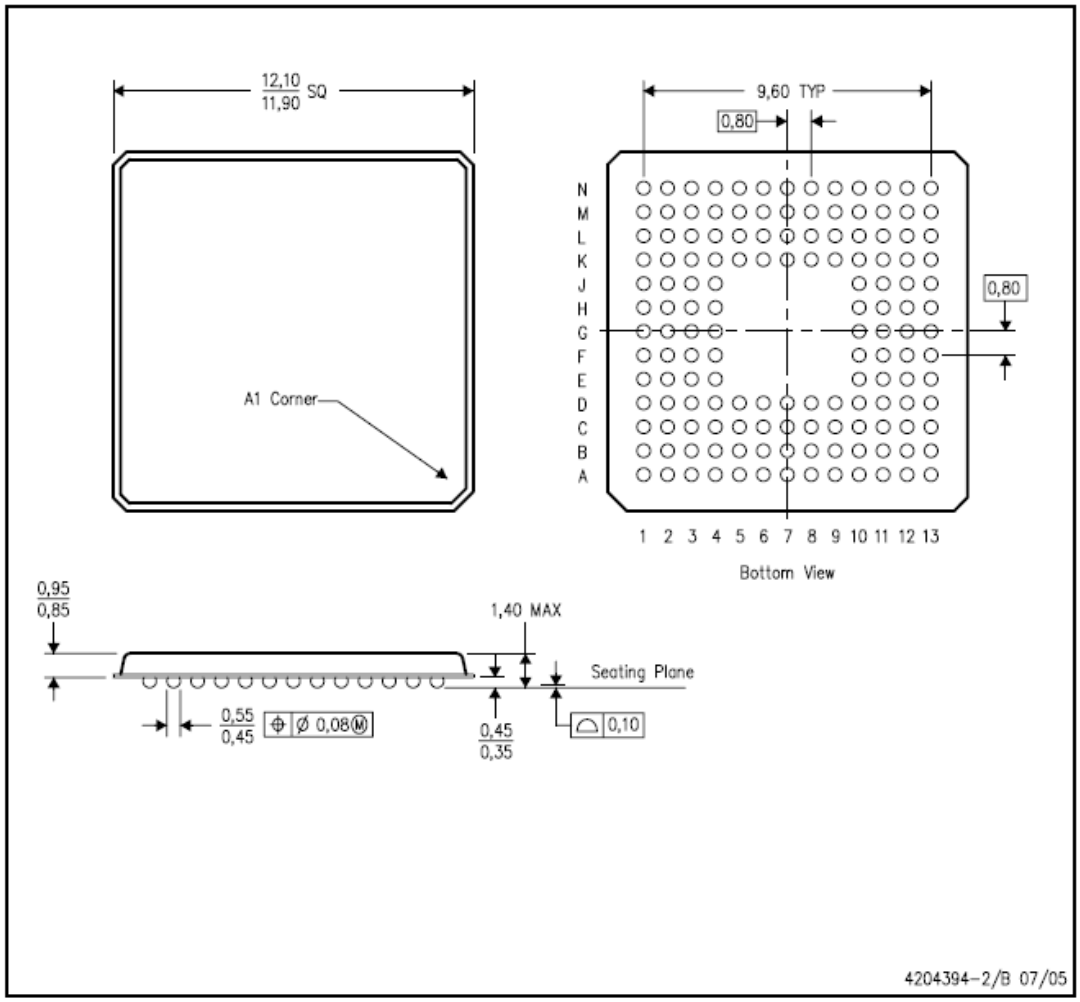
7 Mechanical Data

7.1 *MicroStar ™ BGA Package Information*

MECHANICAL DATA

ZGU (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration
D. This is a lead–free solder ball design.

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PACKAGE OPTION ADDENDUM

21-Oct-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSB43EA42ZGU	ACTIVE	BGA	ZGU	144	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TSB43EC42ZGU	ACTIVE	BGA	ZGU	144	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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