1.6V to 3.6V, 12-Bit, Nanopower, 4-Wire TOUCH SCREEN CONTROLLER with SPI™ Interface

FEATURES

- 4-Wire Touch Screen Interface
- Ratiometric Conversion
- Single 1.6V to 3.6V Supply
- Preprocessing to Reduce Bus Activity
- High-Speed SPI-Compatible Interface
- Internal Detection of Screen Touch
- Register-Based Programmable:
  - 10-Bit or 12-Bit Resolution
  - Sampling Rates
  - System Timing
- On-Chip Temperature Measurement
- Touch Pressure Measurement
- Auto Power-Down Control
- Low Power:
  - 800μW at 1.8V, 50SSPS
  - 600μW at 1.6V, 50SSPS
- Enhanced ESD Protection:
  - ±6kV HBM
  - ±1kV CDM
  - Target ±18kV Air Gap Discharge
  - Target ±15kV Contact Discharge
- 2.5 x 3 WCSP-18 Package

U.S. Patent NO. 6246394; other patents pending.

APPLICATIONS

- Personal Digital Assistants
- Cellular Phones
- Portable Instruments
- Point-of-Sale Terminals
- MP3 Players, Pagers
- Multiscreen Touch Control

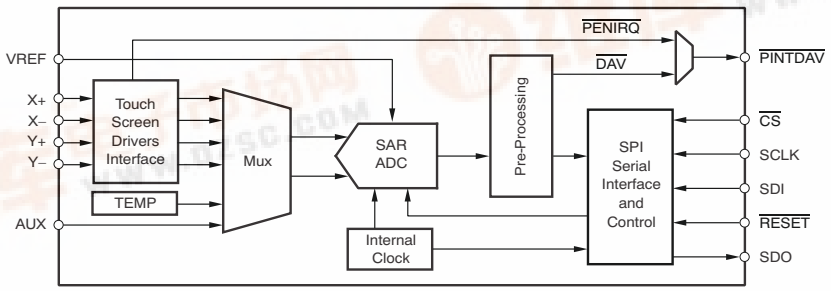
DESCRIPTION

The TSC2005 is a very low-power touch screen controller designed to work with power-sensitive, handheld applications that are based on an advanced low-voltage processor. It works with a supply voltage as low as 1.6V, which can be supplied by a single-cell battery. It contains a complete, ultra-low power, 12-bit, analog-to-digital (A/D) resistive touch screen converter, including drivers and the control logic to measure touch pressure.

In addition to these standard features, the TSC2005 offers preprocessing of the touch screen measurements to reduce bus loading, thus reducing the consumption of host processor resources that can then be redirected to more critical functions.

The TSC2005 supports an SPI-compatible serial bus up to 25MHz. It offers programmable resolution of 10 or 12 bits to accommodate different screen sizes and performance needs.

The TSC2005 is available in a miniature 18-lead, 5 x 6 array, 2.5 x 3 mm^2 wafer chip-scale package (WCSP). The device is characterized for the –40°C to +85°C industrial temperature range.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	TYPICAL INTEGRAL LINEARITY (LSB)	TYPICAL GAIN ERROR (LSB)	NO MISSING CODES RESOLUTION (BITS)	PACKAGE TYPE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TSC2005	±1.5	– 0.2/+4.4	11	18-Pin, 5 x 6 Matrix, 2.5 x 3 WCSP	YZL	–40°C to +85°C	TSC2005I	TSC2005IYZLT	Small Tape and Reel, 250
								TSC2005IYZLR	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

			TSC2005	UNIT
Voltage range	Analog input X+, Y+, AUX to SNSGND		–0.4 to SNSVDD + 0.1	V
	Analog inputX–, Y– to SNSGND		–0.4 to SNSVDD + 0.1	V
	SNSVDD to SNSGND		–0.3 to 5	V
	SNSVDD to AGND		–0.3 to 5	V
	I/OVDD to DGND		–0.3 to 5	V
	SNSVDD to I/OVDD		–2.40 to +0.3	V
Digital input voltage to DGND			–0.3 to I/OVDD + 0.3	V
Digital output voltage to DGND			–0.3 to I/OVDD + 0.3	V
Power dissipation	WCSP package		$(T_J$ Max - $T_A)/\theta_{JA}$	
Thermal impedance, θ_{JA}	WCSP package	Low-K	113	°C/W
		High-K	62	
Operating free-air temperature range, T_A			–40 to +85	°C
Storage temperature range, T_{STG}			–65 to +150	°C
Junction temperature, T_J Max			+150	°C
Lead temperature	Vapor phase (60 sec)		+215	°C
	Infrared (15 sec)		+220	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, SNSVDD = V_{REF} = +1.6V to +3.6V, I/OVDD = +1.2V to +3.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TSC2005 MIN	TSC2005 TYP	TSC2005 MAX	UNIT
AUXILIARY ANALOG INPUT						
Input voltage range			0		VREF	V
Input capacitance				12		pF
Input leakage current			–1		+1	µA
A/D CONVERTER						
Resolution		Programmable: 10 or 12 bits			12	Bits
No missing codes		12-bit resolution	11			Bits
Integral linearity				±1.5		LSB(1)
Offset error		SNSVDD = 1.6V, V_{REF} = 1.6V		–0.8 to +0.3		LSB
		SNSVDD = 3.0V, V_{REF} = 2.5V		+3.2 to +8.9		LSB
Gain error		SNSVDD = 1.6V, V_{REF} = 1.6V		–0.2 to 0		LSB
		SNSVDD = 3.0V, V_{REF} = 2.5V		+3.8 to +4.4		LSB
REFERENCE INPUT						
V_{REF} range			1.6		SNSVDD	V
VREF input current drain		Non-cont. AUX mode, SNSVDD = 3V, V_{REF} = 2.5V, T_A = +25°C, f_{ADC} = 2MHz, f_{SCLK} = 10MHz		5.6		µA
Input impedance		A/D converter not converting		1		GΩ
TOUCH SENSORS						
$\overline{PENIRQ}$ Pull-Up Resistor, R_{IRQ}		T_A = +25°C, SNSVDD = 3V, V_{REF} = 2.5V		51		kΩ
Switch On-Resistance	Y+, X+			6		Ω
	Y–, X–			5		Ω
Switch drivers drive current(2)		100ms duration			50	mA
TEMPERATURE MEASUREMENT						
Temperature range			–40		+85	°C
Resolution		Differential method(3), SNSVDD = 3V V_{REF} = 2.5V		1.6		°C/LSB
		TEMP1(4), SNSVDD = 3V V_{REF} = 2.5V		0.3		°C/LSB
Accuracy		Differential method(3), SNSVDD = 3V V_{REF} = 2.5V		±2		°C/LSB
		TEMP1(4), SNSVDD = 3V V_{REF} = 2.5V		±3		°C/LSB
INTERNAL OSCILLATOR						
Clock frequency, f_{OSC}		SNSVDD = 1.6V		3.6		MHz
		SNSVDD = 3.0V		3.8		MHz
Frequency drift		SNSVDD = 1.6V		0.0056		%/°C
		SNSVDD = 3.0V		0.012		%/°C
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
Logic level	V_{IH}	1.2V ≤ I/OVDD ≤ 1.6V	0.7 × I/OVDD		I/OVDD + 0.3	V
		1.6V ≤ I/OVDD ≤ 3.6V	2.0		I/OVDD + 0.3	V
	V_{IL}	1.2V ≤ I/OVDD ≤ 1.6V	–0.3		0.2 × I/OVDD	V
		1.6V ≤ I/OVDD ≤ 3.6V	–0.3		0.3 × I/OVDD	V
	I_{IL}	SCLK pin or $\overline{CS}$ pin	–1		1	µA
	C_{IN}				10	pF
	V_{OH}	I_{OH} = 2 TTL loads	I/OVDD – 0.2		I/OVDD	V
	V_{OL}	I_{OL} = 2 TTL loads	0		0.2	V
	I_{LEAK}	Floating output	–1		1	µA
	C_{OUT}	Floating output			10	pF
Data format				Straight Binary		

(1) LSB means Least Significant Bit. With V_{REF} = +2.5V, one LSB is 610µV.
(2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation.
(3) Difference between TEMP1 and TEMP2 measurement; no calibration necessary.
(4) Temperature drift is –2.1mV/°C.

ELECTRICAL CHARACTERISTICS (continued)

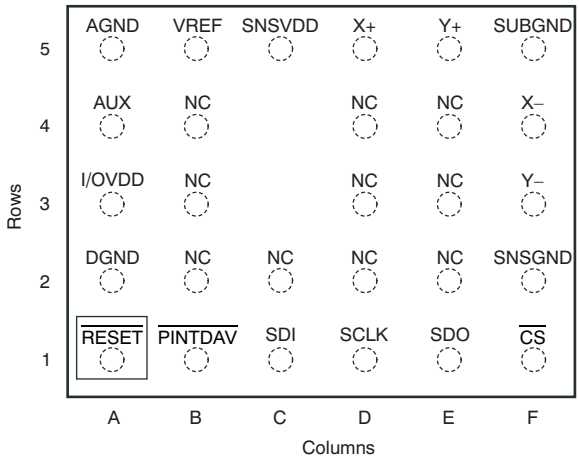
At T_A = –40°C to +85°C, SNSVDD = V_{REF} = +1.6V to +3.6V, I/OVDD = +1.2V to +3.6V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TSC2005			UNIT
		MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage					
SNSVDD(5)	Specified performance	1.6		3.6	V
I/OVDD(6)		1.2		SNSVDD	V
Quiescent supply current(7)	With filter, M = 15, W = 7, PSM = 1, C[3:0] = (0,0,0,0), RM = 1, CL[1:0] = (0,1), M[1:0] = (1,1), W[1:0] = (1,0), MAVEX = 1, MAVEY = 1, MAVEZ = 1, SNSVDD = 1.6V, I/OVDD = 1.6V, f_{ADC} = 2MHz, f_{SCLK} = 10MHz		383		µA
	Bypass filter, M = W = 1, PSM = 1, C[3:0] = (0,0,0,0), RM = 1, CL[1:0] = (0,1), M[1:0] = (0,0), W[1:0] = (0,0), MAVEX = 1, MAVEY = 1, MAVEZ = 1, SNSVDD = 1.6V, I/OVDD = 1.6V, f_{ADC} = 2MHz, f_{SCLK} = 10MHz		361		µA
	Non-cont. AUX mode SNSVDD = 1.6V, I/OVDD = 1.6V, f_{ADC} = 2MHz, f_{SCLK} = 10MHz		481		µA
	Non-cont. AUX mode SNSVDD = 3.0V, I/OVDD = 1.6V, f_{ADC} = 2MHz, f_{SCLK} = 10MHz		943		µA
Power down supply current	$\overline{CS}$ high, SCLK = 0		0	0.8	µA

(5) TSC2005 functions down to 1.4V, typically.
(6) I/OVDD must be ≤ SNSVDD.
(7) Supply current from SNSVDD.

PIN CONFIGURATION

YZL PACKAGE
WCSP-18
(TOP VIEW, SOLDER BUMPS ON BOTTOM SIDE)



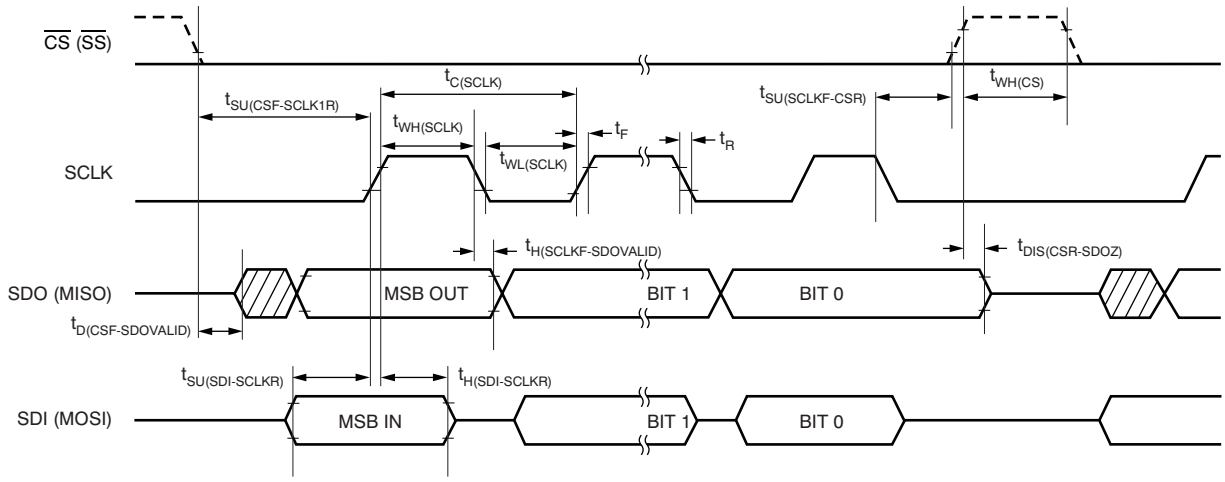
(FRONT VIEW)

PIN ASSIGNMENTS

PIN		I/O	A/D	DESCRIPTION
NO.	NAME			
A1	$\overline{\text{RESET}}$	I	D	System reset. All register values reset to default value.
A2	DGND			Digital ground
A3	I/OVDD			Digital I/O interface voltage
A4	AUX	I	A	Auxiliary channel input
A5	AGND			Analog ground
B1	$\overline{\text{PINTDAV}}$	O	D	Interrupt output. Data available or $\overline{\text{PENIRQ}}$ depends on setting. Pin polarity with active low.
B2, B3, B4, C2, D2, E2, E3, E4	NC			No connection.
B5	VREF	I	A	External reference input
C1	SDI	I	D	Serial data input. This input is the MOSI signal for the SPI interface protocol.
C3, C4, D3, D4	NC			No connection. Sensitive area; avoid trace beneath. Some bumps on the WCSP may be depopulated.
C5	SNSVDD			Power supply for sensor drivers and other analog blocks.
D1	SCLK	I	D	Serial clock input
D5	X+	I	A	X+ channel input
E1	SDO	O	D	Serial data output. This output is the MISO for the SPI interface protocol.
E5	Y+	I	A	Y+ channel input
F1	$\overline{\text{CS}}$	I	D	Chip select. This input is the slave select ($\overline{\text{SS}}$) signal for the SPI interface protocol.
F2	SNSGND			Sensor driver return
F3	Y–	I	A	Y– channel input
F4	X–	I	A	X– channel input
F5	SUBGND			Substrate ground (for ESD current)

TIMING INFORMATION

The TSC2005 supports SPI programming in mode CPOL = 0 and CPHA = 0. The falling edge of SCLK is used to change output (MISO) data and the rising edge is used to latch input (MOSI) data. Eight SCLKs are required to complete the Byte 1 command cycle, and 24 SCLKs are required for the Byte 0 command cycle. $\overline{CS}$ can stay low during the entire 24 SCLKs of a Byte 0 command cycle, or multiple mixed cycles of reading and writing of bytes and register accesses, as long as the corresponding addresses are supplied.



NOTE: CPOL = 0, CPHA = 0, Byte 0 cycle requires 24 SCLKs, and Byte 1 cycle requires 8 SCLKs.

Figure 1. Detailed I/O Timing

TIMING REQUIREMENTS(1)

All specifications typical at –40°C to +85°C, SNSVDD = I/OVDD = 1.6V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{WL(RESET)}$	Reset low time	I/OVDD = SNSVDD ≥ 1.6V(2)	10		µs
$t_{C(SCLK)}$	SPI serial clock cycle time	I/OVDD ≥ 1.6V and < 2.7V, 40% to 60% duty cycle	60		ns
		I/OVDD ≥ 2.7V and ≤ 3.6V, 40% to 60% duty cycle	40		ns
f_{SCLK}	SPI serial clock frequency	I/OVDD ≥ 1.6V and < 2.7V, 10pF load		10	MHz
		I/OVDD ≥ 2.7V and ≤ 3.6V, 10pF load		25	MHz
$t_{WH(SCLK)}$	SPI serial clock high time		0.4 × $t_{C(SCLK)}$	0.6 × $t_{C(SCLK)}$	ns
$t_{WL(SCLK)}$	SPI serial clock low time		0.4 × $t_{C(SCLK)}$	0.6 × $t_{C(SCLK)}$	ns
$t_{SU(CSF-SCLK1R)}$	Enable lead time		30		ns
$t_{D(CSF-SDOVALID)}$	Slave access time			15	ns
$t_{H(SCLKF-SDOVALID)}$	MOSI data hold time		6		ns
$t_{D(SCLKF-SDOVALID)}$	MISO data valid			13	ns
$t_{WH(CS)}$	Sequential transfer delay		15		ns
$t_{SU(SDI-SCLKR)}$	MOSI data setup time		6		ns
$t_{H(SDI-SCLKR)}$	MISO data hold time		4		ns
$t_{DIS(CSR-SDOZ)}$	Slave MISO disable time			15	ns
$t_{SU(SCLKF-CSR)}$	Enable lag time		30		ns
t_R	Rise time	SNSVDD = I/OVDD = 3V, f_{SCLK} = 25MHz		4	ns
t_F	Fall time	SNSVDD = I/OVDD = 3V, f_{SCLK} = 25MHz		4	ns

(1) All input signals are specified with t_R = t_F = 5ns (10% to 90% of I/OVDD) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) Refer to Figure 30.

TYPICAL CHARACTERISTICS

At T_A = –40°C to +85°C, SNSVDD = V_{REF} = +1.6V to +3.6V, I/OVDD = +1.2V to +3.6V, f_{ADC} = f_{OSC}/2, f_{SCLK} = 10MHz, 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE

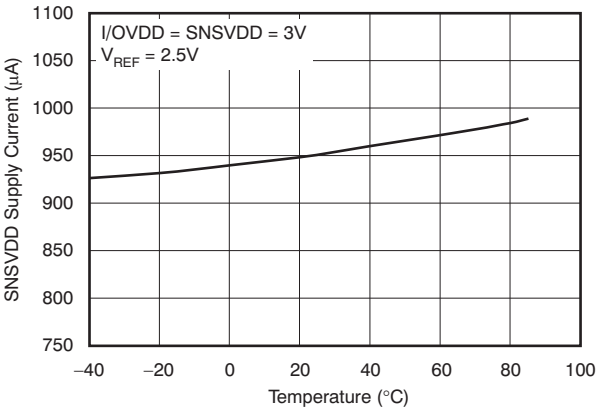


Figure 2.

SUPPLY CURRENT vs TEMPERATURE

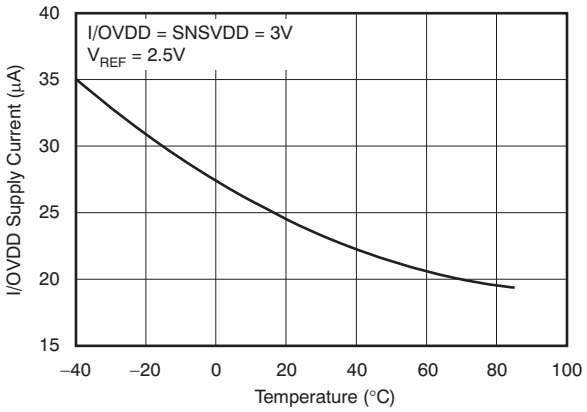


Figure 3.

POWER-DOWN SUPPLY CURRENT vs TEMPERATURE

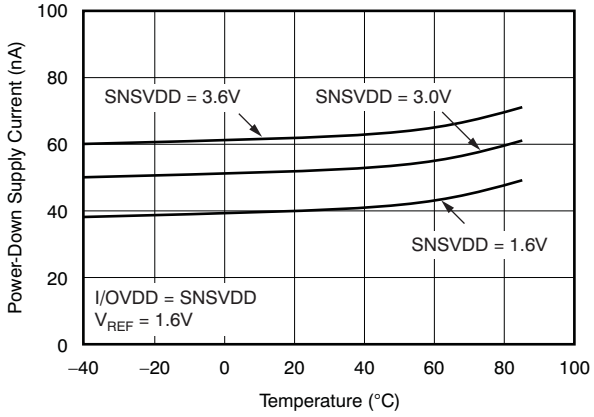


Figure 4.

SUPPLY CURRENT vs SUPPLY VOLTAGE

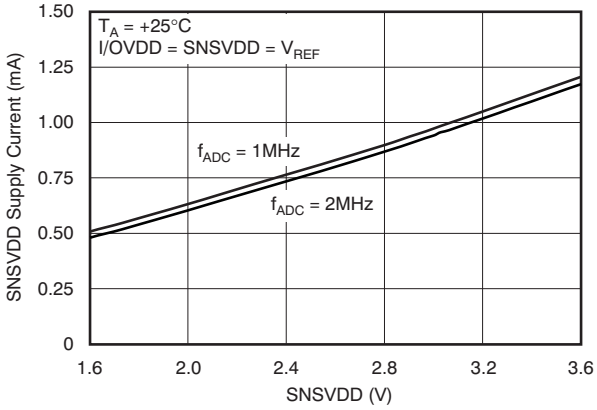


Figure 5.

SUPPLY CURRENT vs SUPPLY VOLTAGE

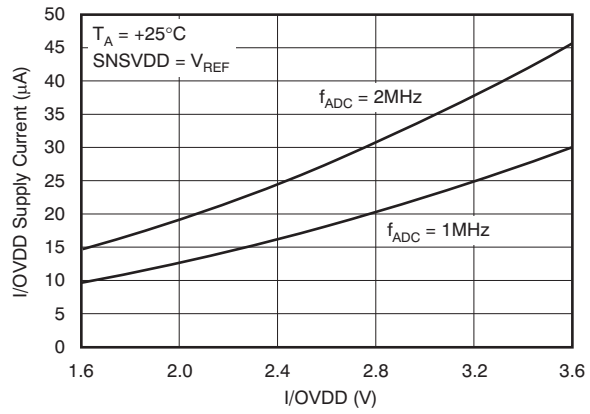


Figure 6.

CHANGE IN GAIN vs TEMPERATURE

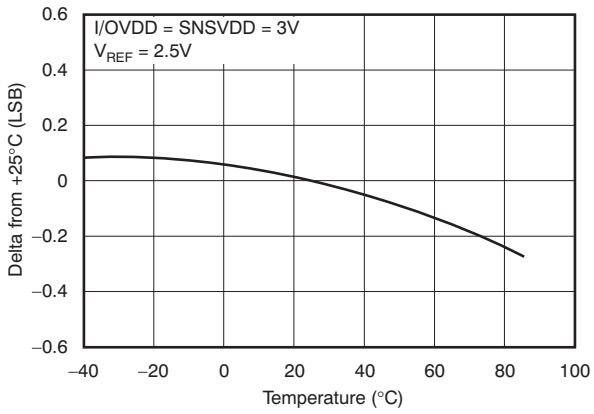


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, SNSVDD = V_{REF} = +1.6V to +3.6V, I/OVDD = +1.2V to +3.6V, $f_{ADC} = f_{OSC}/2$, f_{SCLK} = 10MHz, 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.

CHANGE IN OFFSET vs TEMPERATURE

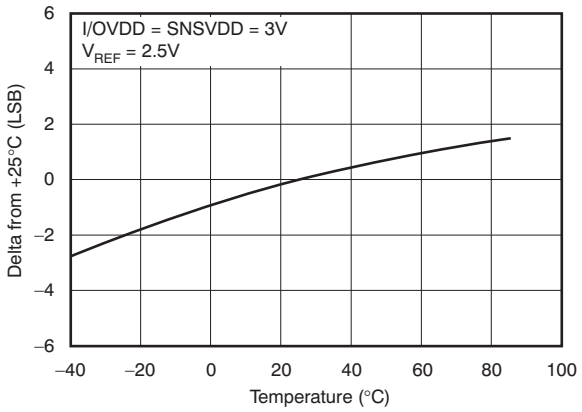


Figure 8.

REFERENCE INPUT CURRENT vs TEMPERATURE

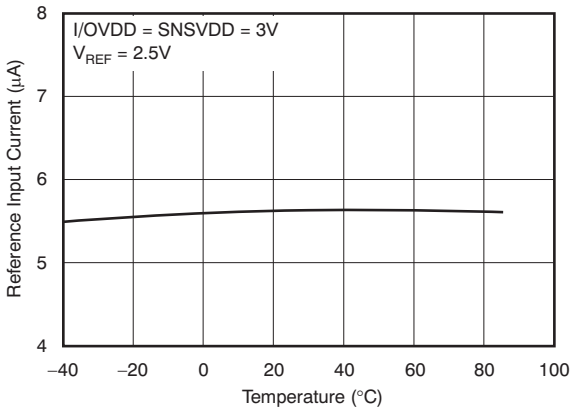


Figure 9.

SWITCH ON-RESISTANCE vs SUPPLY VOLTAGE

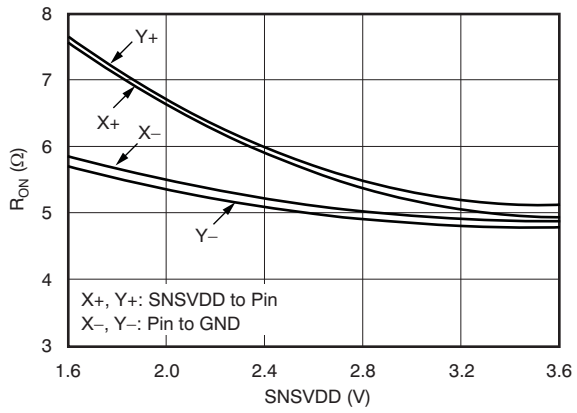


Figure 10.

SWITCH ON-RESISTANCE vs TEMPERATURE

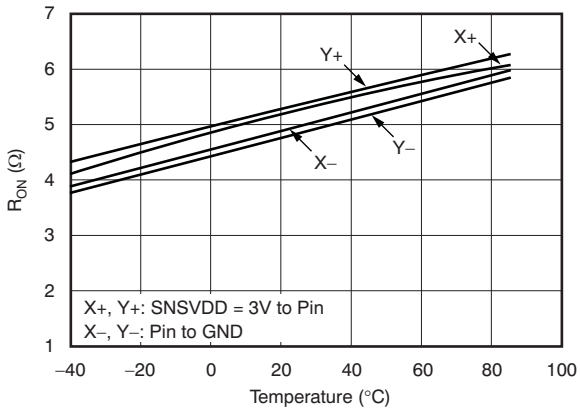


Figure 11.

SWITCH ON-RESISTANCE vs TEMPERATURE

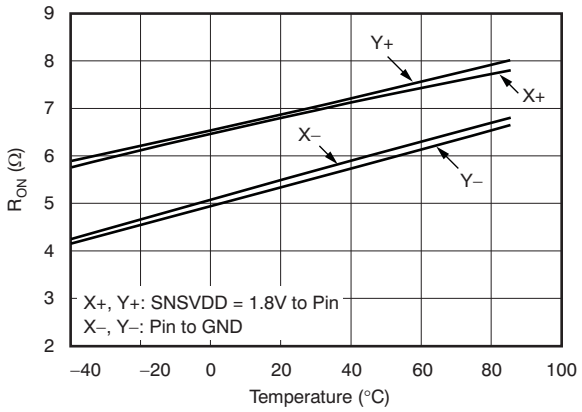


Figure 12.

TEMP DIODE VOLTAGE vs TEMPERATURE

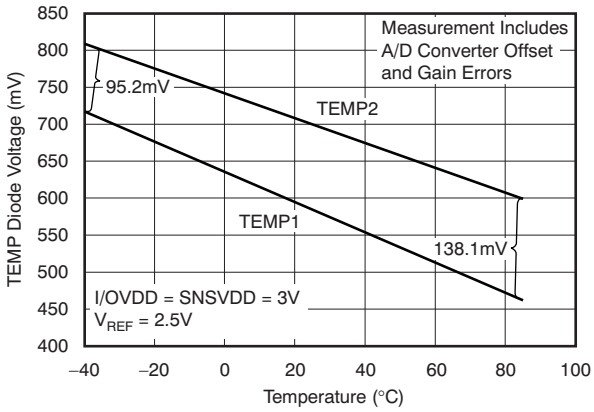


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, SNSVDD = V_{REF} = +1.6V to +3.6V, I/OVDD = +1.2V to +3.6V, $f_{ADC} = f_{OSC}/2$, f_{SCLK} = 10MHz, 12-bit mode, and non-continuous AUX measurement, unless otherwise noted.

TEMP1 DIODE VOLTAGE vs SUPPLY VOLTAGE

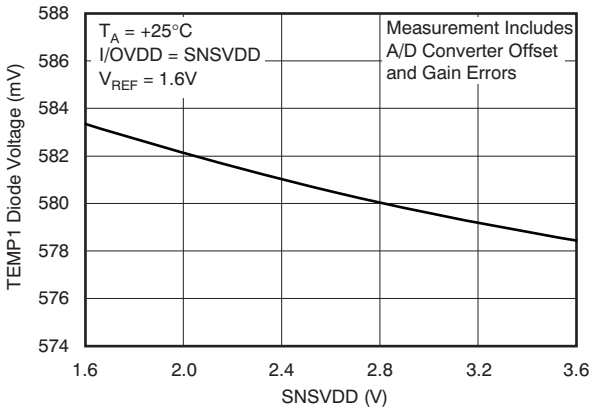


Figure 14.

TEMP2 DIODE VOLTAGE vs SUPPLY VOLTAGE

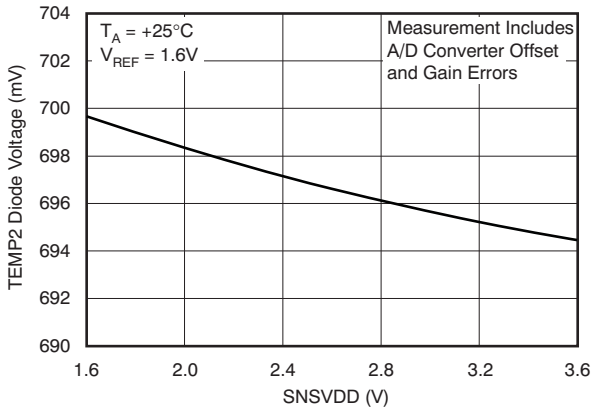


Figure 15.

SUPPLY CURRENT vs SUPPLY VOLTAGE

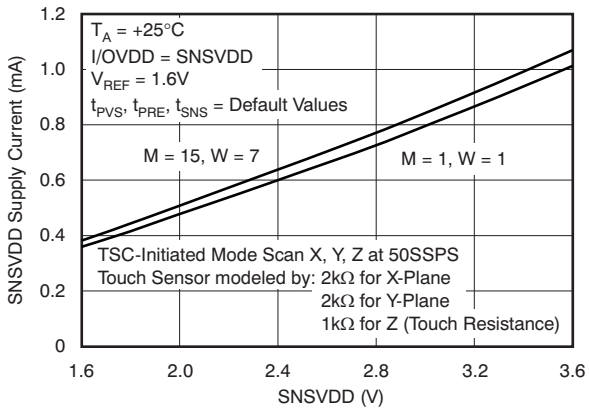


Figure 16.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

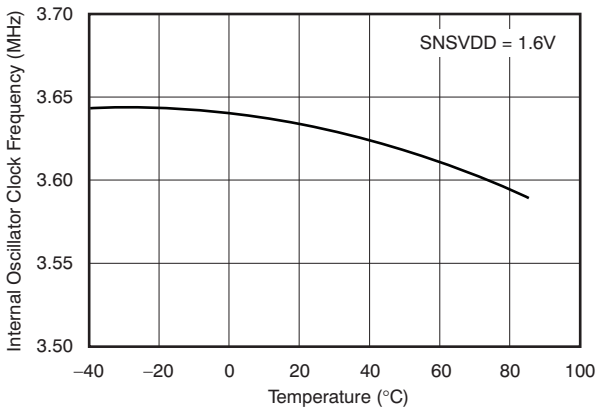


Figure 17.

INTERNAL OSCILLATOR CLOCK FREQUENCY vs TEMPERATURE

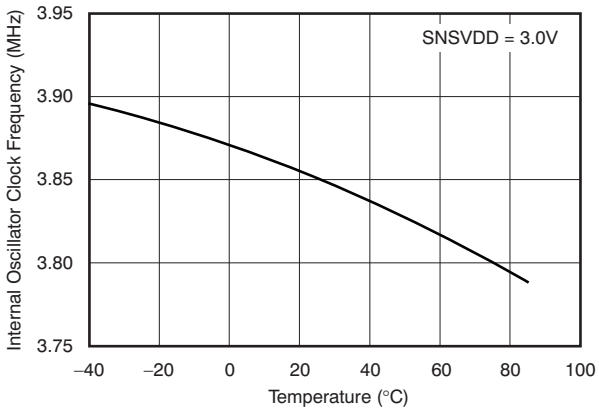


Figure 18.

OVERVIEW

The TSC2005 is an analog interface circuit for a human interface device. A register-based architecture eases integration with microprocessor-based systems through a standard SPI bus. All peripheral functions are controlled through the registers and onboard state machines. The TSC2005 features include:

- Very low-power touch screen controller
- Very small onboard footprint
- Relieves host from tedious routine tasks by flexible preprocessing, saving resources for more critical tasks
- Ability to work on very low supply voltage
- Minimal connection interface allows easiest isolation and reduces the number of dedicated I/O pins required
- Miniature, yet complete; requires no external supporting component. (**NOTE:** Although the TSC2005 can use an external reference, it is also possible to use SNSVDD as the reference.)
- Enhanced ESD up to 6kV

The TSC2005 consists of the following blocks (refer to the block diagram on the front page):

- Touch Screen Interface
- Auxiliary Input (AUX)
- Temperature Sensor
- Acquisition Activity Preprocessing
- Internal Conversion Clock
- SPI Interface

Communication to the TSC2005 is done via an SPI serial interface. The TSC2005 is an SPI slave device; therefore, data is shifted into or out of the TSC2005 under control of the host microprocessor, which also provides the serial data clock.

Control of the TSC2005 and its functions is accomplished by writing to different registers in the TSC2005. A simple command protocol compatible with SPI is used to address these registers. A simple serial command protocol, compatible with SPI, is used to address these registers.

The measurement result is placed in the TSC2005 registers and may be read by the host at any time. This preprocessing frees up the host so that resources can be redirected for more critical tasks. Two optional signals are also available from the TSC2005 to indicate that data is available for the host to read. $\overline{\text{PINTDAV}}$ is a programmable interrupt/status output pin that can be programmed to indicate a pen-touch, data available, or the combination of both. Figure 19 shows a typical application of the TSC2005.

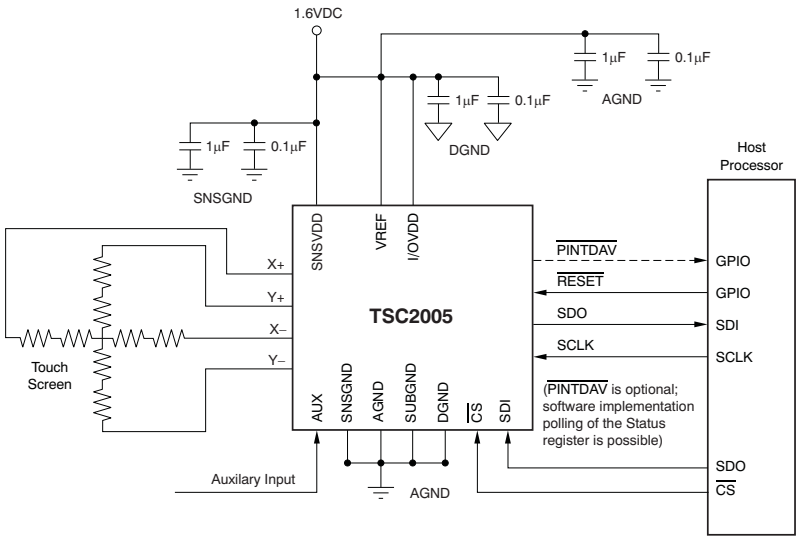


Figure 19. Typical Circuit Configuration

OVERVIEW (continued)

TOUCH SCREEN OPERATION

A resistive touch screen operates by applying a voltage across a resistor network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus, pen, or finger). The change in the resistance ratio marks the location on the touch screen.

The TSC2005 supports the resistive 4-wire configurations, as shown in Figure 20. The circuit determines location in two coordinate pair dimensions, although a third dimension can be added for measuring pressure.

4-WIRE TOUCH SCREEN COORDINATE PAIR MEASUREMENT

A 4-wire touch screen is typically constructed as shown in Figure 20. It consists of two transparent resistive layers separated by insulating spacers.

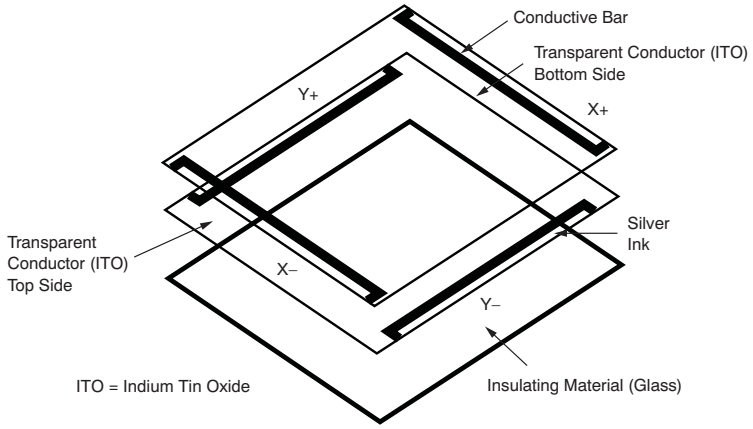


Figure 20. 4-Wire Touch Screen Construction

The 4-wire touch screen panel works by applying a voltage across the vertical or horizontal resistive network. The A/D converter converts the voltage measured at the point where the panel is touched. A measurement of the Y position of the pointing device is made by connecting the X+ input to a data converter chip, turning on the Y+ and Y– drivers, and digitizing the voltage seen at the X+ input. The voltage measured is determined by the voltage divider developed at the point of touch. For this measurement, the horizontal panel resistance in the X+ lead does not affect the conversion because of the high input impedance of the A/D converter.

Voltage is then applied to the other axis, and the A/D converter converts the voltage representing the X position on the screen. This process provides the X and Y coordinates to the associated processor.

Measuring touch pressure (Z) can also be done with the TSC2005. To determine pen or finger touch, the pressure of the *touch* must be determined. Generally, it is not necessary to have very high performance for this test; therefore, 10-bit resolution mode is recommended (however, data sheet calculations will be shown with the 12-bit resolution mode). There are several different ways of performing this measurement. The TSC2005 supports two methods. The first method requires knowing the X-plate resistance, the measurement of the X-Position, and two additional cross panel measurements (Z_2 and Z_1) of the touch screen (see Figure 21). Equation 1 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \cdot \frac{X_{Postition}}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \quad (1)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Equation 2 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \cdot X_{Postition}}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \cdot \left(1 - \frac{Y_{Position}}{4096} \right) \quad (1)$$

OVERVIEW (continued)

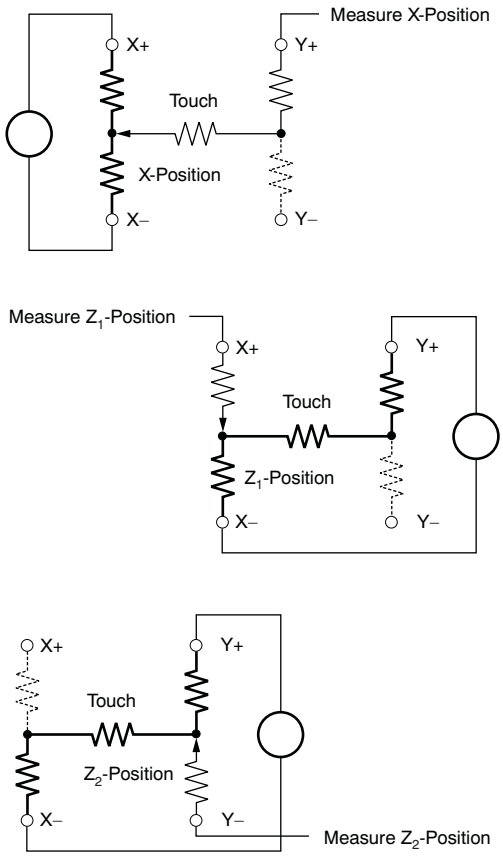


Figure 21. Pressure Measurement

When the touch panel is pressed or touched and the drivers to the panel are turned on, the voltage across the touch panel will often overshoot and then slowly settle down (decay) to a stable DC value. This effect is a result of mechanical bouncing caused by vibration of the top layer sheet of the touch panel when the panel is pressed. This settling time must be accounted for, or else the converted value will be in error. Therefore, a delay must be introduced between the time the driver for a particular measurement is turned on, and the time a measurement is made.

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen (for example, noise generated by the LCD panel or back-light circuitry). The value of these capacitors provides a low-pass filter to reduce the noise, but will cause an additional settling time requirement when the panel is touched.

The TSC2005 offers several solutions to this problem. A programmable delay time is available that sets the delay between turning the drivers on and making a conversion. This delay is referred to as the *panel voltage stabilization time*, and is used in some of the TSC2005 modes. In other modes, the TSC2005 can be commanded to turn on the drivers only without performing a conversion. Time can then be allowed before the command is issued to perform a conversion.

The TSC2005 touch screen interface can measure position (X,Y) and pressure (Z). Determination of these coordinates is possible under three different modes of the A/D converter:

- conversion controlled by the TSC2005 initiated by detection of a touch;
- conversion controlled by the TSC2005 initiated by the host responding to the $\overline{\text{PENIRQ}}$ signal; or
- conversion completely controlled by the host processor.

OVERVIEW (continued)

INTERNAL TEMPERATURE SENSOR

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the TSC2005 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes.

The TSC2005 offers two modes of temperature measurement. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. The TEMP1 diode, shown in Figure 22, is used during this measurement cycle. This voltage is typically 580mV at +25°C with a 10µA current. The absolute value of this diode voltage can vary a few millivolts; the temperature coefficient (T_C) of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in system memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (1LSB = 610µV with V_{REF} = 2.5V).

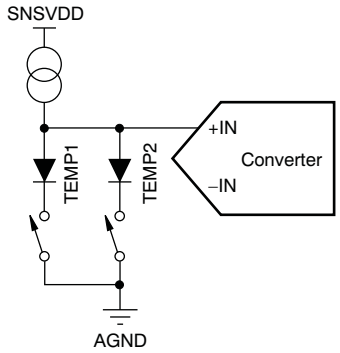


Figure 22. Functional Block Diagram of Temperature Measurement Mode

The second mode does not require a test temperature calibration, but uses a two-measurement (differential) method to eliminate the need for absolute temperature calibration and for achieving 2°C/LSB accuracy. This mode requires a second conversion of the voltage across the TEMP2 diode with a resistance 80 times larger than the TEMP1 diode. The voltage difference between the first (TEMP1) and second (TEMP2) conversion is represented by:

$$\Delta V = \frac{kT}{q} \cdot \ln(N) \quad (3)$$

Where:

N is the resistance ratio = 80,

k = Boltzmann's constant (1.38054×10^{-23} electrons volts/degrees Kelvin),

q = the electron charge (1.602189×10^{-19}°C),

T = the temperature in degrees Kelvin (K).

This method can provide much improved absolute temperature measurement, but a lower resolution of 1.6°C/LSB. The resulting equation to solve for T is:

$$T = \frac{q \cdot \Delta V}{k \cdot \ln(N)} \quad (4)$$

Where:

$\Delta V = V_{BE}$ (TEMP2) – V_{BE}(TEMP1) (in mV)

$\therefore T = 2.648 \bullet \Delta V$ (in K)

°C = 2.648 • Δ V – 273

Temperature 1 and/or temperature 2 measurements have the same timing as Figure 38.

OVERVIEW (continued)

ANALOG-TO-DIGITAL CONVERTER

Figure 23 shows the analog inputs of the TSC2005. The analog inputs (X, Y, and Z touch panel coordinates, chip temperature and auxiliary inputs) are provided via a multiplexer to the Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The A/D architecture is based on capacitive redistribution architecture, which inherently includes a sample-and-hold function.

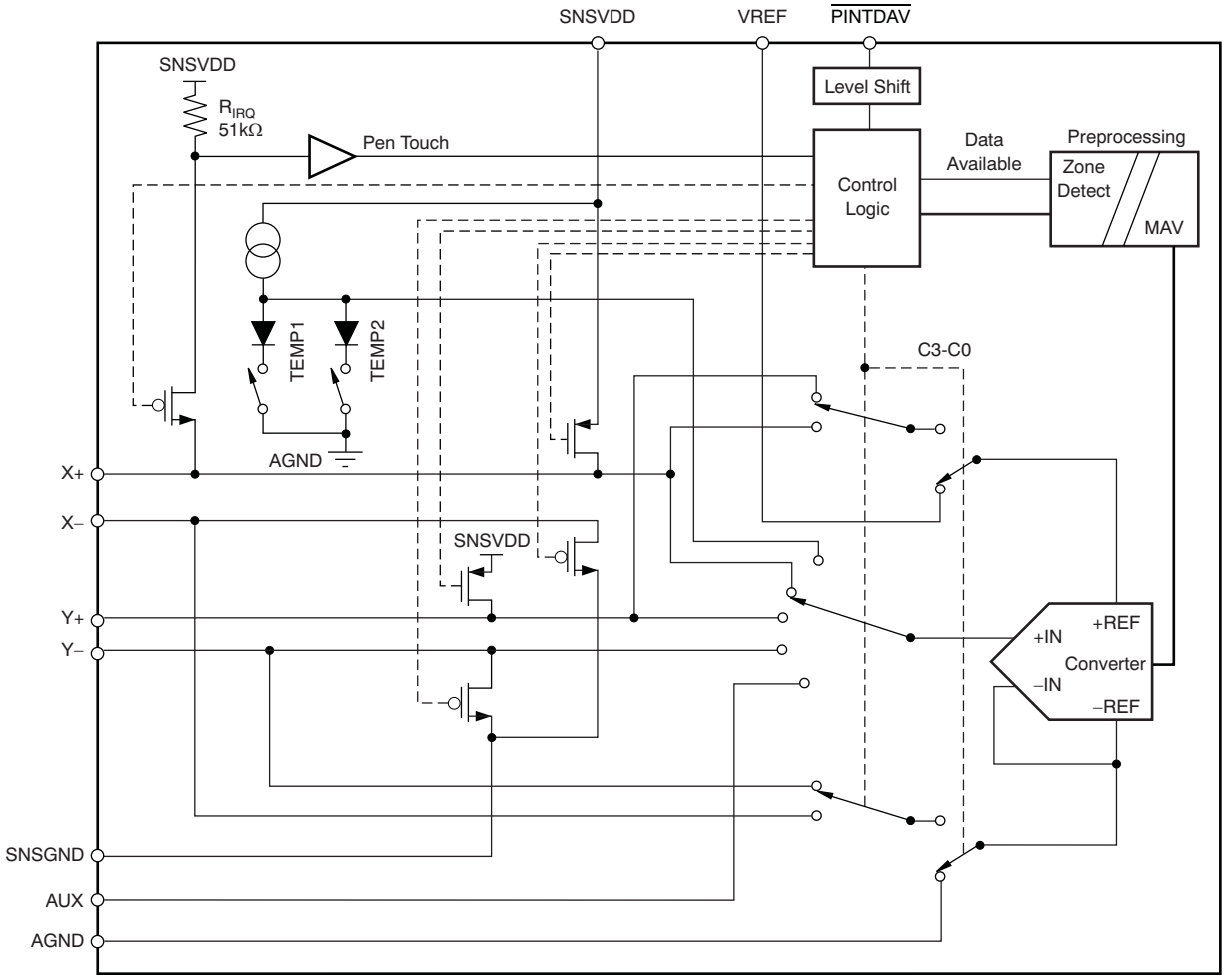


Figure 23. Simplified Diagram of the Analog Input Section

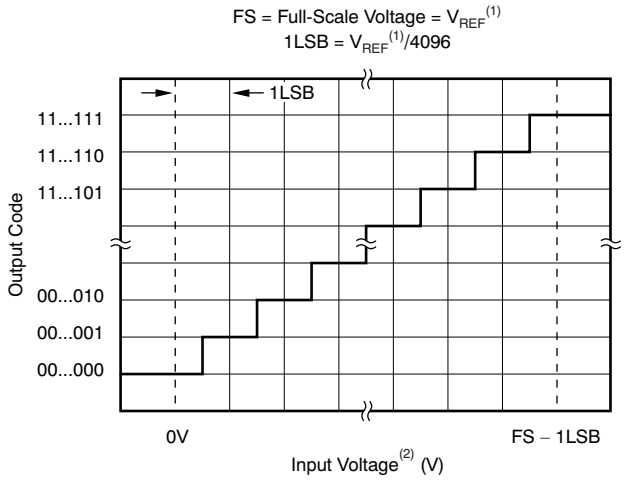
A unique configuration of low on-resistance switches allows an unselected A/D converter input channel to provide power and an accompanying pin to provide ground for driving the touch panel. By maintaining a differential input to the converter and a differential reference input architecture, it is possible to negate errors caused by the driver switch on-resistances.

The A/D converter is controlled by two A/D Converter Control registers. Several modes of operation are possible, depending on the bits set in the control registers. Channel selection, scan operation, preprocessing, resolution, and conversion rate may all be programmed through these registers. These modes are outlined in the sections that follow for each type of analog input. The conversion results are stored in the appropriate result register.

OVERVIEW (continued)

Data Format

The TSC2005 output data is in Straight Binary format as shown in Figure 24. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.



(1) Reference voltage at converter: +REF – (–REF). See Figure 23.

(2) Input voltage at converter, after multiplexer: +IN – (–IN). See Figure 23.

Figure 24. Ideal Input Voltages and Output Codes

Reference

The TSC2005 uses an external voltage reference that applied to the VREF pin. It is possible to use VDD as the reference voltage because the upper reference voltage range is the same as the supply voltage range, .

Variable Resolution

The TSC2005 provides either 10-bit or 12-bit resolution for the A/D converter. Lower resolution is often practical for measureming slow changing signals such as touch pressure. Performing the conversions at lower resolution reduces the amount of time it takes for the A/D converter to complete its conversion process, which also lowers power consumption.

Conversion Clock and Conversion Time

The TSC2005 contains an internal clock (oscillator) that drives the internal state machines that perform the many functions of the part. This clock is divided down to provide a conversion clock for A/D converter. The division ratio for this clock is set in the A/D Converter Control register (see Table 15). The ability to change the conversion clock rate allows the user to choose the optimal value for resolution, speed, and power dissipation. If the 4MHz (oscillator) clock is used directly as the A/D converter clock (when CL[1:0] = (0,0)), the A/D converter resolution is limited to 10-bits. Using higher resolutions at this speed does not result in more accurate conversions. 12-bit resolution requires that CL[1:0] is set to (0,1) or (1,0).

Regardless of the conversion clock speed, the internal clock runs nominally at 3.8MHz at a 3V supply (SNSVDD) and slows down to 3.6MHz at a 1.6V supply. The conversion time of the TSC2005 depends on several functions. While the conversion clock speed plays an important role in the time it takes for a conversion to complete, a certain number of internal clock cycles are needed for proper sampling of the signal. Moreover, additional times (such as the panel voltage stabilization time), can add significantly to the time it takes to perform a conversion. Conversion time can vary depending on the mode in which the TSC2005 is used. Throughout this data sheet, internal and conversion clock cycles are used to describe the amount of time that many functions take. These times must be taken into account when considering the total system design.

OVERVIEW (continued)

Touch Detect

$\overline{\text{PINTDAV}}$ can be programmed to generate an interrupt to the host. Figure 25 details an example for the Y-position measurement. While in the power-down mode, the Y– driver is on and connected to GND. The internal pen-touch signal depends on whether or not the X+ input is driven low. When the panel is touched, the X+ input is pulled to ground through the touch screen and the internal pen-touch output is set to low because of the detection on the current path through the panel to GND, which initiates an interrupt to the processor. During the measurement cycles for X- and Y-Position, the X+ input is disconnected, which eliminates any leakage current from the pull-up resistor to flow through the touch screen, thus causing no errors.

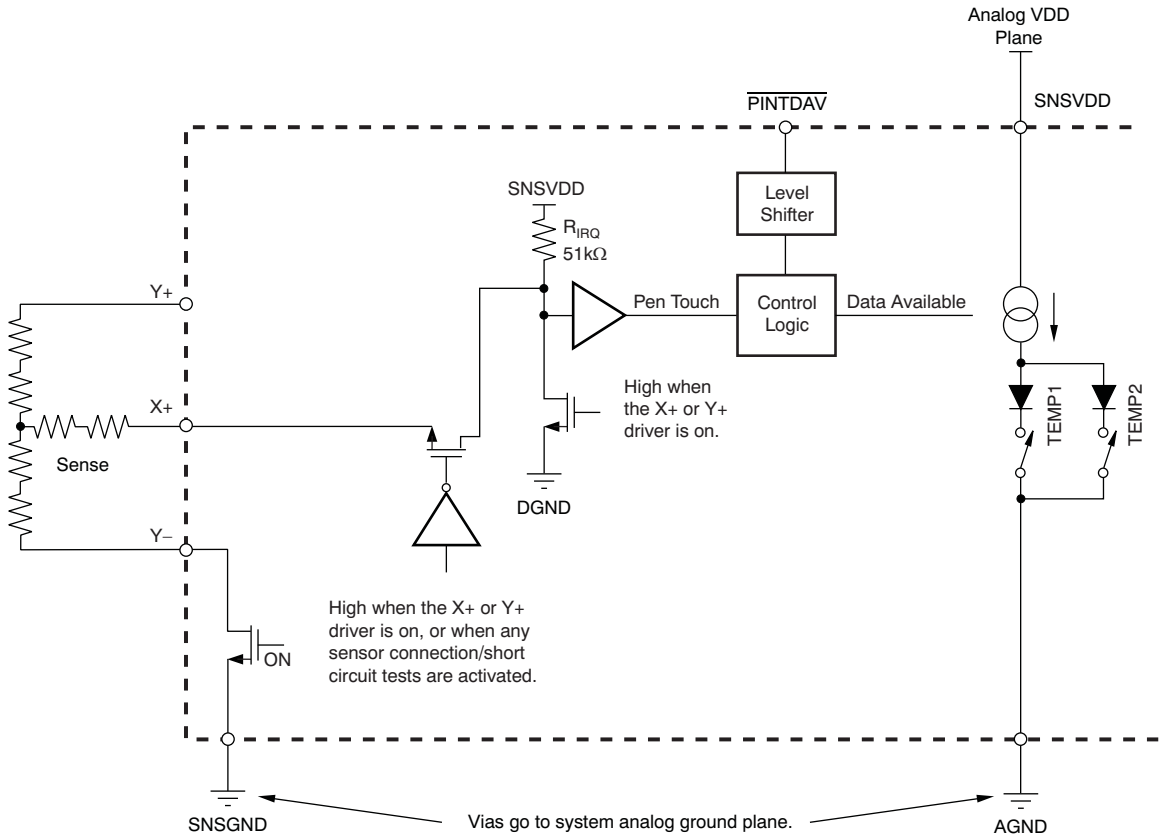


Figure 25. Example of a Pen-Touch Induced Interrupt via the $\overline{\text{PINTDAV}}$ Pin

In modes where the TSC2005 must detect whether or not the screen is still being touched (for example, when doing a pen-touch initiated X, Y, and Z conversion), the TSC2005 must reset the drivers so that the 50kΩ resistor is connected again. Because of the high value of this pull-up resistor, any capacitance on the touch screen inputs will cause a long delay time, and may prevent the detection from occurring correctly. To prevent this possible delay, the TSC2005 has a circuit that allows any screen capacitance to be *precharged*, so that the pull-up resistor does not have to be the only source for the charging current. The time allowed for this precharge, as well as the time needed to sense if the screen is still touched, can be set in the configuration register.

This configuration underscores the need to use the minimum possible capacitor values on the touch screen inputs. These capacitors may be needed to reduce noise, but too large a value will increase the needed precharge and sense times, as well as the panel voltage stabilization time.

OVERVIEW (continued)

Preprocessing

The TSC2005 offers an array of powerful preprocessing operations. The goal is to reduce any unnecessary traffic on the bus and reduce the host processor loading. This reduction is especially critical for the serial interface, where limited bandwidth is a tradeoff, keeping the connection lines to a minimum.

All data acquisition tasks are looking for specific data that meet certain criteria. Many of these tasks fall into a predefined range, while other tasks may be looking for a value in a noisy environment. If these data are all to be retrieved by host processor for processing, the limited bus bandwidth will be quickly saturated, along with the host processor processing capability. In any case, the host processor must always be reserved for more critical tasks, not for routine work.

The preprocessing unit consists of two main functions: the combined MAV filter (median value filter and averaging filter), followed by the zone detection.

Preprocessing - Median Value Filter and Averaging Value Filter

The first preprocessing function, a combined MAV filter, can be operated independently as a median value filter (MVF), an averaging value filter (AVF) and a combined filter (MAVF).

If the acquired signal source is noisy because of the digital switching circuit, it may be necessary to evaluate the data without noise. In this case, the median value filter (MVF) operation helps to discard the noise. The array of *N* converted results is first sorted. The return value is either the middle (median value) of an array of *M* converted results, or the average value of a window size of *W* of converted results:

- N = the total number of converted results used by the MAV filter
- M = the median value filter size programmed
- W = the averaging window size programmed

If M = 1, then N = W. A special case is W = 1, which means the MAVF is bypassed. Otherwise, if W > 1, only averaging is performed on these converted results. In either case, the return value is the averaged value of window size W of converted results. If M > 1 and W = 1, then N = M, meaning only the median value filter is operating. The return value is the middle position converted result from the array of M converted results. If M > 1 and W > 1, then N = M. In this case, W < M. The return value is the averaged value of middle portion W of converted results out of the array of M converted results. Since the value of W is an odd number in this case, the averaging value is calculated with the middle position converted result counted twice (so a total of W + 1 converted results are averaged).

Table 1. Median Value Filter Size Selection

M1	M0	MEDIAN VALUE FILTER M =	POSSIBLE AVERAGING WINDOW SIZE W =
0	0	1	1, 4, 8, 16
0	1	3	1
1	0	7	1, 3
1	1	15	1, 3, 7

Table 2. Averaging Value Filter Size Selection

W1	W0	AVERAGING VALUE FILTER SIZE SELECTION W =	
		M = 1 (Averaging Only)	M > 1
0	0	1	1
0	1	4	3
1	0	8	7
1	1	16	Reserved

NOTE: The default setting for MAVF is MVF (median value filter with averaging bypassed) for any invalid configuration. For example, if (M1, M0, W1, W0) = (1,0, 1,0), the MAVF performs as it was configured for (1,0,0,0), median filter only with filter size = 7 and no averaging. The only exception is M > 1 and (W1, W0) = (1,1). This setting is reserved and should not be used.

Table 3. Combined MAV Filter Setting

M	W	INTERPRETATION	N =	OUTPUT
= 1	= 1	Bypass both MAF and AVF	W	The converted result
= 1	> 1	Bypass MVF only	W	Average of W converted results
> 1	= 1	Bypass AVF only	M	Median of M converted results
> 1	> 1	M > W	M	Average of middle W of M converted results with the median counted twice

The MAV filter is available for all analog inputs including the touch screen inputs, temperature measurements TEMP1 and TEMP2, and the AUX measurement.

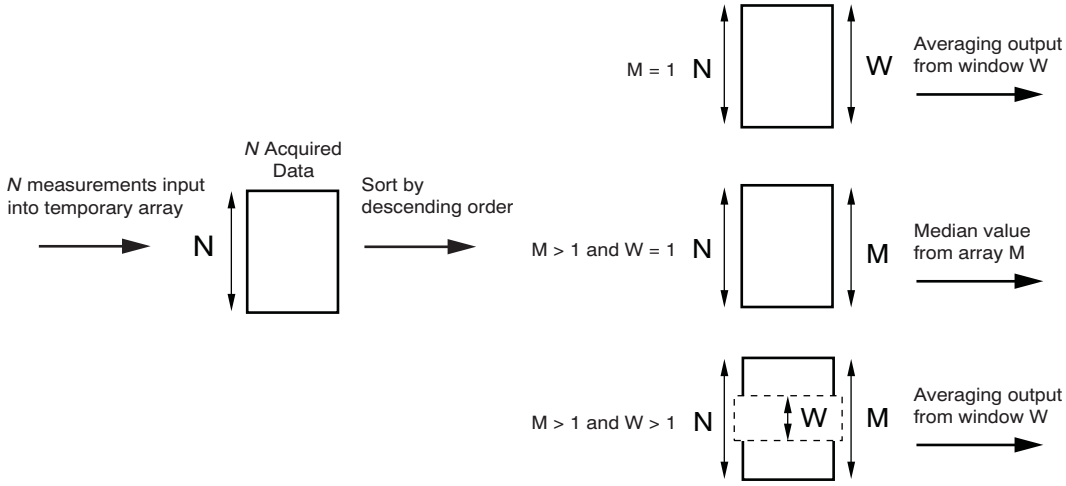


Figure 26. MAV Filter Operation

Zone Detection

The Zone Detection unit is capable of screening all processed data from the MAVF and retaining only the data of interest (data that fit the prerequisite). This unit can be programmed to send an alert if a predefined condition set by two threshold value registers is met. Three different zones may be set for:

1. Above the upper limit (X ≥ Threshold High)
2. Between the two thresholds (Threshold Low < X < Threshold High)
3. Below the lower limit (X ≤ Threshold Low)

The AUX and temperatures TEMP1 and TEMP2 have separate threshold value registers that can be enabled or disabled. This function is not available to the touch screen inputs. Once the preset condition is met, the $\overline{\text{DAV}}$ output to the $\overline{\text{PINTDAV}}$ pin is pulled low and the corresponding DAV bit is set.

DIGITAL INTERFACE

The TSC2005 communicates through a standard SPI bus. The SPI allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master generates the synchronizing clock and initiates transmissions. The SPI slave devices depend on a master to start and synchronize transmissions.

A transmission begins when initiated by a master SPI. The byte from the master SPI begins shifting in on the slave SDI (MOSI—master out, slave in) pin under the control of the master serial clock. As the byte shifts in on the SDI (MOSI) pin, a byte shifts out on the SDO (MISO—master in, slave out) pin to the master shift register.

The idle state of the TSC2005 serial clock is logic low, which corresponds to a clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The TSC2005 interface is designed so that with a clock phase bit setting of 0 (typical microprocessor SPI control bit CPHA = 0), the master begins driving its MOSI pin and the slave begins driving its MISO pin half an SCLK before the first serial clock edge. The $\overline{CS}$ ($\overline{SS}$, slave select) pin can remain low between transmissions.

Table 4. Standard SPI Signal Names vs Common Serial Interface Signal Names

SPI SIGNAL NAMES	COMMON SERIAL INTERFACE NAMES
$\overline{SS}$ (Slave Select)	$\overline{CS}$ (Chip Select)
MISO (Master In Slave Out)	SDO (Serial Data Out)
MOSI (Master Out Slave In)	SDI (Serial Data In)

CONTROL BYTE

Table 5. Control Byte Format:
Start a Conversion and Mode Setting

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
1 (Control Byte 1)	C3	C2	C1	C0	RM	SWRST	STS
0 (Control Byte 0)	A3	A2	A1	A0	Reserved (Write '0')	PND0	R/$\overline{W}$

Table 6. Control Byte 1 Bit Register Description (D7 = 1)

BIT	NAME	DESCRIPTION
D7	Control Byte ID	1
D6-D3	C3:C0	Converter Function Select as detailed in Table 7
D2	RM	0: 10 Bit 1: 12 Bit
D1	SWRST	Software Reset 1: Reset all register values to default
D0	STS	Stop bit for all converter functions

Bit D7: Control Byte ID

1: Control Byte 1 (start conversion and channel select and conversion-related configuration).

0: Control Byte 0 (read/write data registers and non-conversion-related controls).

Bits D6-D3: C3:C0

Converter function select bits. These bits select the input to be converted, and the converter function to be executed. Table 7 lists the possible converter functions.

Table 7. Converter Function Select

C3	C2	C1	C0	FUNCTION
0	0	0	0	Touch screen scan function: X, Y, Z_1, and Z_2 coordinates converted and the results returned to X, Y, Z_1, and Z_2 data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	0	1	Touch screen scan function: X and Y coordinates converted and the results returned to X and Y data registers. Scan continues until either the pen is lifted or a stop bit is sent.
0	0	1	0	Touch screen scan function: X coordinate converted and the results returned to X data register.
0	0	1	1	Touch screen scan function: Y coordinate converted and the results returned to Y data register.
0	1	0	0	Touch screen scan function: Z_1 and Z_2 coordinates converted and the results returned to Z_1 and Z_2 data registers.
0	1	0	1	Auxiliary input converted and the results returned to the AUX data register.
0	1	1	0	A temperature measurement is made and the results returned to the Temperature Measurement 1 data register.
0	1	1	1	A differential temperature measurement is made and the results returned to the Temperature Measurement 2 data register.
1	0	0	0	Auxiliary input is converted ***continuously*** and the results returned to the AUX data register.
1	0	0	1	Touch screen panel connection to X-axis drivers is tested. The test result is output to $\overline{\text{PINTDAV}}$ and shown in STATUS register.
1	0	1	0	Touch screen panel connection to Y-axis drivers is tested. The test result is output to $\overline{\text{PINTDAV}}$ and shown in STATUS register.
1	0	1	1	RESERVED (Note: any condition caused by this command can be cleared by setting the STS bit to 1).
1	1	0	0	Touch screen panel short-circuit (between X and Y plates) is tested through Y-axis. The test result is output to $\overline{\text{PINTDAV}}$ and shown in the STATUS register.
1	1	0	1	Turn on X+, X– drivers
1	1	1	0	Turn on Y+, Y– drivers
1	1	1	1	Turn on Y+, X– drivers

Touch Screen Scan Function for XYZ or XY

C3-C0 = 0000 or 0001: These scan functions can collaborate with the PSM bit that defines the control mode of converter functions. If the PSM bit is set to '1', these scan function select commands are recommended to be issued before a pen touch is detected in order to allow the TSC2005 to initiate and control the scan processes immediately after the screen is touched. If these functions are not issued before a pen touch is detected, the TSC2005 will wait for the host to write these functions before starting a scan process. If PSM stays as '1' after a TSC-initiated scan function is complete, the host is not required to write these function select bits again for each of the following pen touches after the detected touch. In the host-controlled converter function mode (PSM = 0), the host must send these functions select bits repeatedly for each scan function after a detected pen touch.

Touch Screen Sensor Connection Tests for X-Axis and Y-Axis

Range of resistances of different touch screen panels can be selected by setting the TBM bits in CFR1; see Table 20. Once the resistance of the sensor panel is selected, two continuity tests are run separately for the X-axis and Y-axis. The unit under test must pass both connection tests to ensure that a proper connection is secured.

C3-C0 = 1001: $\overline{\text{PINTDAV}}$ = 0 during this connection test. A '1' shown at end of the test indicates the X-axis drivers are well-connected to the sensor; otherwise, X-axis drivers are poorly connected. If drivers fail to connect, then $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

C3-C0 = 1010: $\overline{\text{PINTDAV}}$ = 0 during this connection test. A '1' shown at end of the test indicates the Y-axis drivers are well-connected to the sensor; otherwise, Y-axis drivers are poorly connected. If the drivers are fail to connect, then $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

Touch Sensor Short-Circuit Test

If the TBM bits of CFR1 detailed in Table 20 are set to all '1's, a short-circuit in the touch sensor can be detected.

C3-C0 = 1011: Reserved.

C3-C0 = 1100: $\overline{\text{PINTDAV}}$ = 0 during this short-circuit test. A '1' shown at end of the test indicates there is no short-circuit detected (through Y-axis) between the flex and stable layers. If there is a short-circuit detected, $\overline{\text{PINTDAV}}$ stays low until a stop bit (STS set to '1') is issued.

RM—Resolution select. If RM = 1, the conversion result resolution is 12-bit; otherwise, the resolution is 10-bit. This bit is the same RM bit shown in CFR0.

SWRST—Software reset input. All register values are set to default value if a '1' is written to this bit. This bit must be set to '0' in Control Byte 1 in order to cancel the software reset and resume normal operation.

STS—Stop bit for all converter functions. When writing a '1' to this register, this bit stops the converter function currently running in the TSC2005. A '0' must be written to this register in order to end the stop bit. This bit can only stop converter functions; it does not reset any data, status, or configuration registers. This bit is the same STS bit shown in CFR0, but can only be read through the CFR0 register with different interpretations.

Table 8. STS Bit Operation

OPERATION	VALUE	DESCRIPTION
Write	0	Normal operation
Write	1	Stop converter functions and power down

Table 9. Control Byte 0 Bit Register Description (D7 = 0)

BIT	NAME	DESCRIPTION
D7	Control Byte ID	1: Control Byte 1—start conversion, channel select, and converison-related configuration 0: Control Byte 0—read/write data registers and non-conversion-related controls
D6-D3	A3-A0	Register Address Bits as detailed in Table 10
D2	RESERVED	A '0' must be set in this bit for normal operation
D1	PND0	Power Not Down Control 1: A/D converter biasing circuitry is always on between conversions but is shut down after the converter function stops 0: A/D converter biasing circuitry is shut down either between conversions or after the converter function stops
D0	R/$\overline{\text{W}}$	Register Data Flow Control 1: Read from registers 0: Write to registers

Table 10. Internal Register Map

REGISTER ADDRESS				REGISTER CONTENT	READ/WRITE
A3	A2	A1	A0		
0	0	0	0	X measurement result	R
0	0	0	1	Y measurement result	R
0	0	1	0	Z_1 measurement result	R
0	0	1	1	Z_2 measurement result	R
0	1	0	0	AUX measurement result	R
0	1	0	1	Temp1 measurement result	R
0	1	1	0	Temp2 measurement result	R
0	1	1	1	Status	R
1	0	0	0	AUX high threshold	R/W
1	0	0	1	AUX low threshold	R/W
1	0	1	0	Temp high threshold (apply to both TEMP1 and TEMP2)	R/W
1	0	1	1	Temp low threshold (apply to both TEMP1 and TEMP2)	R/W
1	1	0	0	CFR0	R/W
1	1	0	1	CFR1	R/W
1	1	1	0	CFR2	R/W
1	1	1	1	Converter function select status	R

R/$\overline{W}$—Register read and write control. A '1' indicates the contents of the internal register addressed by A3-A0 are sent to SDO at the next SPI interface clock cycle. A '0' indicates the data following Control Byte 0 on SDI are written into registers addressed by A3-A0.

START A CONVERTER FUNCTION (CONTROL BYTE 1)

Control Byte 1 must begin with D7 = 1, as shown in Figure 27. Control Byte 1 starts the converter function that is chosen by C3-C0, as shown in Table 7. After sending Control Byte 1, the master does not need to hold $\overline{CS}$ low, and can release $\overline{CS}$ for operating other slave devices that share the same SCLK. After the converter function completes or stops, the preprocessed data or data set are stored in data registers and can be read by sending Control Byte 0 with Read Bit and a proper address in A3-A0. For the detailed operating procedures, see the Operation section.

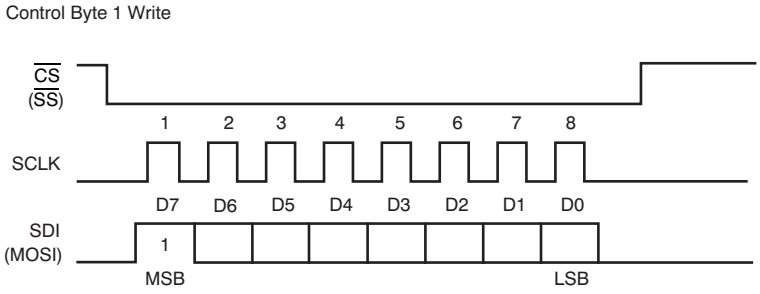


Figure 27. Interface Timing — Control Byte 1

REGISTER ACCESS (Control Byte 0 with R/$\overline{W}$ Bit)

Control byte 0, beginning with D7 = 0, is used to access the internal registers. This control byte uses the last bit, D0, to control the flow of data. If D0 is '1', then the content of the register pointed by the address bits (A3-A0) is output to SDO (MISO) in the next cycle. Otherwise, the data coming from SDI (MOSI) is written to the register properly pointed to by the address bits in the control byte (if the write mode is available for the pointed register). After Control Byte 0 with Read/Write Bit followed by a 16-bit word on SDO/SDI completes, the master can hold $\overline{CS}$ low to send another Control Byte 0 with Read/Write Bit followed by a 16-bit word on SDO/SDI as many times as the master manages to operate.

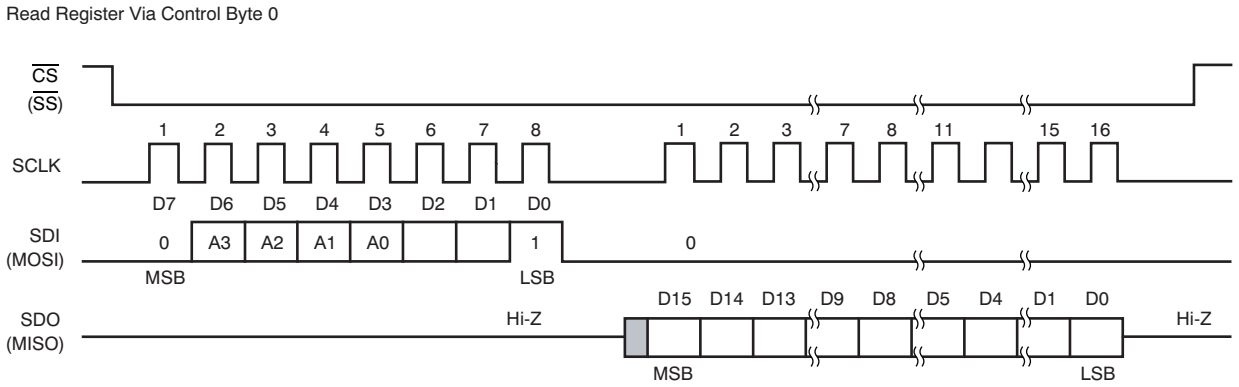


Figure 28. Interface Timing — Sending Control Byte 0 with Read Bit

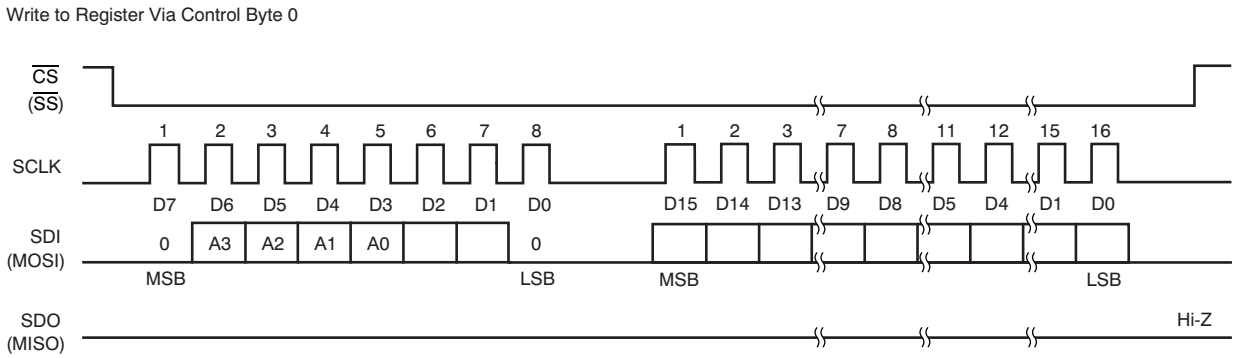


Figure 29. Interface Timing — Sending Control Byte 0 with Write Bit

COMMUNICATION PROTOCOL

The TSC2005 is controlled entirely by registers. Reading and writing to these registers are accomplished by the use of Control Byte 0, which includes a 4-bit address plus one read/write control bit. The data registers defined in Table 10 are all 16-bit, right-adjusted. **NOTE:** Except for some configuration registers and the Status register that are full 16-bit registers, the rest of the value registers are 12-bit (or 10-bit) data preceded by four (or six) zeros.

Configuration Register 0

Table 11. Configuration Register 0 (Reset Value = 4000h for Read; 0000h for Write)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
PSM	STS	RM	CL1	CL0	PV2	PV1	PV0	PR2	PR1	PR0	SN2	SN1	SN0	DTW	LSM

PSM—Pen status/control mode. Reading this bit allows the host to determine if the screen is touched. Writing to this bit selects the mode used to control the flow of converter functions that are either initiated and/or controlled by host or under control of the TSC2005 responding to a pen touch. When reading, the PSM bit indicates if the pen is down or not. When writing to this register, this bit determines if the TSC2005 controls the converter functions, or if the converter functions are host-controlled. The default state is the host-controlled converter function mode (0). The other state (1) is the TSC-initiated scan function mode that must only collaborate with C3-C0 = 0000 or 0001 in order to allow the TSC2005 to initiate and control the scan function for XYZ or XY when a pen touch is detected.

Table 12. PSM Bit Operation

OPERATION	VALUE	DESCRIPTION
Read	0	No screen touch detected
Read	1	Screen touch detected
Write	0	Converter functions initiated and/or controlled by host
Write	1	Converter functions initiated and controlled by the TSC2005

STS—A/D converter status. When reading, this bit indicates if the converter is busy or not busy. Continuous scans or conversions can be stopped by writing a '1' to this bit, immediately halting the running converter function (even if the pen is still down) and causing the A/D converter to power down. The default state for write is 0 (normal operation), and the default state for read is 1 (converter is not busy). **NOTE:** The same bit can be written through Control Byte 1.

Table 13. STS Bit Operation

OPERATION	VALUE	DESCRIPTION
Read	0	Converter is busy
Read	1	Converter is not busy
Write	0	Normal operation
Write	1	Stop converter function and power down

RM—Resolution control. The A/D converter resolution is specified with this bit. See Table 14 for a description of these bits. This bit is the same whether reading or writing, and defaults to 0. Note that the same bit can be written through Control Byte 1.

Table 14. A/D Converter Resolution Control

RM	FUNCTION
0	10-bit resolution. Power-up and reset default.
1	12-bit resolution

CL1, CL0—Conversion clock control. These two bits specify the clock rate that the A/D converter uses to perform conversion, as shown in Table 15. These bits are the same whether reading or writing.

Table 15. A/D Converter Conversion Clock Control

CL1	CL0	FUNCTION
0	0	$f_{ADC} = f_{OSC}/1$. This is referred to as the 4MHz A/D converter clock rate, 10-bit resolution only.
0	1	$f_{ADC} = f_{OSC}/2$. This is referred to as the 2MHz A/D converter clock rate.
1	0	$f_{ADC} = f_{OSC}/4$. This is referred to as the 1MHz A/D converter clock rate.
1	1	Reserved

PV2-PV0—Panel voltage stabilization time control. These bits specify a delay time from the moment the touch screen drivers are enabled to the time the voltage is sampled and a conversion is started. These bits allow the user to adjust the appropriate settling time for the touch panel and external capacitances. See Table 16 for settings of these bits. The default state is 000, indicating a 0µs stabilization time. These bits are the same whether reading or writing.

Table 16. Panel Voltage Stabilization Time Control

PV2	PV1	PV0	STABILIZATION TIME (t_{PVS})
0	0	0	0µs
0	0	1	100µs
0	1	0	500µs
0	1	1	1ms
1	0	0	5ms
1	0	1	10ms
1	1	0	50ms
1	1	1	100ms

PR2-PR0—Precharge time selection. These bits set the amount of time allowed for precharging any pin capacitance on the touch screen prior to sensing if a pen touch is happening.

Table 17. Precharge Time Selection

PR2	PR1	PR0	PRECHARGE TIME(t_{PRE})
0	0	0	20µs
0	0	1	84µs
0	1	0	276µs
0	1	1	340µs
1	0	0	1.044ms
1	0	1	1.108ms
1	1	0	1.300ms
1	1	1	1.364ms

SNS2-SNS0—Sense time selection. These bits set the amount of time the TSC2005 waits to sense whether the screen is touched after converting a coordinate.

Table 18. Sense Time Selection

SNS2	SNS1	SNS0	SENSE TIME (t_{SNS})
0	0	0	32µs
0	0	1	96µs
0	1	0	544µs
0	1	1	608µs
1	0	0	2.080ms
1	0	1	2.144ms
1	1	0	2.592ms
1	1	1	2.656ms

DTW—Detection of pen touch in wait. Writing a '1' to this bit enables the pen touch detection in background while waiting for the host to issue the converter function in host-initiated/controlled modes. This detection in background allows the TSC2005 to pull high at $\overline{\text{PINTDAV}}$ to indicate no pen touch detected while waiting for the host to issue the converter function. If the host polls a high state at $\overline{\text{PINTDAV}}$ before the convert function is sent, the host can abort the issuance of the convert function and stay in the polling $\overline{\text{PINTDAV}}$ mode until the next pen touch is detected.

LSM—Longer sampling mode. When this bit is set to '1', the extra 500ns of sampling time is added to the normal sampling cycles of each conversion. This additional time is represented as approximatly two A/D converter clock cycles set by CL1-CL0.

Configuration Register 1

Configuration register 1 (CFR1) defines the connection test-bit modes configuration and the batch delay selection.

Table 19. Configuration Register 1 (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
Resrvd	Resrvd	Resrvd	Resrvd	TBM3	TBM2	TBM1	TBM0	Resrvd	Resrvd	Resrvd	Resrvd	Resrvd	BTD2	BTD1	BTD0

TBM3-TBM0—Connection test-bit modes. These bits specify the mode of test bits used for the predefined range of touch screen panel resistance.

Table 20. Touch Screen Resistance Range and Test-Bit Modes

TEST-BIT MODES				R_{TS} (kΩ)
TBM3	TBM2	TBM1	TBM0	
0	0	0	0	0.17
0	0	0	1	$0.17 < R_{TS} \le 0.52$
0	0	1	0	$0.52 < R_{TS} \le 0.86$
0	0	1	1	$0.86 < R_{TS} \le 1.6$
0	1	0	0	$1.6 < R_{TS} \le 2.2$
0	1	0	1	$2.2 < R_{TS} \le 3.6$
0	1	1	0	$3.6 < R_{TS} \le 5.0$
0	1	1	1	$5.0 < R_{TS} \le 7.8$
1	0	0	0	$7.8 < R_{TS} \le 10.5$
1	0	0	1	$10.5 < R_{TS} \le 16.0$
1	0	1	0	$16.0 < R_{TS} \le 21.6$
1	0	1	1	$21.6 < R_{TS} \le 32.6$
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Only for short-circuit panel test

BTD2-BTD0—Batch delay modes. These bits specify the selection of the batch delays that are triggered when a TSC-initiated scan (XYZ or XY) begins corresponding to a pen touch. After the first processed sample set completes during the batch delay, the scan enters a wait mode until the end of the batch delay is reached. If a pen touch is still detected at that moment, the scan continues to process the next sample set, and the batch delay is resumed. The throughput of the processed sample sets (shown in Table 21 as sample sets per second, or SSPS) is regulated by the selected batch delay during the time of the detected pen touch. A TSC-initiated scan (XYZ or XY) takes effect by setting the PSM bit to '1' in CFR0 and C[3:0] to '0000' or '0001' in Control Byte 1. The batch delay select bits are shown in Table 21. Note that the throughput of the processed sample set also depends on the setting of stabilization time, precharge time, sense time, and the total number of samples to be processed per coordinates. If the accrual time of these factors exceeds the batch delay time, the accrual time dominates. Batch delay time starts when the pen touch initiates the scan function that converts coordinates.

Table 21. Touch Screen Throughput and Batch Selection Bits

BATCH DELAY SELECTION			DELAY TIME (ms)	THROUGHPUT for TSC-INITIATED SCAN XYZ or XY (SSPS)
BTD2	BTD1	BTD0		
0	0	0	0	Normal operation throughput depends on settings.
0	0	1	1	1000
0	1	0	2	500
0	1	1	4	250
1	0	0	10	100
1	0	1	20	50
1	1	0	40	25
1	1	1	100	10

For example, if stabilization time, precharge time, and sense time are selected as 100µs, 84µs, and 96µs, respectively, and the batch delay time is 2ms, then the scan function enters wait mode after the first processed sample set until the 2ms of batch delay time is reached. When the scan function starts to process the second sample set (if the screen is still touched), the batch delay restarts at 2ms (in this example). This procedure remains regulated by 2ms until the pen touch is not detected or the scan function is stopped by a stop bit or any reset form.

Configuration Register 2

Configuration register 2 (CFR2) defines the preprocessor configuration.

Table 22. Configuration Register 2 (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
PINTS1	PINTS0	M1	M0	W1	W0	TZ1	TZ0	AZ1	AZ0	Resrvd	MAVE X	MAVE Y	MAVE Z	MAVE AUX	MAVE TEMP

PINTS1 (default 0)—This bit controls the output format of the $\overline{\text{PINTDAV}}$ pin. When this bit is set to '0', the output format is shown as the AND-form of internal signals of $\overline{\text{PENIRQ}}$ and DAV). When this bit is set to '1', $\overline{\text{PINTDAV}}$ outputs $\overline{\text{PENIRQ}}$ only.

PINTS0 (default 0)—This bit selects what is output on the $\overline{\text{PINTDAV}}$ pin. If this bit set to '0', the output format of $\overline{\text{PINTDAV}}$ depends on the selection made on the PINTS1 bit. If this bit set to '1', the internal signal of $\overline{\text{DAV}}$ is output on $\overline{\text{PINTDAV}}$.

Table 23. PINTSx Selection

PINTS1	PINTS0	$\overline{\text{PINTDAV}}$ PIN OUTPUT =
0	0	An AND combination of $\overline{\text{PENIRQ}}$ (active low) and DAV (active high).
0	1	A delayed data_ava, $\overline{\text{DAV}}$ (active low).
1	0	An interrupt, $\overline{\text{PENIRQ}}$ (active low) generated by pen-touch.
1	1	A delayed data_ava, $\overline{\text{DAV}}$ (active low).

M1, M0, W1, W0 (default 0000)—Preprocessing MAV filter control. Note that when the MAV filter is processing data, the STS bit and the corresponding DAV bits in the status register will indicate that the converter is busy until all conversions necessary for the preprocessing are complete. The default state for these bits is 0000, which bypasses the preprocessor. These bits are the same whether reading or writing.

TZ1 and TZ0, or AZ1 and AZ0 (default 00)—Zone detection bit definition (for TEMP or AUX measurements). TZ1 and TZ0 are for the TEMP measurement. AZ1 and AZ0 are for the AUX measurement. The action taken in zone detection is to store the processed data in the corresponding data registers and to update the corresponding DAV bits in status register. If the processed data do not meet the selected criteria, these data are ignored and the corresponding DAV bits are not updated. When zone detection is disabled, the processed data are simply stored in the corresponding data registers and the corresponding DAV bits are updated without any comparison of criteria. Note that the converted samples are always processed according to the setting of the MAVE bits for AUX/TEMP before zone detection takes effect. SeeTable 30 for thresholds.

Table 24. Zone Detection Bit Definition

TZ1/AZ1	TZ0/AZ0	FUNCTION
0	0	Zone detection is disabled.
0	1	When the processed data is below low threshold
1	0	When the processed data is between low and high thresholds
1	1	When the processed data is above high threshold

MAVE (default is 00000)—MAV filter function enable bit. When the corresponding bit is set to 1, the MAV filter setup is applied to the corresponding measurement.

Converter Function Select Register

The Converter Function Select (CFN) register reflects the converter function select status.

Table 25. Converter Function Select Status Register (Reset Value = 0000h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
CFN15	CFN14	CFN13	CFN12	CFN11	CFN10	CFN9	CFN8	CFN7	CFN6	CFN5	CFN4	CFN3	CFN2	CFN1	CFN0

CFN15-CFN0—Converter function select status. These bits represent the current running converter function that is set in bits C3-C0 of Control Byte 1. These bits are decoded hexidecimal values of converter function select bits C3-C0. The CFNx bit is the corresponding bit for the hex value of each combination of the converter function select bits C3-C0. The CFNx bit is set to '1' if C3-C0 = *x*, where x is the decimal value of converter function select bits C3-C0. In other words, when CFN0 shows '1', it indicates the converter function of setting C3-C0 = 0000 is running. These bits are reset to 0000h whenever the converter function is complete, stopped by STS bit, or reset by the hardware reset from the $\overline{\text{RESET}}$ pin or the software reset from SWRST bit in Control Byte 1. However, if the TSC-initiated scan function mode is issued by setting the PSM bit in the CFR0 register to '1', these bits will not be reset when the converter function is complete because there is no detection of pen touch. This allows the TSC2005 to initiate the scan process immediately when the next pen touch is detected. Bits CFN15-CFN13 reflect the functions being activated; these bits may not be practical to read because they change frequently.

Table 26. STATUS Register (Reset Value = 0004h)

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
DAV Due X	DAV Due Y	DAV Due Z1	DAV Due Z2	DAV Due AUX	DAV Due TEMP1	DAV Due TEMP2	RESRVD (read '0')	RESET Flag	X CON	Y CON	RESRVD (read '0')	Y SHR	PDST	ID1	ID0

DAV Bits—Data available bits. These seven bits mirror the operation of the internal signals of DAV. When any processed data are stored in data registers, the corresponding DAV bit is set to '1'. It stays at '1' until the register(s) updated to the processed data have been read out by the host.

Table 27. DAV Function

DAV	DESCRIPTION
0	No new processed data are available.
1	Processed data are available. This will stay at 1 until the host has read out all updated registers.

RESET Flag—See Table 28 for the interpretation of the RESET flag bits.

Table 28. RESET Flag Bits

RESET Flag	DESCRIPTION
0	Device was reset since last status poll (hardware or software reset).
1	Device has not been reset since last status poll.

X CON—This bit is '1' if the X axis of the touch screen panel is properly connected to the X drivers. This bit is the connection test result.

Y CON—This bit is '1' if the Y axis of the touch screen panel is properly connected to the Y drivers. This bit is the connection test result.

Y SHR—This bit is '1' if there is no short-circuit tested at the Y axis of the touch screen panel. This bit is the short-circuit test result.

PDST—Power down status. This bit reflects the setting of the PND0 bit in Control Byte 0. When this bit shows '0', it indicates ADC bias circuitry is still powered on after each conversion and before the next sampling; otherwise, it indicates ADC bias circuitry is powered down after each conversion and before the next sampling. However, it is powered down between conversion sets. Because this status bit is synchronized with the internal clock, it does not reflect the setting of the PND0 bit until a pen touch is detected or a converter function is running.

ID[1:0] Device ID bits: These bits represent the version ID of TSC2005. This version defaults to '00'.

DATA REGISTERS

The data registers of the TSC2005 hold data results from conversions. All of these registers default to 0000h upon reset.

X, Y, Z1, Z2, AUX, TEMP1 and TEMP2 REGISTERS

The results of all A/D conversions are placed in the appropriate data registers, as described in Table 10. The data format of the result word (R) of these registers is right-justified, as shown in Table 29:

Table 29. Internal Register Format

MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

Register Map

The TSC2005 has several 16-bit registers that allow control of the device, as well as providing a location to store results from the TSC2005 until read out by the host microprocessor. Table 30 shows the memory map.

Table 30. Register Content and Reset Values(1)

A3-A0 (HEX)	REGISTER NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	RESET VALUE (HEX)
0	X	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
1	Y	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
2	Z1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
3	Z2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
4	AUX	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
5	Temp1	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
6	Temp2	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
7	Status	S15	S14	S13	S12	S11	S10	S9	0	S7	S6	S5	Rsvd (2)	S3	S2	S1	S0	0004
8	AUX High	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0FFF
9	AUX Low	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
A	Temp High	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0FFF
B	Temp Low	0	0	0	0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000
C	CFR0	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	4000
D	CFR1	0	0	0	0	R11	R10	R9	R8	0	0	0	0	0	R2	R1	R0	0000
E	CFR2	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	0	R4	R3	R2	R1	R0	0000
F	Converter Function Select Status	R15	R14	R13	R12	Rsvd (2)	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	0000

(1) For all combination bits, the pattern marked as reserved must not be used. The default pattern is read back after reset.
(2) This bit is reserved.

REGISTER RESET

There are three way to reset the TSC2005. First, at power-on, a power good signal will generate a prolonged reset pulse internally to all registers.

Second, an external pin, $\overline{\text{RESET}}$, is available to perform a system reset or allow other peripherals (such as a display) to reset the device if the pulse meets the timing requirement (at least 10µs wide). Any $\overline{\text{RESET}}$ pulse less than 5µs will be rejected. To accommodate the timing drift between devices because of process variation, a $\overline{\text{RESET}}$ pulse width between 5µs to 10µs falls into the gray area that will not be recognized and the result is undetermined; this situation should be avoided. Refer to Figure 30 for details. A good reset pulse must be low for at least 10µs. There is an internal spike filter to reject spikes up to 20ns wide.

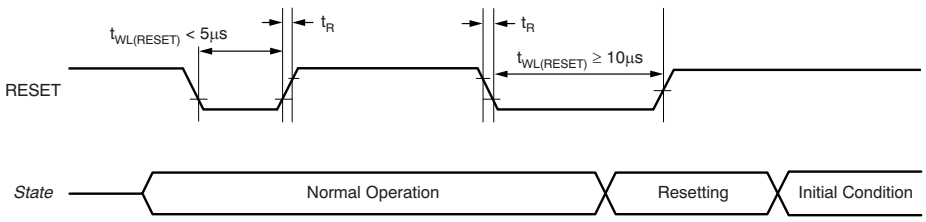


Figure 30. External Reset Timing

Finally, a software reset can be activated by writing a '1' to CB1.1 (bit 1 of control byte 1). It should be noted this reset is not self-cleared, so the user must write a '0' to remove the software reset.

A reset clears all registers and loads default values. A power-on reset and external (hardware) reset take precedence over a software reset. If a software reset not cleared by the user, it will be cleared by either a power-on reset or an external (hardware) reset.

OPERATION

TOUCH SCREEN MEASUREMENTS

As noted previously in the discussion of the A/D converter, several operating modes can be used that allow great flexibility for the host processor. This section examines these different modes.

Conversion Controlled by TSC2005 Initiated by TSC2005 (TSMode 1)

In TSMode 1, before a pen touch can be detected, the TSC2005 must be programmed with PSM = 1 and one of two scan modes:

1. X-Y-Z Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0000); or
2. X-Y Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0001).

See Table 7 for more information on the converter function select bits.

When the touch panel is touched, which causes the internal pen-touch signal to activate, this lowers the $\overline{\text{PINTDAV}}$ output if it is programmed as $\overline{\text{PENIRQ}}$. The TSC2005 will then execute the preprogrammed scan function without a host intervention.

At the same time, the TSC2005 starts up its internal clock. It then turns on the Y-drivers, and after a programmed panel voltage stabilization time, powers up the A/D converter and converts the Y coordinate. If preprocessing is selected, several conversions may take place. When data preprocessing is complete, the Y coordinate result is stored in a temporary register.

If the screen is still touched at this time, the X-drivers are enabled, and the process repeats, but measuring the X coordinate instead, and storing the result in a temporary register.

If only X and Y coordinates are to be measured, then the conversion process is complete. A set of X and Y coordinates are stored in the X and Y registers. Figure 31 shows a flowchart for this process. The time it takes to go through this process depends upon the selected resolution, internal conversion clock rate, panel voltage stabilization time, precharge and sense times, and whether preprocessing is selected. The time needed to get a complete X and Y coordinate (sample set) reading can be calculated by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + 2 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 2 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (5)$$

Where:

$t_{COORDINATE}$ = time to complete X/Y coordinate reading.
t_{PVS} = panel voltage stabilization time, as given in Table 16.
t_{PRE} = precharge time, as given in Table 17.
t_{SNS} = sense time, as given in Table 18.
N = number of measurements for MAV filter input, as given in Table 3 as N.
(For no MAV: M1-0[1:0] = '00', W1-0[1:0] = '00', N = 1.)
B = number of bits of resolution.
f_{OSC} = TSC onboard OSC clock frequency. See Electrical Characteristics for supply frequency (SNSVDD).
f_{ADC} = A/D converter clock frequency, as given in Table 15.
OH1 = overhead time #1 = 2.5 internal clock cycles.
OH_{DLY1} = total overhead time for t_{PVS}, t_{PRE}, and t_{SNS} = 10 internal clock cycles.
OH_{CONV} = total overhead time for A/D conversion = 3 internal clock cycles.
L_{PPRO} = pre-processor preocessing time as given in Table 31.

OPERATION (continued)

Table 31. Preprocessing Delay

M =	W =	L_{PPRO} =	
		FOR B = 12 BIT	FOR B = 10 BIT
1	1, 4, 8, 16	2	2
3, 7	1	28	24
7	3	31	27
15	1	31	29
15	3	34	32
15	7	38	36

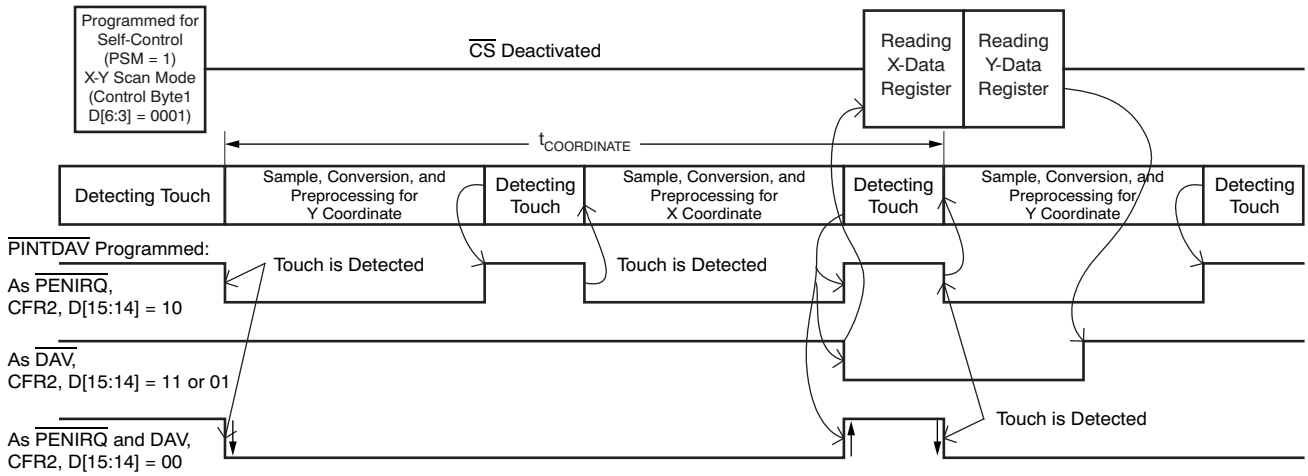


Figure 31. X and Y Coordinate Touch Screen Scan using TSMode 1

If the pressure of the touch is also to be measured, the process continues in the same way, but measuring the Z_1 and Z_2 values instead, and storing the results in temporary registers. Once the complete sample set of data (X, Y, Z_1, and Z_2) are available, they are loaded in the X, Y, Z_1, and Z_2 registers. This process is illustrated in Figure 32. As before, this process time depends upon the settings described above. The time for a complete X, Y, Z_1, and Z_2 coordinate reading is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + 3 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 4 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (6)$$

Where:

OH2 = overhead time #2 = 3.5 internal clock cycles.

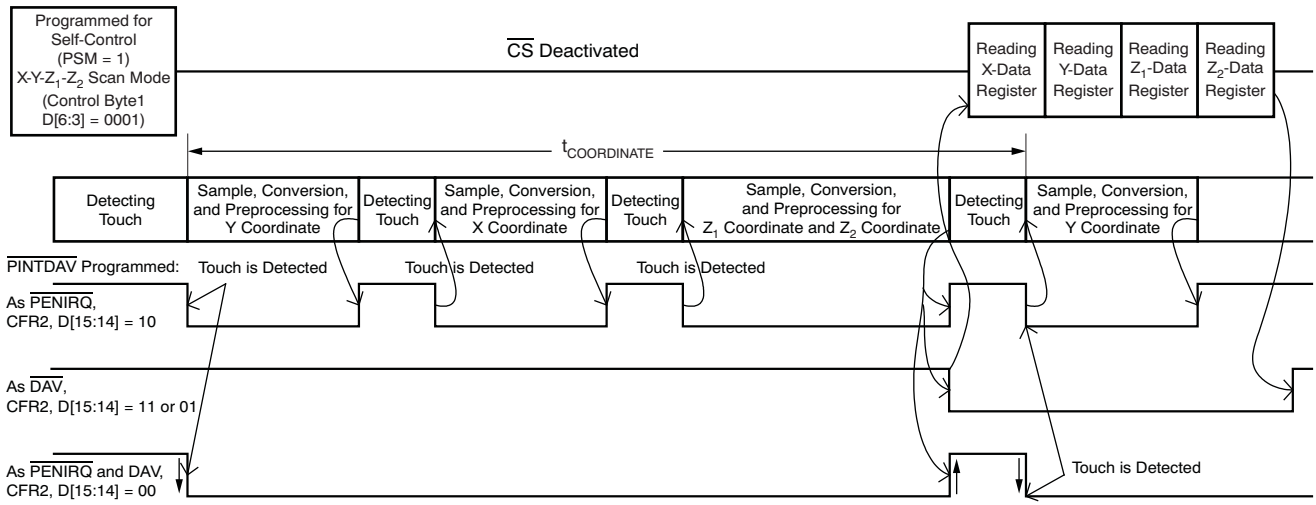


Figure 32. X, Y, and Z Coordinate Touch Screen Scan using TSMode 1

Conversion Controlled by TSC2005 Initiated by Host (TSMode 2)

In TSMode 2, the TSC2005 detects when the touch panel is touched and causes the internal Pen-Touch signal to activate, which lowers the $\overline{\text{PINTDAV}}$ output, if it is programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request, and then writes to the A/D Converter Control register to select one of the two touch screen scan functions:

1. X-Y-Z Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0000); or
2. X-Y Scan (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0001).

See Table 7 for more information on the converter function select bits.

The conversion process then proceeds as described previously.

The main difference between this mode and the previous mode is that the host, not the TSC2005, decides when the touch screen scan begins.

The time needed to convert both X and Y coordinates under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + 2 \cdot \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}} \right) + 2 \cdot \left(N \cdot \left((B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \right) \quad (7)$$

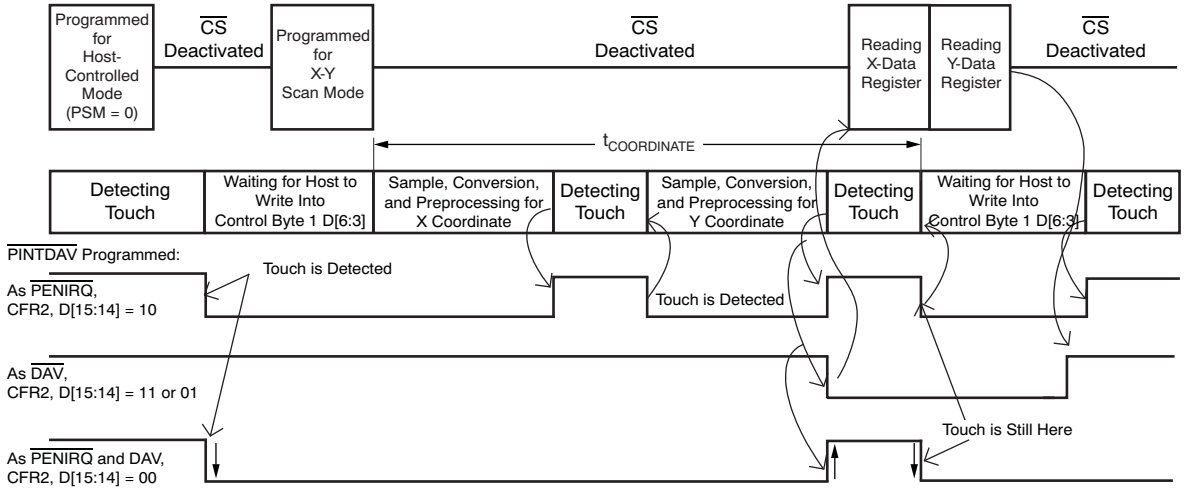


Figure 33. Example of an X and Y Coordinate Touch Screen Scan using TSMode 2

Conversion Controlled by Host (TSMode 3)

In TSMode 3, the TSC2005 detects when the touch panel is touched and causes the internal Pen-Touch signal to be active, which lowers the $\overline{\text{PINTDAV}}$ output, if it is programmed as $\overline{\text{PENIRQ}}$. The host recognizes the interrupt request. Instead of starting a sequence in the TSC2005, which then reads each coordinate in turn, the host must now control all aspects of the conversion. Generally, upon receiving the interrupt request, the host turns on the X drivers. (**NOTE:** If drivers are not turned on, the device detects this condition and turns them on before the scan starts. This situation is why the event of *turn on drivers* is shown as optional in Figure 34 and Figure 35.) After waiting for the settling time, the host then addresses the TSC2005 again, this time requesting an X coordinate conversion.

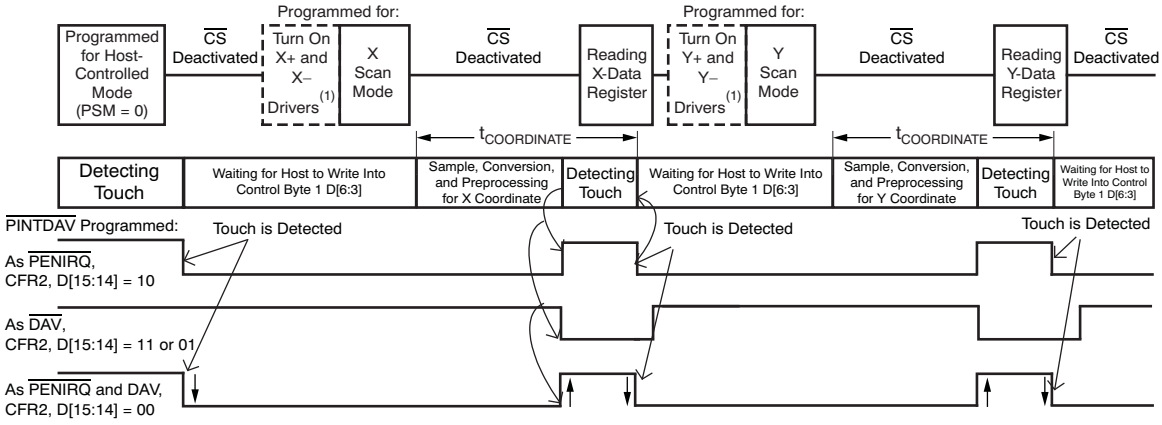
The process is then repeated for the Y and Z coordinates. The processes are outlined in Figure 34 and Figure 35. Figure 34 shows two consecutive scans on X and Y. Figure 35 shows a single Z scan.

The time needed to convert any single coordinate X or Y under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + \left(t_{PRE} + t_{SNS} + \frac{OH_{DLY2}}{f_{OSC}}\right) + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (8)$$

Where:

OH_{DLY2} = total overhead time for t_{PRE} and t_{SNS} = 6 internal clock cycles.

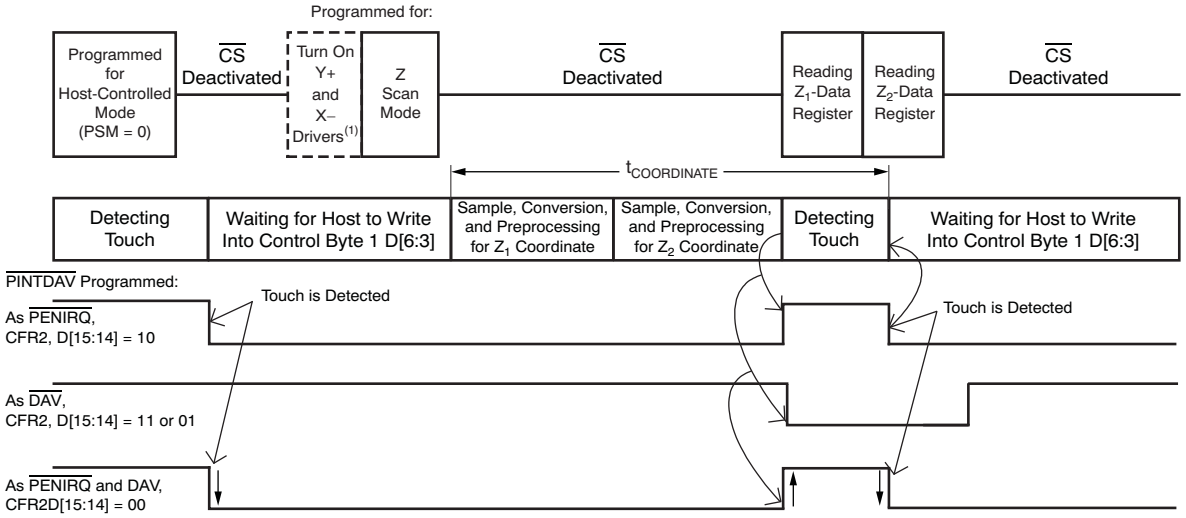


NOTE: (1) Optional. If not turned on, it will be turned on by the Scan mode, once detected.

Figure 34. Example of X and Y Coordinate Touch Screen Scan using TSMode 3

The time needed to convert any Z_1 and Z_2 coordinate under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + \left(t_{PRE} + t_{SNS} + \frac{OH_{DLY2}}{f_{OSC}}\right) + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (9)$$



NOTE: (1) Optional. If not turned on, it will be turned on by the Scan mode, once detected.

Figure 35. Example of Z_1 and Z_2 Coordinate Touch Screen Scan (without Panel Stabilization Time) using TSMode 3

The time needed to convert the Z_1 and Z_2 coordinates under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{COORDINATE} = \frac{OH2}{f_{OSC}} + \left(t_{PVS} + t_{PRE} + t_{SNS}\frac{OH_{DLY1}}{f_{OSC}}\right) + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (10)$$

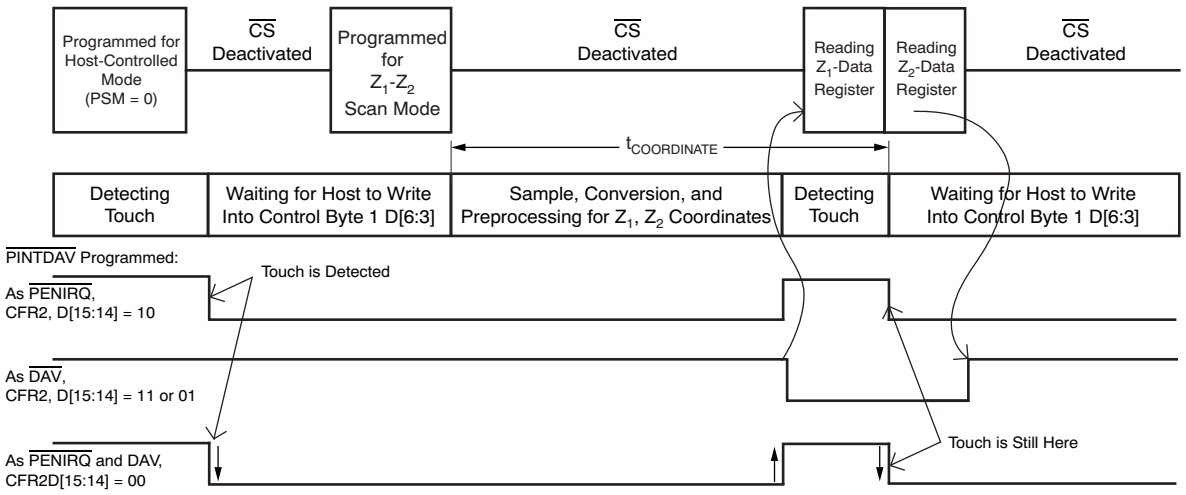


Figure 36. Example of a Z_1 and Z_2 Coordinate Touch Screen Scan (with Panel Stabilization Time) using TSMode 3

The time needed to convert any single coordinate (either X or Y) under host control (not including the time needed to send the command over the SPI bus) is given by:

$$t_{COORDINATE} = \frac{OH1}{f_{OSC}} + \left(t_{PVS} + t_{PRE} + t_{SNS} + \frac{OH_{DLY1}}{f_{OSC}}\right) + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV}\right) \cdot \left(\frac{1}{f_{OSC}}\right) + \left(\frac{L_{PPRO}}{f_{OSC}}\right) \quad (11)$$

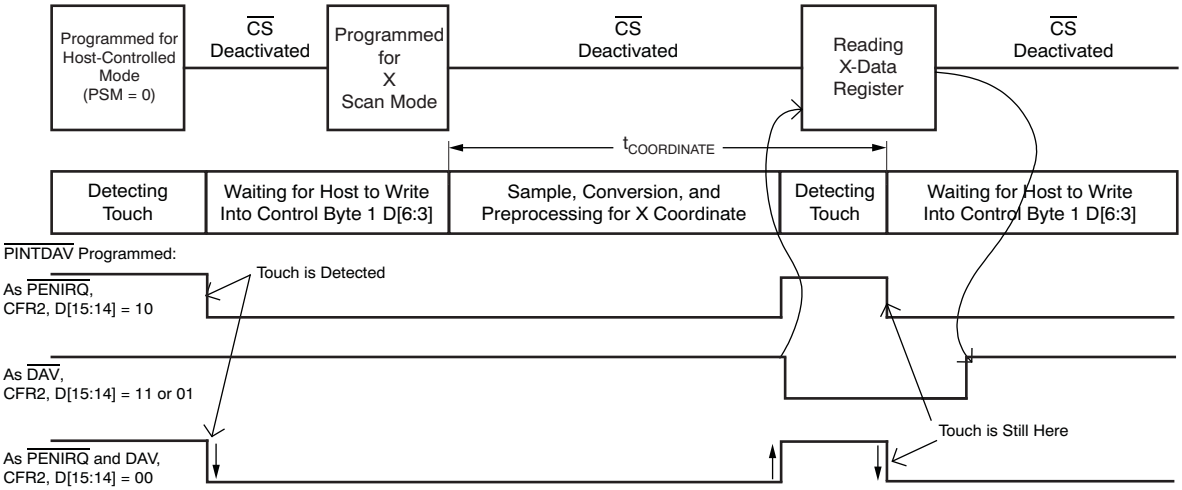


Figure 37. Example of a Single X Coordinate Touch Screen Scan (with Panel Stabilization Time) using TSMode 3

AUXILIARY AND TEMPERATURE MEASUREMENT

The TSC2005 can measure the voltage from the auxiliary input (AUX) and from the internal temperature sensor. Applications for the AUX can include external temperature sensing, ambient light monitoring for controlling backlighting, or sensing the current drawn from batteries. There are two converter functions that can be used for the measurement of the AUX:

1. Non-continuous AUX measurement shown in Figure 38 (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0101); or
2. Continuous AUX Measurement shown in Figure 39 (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 1000).

See Table 7 for more information on the converter function select bits.

There are also two converter functions for the measurement of the internal temperature sensor:

1. TEMP1 measurement (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0110); or
2. TEMP2 measurement (converter function select bits C[3:0] = Control Byte 1 D[6:3] = 0111).

See Table 7 for more information on the converter function select bits.

For the detailed calculation of the internal temperature sensor, please see the SubSec1 9.3 section. These two converter functions have the same timing as the non-continuous AUX measurement operation as shown in Figure 38; therefore, Equation 12 can also be used for internal temperature sensor measurement. The time needed to make a non-continuous auxiliary measurement or an internal temperature sensor measurement is given by:

$$t_{COORDINATE} = \frac{OH3}{f_{OSC}} + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \quad (12)$$

Where:

OH3 = overhead time #3 = 3.5 internal clock cycles.

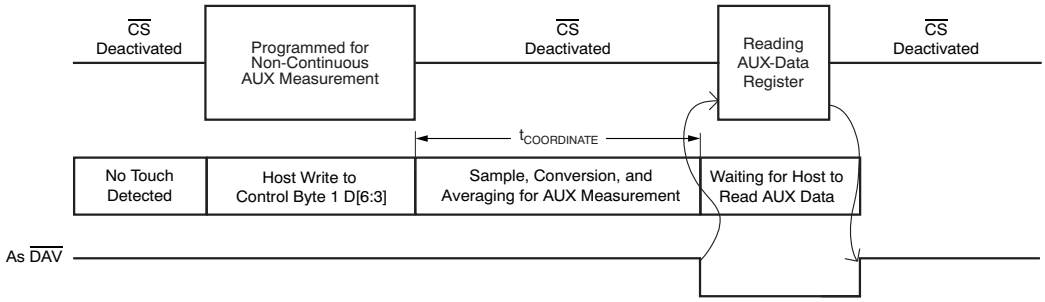


Figure 38. Non-Touch Screen, Non-Continuous AUX Measurement

The time needed to make continuous auxiliary measurement is given by:

$$t_{COORDINATE} = \frac{OH3}{f_{OSC}} + \left(N \cdot (B+2) \cdot \frac{f_{OSC}}{f_{ADC}} + OH_{CONV} \right) \cdot \left(\frac{1}{f_{OSC}} \right) + \left(\frac{L_{PPRO}}{f_{OSC}} \right) \quad (13)$$

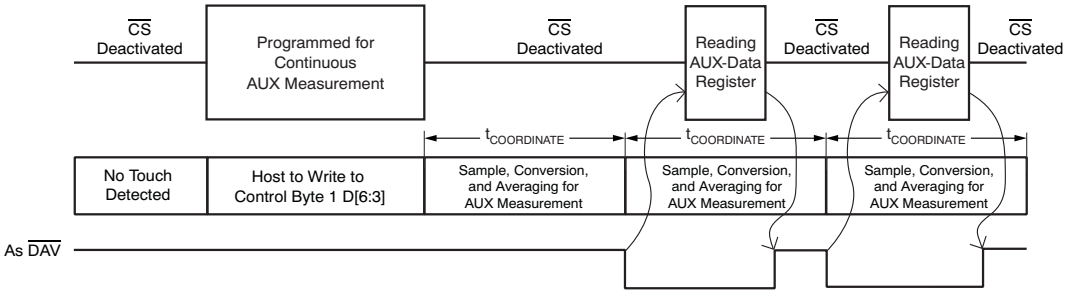


Figure 39. Non-Touch Screen, Continuous AUX Measurement

LAYOUT

The following layout suggestions should obtain optimum performance from the TSC2005. However, many portable applications have conflicting requirements concerning power, cost, size, and weight. In general, most portable devices have fairly clean power and grounds because most of the internal components are very low power. This situation would mean less bypassing for the converter power and less concern regarding grounding. Still, each situation is unique and the following suggestions should be reviewed carefully.

For optimum performance, care should be taken with the physical layout of the TSC2005 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the SCLK input.

With this in mind, power to the TSC2005 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be added between (SNSVDD to AGND and SNSGND) or (I/OVDD to DGND). A 0.1µF decoupling capacitor between VREF to AGND is also needed unless the SNSVDD is used as a reference input and is connected to VREF. These capacitors need to be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between SNSVDD and the power supply is high. The I/OVDD needs to be shorted to the same supply plane as the SNSVDD. Short both SNSVDD and I/OVDD to the analog VDD plane.

The TSC2005 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input, which is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove. Some package options have pins labeled as VOID. Avoid any active trace going under those pins marked as VOID unless they are shielded by a ground or power plane.

All GND (AGND, DGND, SUBGND and SNSGND) pins should be connected to a clean ground point. In many cases, this point will be the analog ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry or battery connection point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

In the specific case of use with a resistive touch screen, care should be taken with the connection between the converter and the touch screen. Since resistive touch screens have fairly low resistance, the interconnection should be as short and robust as possible. Loose connections can be a source of error when the contact resistance changes with flexing or vibrations.

As indicated previously, noise can be a major source of error in touch-screen applications (for example, applications that require a back-lit LCD panel). This electromagnetic interfence (EMI) noise can be coupled through the LCD panel to the touch screen and cause flickering of the converted ADC data. Several things can be done to reduce this error, such as using a touch screen with a bottom-side metal layer connected to ground, which will couple the majority of noise to ground. Additionally, filtering capacitors, from Y+, Y–, X+, and X– to ground, can also help. Note, however, that the use of these capacitors increases screen settling time and requires longer panel voltage stabilization times, and also increases precharge and sense times for the $\overline{\text{PINTADV}}$ circuitry of the TSC2005. The resistor value varies depending on the touch screen sensor used. The internal 51kΩ resistor (R_{IRQ}) may be adequate for most of sensors.

PACKAGE OPTION ADDENDUM

25-Dec-2006

PACKAGING INFORMATION

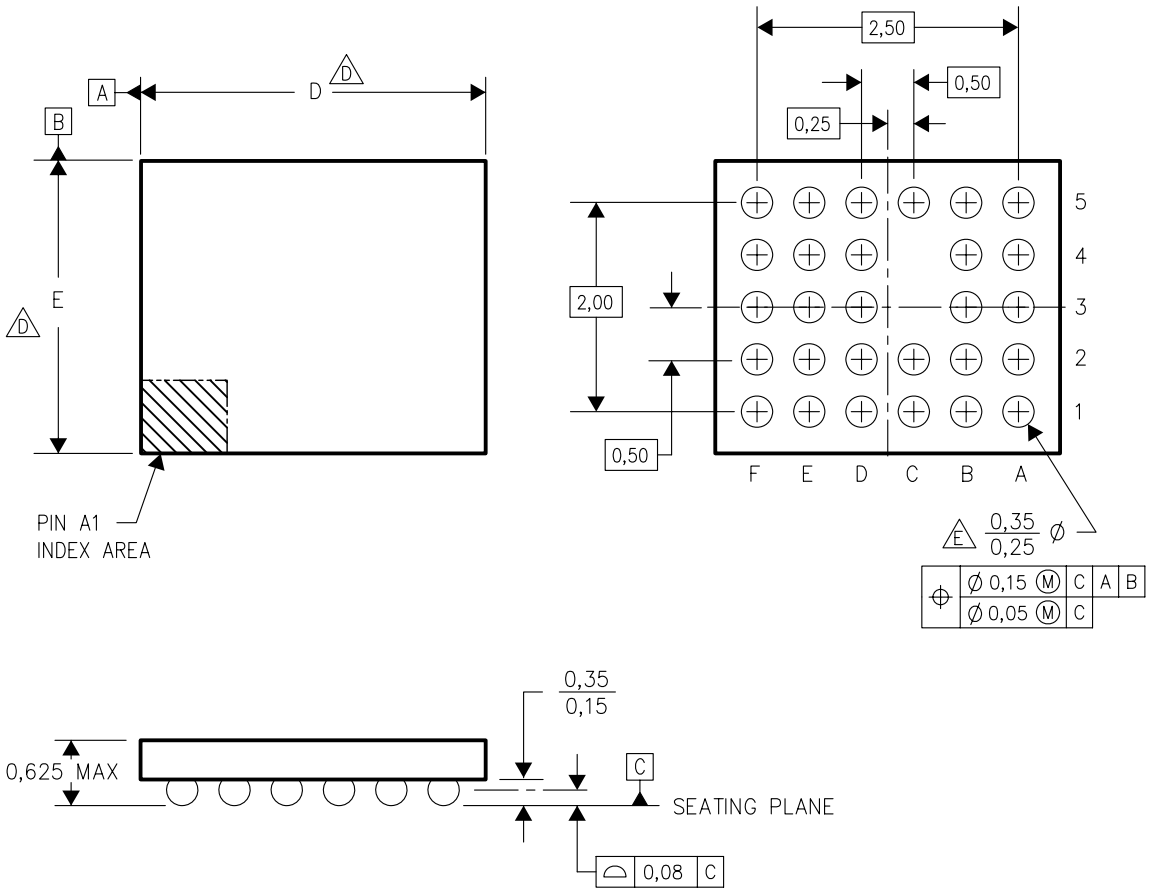
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TSC2005IYZLR	ACTIVE	DSBGA	YZL	28	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TSC2005IYZLT	ACTIVE	DSBGA	YZL	28	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

YZL (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY



4205063–2/D 01/07

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZL package can have dimension D ranging from 2.85 to 3.65 mm and dimension E ranging from 2.35 to 3.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 6 x 5 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEL (Drawing #4204186) for tin–lead (SnPb) balls.

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