TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM2N7000

60V N-Channel MOSFET

SOT-92

Pin Definition:
1. Gate
2. Source
3. Drain

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(Ω)	I_D (mA)
60	5 @ V_{GS} = 10V	500

Features

- Fast Switching Speed
- Low Input and Output Leakage

Application

- Direct Logic-Level Interface: TTL/CMOS
- Solid-State Relays

Block Diagram

N-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM2N7000CT B0	TO-92	1Kpcs / Bulk
TSM2N7000CT A3	TO-92	2Kpcs / Ammo

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current		I_D	200	mA
Pulsed Drain Current		I_{DM}	500	mA
Continuous Source Current (Diode Conduction)[a,b]		I_S	500	mA
Maximum Power Dissipation	Ta = 25°C	P_D	350	mW
	Ta = 75°C		280	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	357	°C/W

Notes:
a. Pulse width limited by the Maximum junction temperature
b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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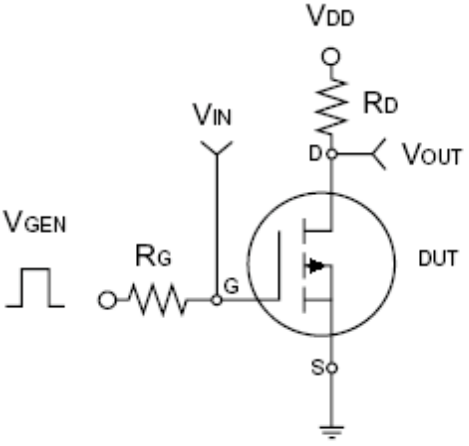
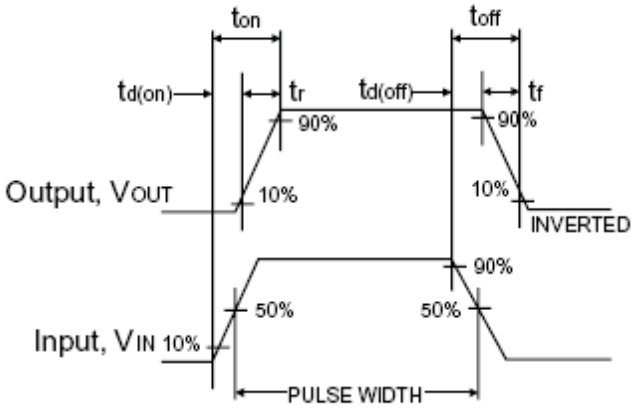
Electrical Specifications (Ta = 25°C, unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 10μA	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	$V_{GS(TH)}$	0.8	--	3.0	V
Gate Body Leakage	V_{GS} = ±15V, V_{DS} = 0V	I_{GSS}	--	--	±10	nA
Zero Gate Voltage Drain Current	V_{DS} = 48V, V_{GS} = 0V	I_{DSS}	--	--	1.0	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 500mA	$R_{DS(ON)}$	--	--	5.0	Ω
	V_{GS} = 5V, I_D = 50mA		--	7.5	--	
Forward Transconductance	V_{DS} = 15V, I_D = 300mA	g_{fs}	--	320	--	mS
Diode Forward Voltage	I_S = 200mA, V_{GS} = 0V	V_{SD}	--	1.3	1.5	V
Dynamic[b]						
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	60	--	pF
Output Capacitance		C_{oss}	--	25	--	
Reverse Transfer Capacitance		C_{rss}	--	5	--	
Switching[c]						
Turn-On Rise Time	V_{DD} = 15V, R_L = 30Ω, I_D = 500mA, V_{GEN} = 10V, R_G = 25Ω	t_r	--	10	--	nS
Turn-Off Fall Time		t_f	--	10	--	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



Switching Test Circuit



Switchin Waveforms

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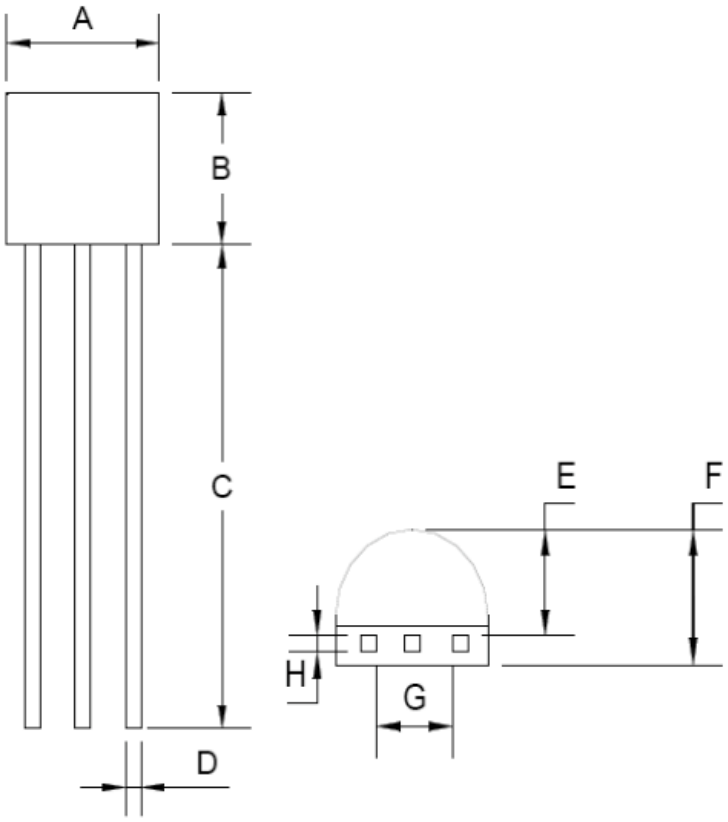
TO-92 Mechanical Drawing



TO-92 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.70	0.169	0.185
B	4.30	4.70	0.169	0.185
C	14.30(typ)		0.563(typ)	
D	0.43	0.49	0.017	0.019
E	2.19	2.81	0.086	0.111
F	3.30	3.70	0.130	0.146
G	2.42	2.66	0.095	0.105
H	0.37	0.43	0.015	0.017

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