查询TSSOP供应商

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TSSOP and **MSOP**

Small Outline Packages

- Wide range of body sizes
- 8 to 56 lead counts
- Thermally enhanced versions available (TSSOP-ep and MSOP-ep)



FEATURES

TSSOP

- Body Size: 3.0 x 4.4mm to 14.0 x 6.1mm
- Lead Count: 8L to 56L
- Lead Pitch: 0.50mm & 0.65mm
- Package Height: 1.20mm max.
- JEDEC standard compliant (MO-153)
- Lead-free (Pb-free) and Green
- Thermal Enhancements: ep (exposed pad)

MSOP

- Body Size: 3 x 3mm
- Lead Count: 8L & 10L
- Lead Pitch: 0.65mm (8L) and 0.50mm (10L)
- JEDEC standard compliant
- Lead-free (Pb-free) and Green
- Thermal enhancements: ep (exposed pad)

APPLICATIONS

- Analog and Operation Amplifiers
- Controllers and Drivers
- Logic, Memory, and RF/Wireless
- Disk drives, video/audio and consumer electronics/ appliances

DESCRIPTION

STATS ChipPAC offers a complete line of Small Outline Package (SOP) families including TSSOP, TSSOP-ep, and MSOP. STATS ChipPAC's TSSOP (Thin Shrink Small Outline Package) is suitable for applications requiring a thin profile. TSSOP is a leadframe based, plastic encapsulated package with gull wing shaped leads on two sides with lead count ranging from 8 to 56 leads. The ultra thin TSSOP is made possible by optimal wire looping control during the wire bonding process as well as optimal package warpage control during the molding process. TSSOP is designed to fill the niche of low pin count devices where low profile and small footprint are key design considerations. The TSSOP features 0.5 and 0.65mm lead pitch, and is ideal for low pin count analog and mixed signal devices in handheld applications such as PDAs and mobile / cellular phones.

Taking the reliability of Small Outline Packages (SOP) one step further, STATS ChipPAC offers a Micro Small Outline Package (MSOP) for applications requiring thin, small, and high reliability. This smaller package offers a smaller footprint, shorter wires for improved electrical connections, and better moisture reliability (MRT/MSL).

In addition to standard TSSOP and MSOP, STATS ChipPAC offers thermally enhanced "ep" versions featuring an exposed die paddle for efficient heat dissipation. The exposed die attach pad design of the TSSOP package can provide excellent thermal dissipation by soldering the copper die attach pad directly onto the PCB, and is ideal for low pin count analog and mixed signal devices.

STATS ChipPAC uses the latest leadframe technology and state of the art design and simulation tools to achieve optimum electrical and thermal performance. STATS ChipPAC's state of the art assembly facility and proven materials assure high yield manufacturing and long term reliability.



TSSOP and **MSOP**

Small Outline Packages

SPECIFICATIONS (TSSOP)

Die Thickness	9-11mil range preferred (TSSOP) 6-16mil range preferred (TSSOP-ep)					
Gold Wire	20µm (0.8mils) diameter, 99.99% Au					
Lead Finish	Sn/Pb (85/15%) or Matte Tin					
Marking	Laser					
Packing Options	Tube					
	(11000)					

Temperature Cycling					
Temp/Humidity Test					
Pressure Cooker Test					

RELIABILITY (all)

Condition C, -65°C/150°C, 1000 cycles 85°C/85% RH, 1000 hrs 121°C, 100% RH, 2 atm, 250 hrs

SPECIFICATIONS (MSOP)

Die Thickness	6-9mil range preferred
Gold Wire	20µm (0.8mils) diameter, 99.99% Au
Lead Finish	Sn/Pb (85/15%) or Matte Tin
Marking	Laser
Packing Options	Tube

THERMAL PERFORMANCE, Øja (°C/W)

Package	Body Size (mm)	Pad Size	Die Size	PCB Vias	Thermal Performance Øja (°C/W)
30L TSSOP	4.4 x 7.8 x 0.9	3.0 x 3.0	2.54 x 2.54	0	74.0
30L TSSOP-ep	4.4 x 7.8 x 0.9	3.0 x 3.0	2.54 x 2.54	9	49.5

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-5) under natural convection as defined in JESD51.2.

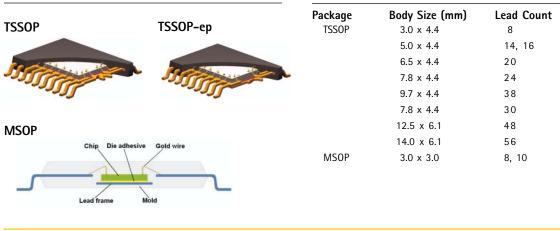
ELECTRICAL PERFORMANCE: 4.4 x 9.7 x 0.9 (38L)

Conductor	Pad Size	Lead/Wire	Resistance	Inductance		Capacitance	
Component	(mm)	(mm)	(mOhm)	Self (nH)	Mutual (nH)	Self (pF)	Mutual (pF)
Lead	185 x 113	0.6-3.09	5-25	0.30-1.70	0.14-0.77	0.09-0.46	0.04-0.21
Wire		1.65	99	1.36	0.37-0.65	0.08	0.01-0.02
TOTALS			104-124	1.66-3.06	0.51-1.42	0.17-0.54	0.05-0.23

PACKAGE CONFIGURATIONS

Note: Results are simulated values at 100MHz

CROSS-SECTION



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