FEATURES

- Offers Bandwidth Allocation of PCI Express™ Signal Using Two-Lane 1:2 Multiplexer/Demultiplexer
- Vcc Operating Range From 1.7 V to 1.9 V
- Supports Data Rates of 2.5 Gbps
- Port-Port Crosstalk (–39 dB at 1.25 GHz)
- OFF Port Isolation (–38 dB at 1.25 GHz)
- Low ON-State Resistance (10 Ω Typ)
- Low Input/Output Capacitance (3.5 pF Typ)
- Excellent Differential Skew (5 ps Max)
- Minimal Propagation Delay
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

DESCRIPTION/ORDERING INFORMATION

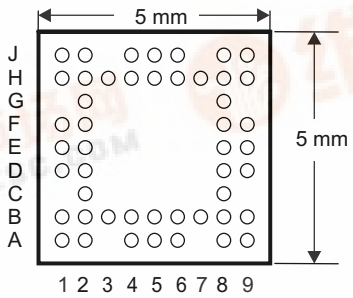
The TS2PCIE2212 can be used to muxltiplex/demultiplex two PCI Express™ lanes, each representing differential pairs of receive (RX) and transmit (TX) signals. The switch operates at the PCI Express bandwidth standard of 2.5-Gbps signal-processing speed. The device is composed of two banks, with each bank accommodating two sources (source A and source B) and two destinations (destination A and destination B).

When a logic-level low is applied to the control (CTRL) pin, source A is connected to destination A and source B is connected to destination B. When a logic-level high is applied to CTRL, source A is connected to destination B, while source B and destination A are open.

ORDERING INFORMATION

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 85°C	BGA – ZAH	Tape and reel	TS2PCIE2212ZAHR	

ZAH PACKAGE
(BOTTOM VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4	5	6	7	8	9
A	CTRL0	TxSB:0P		TxSA:0P	GND	TxDA:0P		TxDB:0P	NC
B	RxSA:0P	GND	TxSB:0N	TxSA:0N	VDD	TxDA:0N	TxDB:0N	GND	RxDA:0P
C		RxSA:0N						RxDA:0N	
D	RxSB:0P	RxSB:0N						RxDB:0N	RxDB:0P
E	GND	VDD						VDD	GND
F	TxSA:1P	TxSA:1N						TxDA:1N	TxDA:1P
G		TxSB:1N						TxDB:1N	
H	TxSB:1P	GND	RxSA:1N	RxSB:1N	VDD	RxDB:1N	RxDA:1N	GND	TxDB:1P
J	NC	RxSA:1P		RXSB:1P	GND	RXDB:1P		RxDA:1P	CTRL1

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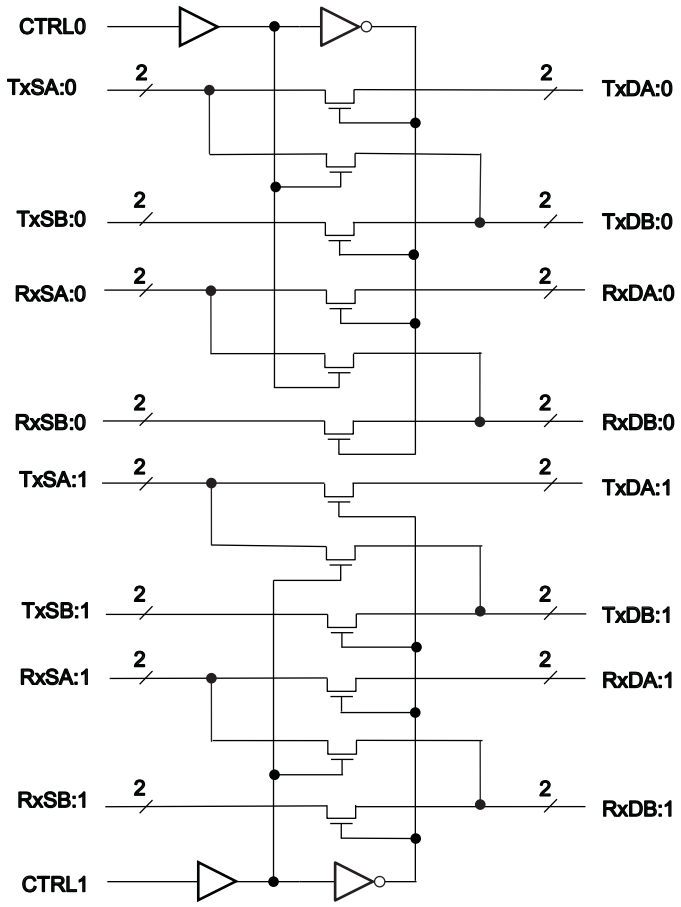
PIN DESCRIPTION

NAME	FUNCTION
TxSA:nP, TxSA:nN	Source A transmit pair
RxSA:nP, RxSA:nN	Source A receive pair
TxSB:nP, TxSB:nN	Source B transmit pair
RxSB:nP, RxSB:nN	Source B receive pair
TxDA:nP, TxDA:nN	Destination A transmit pair
RxDA:nP, RxDA:nN	Destination A receive pair
TxDB:nP, TxDB:nN	Destination B transmit pair
RxDB:nP, RxDB:nN	Destination B receive pair
CTRL0	Control signal for bank 0
CTRL1	Control signal for bank 1
V_{DD}	Positive supply voltage
GND	Ground (0 V)
NC	No internal connection

LOGIC DIAGRAM



FUNCTION TABLE

CTRLn	FUNCTION
L	SA:n = DA:n, SB:n = DB:n
H	SA:n = DB:n, DA:n = open, SBin = open

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	2.5	V
V_{IN}	Control input voltage range(2)(3)		–0.5	2.5	V
$V_{I/O}$	Switch I/O voltage range(2)(3)(4)		–0.5	2.5	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ and $V_{I/O} < 0$		50	mA
$I_{I/OK}$	I/O port clamp current	$V_{IN} < 0$ and $V_{I/O} < 0$		50	mA
$I_{I/O}$	ON-state switch current(5)			±100	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance(6)			TBD	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		1.7	1.8	1.9	V
V_{IH}	High-level control input voltage	CTRL	0.65 V_{DD}			V
V_{IL}	Low-level control input voltage	CTRL			0.35 V_{DD}	V
V_{IO}	Data input/output voltage		0		V_{DD}	V
T_A	Operating free-air temperature		0		85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A = 0°C to 85°C			UNIT
					MIN	TYP	MAX	
V_{IK}	Control inputs	V_{DD} = 1.7 V,	I_{IN} = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{DD} = 1.9 V,	V_{IN} = V_{DD} or GND				±1	µA
I_{OZ}		V_{DD} = 1.9 V,	V_O = 0 to 1.9 V, V_I = 0,	Switch OFF			±5	µA
I_{CC}		V_{DD} = 1.9 V, V_{IN} = V_{DD} or GND,	$I_{I/O}$ = 0,	Switch ON or OFF		160	300	µA
C_{in}	Control inputs	V_{DD} = 1.9 V,	V_{IN} = V_{DD} or GND			0.5	1.0	pF
$C_{IO(OFF)}$	SB or DA port	$V_{I/O}$ = 0 V,	Switch OFF			1.4	1.5	pF
$C_{IO(ON)}$		$V_{I/O}$ = 0 V,	Switch ON			3.5	4	pF
r_{on}		V_{DD} = 1.7 V,	V_I = 0 V,	I_O = 10 mA		10	14	Ω
		V_{DD} = 1.7 V,	V_I = 1.5 V,	I_O = –10 mA		12	17	
$\Delta r_{on(flat)}$		V_{DD} = 1.7 V,	I_O = 10 mA,	V_I = 1.5 V ± 0.4 V		2.5	5	Ω

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	T_A = 0°C to 85°C			UNIT
			MIN	TYP	MAX	
DR	Data rate per TX or RX pair			2.5		Gbps
t_{pd}	Propagation delay, Sx to Dx	See Figure 7		250		ps
t_{sk}	Intra-pair skew	f =1.25 GHz, See Figure 7			5	ps
t_{en} (t_{PZL}, t_{PZH})	Switch turn-on delay, CTRL to DA	See Figure 6			5	ns
t_{dis} (t_{PLZ}, t_{PHZ})	Switch turn-off delay, CTRL to DA	See Figure 6			2.5	ns
I_{LOSS}	Differential insertion loss	f =1.25 GHz, R_{LOAD} = 50 Ω, See Figure 1		–2.5	–3.2	dB
R_{LOSS}	Differential return loss	f =1.25 GHz, R_{LOAD} = 50 Ω, See Figure 2	–7.2	–9.5		dB
$I_{LOSS(CM)}$	Common-mode insertion loss	f =1.25 GHz, R_{LOAD} = 50 Ω, See Figure 3		–2		dB
O_{IFF}	Differential OFF isolation	f =1.25 GHz, R_{LOAD} = 50 Ω, See Figure 4	–33	–38		dB
X_{TALK}	Differential crosstalk	f =1.25 GHz, R_{LOAD} = 50 Ω, See Figure 5	–33	–39		dB

OPERATING CHARACTERISTICS

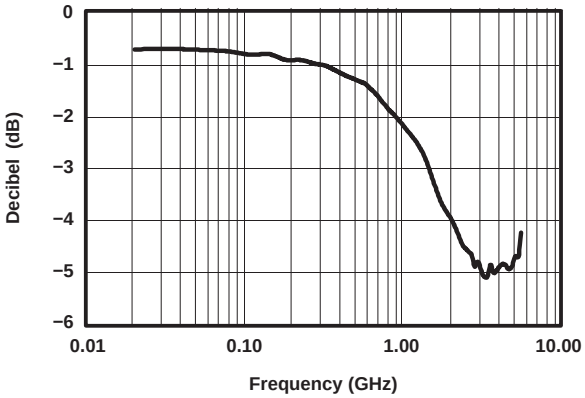


Figure 1. Differential Insertion Loss vs Frequency

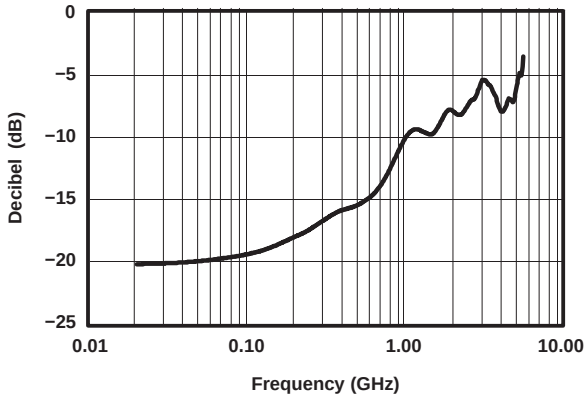


Figure 2. Differential Return Loss vs Frequency

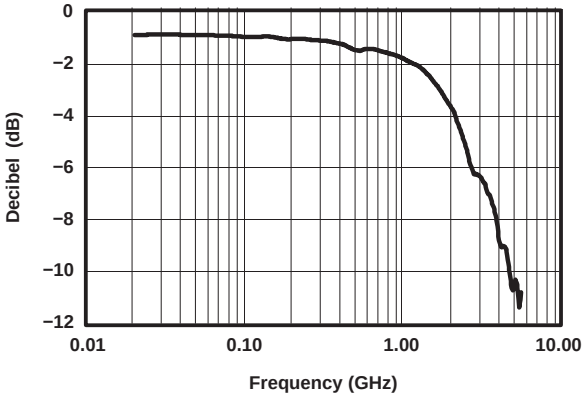


Figure 3. Common-Mode Insertion Loss vs Frequency

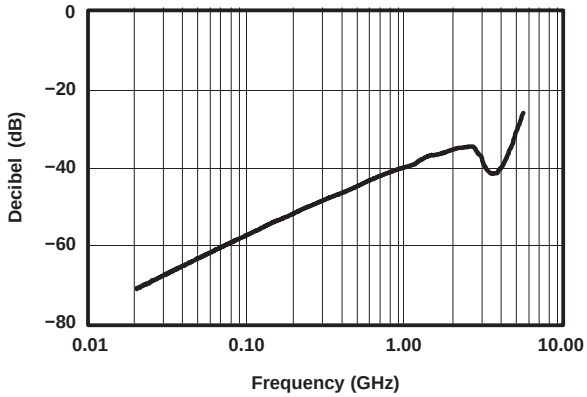


Figure 4. Differential OFF Isolation vs Frequency

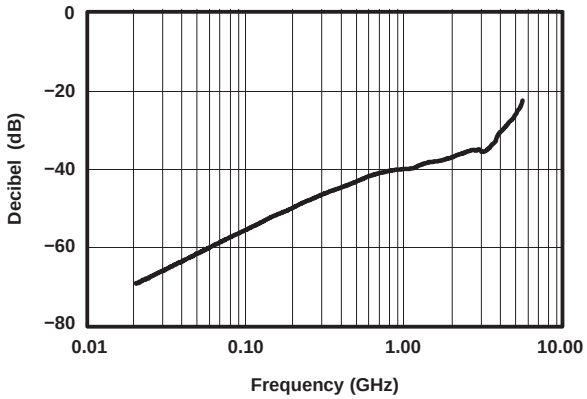
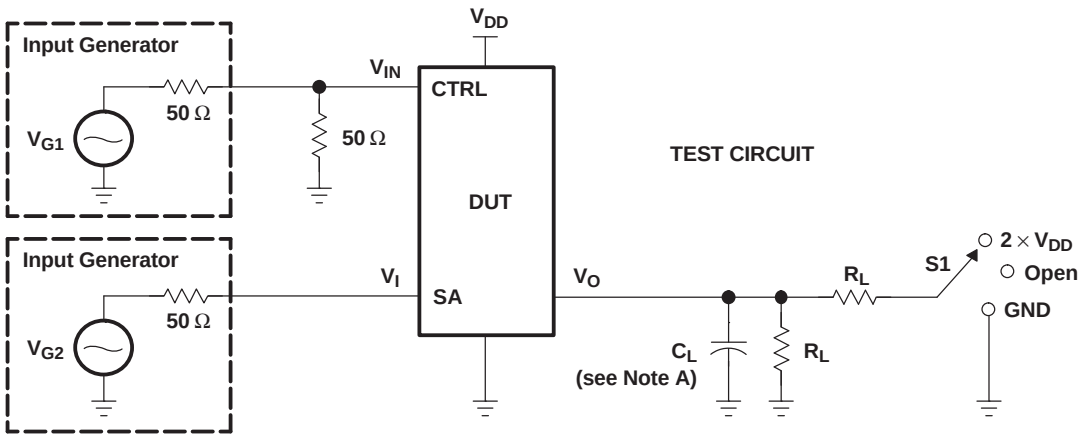
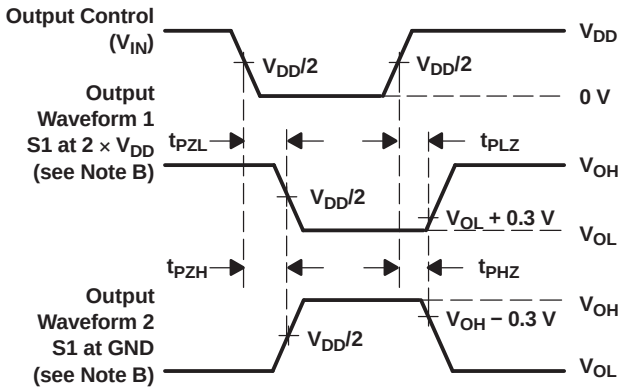


Figure 5. Differential Crosstalk vs Frequency

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	1.8 V ± 0.1 V	2 × V_{DD}	100 Ω	GND	No Load	0.3 V
t_{PHZ}/t_{PZH}	1.8 V ± 0.1 V	GND	100 Ω	V_{DD}	No Load	0.3 V

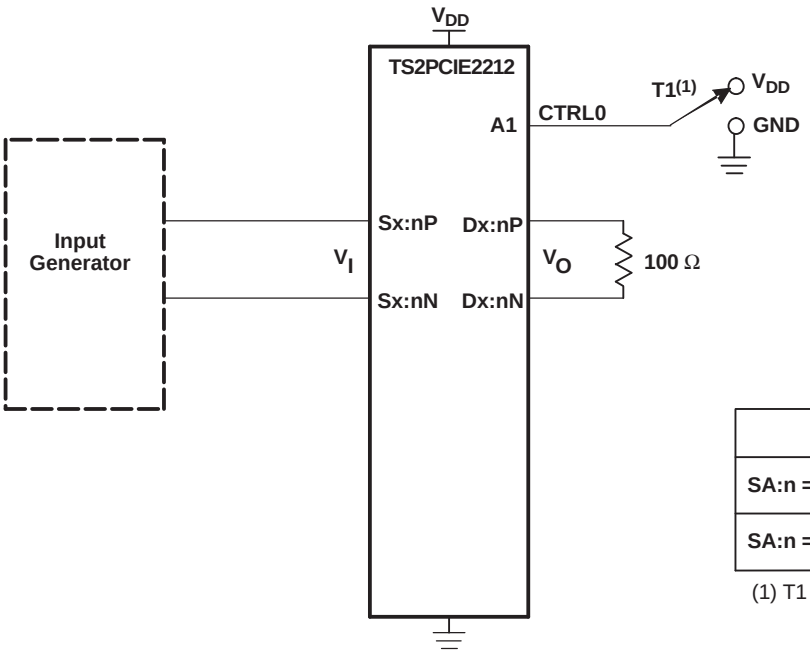


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

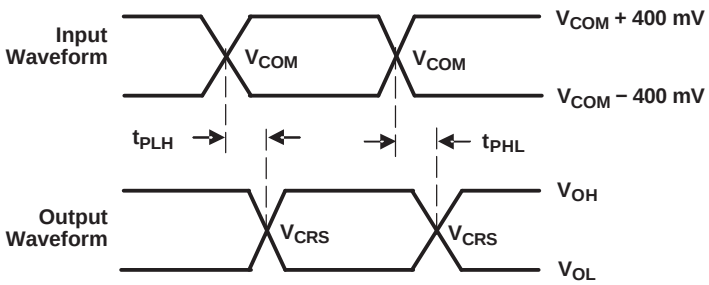
Figure 6. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST PATH	T1(1)
SA:n = DA:n, SB:n = DB:n	GND
SA:n = DB:n, DA:n = open	V_{DD}

(1) T1 is an external terminal.



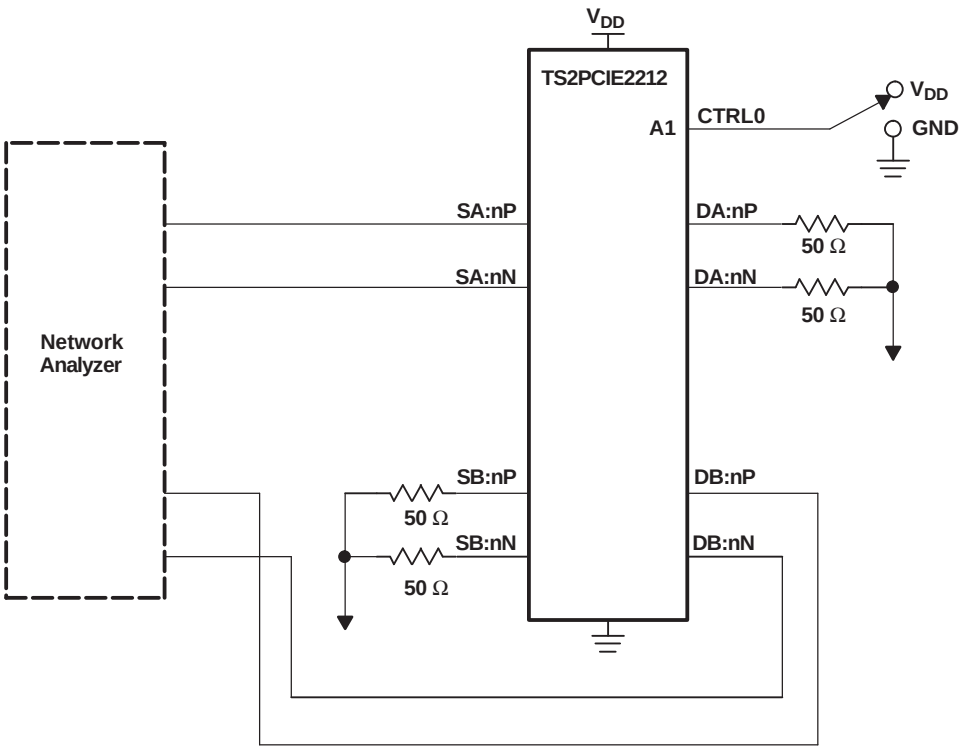
V_{COM} = 1.5 V

V_{CRS} is the cross point of the differential signal.

$t_{sk} = |t_{PLHn} - t_{PHLn}|$

Figure 7. Test Circuit for Propagation Delay and Intra-Pair Skew

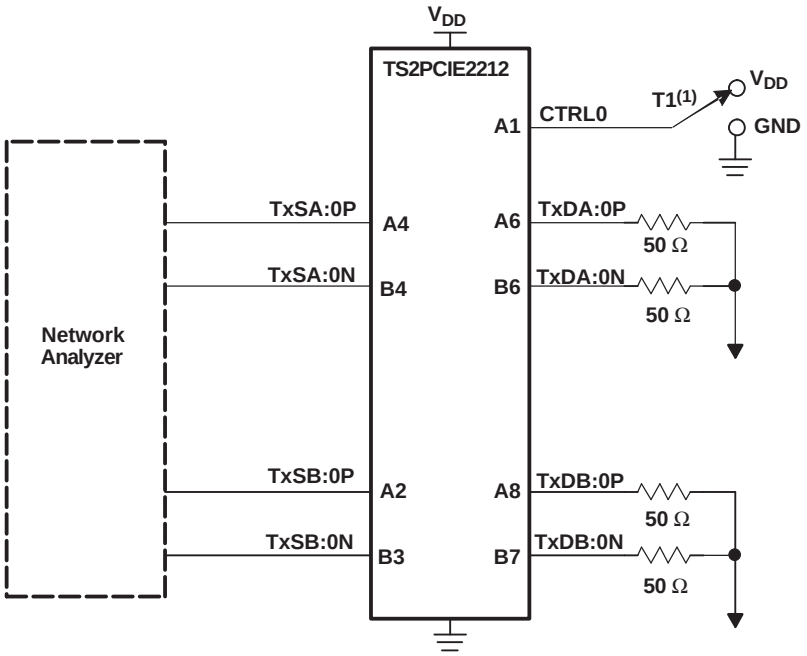
PARAMETER MEASUREMENT INFORMATION (continued)



TEST	VNA MEASUREMENT
Differential insertion loss	S_{21}
Differential return loss	S_{11}
Common-mode insertion loss	S_{21}

Figure 8. Differential Insertion Loss, Differential Return Loss, and Common-Mode Insertion Loss Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST	T1(1)
Differential crosstalk	GND
Differential OFF isolation	V_{DD}

(1) T1 is an external terminal.

Figure 9. Differential Crosstalk and OFF Isolation Test Circuit

PACKAGE OPTION ADDENDUM

18-Jul-2006

PACKAGING INFORMATION

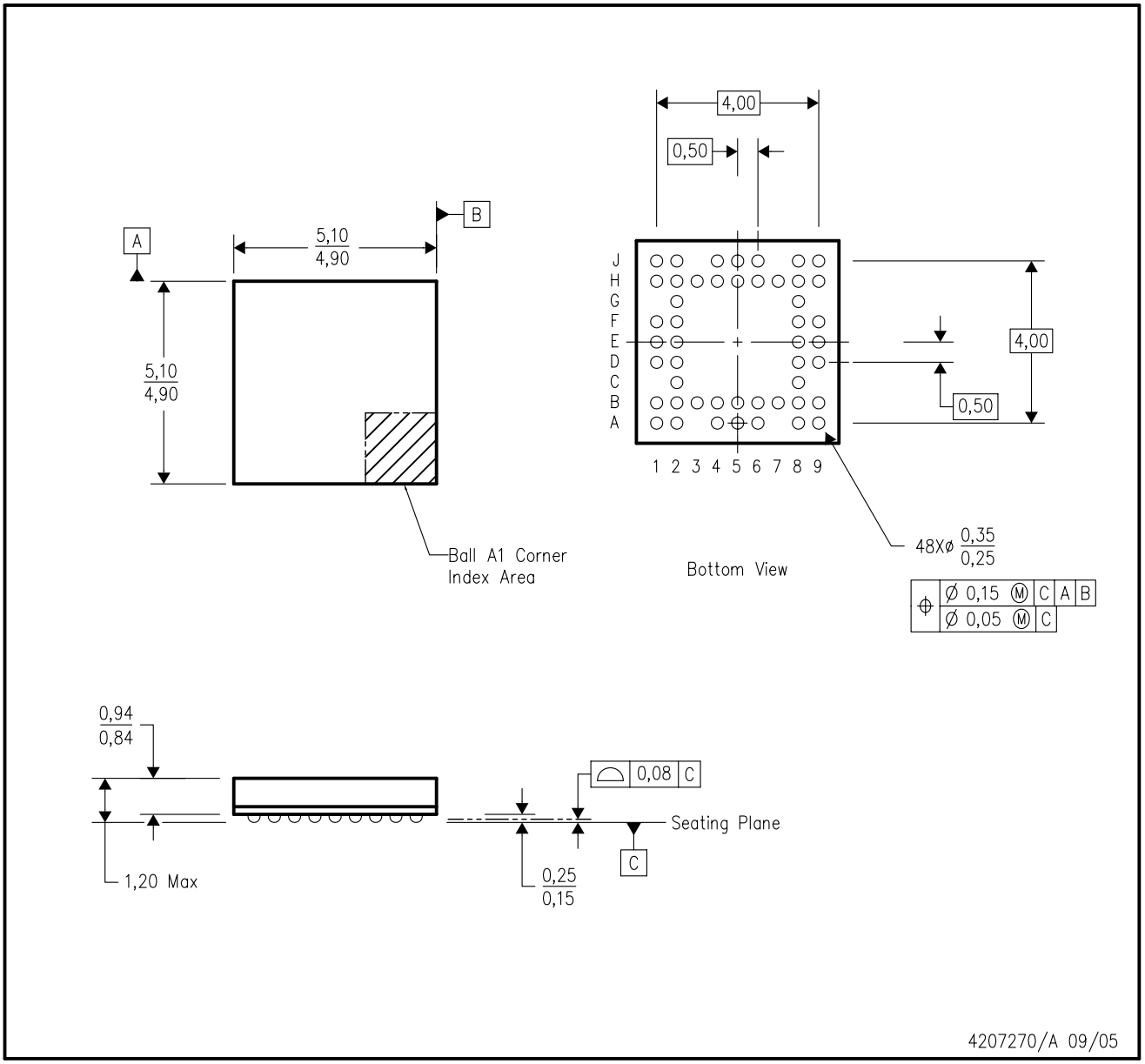
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS2PCIE2212ZAHR	ACTIVE	BGA	ZAH	48	3000	Pb-Free (RoHS)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

ZAH (S-PBGA-N48) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO-225 registration is pending.
D. This is a lead-free solder ball design.

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