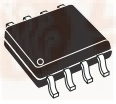
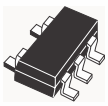
TS321

Low Power Single Operational Amplifier

- Large output voltage swing:
- 0 to 3.5V min. (@V_{CC} = 5V)
- Low supply current: 500µA
- Low input bias current: 20nA
- Low input offset voltage: 2mV max.
- Wide power supply range:
- Single supply: +3V to +30V
- Dual supplies: ±1.5V to ±15V
- Stable with high capacitive loads

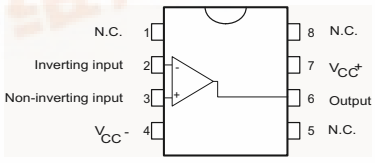


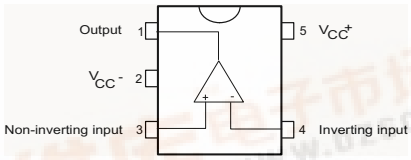
D
SO-8
(Plastic Micropackage



L
SOT23-5
(Plastic Package)

Pin connections (top view)





Description

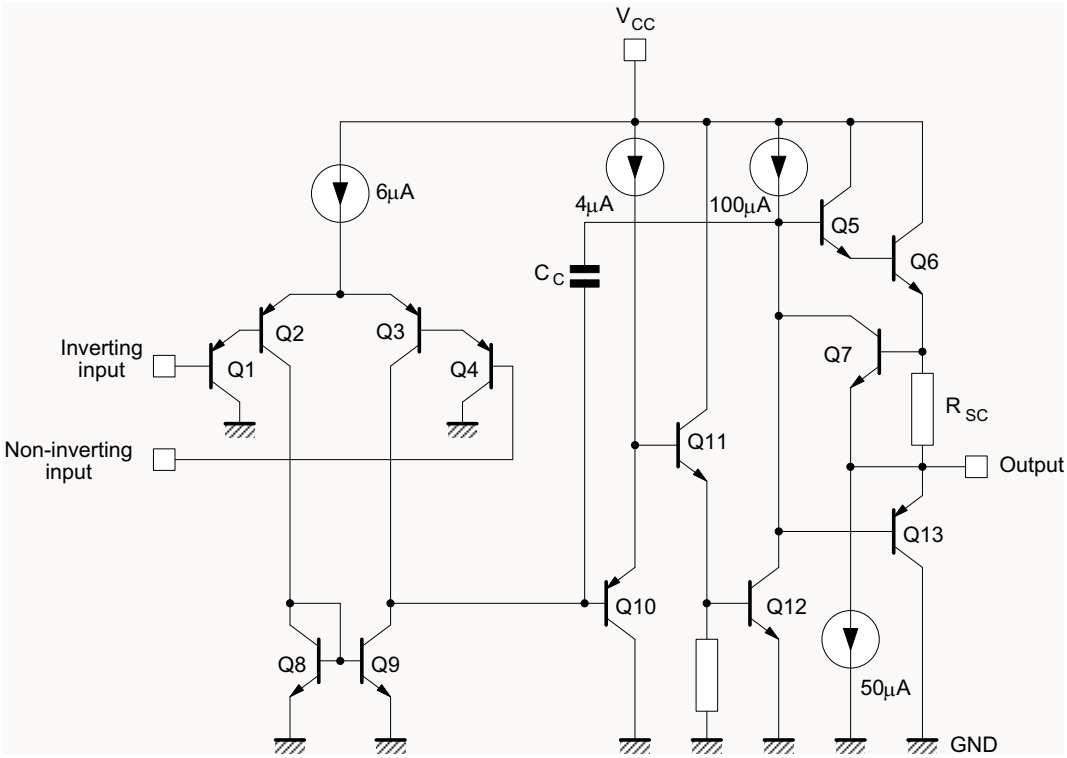
The TS321 is intended for cost-sensitive applications where space saving is of great importance. This bipolar op-amp offers the benefits of a reduced component size (SOT23-5 package), with specifications that match (or are better) industry standard devices (like the popular LM358A, LM324, etc.). The TS321 has an input common mode range (V_{icm}) that includes ground, and therefore can be employed in single supply applications.

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS321ILT	-40°C, +125°C	SOT23-5L	Tape & Reel	K401
TS321ID/IDT		SO8	Tube or Tape & Reel	321I
TS321AILT		SOT23-5L	Tape & Reel	K402
TS321AID/AIDT		SO8	Tube or Tape & Reel	321AI
TS321IYLT		SOT23-5L (automotive grade level)	Tape & Reel	K406
TS321AIYLT				
TS321IYD/IYDT		SO-8 (automotive grade level)	Tube or Tape & Reel	
TS321AIYD/AIYDT				

1 Typical Application Schematics

Figure 1. Typical application schematics



2 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±16 to 32	V
Vi	Input Voltage	-0.3 to +32	V
V_{id}	Differential Input Voltage	+32	V
	Output Short-circuit Duration - note (1)	Infinite	
I_{in}	Input Current - note (2)	50	mA
T_{oper}	Operating Free Air Temperature Range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
R_{thja}	Thermal Resistance Junction to Ambient (3) SOT23-5 SO8	 250 125	°C/W
R_{thjc}	Thermal Resistance Junction to Case SOT23-5 SO8	 81 40	°C/W
ESD	HBM: Human Body Model(4)	300	V
	MM: Machine Model(5)	200	V

1. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}.
2. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative. This is not destructive and normal output will set up again for input voltage higher than -0.3V.
3. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers. All values are typical.
4. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
5. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

3 Electrical Characteristics

Table 2. V_{cc}^+ = +5V, V_{cc}^- = Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (1)	T_{amb} = +25°C TS321A $T_{min.} \le T_{amb} \le T_{max.}$ TS321A		0.5	4 2 5 3	mV
I_{io}	Input Offset Current	T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		2	30 50	nA
I_{ib}	Input Bias Current (2)	T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max}$		20	150 200	nA
A_{vd}	Large Signal Voltage Gain	V_{CC}^+ = +15V, R_L = 2kΩ, Vo = 1.4V to 11.4V T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio	**$R_s \le$ 10kΩ** V_{CC}^+ = 5 to 30V T_{amb} = +25°C	65	110		dB
I_{CC}	Supply Current, no load	T_{amb} = +25°C, V_{CC} = +5V V_{CC} = +30V $T_{min.} \le T_{amb} \le T_{max.}$, V_{CC} = +5V V_{CC} = +30		500 600 600	800 900 900 1000	µA
V_{icm}	Common Mode Input Voltage Range (3)	**V_{CC} = +30V** T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common Mode Rejection Ratio	**$R_s \le$ 10kΩ** T_{amb} = +25°C	65	85		dB
I_{source}	Output Current Source	**V_{id} = +1V** V_{CC} = +15V, V_o = +2V	20	40		mA
I_{sink}	Output Sink Current	**V_{id} = -1V** V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		mA µA
I_o	Short Circuit to Ground	**V_{CC} = +15V**		40	60	mA
V_{OH}	High Level Output Voltage	**V_{CC} = +30V** T_{amb} = +25°C, R_L = 2kΩ $T_{min.} \le T_{amb} \le T_{max.}$ T_{amb} = +25°C, R_L = 10kΩ $T_{min.} \le T_{amb} \le T_{max.}$ V_{CC} = +5V, R_L = 2kΩ T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$	26 25.5 27 26.5 3.5 3	27 28 		V
V_{OL}	Low Level Output Voltage	**R_L = 10kΩ** T_{amb} = +25°C $T_{min.} \le T_{amb} \le T_{max.}$		5	15 20	mV

Table 2. V_{cc}^{+} = +5V, V_{cc}^{-} = Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew Rate	V_{CC} = +15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, T_{amb} = +25°C, unity gain		0.4		V/µs
GBP	Gain Bandwith Product	V_{CC} = 30V, f = 100kHz, T_{amb} = +25°C, V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF		0.8		MHz
ϕm	Phase Margin			60		Degrees
THD	Total Harmonic Distortion	f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = 2Vpp, C_L = 100pF, T_{amb} = +25°C, V_{CC} = 30V		0.015		%
en	Equivalent Input Noise Voltage	f = 1kHz, R_s = 100Ω, V_{CC} = 30V		40		$\frac{nV}{\sqrt{Hz}}$

1. Vo = 1.4V, Rs = 0W, 5V < V_{CC}+ < 30V, 0 < V_{ic} < V_{CC}+ - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}+ - 1.5V, but either or both inputs can go to +32V without damage.

Figure 2. $I_{CC} = f(t)$

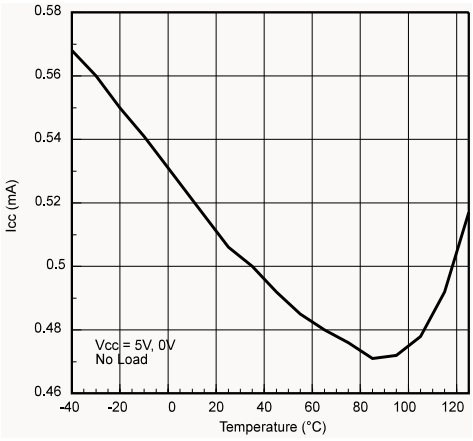


Figure 3. AC coupled inverting amplifier

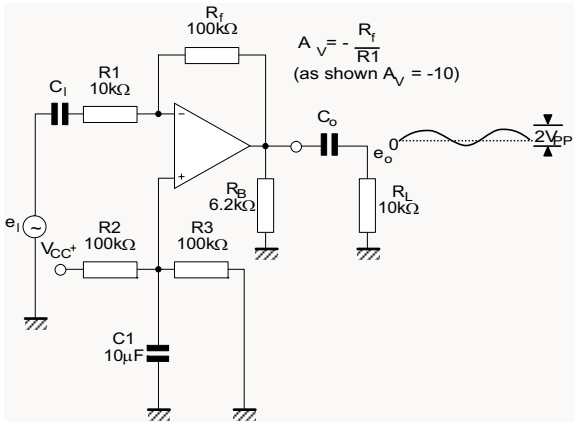


Figure 4. Non-inverting DC gain

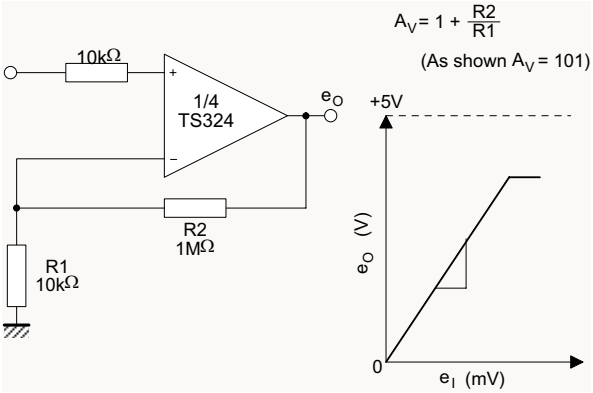


Figure 5. AC coupled non-inverting amplifier

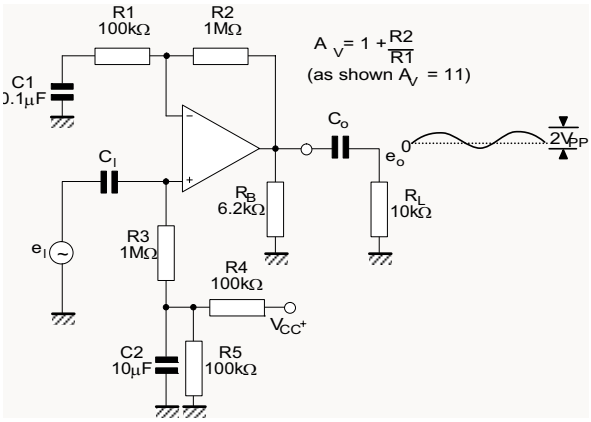
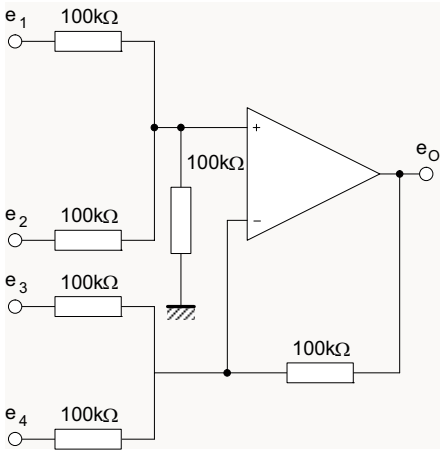


Figure 6. DC summing amplifier



4 Macromodel

Note: Please consider following remarks before using this macromodel:
All models are a trade-off between accuracy and complexity (i.e. simulation time).
Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.
Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc) or even worse: outside of the device operating conditions (Vcc, Vicm, etc) are not reliable in any way.

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT TS321 1 2 3 4 5
*****************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
```

```
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

Table 3. $V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L, C_L connected to $V_{CC/2}$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 2k\Omega$	100	V/mV
I_{CC}	No load, per operator	300	µA
V_{icm}		0 to +3.5	V
V_{OH}	$R_L = 2k\Omega$	+3.5	V
V_{OL}	$R_L = 2k\Omega$	5	mV
I_{os}	$V_o = 0V$	40	mA
GBP	$R_L = 2k\Omega$, $C_L = 100pF$	0.8	MHz
SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.4	V/µs
∅m	$R_L = 2k\Omega$, $C_L = 100pF$	60	Degrees

Figure 7. $I_{CC} = f(t)$

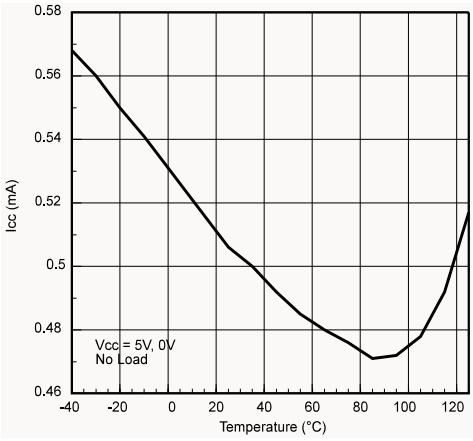


Figure 8. AC coupled inverting amplifier

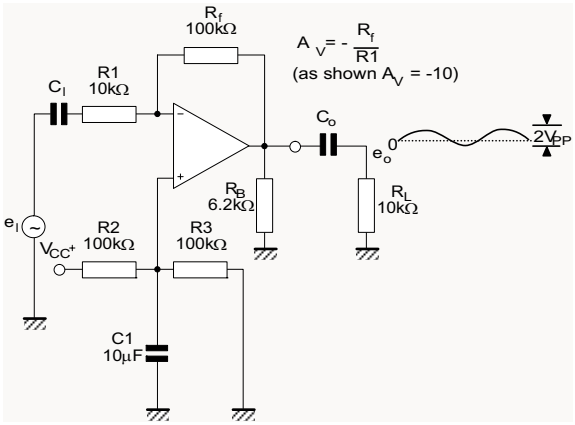


Figure 9. Non-inverting DC gain

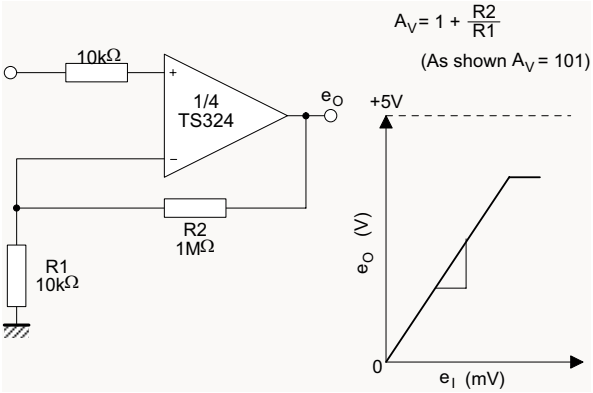


Figure 10. AC coupled non-inverting amplifier

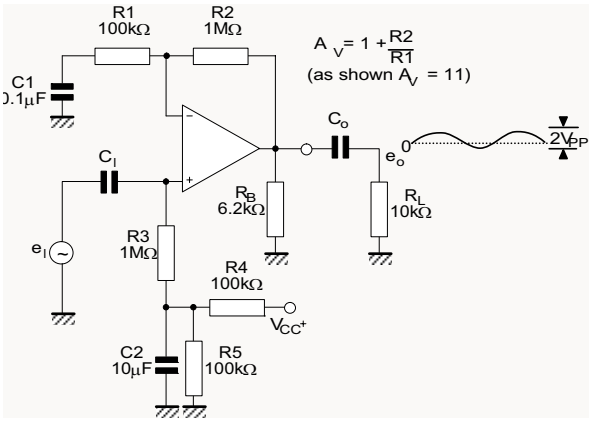
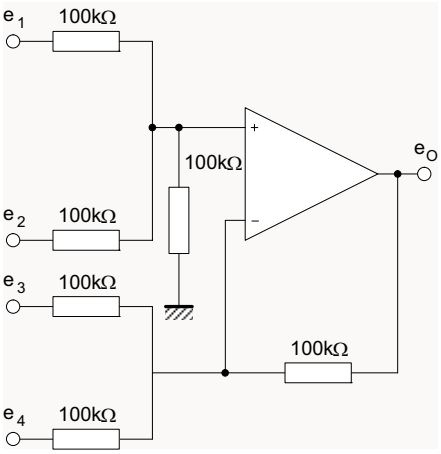


Figure 11. DC summing amplifier



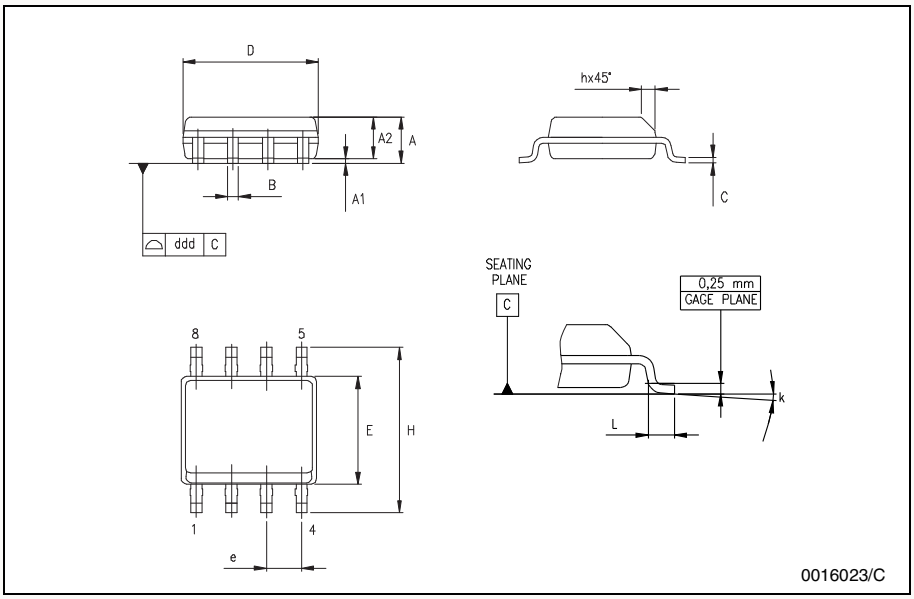
5 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

5.1 SO-8 Package

SO-8 MECHANICAL DATA

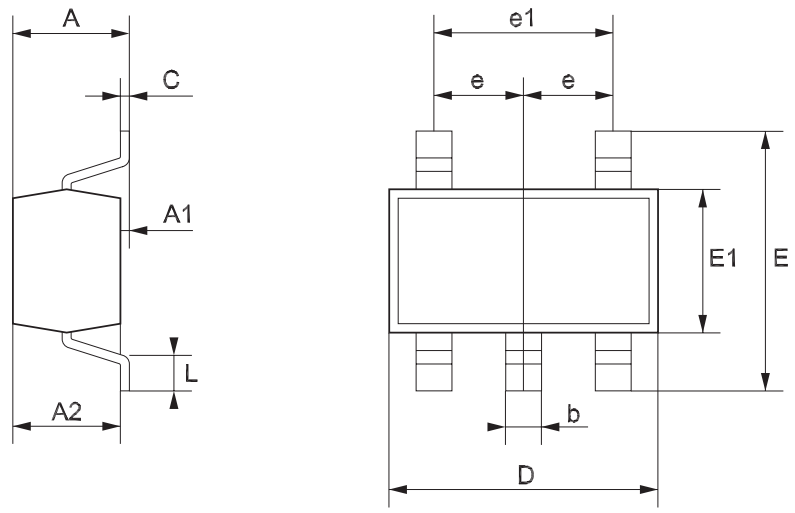
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



5.2 SOT23-5 Package

SOT23-5L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e		0.95			37.4	
e1		1.9			74.8	
L	0.35		0.55	13.7		21.6



6 Revision history

Table 4. Document revision history

Date	Revision	Changes
June 2001	1	– Initial release.
July 2005	2	– PPAP references inserted in the datasheet see table order codes table *on page 1*. – ESD protection inserted in *Table 1 on page 3*
Sept. 2005	3	– Correction of errors in package names and markings in order codes table *on page 1*. – Minor grammatical and formatting corrections.
Dec. 2005	4	– Missing PPAP references inserted see order codes table *on page 1*. – Thermal Resistance Junction to Ambient and Thermal Resistance Junction to Case information added in *Table 1 on page 3*. – Macromodel updated see *Chapter 4: Macromodel*.