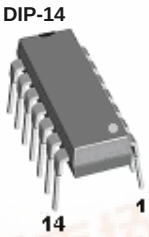
TS339

Quad Voltage Comparator



Supply Voltage Range -18 V to 18V
Quad Channel Comparator

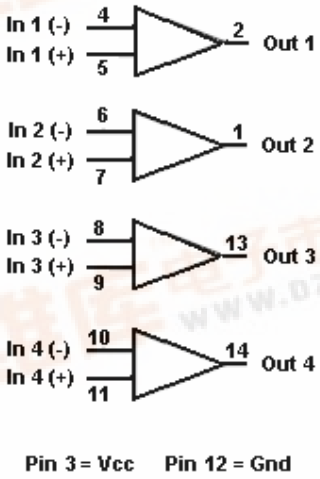
General Description

The TS339 is quad independent precision voltage comparators capable of single-supply or split-supply operation. The specifications as low as 2.0 mV make this device an excellent ground level with single-supply operation. Input offset-voltage selection for many applications in consumer automotive, and It is designed to permit a common mode range-to- industrial electronics.
The TS339 is offered in SOP-14 and DIP-14 package.

Features

- ✧ Output voltage compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels
- ✧ Low input bias current -25nA
- ✧ Low input offset current -5.0nA
- ✧ Low input offset voltage --5.0mV(max)
- ✧ Input common mode range to ground level
- ✧ Differential input voltage range equal to power supply voltage

Pin Assignment

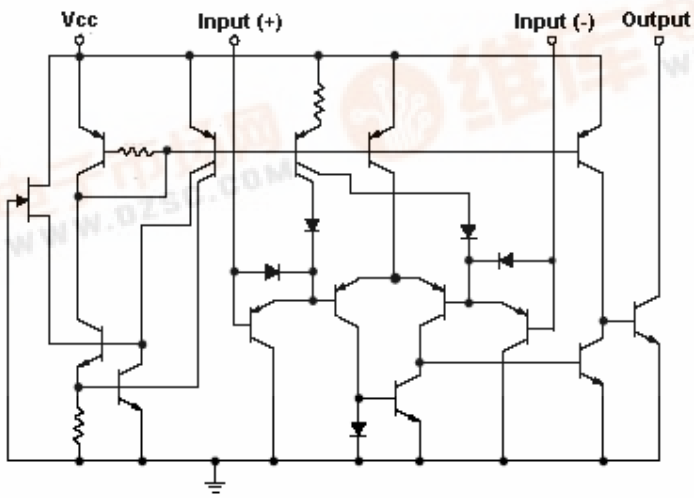


Pin 3 = Vcc Pin 12 = Gnd

Ordering Information

Part No.	Operating Temp.	Package
TS339CD	0 ~ +70 °C	DIP-14
TS339CS		SOP-14

Schematic (each comparator)



Absolute Maximum Rating

Supply Voltage	Vcc	+36 or ±18	Vdc
Differential Input Voltage	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	-0.3 to 36	Vdc
Input Current (note 2)	Iin	50	mA
Output Short Circuit to Ground	Isc	Continuous	
Output Sink Current (note 1)	Isink	20	mA
Power Dissipation @ Ta=25 °C		1.0	W
Derate above 25 °C	1/Rθja	8	mW/ °C
Operating Junction Temperature Range	T_J	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Lead Temperature 1.6mm(1/16") from case for 10Sec.	T_{LEAD}	260	°C

Electrical Characteristics (V_{CC} = 5V, Ta =25 °C; unless otherwise specified.)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Input Offset Voltage (note 3)	Vio		--	±2.0	±5.0	mV
Input Offset Current (note 3)	Iio		--	±5.0	±50	nA
Input Bias Current (note 3, 4) (output in linear range)	I_{IB}		--	25	250	nA
Input Common Mode Voltage Range (note 6)	V_{ICR}		0	--	V_{CC}-1.5	Volts
Voltage Gain	A_{VOL}	R_L ≥15K, Vcc = 15Vdc.	--	200	--	V/mV
Large Signal Response Time	--	Vin = TTL Logic Swing. Vref = 1.4Vdc, VRL = 5Vdc. RL= 5.1KΩ	--	300	--	nS
Response Time (note 6)	t_{TLH}	VRL = 5Vdc, RK = 5.1KΩ	--	1.3	--	uS
Output Sink Current	I_{SINK}	Vin-≥1Vdc, Vin+=0Vdc, V_{O-} ≤15 Vdc	6	16	--	mA
Output Saturation Voltage	V_{OL}	Vin- ≥1Vdc, Vin+=0, I_{SINK} ≤4mA,	--	130	400	mV
Output Leakage Current	I_{OL}	Vin-=0V, Vin+≥1Vdc, Vo=5Vdc	--	0.1	--	nA
Input Offset Voltage (note 3)	Vio	T_{LOW} ≤ Ta ≤T_{HIGH}	--	--	±9.0	mV
Input Offset Current (note 3)	Iio	T_{LOW} ≤ Ta ≤T_{HIGH}	--	--	±150	nA
Input Bias Current (note 3, 4) (output in linear range)	I_{IB}	T_{LOW} ≤ Ta ≤T_{HIGH}	--	--	400	nA
Input Common Mode Voltage Range (note 6)	V_{ICR}	T_{LOW} ≤ Ta ≤T_{HIGH}	0	--	V_{CC}-2.0	Volts
Output Saturation Voltage	V_{OL}	Vin- ≥1Vdc, Vin+=0, I_{SINK} ≤4mA, T_{LOW} ≤Ta ≤T_{HIGH}	--	--	700	mV
Output Leakage Current	I_{OL}	Vin-=0V, Vin+≥1Vdc, Vo=30V	--	0.1	--	nA
Input Differential Voltage	V_{ID}	All Vin ≥ 0Vdc, T_{LOW} ≤Ta≤T_{HIGH}	--	--	V_{CC}	V
Supply Current	Icc	R_L = ∞ (for all comparators)	--	0.8	2.0	mA

Electrical Characteristics (Continues)

Note 1. The maximum output current may be as high as 20mA, independent of the magnitude of V_{CC} Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

Note 2. This magnitude of input current will only occur if the leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction become forward biased, acting as an input clamp diode. There is also a lateral PNP parasitic transistor action which can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time that an input is driven negative. This will not destroy the device when limited to the max rating and normal output states will recover when the inputs become ≥ground or negative supply.

Note 3. At the output switch point, V_O=1.4Vdc, R_S ≤100Ω, 5.0Vdc≤ V_{CC} ≤30Vdc, with the inputs over the full common-mode range (0Vdc to V_{CC} -1.5Vdc).

Note 4. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.

Note 5. The response time specified is for a 100mV input step with 5mV overdrive For larger signals, 300ns is typical.

Note 6. Positive excursions of input voltage may exceed the power supply level. As long as one of the inputs remain within the common-mode range, the comparator will provide the proper output state.

Note 7. The comparator will inhibit proper output state if one of the inputs is become greater than $V_{CC,}$ the other input must remain within the common mode range. The low input state must not be less than -0.3volts of ground of minus supply.

Applications Information

This quad comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitive coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors<10KΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3V should not be used.

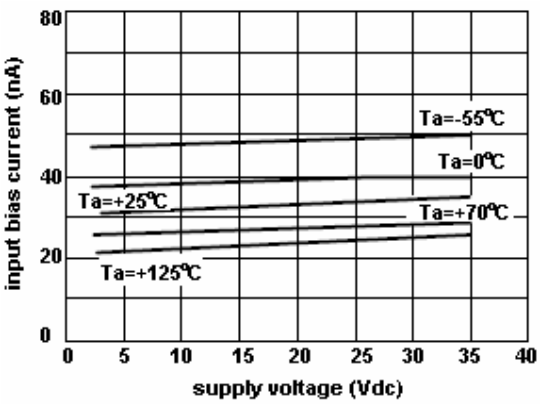


Figure 1. input bias current vs power supply voltage

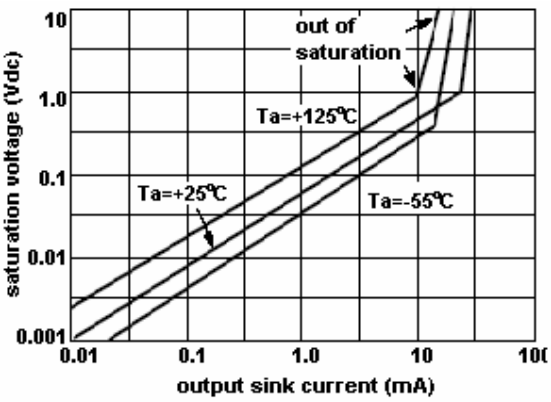


Figure 2. output saturation voltage vs output sink current

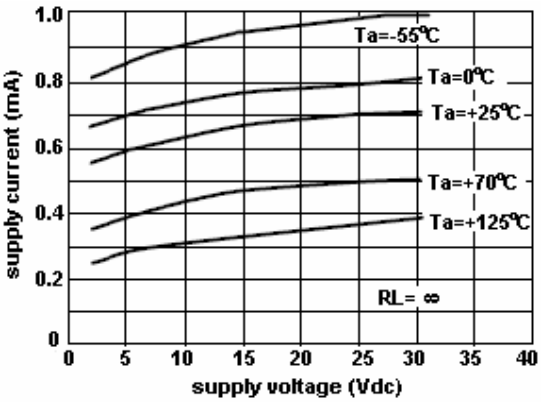


Figure 3. power supply current vs power supply voltage

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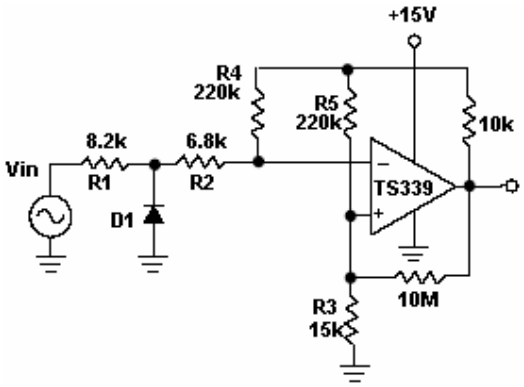
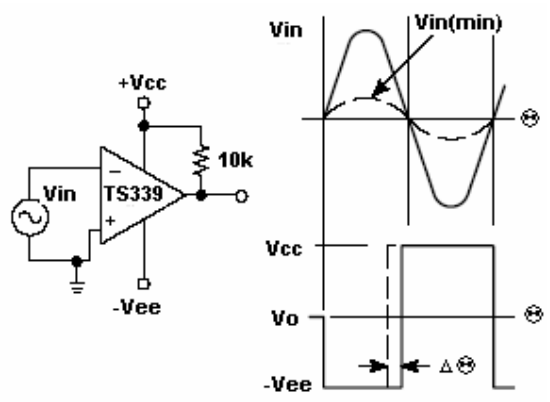
Electrical Characteristics Curve



D1 prevents input from going engative
by more than 0.6V, R1 + R2 = R3
R3 <= R5 / 10 for small error in zero crosing

Figure 4. zero crossing detector (single supply)



Vin(min)=0.4V peak for 1% phase distortion (Δ㋡)

Figure 5. zero crossing detector (split supply)

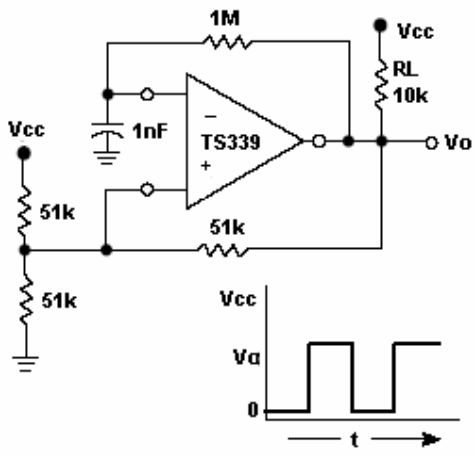


Figure 6. free-running square-wave oscillator

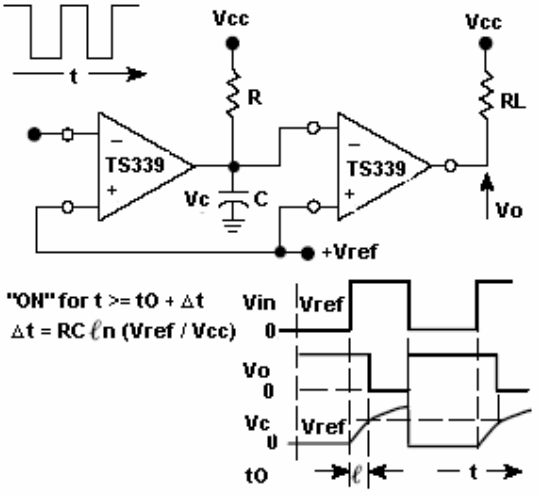
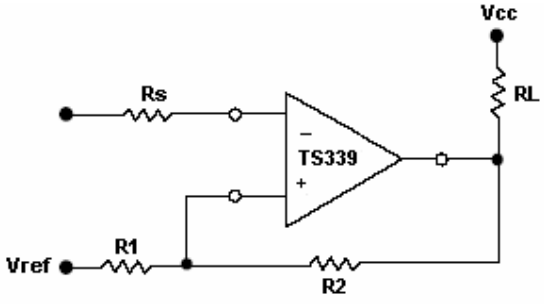


Figure 7. time delay generator



$$Rs = R1 \,||\, R2$$

$$Vth1 = Vref + \frac{(Vcc - Vref) * R1}{R1 + R2 + RL}$$

$$Vth2 = Vref - \frac{(Vref - Vo\ low) * R1}{R1 + R2}$$

Figure 8. comparator with hysteresis

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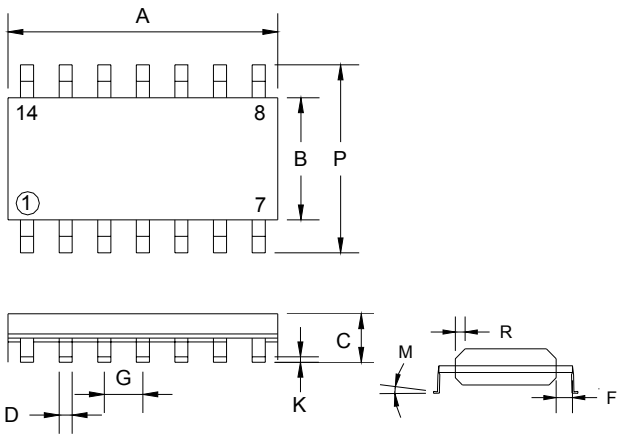
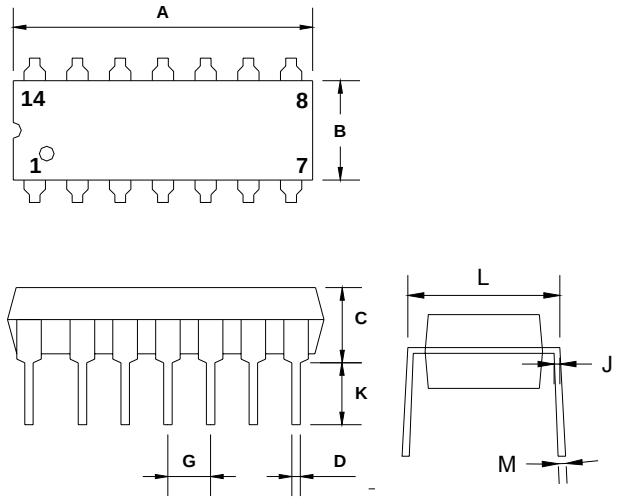
SOP-14 Mechanical Drawing



SOP-14 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0^o	7^o	0^o	7^o
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DIP-14 Mechanical Drawing



SOP-14 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.55	19.56	0.730	0.770
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10^o	-	10^o