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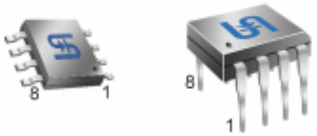
TS393

Dual Voltage Comparator

SOP-8 DIP-8



Pin assignment:
1. Output
2. Input A (-)
3. Input A (+)
4. Gnd
5. Input B (+)
6. Input B (-)
7. Output B
8. Vcc

Supply Voltage Range -18 V to 18V
Dual Channel Comparator

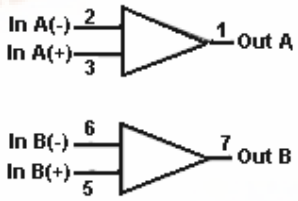
General Description

The TS393 is dual independent precision voltage comparators capable of single-supply or split-supply operation. The specifications as low as 2.0 mV make this device an excellent ground level with single-supply operation. Input offset-voltage selection for many applications in consumer automotive, and It is designed to permit a common mode range-to- industrial electronics.
The TS393 is offered in 8 pin SOP-8 and DIP-8 package.

Features

- ✧ Output voltage compatible with DTL, ECL, TTL, MOS and CMOS Logic Levels
- ✧ Low input bias current -25nA
- ✧ Low input offset current -5.0nA
- ✧ Low input offset voltage --5.0mV(max)
- ✧ Input common mode range to ground level
- ✧ Differential Input voltage range equal to power supply voltage
- ✧ Very low current drain independent of supply voltage - 0.4mA
- ✧ Wide single-supply range - 2.0Vdc to 36Vdc
- ✧ Split-supply range ±1.0Vdc to ±18Vdc

Block Diagram

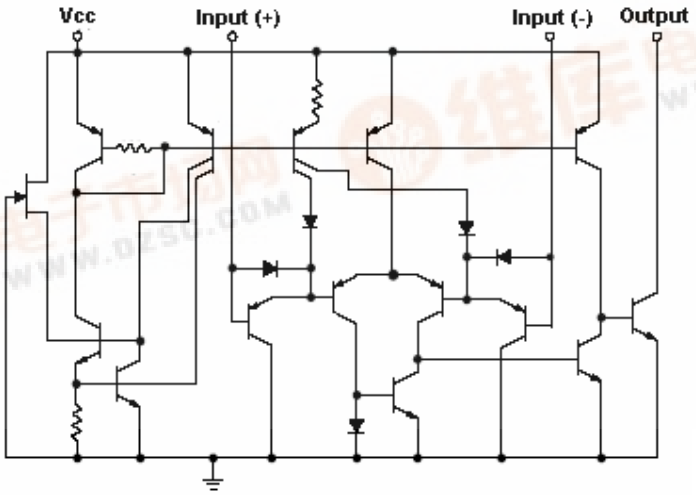


Pin 4 = Gnd Pin 8 = Vcc

Ordering Information

Part No.	Operating Temp.	Package
TS393CD	0 ~ +70 °C	DIP-8
TS393CS		SOP-8

Schematic (each comparator)



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Absolute Maximum Rating

Supply Voltage	Vcc	+36 or ±18	Vdc
Differential Input Voltage	V_{IDR}	36	Vdc
Input Common Mode Voltage Range Input Current (note 2)	V_{ICR} Iin	-0.3 to 36 50	Vdc mA
Output Short Circuit to Ground Output Sink Current (note 1)	Isc Isink	Continuous 20	 mA
Power Dissipation @ Ta=25 °C Derate above 25 °C	 1/Rθja	570 5.7	mW mW/ °C
Operating Junction Temperature Range	T_J	0 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C
Lead Temperature 1.6mm(1/16") from case for 10Sec.	T_{LEAD}	260	°C

Electrical Characteristics

(V_{CC} = 5V, $T_{LOW} \leq Ta \leq T_{HIGH}$; unless otherwise specified.)

Characteristics	Symbol	Test condition	Min	Typ	Max	Unit
Input Offset Voltage (note 3)	Vio	Ta =25 °C $T_{LOW} \leq Ta \leq T_{HIGH}$	-- --	±1.0 --	±5.0 9.0	mV
Input Offset Current	Iio	Ta =25 °C $T_{LOW} \leq Ta \leq T_{HIGH}$	-- --	±5.0 --	±50 ±150	nA
Input Offset Current (note 4)	I_{IB}	Ta =25 °C $T_{LOW} \leq Ta \leq T_{HIGH}$	-- --	25 --	250 400	nA
Input Common Mode Voltage Range (note 5)	V_{ICR}	Ta =25 °C $T_{LOW} \leq Ta \leq T_{HIGH}$	0 0	-- --	V_{CC}-1.5 V_{CC}-2.0	Volts
Voltage Gain	A_{VOL}	$R_L \geq$15K, Vcc = 15Vdc. Ta =25 °C	50	200	--	V/mV
Large Signal Response Time	--	Vin = TTL Logic Swing. Vref = 1.4Vdc, VRL = 5Vdc. RL 5.1KΩ, Ta =25 °C	--	300	--	nS
Response Time (note 6)	t_{TLH}	VRL = 5Vdc, RK = 5.1KΩ Ta =25 °C	--	1.3	--	uS
Input Differential Voltage (note 7)	V_{ID}	All Vin ≥ Gnd or V-Supply (if used)	--	--	V_{CC}	V
Output Sink Current	I_{SINK}	Vin-≥1Vdc, Vin+=0Vdc, $V_{O-} \leq$1 Vdc, Ta =25 °C	60	16	--	mA
Output Saturation Voltage	V_{OL}	Vin- ≥1Vdc, Vin+=0, $I_{SINK} \leq$4mA, Ta =25 °C $T_{LOW} \leq Ta \leq T_{HIGH}$	 -- --	 150 --	 400 700	mV
Output Leakage Current	I_{OL}	Vin-=0V, Vin+≥1Vdc, P=5Vdc. Ta =25 °C Vin-=0V, Vin+≥1V, V_O=30Vdc $T_{LOW} \leq Ta \leq T_{HIGH}$	 -- --	 0.1 --	 -- 1000	nA
Supply Current	Icc	$R_L = \infty$, Ta =25 °C $R_L = \infty$, V_{CC} =30 V	-- --	0.4 --	1.0 2.5	mA

Electrical Characteristics (Continues)

Note 1. The max. Output current may be as high as 20mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.

Note 2. This magnitude of input current will only occur if the input leads are driven more negative than ground or the negative supply voltage. This is due to the input PNP collector base junction becoming forward biased acting as an input clamp diode. There is also a lateral PNP parasitic transistor action on the IC chip. This phenomena can cause the output voltage of the comparators to go to the V_{CC} voltage level (or ground if overdrive is large) during the time the input is driven negative. This will not destroy the device and normal output states will recover when the inputs become -0.3V of ground or negative supply.

Note 3. At output switch point, V_O=1.4Vdc, R_S=0Ω with V_{CC} from 5Vdc to 30Vdc, and over the full input common-mode

Note 4. Due to the PNP transistor inputs, bias current will flow out of the inputs, this current is essentially constant independent of the output state, therefore, no loading changes will exist on the input lines.

Note 5. Input common mode of either input should not be permitted to go more than 0.3V negative of ground or minus supply. The upper limit of common mode range is V_{CC} - 1.5V but either or both inputs can betaken to as high as 30volts without damage.

Note 6. Response time is specified with a 100mV step and 5.0mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

Note 7. The comparator will inhibit proper output state if one of the inputs is become greater than $V_{CC,}$ the other input must remain within the common mode range. The low input state must not be less than -0.3volts of ground of minus supply.

Applications Information

This dual comparator feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitive coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors<10KΩ should be used. The addition of positive feedback (<10 mV) is also recommended.

It is good design practice to ground all unused pins. Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than -0.3V should not be used.

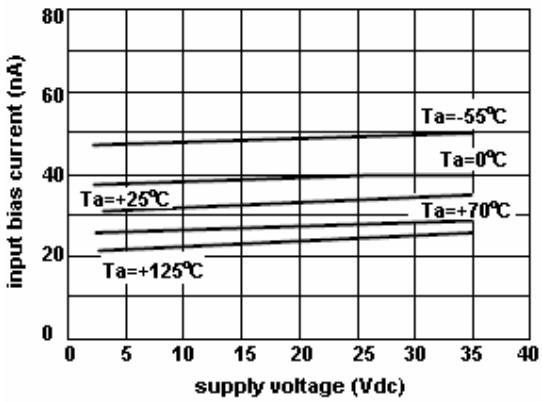


Figure 1. input bias current vs power supply voltage

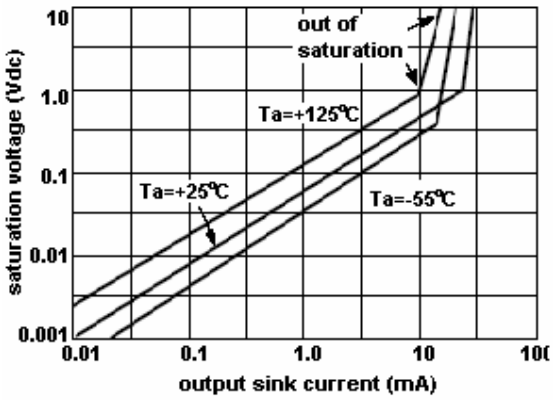


Figure 2. output saturation voltage vs output sink current

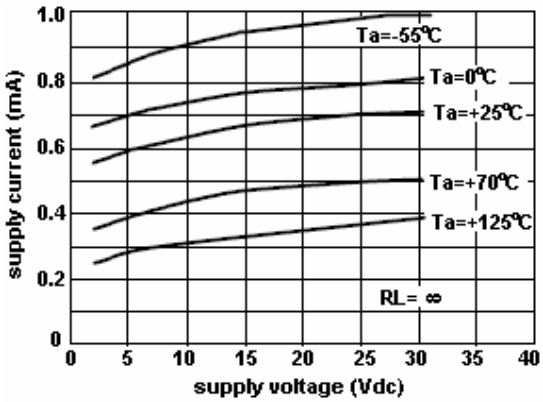
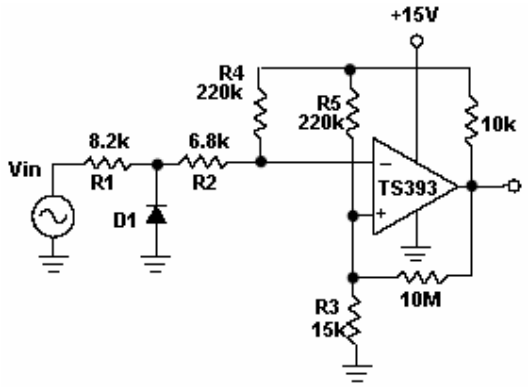


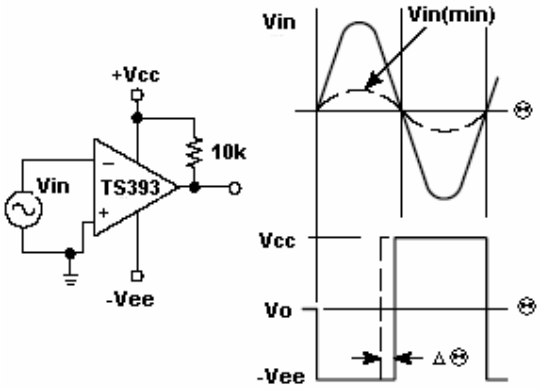
Figure 3. power supply current vs power supply voltage

Electrical Characteristics Curve



D1 prevents input from going engative
by more than 0.6V, R1 + R2 = R3
R3 <= R5 / 10 for small error in zero crosing

Figure 4. zero crossing detector
(single supply)



Vin(min)=0.4V peak for 1% phase distortion (Δ⊛)

Figure 5. zero crossing detector
(split supply)

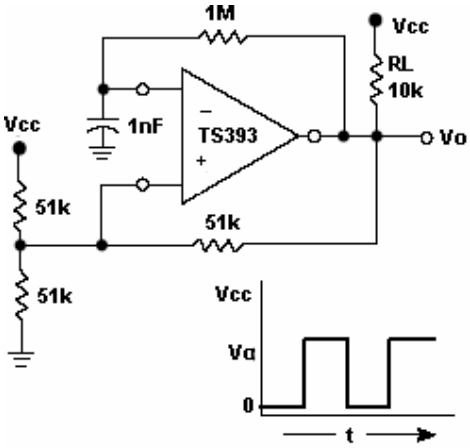


Figure 6. free-running square-wave
oscillator

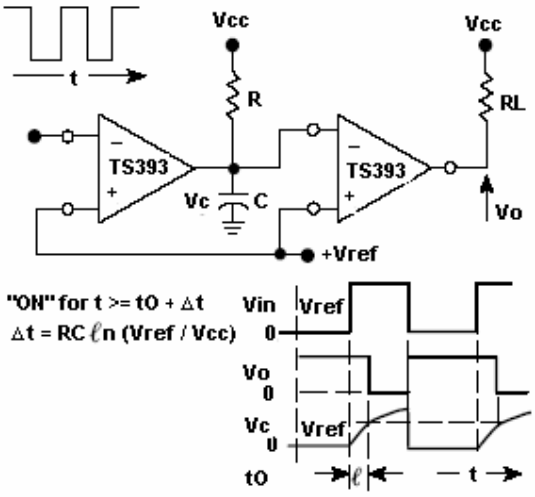
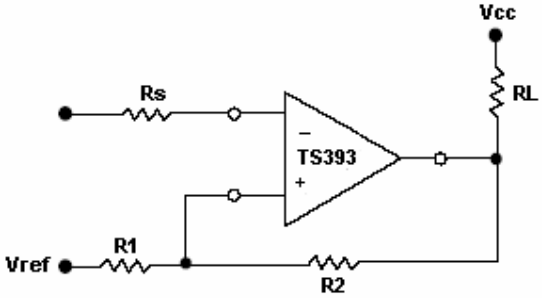


Figure 7. time delay generator



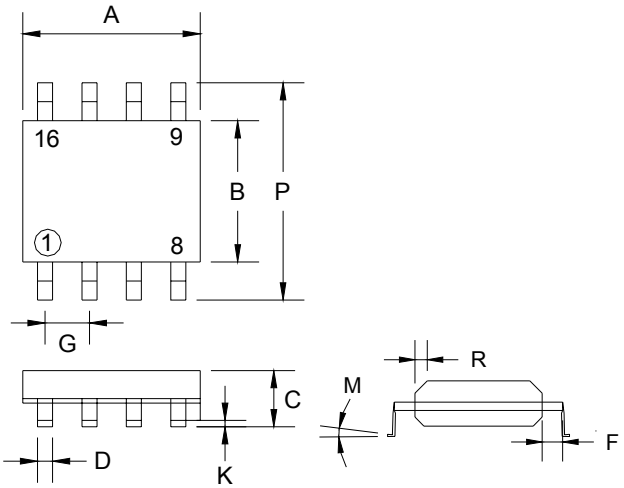
$$Rs = R1 \,||\, R2$$

$$Vth1 = Vref + \frac{(Vcc - Vref) * R1}{R1 + R2 + RL}$$

$$Vth2 = Vref - \frac{(Vref - Vo\ low) * R1}{R1 + R2}$$

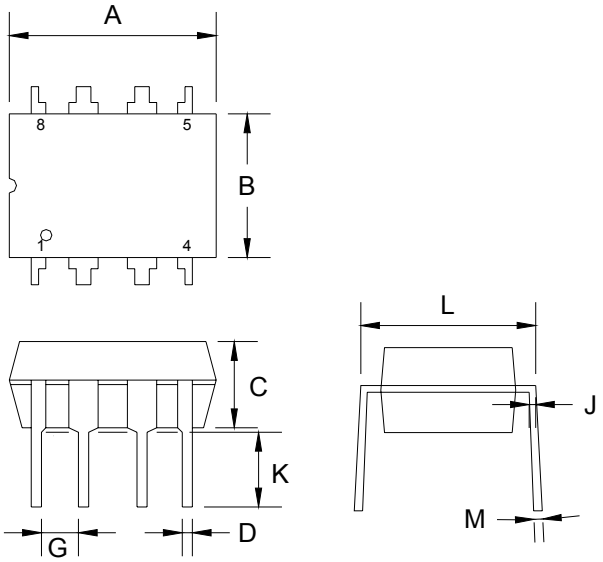
Figure 8. comparator with hysteresis

SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DIP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.07	9.32	0.357	0.367
B	6.22	6.48	0.245	0.255
C	3.18	4.45	0.125	0.135
D	0.35	0.55	0.019	0.020
G	2.54 (typ)		0.10 (typ)	
J	0.29	0.31	0.011	0.012
K	3.25	3.35	0.128	0.132
L	7.75	8.00	0.305	0.315
M	-	10°	-	10°