IEC LEVEL 4 ESD-PROTECTED 0.75-Ω SPDT ANALOG SWITCH WITH 1.8-V COMPATIBLE INPUT LOGIC

FEATURES

- Low ON-State Resistance (0.75 Ω)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Isolation in Power-Down Mode, V_+ = 0
- Specified Break-Before-Make Switching
- 2.25-V to 5.5-V Power Supply (V_+)
- 6-MΩ Input Pulldown Allows Control Input (IN) to Be Unconnected
- 1.8-V Compatible Control Input Threshold Indepedent of V_+
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 3000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- ESD Performance COM Port to GND
  - 8000-V Human-Body Model (A114-B, Class II)
  - ±8-kV Contact Discharge (IEC 61000-4-2)
  - ±15-kV Air-Gap Discharge (IEC 61000-4-2)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- MP3 Players
- Portable Media Players

YFP PACKAGE

(Laser Marking View) (Bump View)

TERMINAL ASSIGNMENTS

C	V_+	NC
B	COM	GND
A	IN	NO
	2	**1**

DESCRIPTION/ORDERING INFORMATION

The TS5A12301E is a single-pole double-throw (SPDT) analog switch that is designed to operate from 2.25 V to 5.5 V. The device offers a low ON-state resistance with an excellent channel-to-channel ON-state resistance matching, and the break-before-make feature to prevent signal distortion during the transferring of a signal from one path to another.

The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications. The control input (IN) pin can be connected to low-voltage GPIOs, allowing it to be controlled by 1.8-V signals.

The TS5A12301E has ±15-kV Air-Gap Discharge and ±8-kV Contact Discharge ESD protection for the COM port to GND, which make it compliant with the IEC Level 4 ESD standard (IEC 61000-4-2).

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	WCSP (DSBGA) 0.4-mm Pitch – YFP (Pb-free)	Tape and reel	TS5A12301EYFPR	_ _ _ 3W_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) YFP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

SUMMARY OF CHARACTERISTICS(1)

Configuration	2:1 Multiplexer/Demultiplexer (1 × SPDT)
Number of channels	1
ON-state resistance (r_{on})	0.75 Ω max
ON-state resistance match (Δr_{on})	0.1 Ω max
ON-state resistance flatness ($r_{on(flat)}$)	0.1 Ω max
Turn-on/turn-off time (t_{ON}/t_{OFF})	110 ns/100 ns
Break-before-make time (t_{BBM})	10 ns
Charge injection (Q_C)	97 pC
Bandwidth (BW)	55 MHz
OFF isolation (O_{ISO})	–63 dB at 1 MHz
Crosstalk (X_{TALK})	–63 dB at 1 MHz
Total harmonic distortion (THD)	0.003%
Leakage current ($I_{NO(OFF)}/I_{NC(OFF)}$)	20 nA
Package option	6-pin WCSP, 0.4-mm pitch

(1) V_+ = 5 V, T_A = 25°C

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L or Open	ON	OFF
H	OFF	ON

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6.5	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3)(4)(5)		–0.5	V_+ + 0.5	V
I_{IK}	Analog port diode current	$V_+ < V_{NC}$, V_{NO}, V_{COM} or V_{NC}, V_{NO}, $V_{COM} < 0$	–50	50	mA
I_{NC} I_{NO} I_{COM}	On-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–200	200	mA
	On-state peak switch current(6)		–400	400	
V_I	Digital input voltage range(3)(4)		–0.5	6.5	V
I_{IK}	Digital input clamp current	$V_I < 0$	–50		mA
I_+ I_{GND}	Continuous current through V_+ or GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance(1)	YFP package	154.2	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	See Figure 14	25°C	4.5 V		0.5	0.75	Ω
				Full				0.8	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –100 mA,	See Figure 14	25°C	4.5 V		0.05	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	See Figure 14	25°C	4.5 V		0.15		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	See Figure 14	25°C			0.1	0.2	
				Full				0.25	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} = 1 V, 4.5 V, V_{COM} = 4.5 V, 1 V, V_{NC} = Open, or V_{NO} = 1 V, 4.5 V, V_{COM} = 4.5 V, 1 V, V_{NO} = Open,	See Figure 15	25°C	5.5 V	–20	2	20	nA
				Full		–100		100	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NO} or V_{NC} = 0 to 5.5 V, V_{COM} = 5.5V to 0	See Figure 15	25°C	0 V	–10		10	µA
				Full		–10		10	
NC, NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, 4.5 V, V_{COM}, V_{NC} = Open, or V_{NC} = 1 V, 4.5 V, V_{COM}, V_{NO} = Open,	See Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–200		200	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, 4.5 V, V_{NO} and V_{NC} = Open, or V_{COM} = 1 V, 4.5 V, V_{NO} or V_{NC} = Open,	See Figure 16	25°C	5.5 V	–20	2	20	nA
				Full		–200		200	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or V_{NC} = 0 to 5.5 V, V_{COM} = 5.5V to 0	See Figure 15	25°C	0 V	–10		10	µA
				Full		–10		10	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full	5.5 V	1.05		5.5	V
Input logic low	V_{IL}			Full	5.5 V	0		0.65	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		Full	5.5 V	–0.05		0.5	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	5.5 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 18	25°C	5 V		110	225	ns
				Full	4.5 V			250	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	5 V		100	215	ns
				Full	4.5 V			225	
Break-before-make time	t_{BBM}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V	1	10	15	ns
				Full	4.5 V	1		20	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	5 V		97		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 17	25°C	5 V		28		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 17	25°C	5 V		112		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 17	25°C	5 V		112		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 17	25°C	5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	5 V		55		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 21	25°C	5 V		–63		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 22	25°C	5 V		–63		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.003		%
Supply									
Positive supply current	I+	V_I = V_+ or GND		Full	5.5 V			10	µA

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		0.75	0.9	Ω
				Full				1.2	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	3 V		0.2		Ω
		V_{NO} or V_{NC} = 0.8 V, 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C			0.1	0.2	
				Full				0.3	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} = 1 V, 3 V, V_{COM} = 3 V, 1 V, V_{NC} = Open, or V_{NC} = 1 V, 3 V, V_{COM} = 3 V, 1 V, V_{NO} = Open,	Switch OFF, See Figure 15	25°C	3.6 V	–20	2	20	nA
				Full		–50		50	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NO} or V_{NC} = 0 to 3.6 V, V_{COM} = 3.6V to 0		25°C	0 V	–10		10	µA
				Full		–10		10	
NC, NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V, 3 V, V_{NC} and V_{COM} = Open, or V_{NC} = 1 V, 3 V, V_{NO} and V_{COM} = Open,	Switch ON, See Figure 16	25°C	3.6 V	–20	2	20	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NO} and V_{NC} = Open, or V_{COM} = 3 V, V_{NO} and V_{NC} = Open,	See Figure 16	25°C	3.6 V	–20	2	20	nA
				Full		–100		100	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0	See Figure 15	25°C	0 V	–10		10	µA
				Full		–10		10	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full	3.6 V	1.05		5.5	V
Input logic low	V_{IL}			Full	3.6 V	0		0.65	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		Full	3.6 V	–0.05		0.5	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	3.6 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 18	25°C	3.3 V		72	175	ns
				Full	3 V			185	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	3.3 V		105	165	ns
				Full	3 V			170	
Break-before-make time	t_{BBM}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V	1	16	30	ns
				Full	3 V	1		35	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3V		97		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 17	25°C	3.3 V		28		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 17	25°C	3.3 V		115		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 17	25°C	3.3 V		115		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 17	25°C	3.3 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	3.3 V		54		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 21	25°C	3.3 V		–63		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 22	25°C	3.3 V		–63		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.004		%
Supply									
Positive supply current	I+	V_I = 1.95 V or GND		25°C	3.6 V			10	µA

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.25 V to 2.75 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}					0		V_+	V
ON-state resistance	r_{on}	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	2.25 V		1.1	1.3	Ω
				Full				1.6	
ON-state resistance match between channels	Δr_{on}	V_{NO} or V_{NC} = 1.8 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	2.25 V		0.15	0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO} or V_{NC}) ≤ V_+, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C	2.25 V		0.4		Ω
		V_{NO} or V_{NC} = 0.8 V, 1 V, 1.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 14	25°C			0.25	0.5	
				Full				0.6	
NO, NC OFF leakage current	$I_{NO(OFF)}$, $I_{NC(OFF)}$	V_{NO} = 0.5 V, 2.2 V, V_{COM} = 2.2 V, 0.5 V, V_{NC} = Open, or V_{NC} = 0.5 V, 2.2 V, V_{COM} = 2.2 V, 0.5 V, V_{NO} = Open,	Switch OFF, See Figure 15	25°C	2.75 V	–20	2	20	nA
				Full		–50		50	
	$I_{NO(PWROFF)}$, $I_{NC(PWROFF)}$	V_{NO} or V_{NC} = 0 to 2.75 V, V_{COM} = 2.75 V to 0		25°C	0 V	–10		10	µA
				Full		–10		10	
NC, NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V, 2.2 V, V_{NC} and V_{COM} = Open, or V_{NC} = 2.2 V, 0.5 V, V_{NO} and V_{COM} = Open,	Switch ON, See Figure 16	25°C	2.75 V	–20	2	20	nA
				Full		–100		100	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 0.5 V, V_{NO} and V_{NC} = Open, or V_{COM} = 2.2 V, V_{NO} and V_{NC} = Open,	Switch ON, See Figure 16	25°C	2.75 V	–20	2	20	nA
				Full		–100		100	
COM OFF leakage current	$I_{COM(PWROFF)}$	V_{NO} or V_{NC} = 0 to 2.75 V, V_{COM} = 2.75 V to 0	See Figure 15	25°C	0 V	–10		10	µA
				Full		–10		10	
Digital Control Input (IN)									
Input logic high	V_{IH}			Full	2.75 V	1.05		5.5	V
Input logic low	V_{IL}			Full	2.75 V	0		0.65	V
Input leakage current	I_{IH}, I_{IL}	V_I = 1.95 V or 0		Full	2.75 V	–0.05		0.5	µA
Input resistance	r_{IN}	V_I = 1.95 V		Full	2.75 V		6		MΩ

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (continued)

V_+ = 2.25 V to 2.75 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 50 Ω,	C_L= 35 pF, See Figure 18	25°C	2.5 V		97	170	ns
				Full	2.25 V			175	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 18	25°C	2.5 V		80	155	ns
				Full	2.25 V			160	
Break-before-make time	t_{BBM}	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	5	18	35	ns
				Full	2.25 V	5		40	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		82		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_+ or GND, Switch OFF,	See Figure 17	25°C	2.5 V		29		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 17	25°C	2.5 V		116		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON,	See Figure 17	25°C	2.5 V		116		pF
Digital input capacitance	C_I	V_I = V_+ or GND,	See Figure 17	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	2.5 V		54		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	See Figure 21	25°C	2.5 V		–63		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	See Figure 22	25°C	2.5 V		–63		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.008		%
Supply									
Positive supply current	I+	V_I = 1.95 V or GND		Full	2.75 V			10	µA

TYPICAL PERFORMANCE

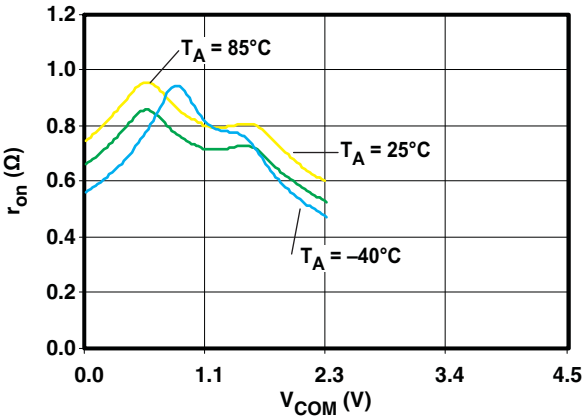


Figure 1. r_{on} vs V_{COM} (V_+ = 2.25 V)

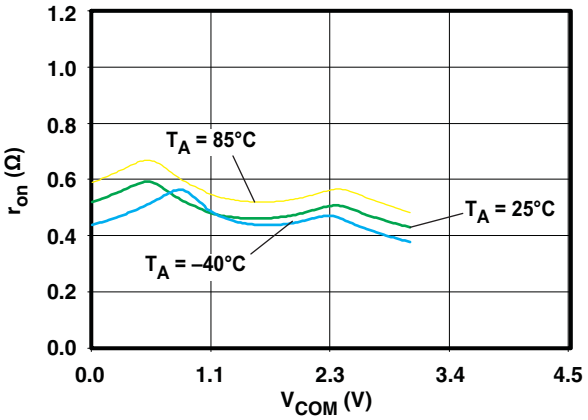


Figure 2. r_{on} vs V_{COM} (V_+ = 3 V)

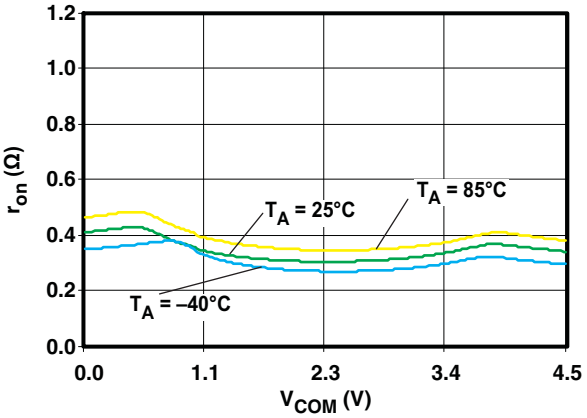


Figure 3. r_{on} vs V_{COM} (V_+ = 4.5 V)

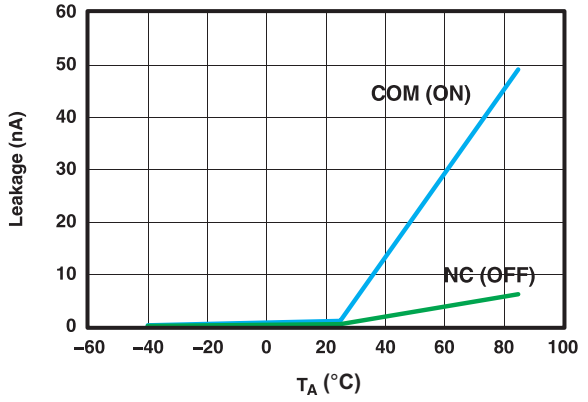


Figure 4. Leakage Current vs Temperature (V_+ = 5 V)

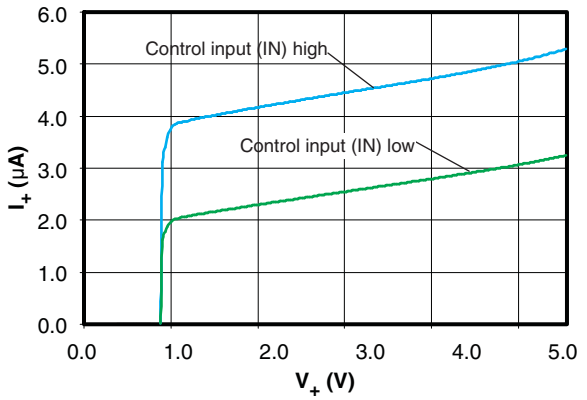


Figure 5. I_+ vs V_+ (T_A = 25°C)

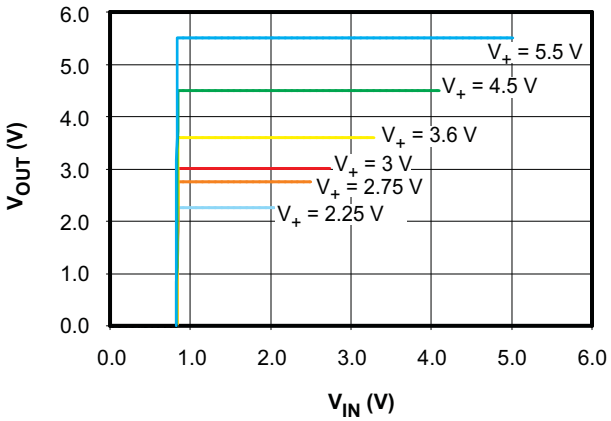


Figure 6. Control Input Thresholds

TYPICAL PERFORMANCE (continued)

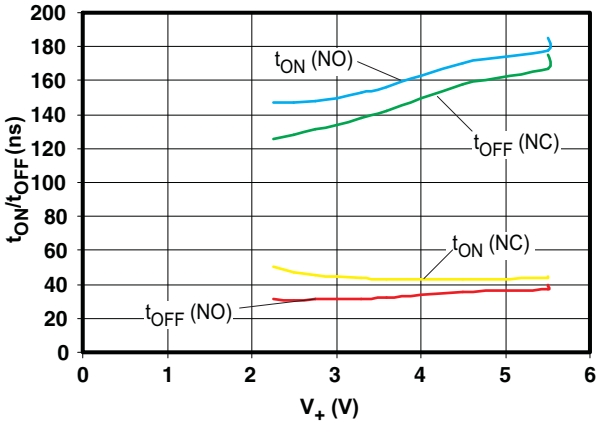


Figure 7. t_{ON}/t_{OFF} vs Supply Voltage

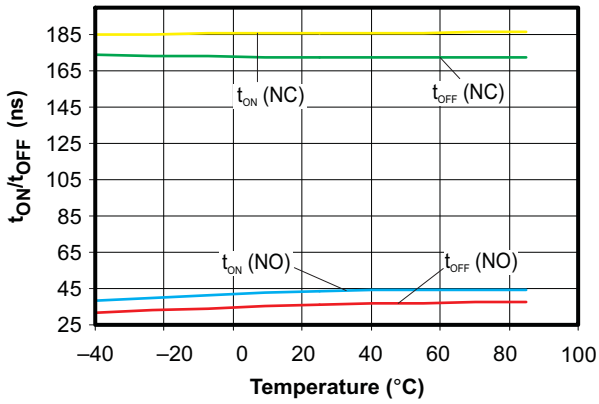


Figure 8. t_{ON}/t_{OFF} vs Temperature

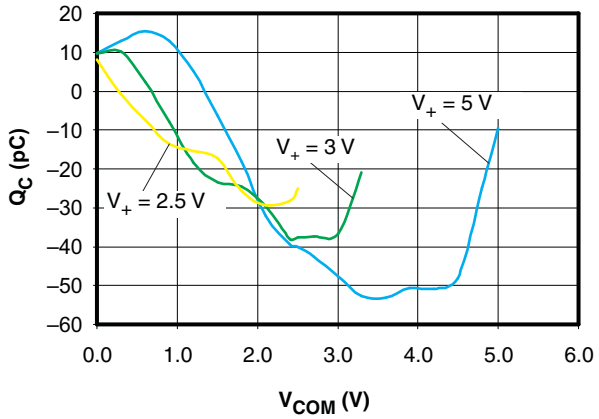


Figure 9. Charge Injection (Q_C) vs V_{COM}

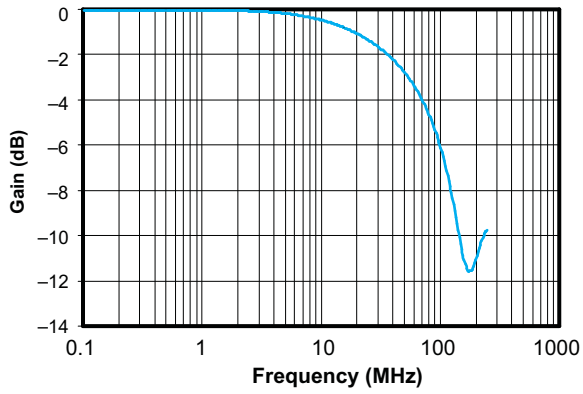


Figure 10. Gain vs Frequency

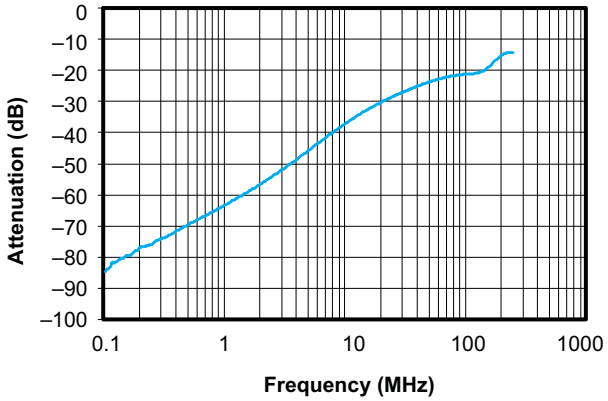


Figure 11. OFF Isolation vs Frequency

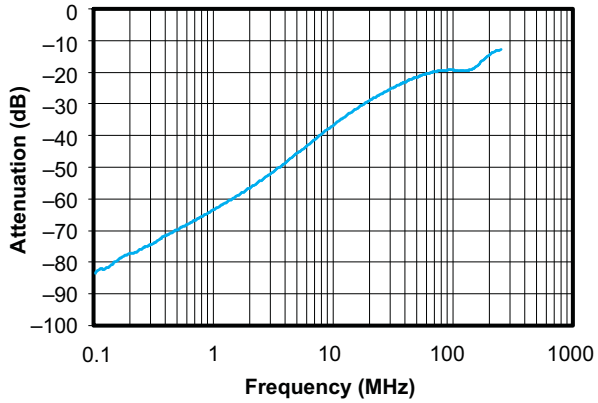


Figure 12. Crosstalk vs Frequency

TYPICAL PERFORMANCE (continued)

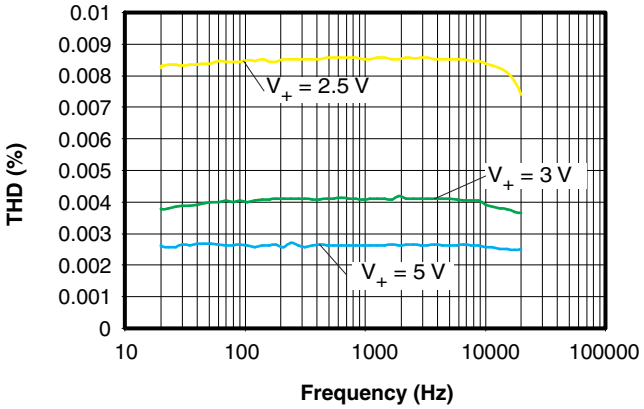


Figure 13. Total Harmonic Distortion (THD) vs Frequency

PARAMETER MEASUREMENT INFORMATION

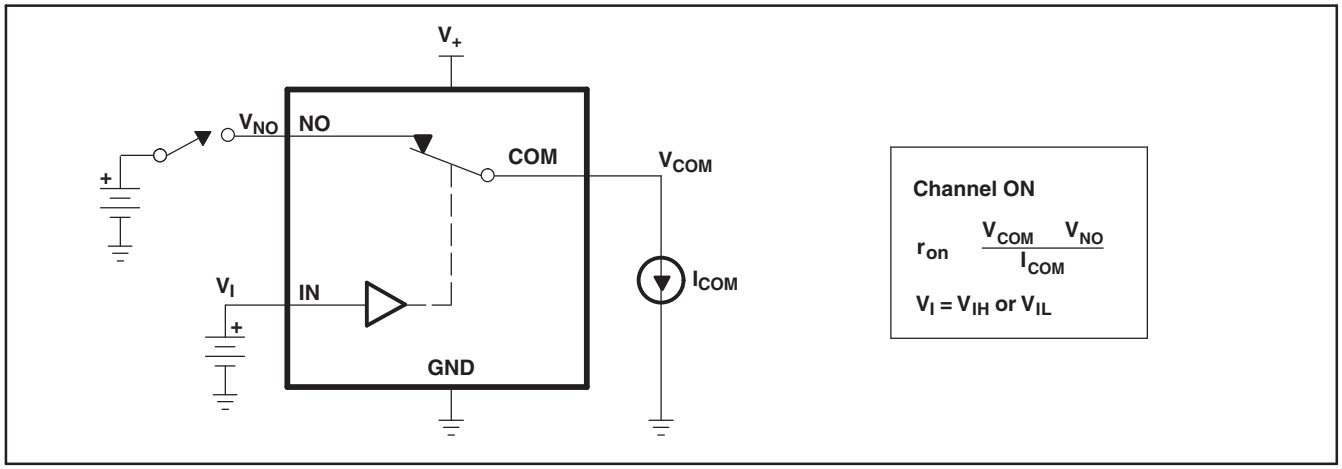


Figure 14. ON-State Resistance (r_{on})

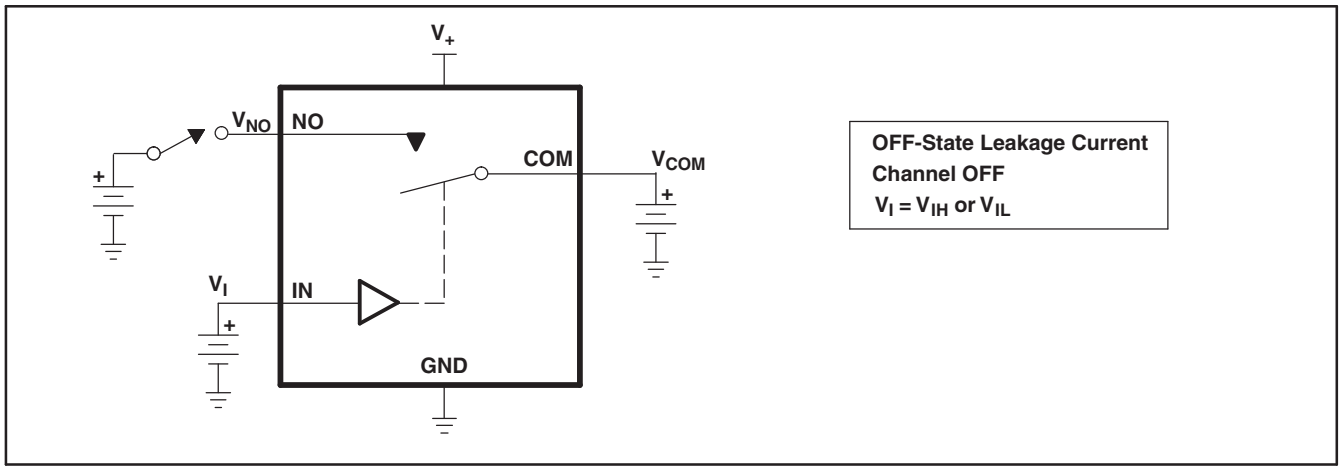


Figure 15. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWR(FF)}$)

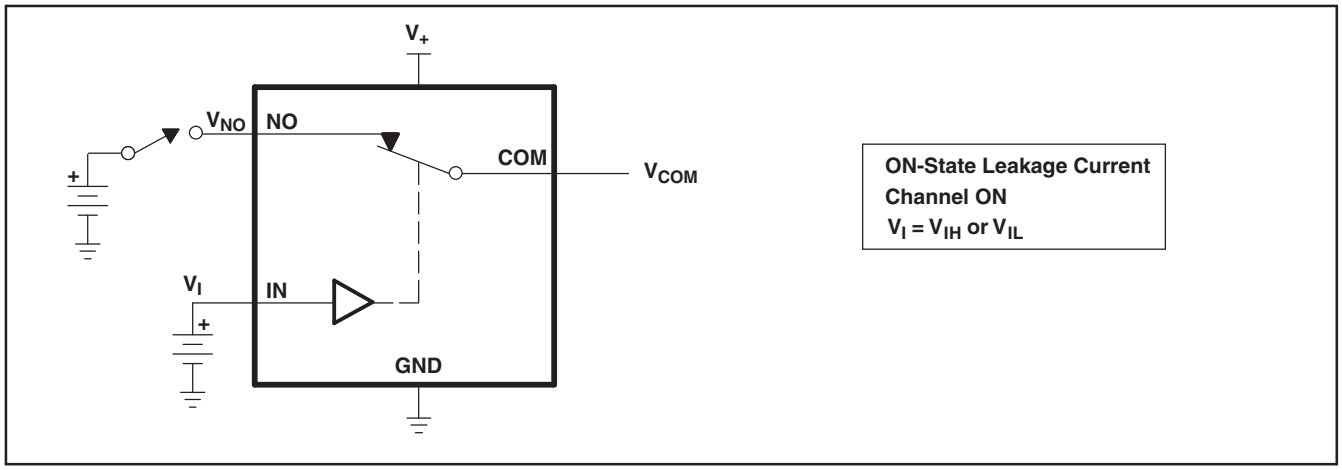


Figure 16. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

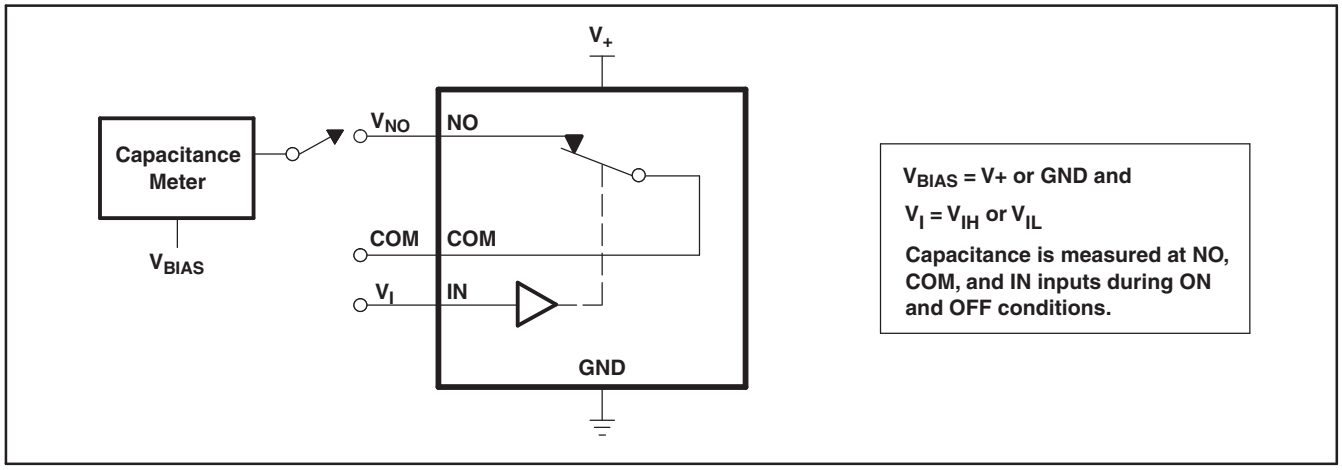
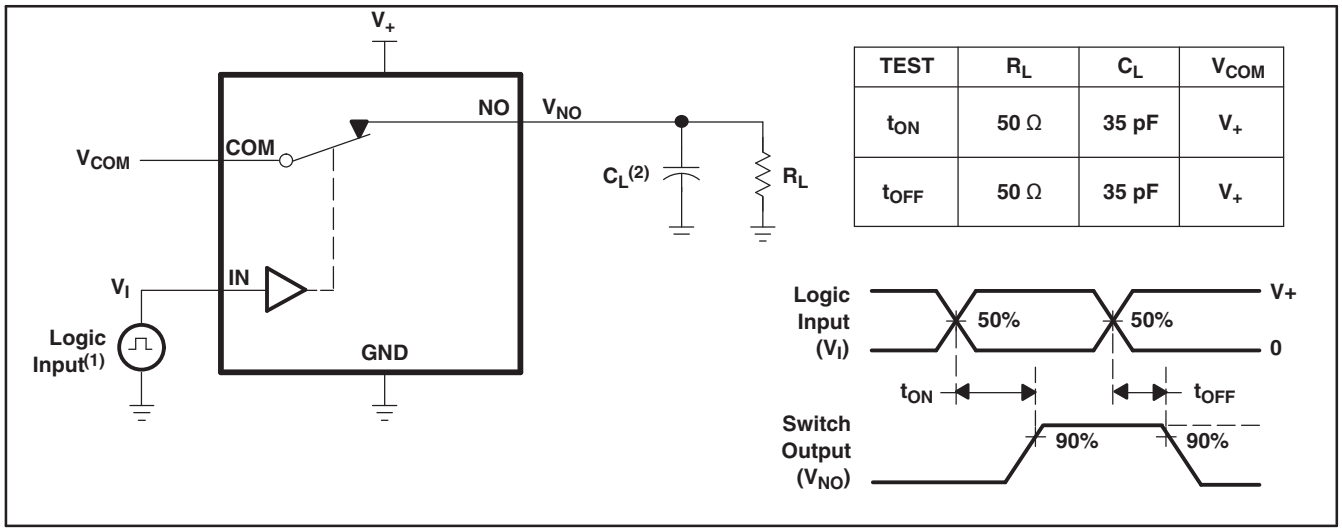


Figure 17. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



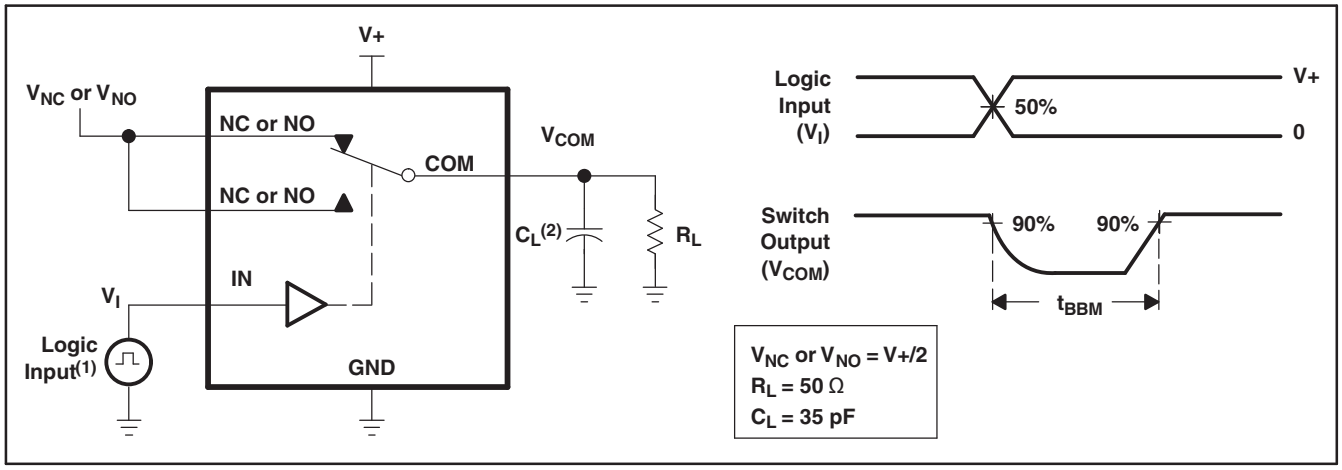
TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 18. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 19. Break-Before-Make Time (t_{BBM})

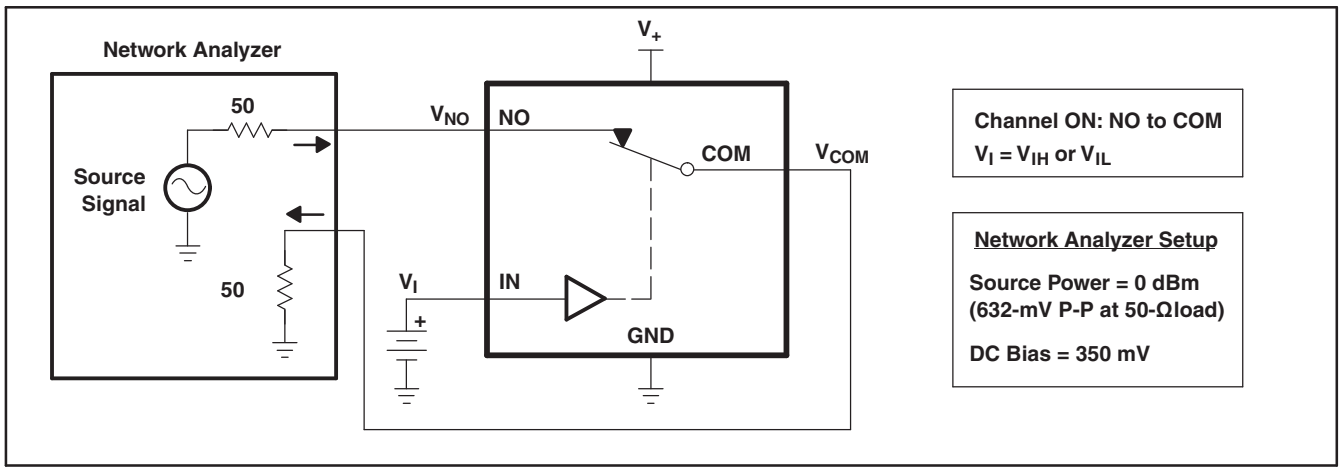


Figure 20. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

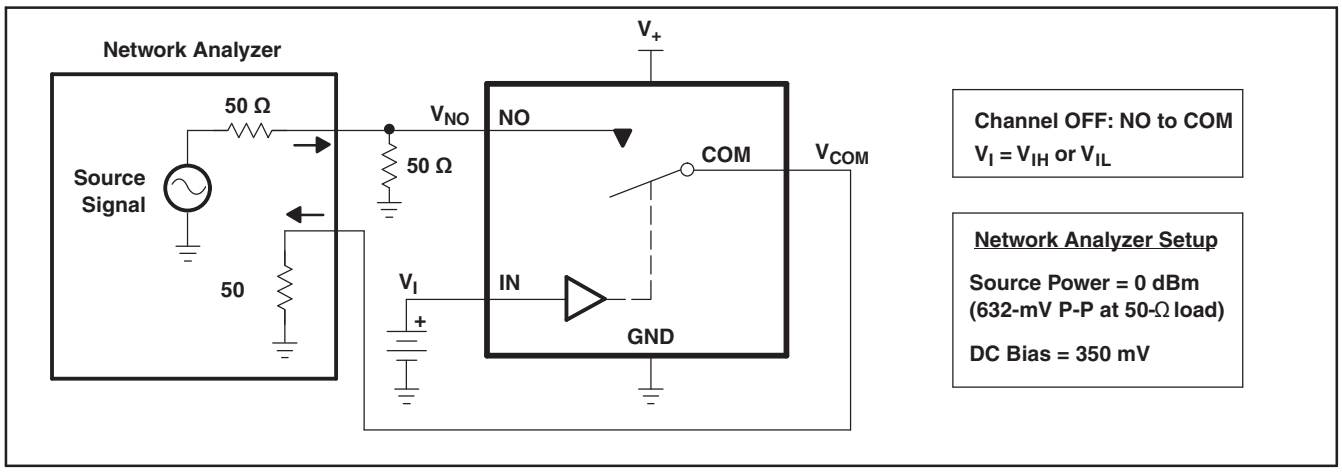


Figure 21. OFF Isolation (O_{ISO})

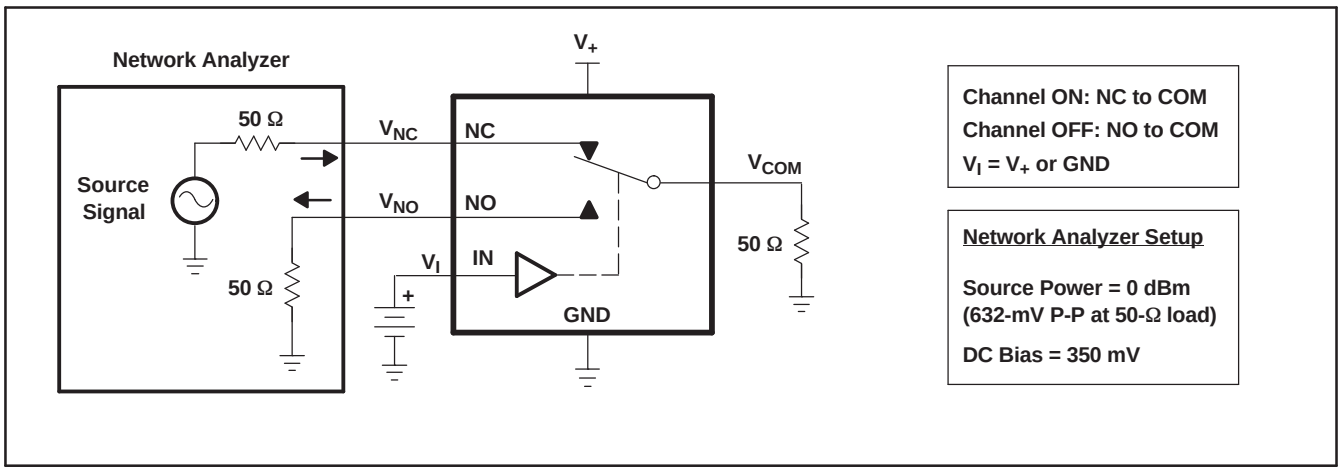
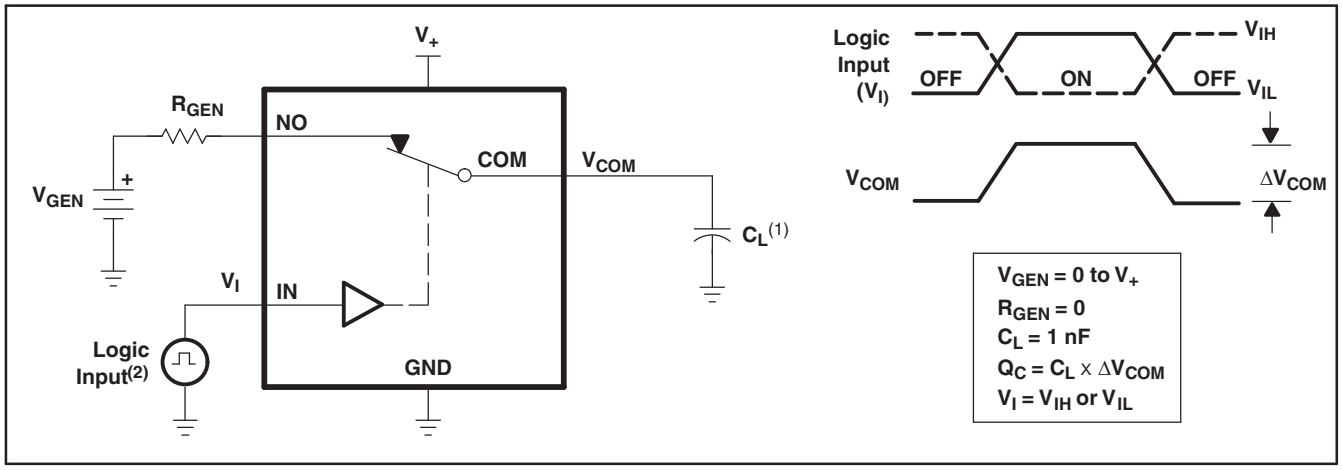


Figure 22. Crosstalk (X_{TALK})

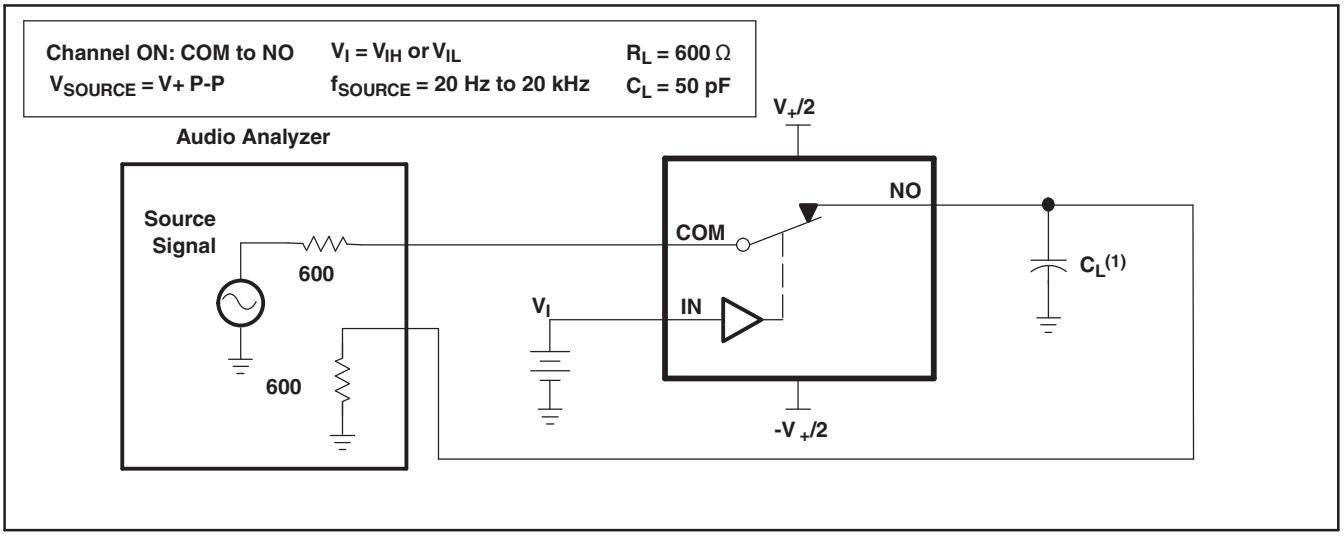
PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

Figure 23. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD)

PACKAGE OPTION ADDENDUM

14-Aug-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS5A12301EYFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

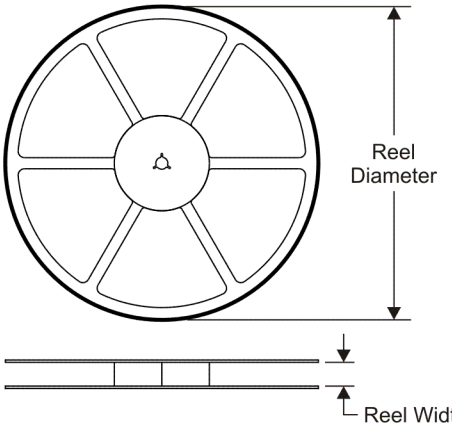
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

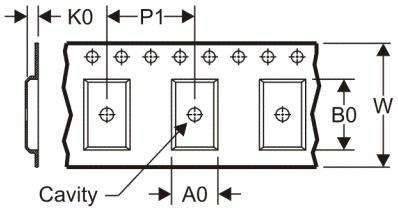
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

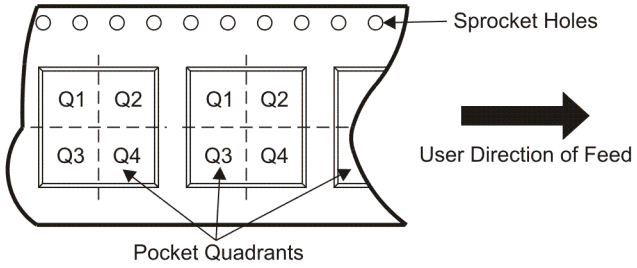


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

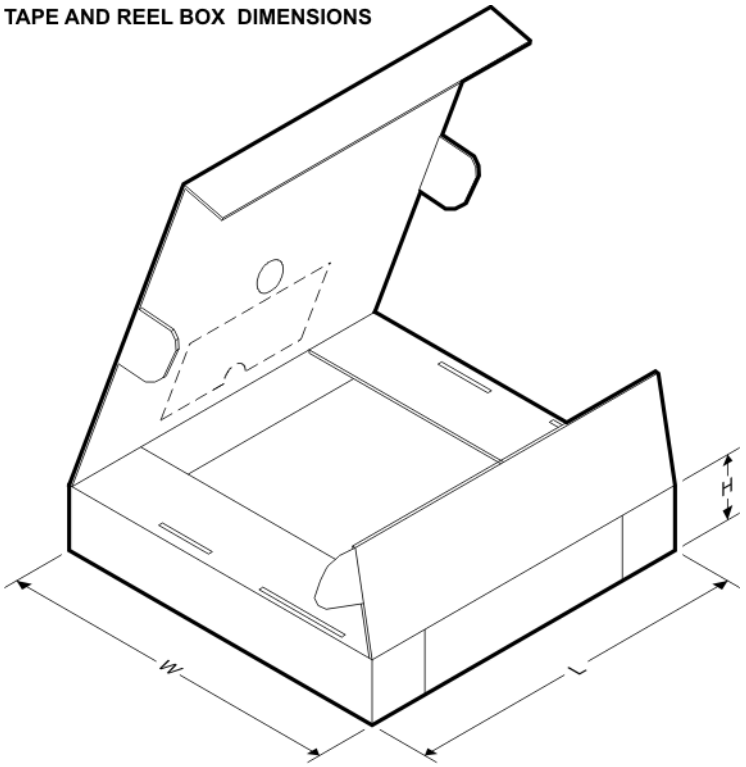
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A12301EYFPR	DSBGA	YFP	6	3000	180.0	8.4	0.9	1.3	0.6	4.0	8.0	Q1

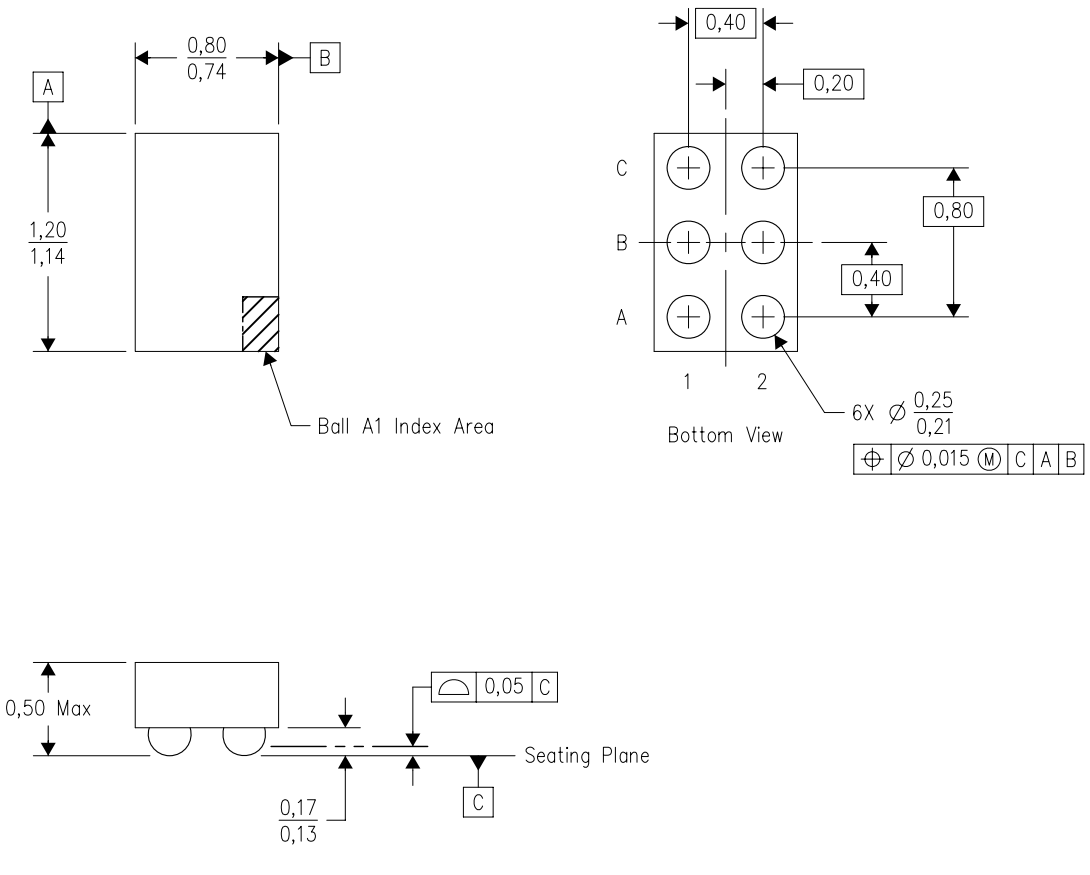
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A12301EYFPR	DSBGA	YFP	6	3000	220.0	220.0	34.0

YFP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



4206986–3/O 08/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This is a Pb–free solder ball design.

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