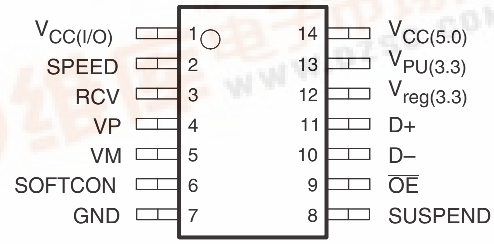
FEATURES

- **Complies With Universal Serial Bus Specification Rev. 2.0 (USB 2.0)**
- **Transmits and Receives Serial Data at Both Full-Speed (12-Mbit/s) and Low-Speed (1.5-Mbit/s) Data Rates**
- **Integrated Bypassable 5-V to 3.3-V Voltage Regulator for Powering Via USB VBUS**
- **Low-Power Operation, Ideal for Portable Equipment**
- **Meets the IEC-61000-4-2 Contact (±9KV) and Air-gap (±9KV) ESD Ratings**
- **Separate I/O Supply With Operation Down to 1.65 V**
- **Very-Low Power Consumption to Meet USB Suspend Current Requirements**
- **No Power-Supply Sequencing Requirements**

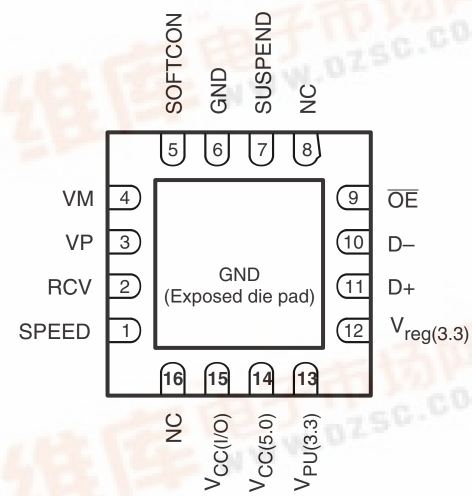
APPLICATIONS

- **Cellular Phones**
- **Personal Digital Assistants (PDAs)**
- **Handheld Computers**

PW PACKAGE
(TOP VIEW)



RGT PACKAGE
(BOTTOM VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TUSB2551 is a single-chip transceiver that complies with the physical-layer specifications of universal serial bus (USB) 2.0. The device supports both full-speed (12-Mbit/s) and low-speed (1.5-Mbit/s) operation. The TUSB2551 delivers superior edge rate control, producing crisper eye diagrams, which ease the task of passing USB compliance testing.

A dual supply-voltage operation allows the TUSB2551 to reference the system interface I/O signals to a supply voltage down to 1.6 V, while independently powered by the USB $V_{CC(5.0)}$. This allows the system interface to operate at its core voltage without the addition of buffering logic, and also reduce system operating current.

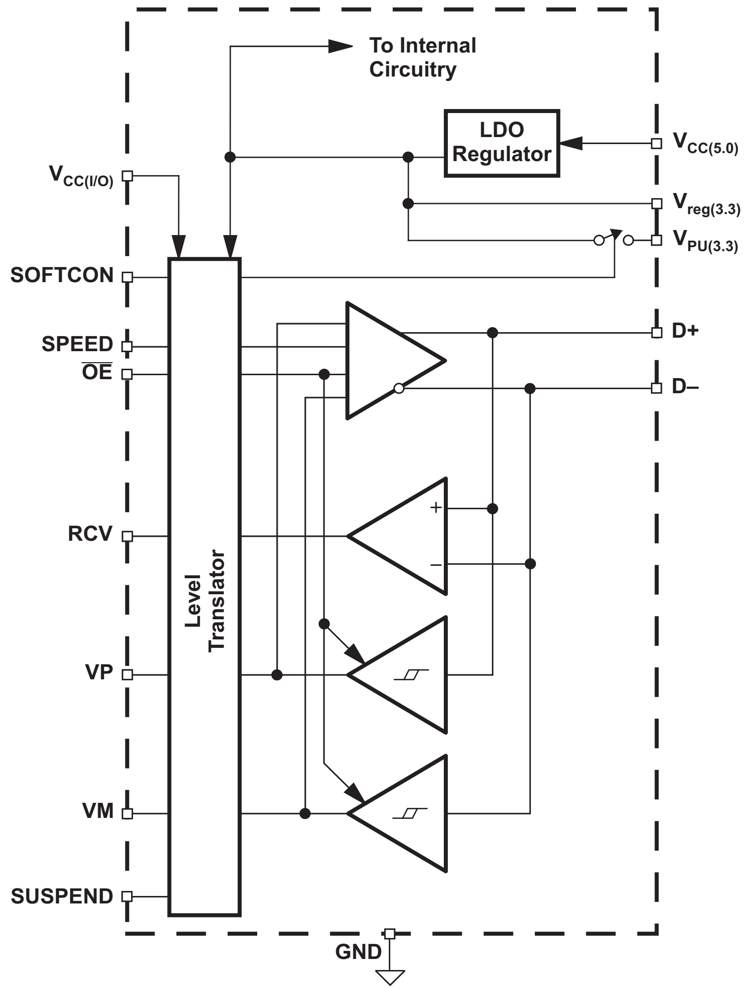
ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGT	Reel of 2000	TUSB2551RGTR	ZWT
	TSSOP – PW	Reel of 3000	TUSB2551PWR	TU2551

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	RGT NO.	PW NO.		
$V_{CC(I/O)}$	15	1	I	System interface supply voltage. Used to provide reference supply voltage for system I/O interface signaling.
SPEED	1	2	I	Speed. Edge-rate control: A logic HIGH operates at edge rates for full-speed operation. A logic LOW operates at edge rates for low-speed operation.
RCV	2	3	O	Receive data. Output for USB differential data.
VP	3	4	I/O	If $\overline{OE}$ = 1, VP = Receiver output (+) If $\overline{OE}$ = 0, VP = Driver input (+)
VM	4	5	I/O	If $\overline{OE}$ = 1, VM = Receiver output (–) If $\overline{OE}$ = 0, VM = Driver input (–)
SOFTCON	5	6	I	Soft connect. Controls state of $V_{PU(3.3)}$. Refer to $V_{PU(3.3)}$ pin description for details.
GND	6	7		Ground reference
SUSPEND	7	8	I	Suspend. Active high. Turns off internal circuits to reduce supply current.
NC	8, 16			No internal connection
$\overline{OE}$	9	9	I	Output enable. Active low. Enables the transceiver to transmit data onto the bus. When inactive, the transceiver is in the receive mode.
D–, D+	10, 11	10, 11	I/O	Differential data lines conforming to the USB standard
$V_{reg(3.3)}$	12	12	O	3.3-V reference supply. Requires a minimum 0.1-µF decoupling capacitor for stability. A 1-µF capacitor is recommended.
$V_{PU(3.3)}$	13	13	O	Pullup supply voltage. Used to connect 1.5-kΩ pullup speed detect resistor. If SOFTCON = 1, $V_{PU(3.3)}$ is high impedance. If SOFTCON = 0, $V_{PU(3.3)}$ = 3.3 V.
$V_{CC(5.0)}$	14	14	I	USB bus supply voltage. Used to power USB transceiver and internal circuitry.

FUNCTIONAL DESCRIPTION

FUNCTION SELECTION

SUSPEND	$\overline{OE}$	D+, D–	RCV	VP, VM	FUNCTION
0	0	Driving	Active	Active	Normal transmit mode
0	1	Receiving	Active	Active	Normal receive mode
1	0	Hi-Z	0	Not active	Low power state
1	1	Hi-Z	0	Active	Receiving during suspend (low power state)(1)

(1) During suspend, VP and VM are active in order to detect out-of-band signaling conditions.

TRUTH TABLE DURING NORMAL MODE

$\overline{OE}$ = 0					
INPUT		OUTPUT			RESULT
VP	VM	D+	D–	RCV	
0	0	0	0	X(1)	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X(1)	Undefined
$\overline{OE}$ = 1					
Input		Output			RESULT
D+	D–	VP	VM	RCV	
0	0	0	0	X(1)	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X(1)	Undefined

(1) X = Undefined

TEXAS INSTRUMENTS
www.ti.com

Power-Supply Configurations

The TUSB2551 can be used with different power-supply configurations, which can be dynamically changed. An overview is given in Table 1.

- Normal mode – Both $V_{CC(I/O)}$ and $V_{CC(5.0)}$ or $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected. For 5-V operation, $V_{CC(5.0)}$ is connected to a 5-V source (4 V to 5.5 V). The internal voltage regulator then produces 3.3 V for the USB connections. For 3.3-V operation, both $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to a 3.3-V source (3 V to 3.6 V). $V_{CC(I/O)}$ is independently connected to a voltage source (1.65 V to 3.6 V), depending on the supply voltage of the external circuit.
- Disable mode – $V_{CC(I/O)}$ is not connected; $V_{CC(5.0)}$ or $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected. In this mode, the internal circuits of the TUSB2551 ensure that the D+ and D– pins are in 3-state, and the power consumption drops to the low-power (suspended) state level. Some hysteresis is built into the detection of $V_{CC(I/O)}$ lost.
- Sharing mode – $V_{CC(I/O)}$ is connected; $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are not connected. In this mode, the D+ and D– pins are made 3-state, and the TUSB2551 allows external signals of up to 3.6 V to share the D+ and D– lines. The internal circuits of the TUSB2551 ensure that virtually no current (maximum 10 mA) is drawn via the D+ and D– lines. The power consumption through $V_{CC(I/O)}$ drops to the low-power (suspended) state level. Both the VP and VM pins are driven HIGH to indicate this mode. Pin RCV is made LOW. Some hysteresis is built into the detection of $V_{reg(3.3)}$ lost.

Table 1. Power-Supply Configuration Overview

Configuration Mode	VBUS/VTRM	VIF	Notes
Normal	Connected	Connected	Normal supply configuration and operation.
Disconnect (D+/D– sharing)	Open	Connected	VP/VM are HIGH outputs, RCV is LOW. With OE# = 0 and SUSPEND = 1, data lines may be driven with external devices up to 3.6 V. With D+, D– floating, $I_{CC(I/O)}$ draws less than 1 µA.
Disconnect	Ground	Connected	VP/VM are HIGH outputs, RCV is LOW. With D+, D– floating, $I_{CC(I/O)F}$ draws less than 1 µA.
Disable Mode	Connected	Open	Logic controlled inputs pins are Hi-Z
Prohibited	Connected	Ground	Prohibited condition

Table 2. Pin States in Disable or Sharing Mode

PINS	DISABLE-MODE STATE	SHARING-MODE STATE
$V_{CC(5.0)}/V_{reg(3.3)}$	5-V input/3.3-V output, 3.3-V input/3.3-V input	Not present
$V_{CC(I/O)}$	Not present	1.65-V to 3.6-V input
$V_{PU(3.3)}$	High impedance (off)	High impedance (off)
D+, D–	High impedance	High impedance
VP, VM	Invalid [1]	H
RCV	Invalid [1]	L
Inputs (SPEED, SUSPEND, $\overline{OE}$, SOFTCON)	High impedance	High impedance

(1) High impedance or driven LOW

Power-Supply Input Options

The TUSB2551 has two power-supply input options.

- Internal regulator – $V_{CC(5.0)}$ is connected to 4 V to 5.5 V. The internal regulator is used to supply the internal circuitry with 3.3 V (nominal). $V_{reg(3.3)}$ becomes a 3.3-V output reference.
- Regulator bypass – $V_{CC(5.0)}$ and $V_{reg(3.3)}$ are connected to the same supply. The internal regulator is bypassed, and the internal circuitry is supplied directly from the $V_{reg(3.3)}$ power supply. The voltage range is 3 V to 3.6 V to comply with the USB specification.

The supply-voltage range for each input option is specified in Table 3.

Table 3. Power-Supply Input Options

INPUT OPTION	$V_{CC(5.0)}$	$V_{reg(3.3)}$	$V_{CC(I/O)}$
Internal regualtor	Supply input for internal regulator (4 V to 5.5 V)	Voltage-reference output (3.3 V, 300 μA)	Supply input for digital I/O pins (1.4 V to 3.6 V)
Regulator bypass	Connected to $V_{reg(3.3)}$ with maximum voltage drop of 0.3 V (2.7 V to 3.6 V)	Supply input (3 V to 3.6 V)	Supply input for digital I/O pins (1.4 V to 3.6 V)

Electrostatic Discharge (ESD)

PIN NAME	ESD	TYP	UNIT
D+, D–, $V_{CC(5.0)}$	IEC61000-4-2, Air-Gap Discharge	±9	kV
	IEC61000-4-2, Contact Discharge	±9	
	Human-Body Model	±15	
All other pins	Human-Body Model	±2	kV

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC(5.0)}$	Supply voltage range	–0.5	6	V
$V_{CC(I/O)}$	I/O supply voltage range	–0.5	4.6	V
$V_{reg(3.3)}$	Regulated voltage range	–0.5	4.6	V
V_I	DC input voltage range	–0.5	$V_{CC(I/O)}$ + 0.5	mA
$I_{O(D+, D-)}$	Output Current (D+, D-)		±50	mA
I_O	Output Current (all others)		±15	mA
I_I	Input Current		±50	mA
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(5.0)}$	Supply voltage, internal regulator option	5-V operation	4	5	5.25	V
$V_{reg(3.3)}$	Supply voltage, regulator bypass option	3.3-V operation	3	3.3	3.6	V
$V_{CC(I/O)}$	I/O supply voltage		1.65		3.6	V
V_{IL}	Low-level input voltage(1)		$V_{CC(I/O)}$ –0.3		0.15 $V_{CC(I/O)}$	V
V_{IH}	High-level input voltage(1)		0.85 $V_{CC(I/O)}$		$V_{CC(I/O)}$ + 0.3	V
D+, D–	Input voltage on analog I/O pins		0		3.6	V
T_c	Junction temperature range		–40		85	°C

(1) Specification applies to the following pins: SUSPEND, SPEED, RCV, SOFTCON, VP, VM, $\overline{OE}$

DC ELECTRICAL CHARACTERISTICS SYSTEM AND USB INTERFACE[1]

$V_{CC(I/O)}$ = 3.6 V, $V_{CC(5.0)}$ = 5 V (unless otherwise noted), T_A = 25 C. Bold indicates specifications over temperature, –40°C to 85°C

PARAMETER		TEST CONDITIONS					MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage[2]	I_{OH} = 20 µA					0.9 $V_{CC(I/O)}$			V
V_{OL}	Low-level output voltage[2]	I_{OL} = 20 µA							0.1	V
I_{IL}	Input leakage current[2]						–5	1.5	5	µA
$I_{CC(I/O)}$	$V_{CC(I/O)}$ supply current	**SPEED**	**SUSPEND**	**$\overline{OE}$**	**VOLTAGE**	**LOAD**				
		1	0	1	$V_{CC(5.0)}$ = 5.25 V, $V_{CC(I/O)}$ = 3.6 V			1	5	µA
		1	0	0				1	5	µA
		0	0	1				1	5	µA
		0	0	0				1	5	µA
		0	1	0				1	5	µA
		1	0	0		f = 6 MHz, C_L = 50 pF		1	2	mA
		0	0	0		f = 750 kHz, C_L = 600 pF		260	280	µA
$I_{CC(5.0)}$	$V_{CC(5.0)}$ supply current	1	0	1	$V_{CC(5.0)}$ = 5.25 V, $V_{CC(I/O)}$ = 3.6 V			800	1100	µA
		1	0	0				3000	5000	µA
		0	0	1				230	350	µA
		0	0	0				400	700	µA
		0	1	0				130	200	µA
		1	0	0		f = 6 MHz, C_L = 50 pF		6	10	mA
		0	0	0		f = 750 kHz, C_L = 600 pF		4..3	5	mA
$I_{PU(3.3)LEAK}$	$V_{PU(3.3)}$ leakage current	SOFTCON = 1, $V_{PU(3.3)}$ = 0 V					–5		5	µA
$I_{CC(I/O)LEAK}$	$V_{CC(I/O)}$ leakage current	$V_{CC(I/O)}$ = 3.6 V, $V_{CC(5.0)}$ = 0 V					–5		5	µA
$V_{PU(3.3)}$	Pullup output voltage	$I_{reg(3.3)}$ = 200 µA, $V_{CC(5.0)}$ = 4 V to 5.25 V					3	3.3	3.6	V
R_{SW}	$V_{PU(3.3)}$ switch resistance	$I_{reg(3.3)}$ = 10 mA, $V_{CC(5.0)}$ = 4 V to 5.25 V						10		Ω
ESD PROTECTION										
IEC-61000-4-2 (D+, D–, $V_{CC(5.0)}$ only)	Air-Gap Discharge	10 pulses						±9		kV
	Contact Discharge	10 pulses						±9		kV

(1) Specification for packaged product only
(2) Specification applies to the following pins: RCV, VP, VM, $\overline{OE}$.

DC ELECTRICAL CHARACTERISTICS TRANSCEIVER[(1)]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LEAKAGE CURRENT						
I_{LO}	Hi-Z state data line leakage (suspend mode)	0 V < V_{IN} < 3.3 V, SUSPEND = 1	–10		10	µA
INPUT LEVELS						
V_{DI}	Differential input sensitivity	|(D+) – (D–)|	0.2			V
V_{CM}	Differential common mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2	V
	Receiver hysteresis			200		mV
OUTPUT LEVELS						
V_{OL}	Static output low	R_L = 1.5 kΩ to 3.6 V			0.3	V
V_{OH}	Static output high	R_L = 15 kΩ to GND	2.8		3.6	V
CAPACITANCE						
C_{IN}	Transceiver capacitance	Pin to GND		10		pF
Z_{DRV}	Driver output resistance	Steady-state drive	1	6	11	Ω

(1) Specification for packaged product only

AC ELECTRICAL CHARACTERISTICS[1]

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
DRIVER CHARACTERISTICS (LOW SPEED)					
T_R	Transition rise time	C_L = 200 pF, See Figure 2 C_L = 600 pF	75	300	ns
T_F	Transition fall time	C_L = 200 pF, See Figure 2 C_L = 600 pF	75	300	ns
LRFM	Rise/fall time matching	T_R, T_F	80	125	%
V_{CRS}	Output signal crossover voltage		1.3	2	V
DRIVER CHARACTERISTICS (FULL SPEED)					
T_R	Transition rise time	C_L = 50 pF, See Figure 2	4	20	ns
T_F	Transition fall time	C_L = 50 pF, Figure 2	4	20	ns
FRFM	Rise/fall time matching	(TR, TF)	90	111.1	%
V_{CRS}	Output signal crossover voltage		1.3	2	V
TRANSCEIVER TIMING (FULL SPEED)					
t_{PVZ}	$\overline{OE}$ to receiver 3-state delay	See Figure 1		15	ns
t_{PZD}	Receiver 3-state to transmit delay	See Figure 1	15		ns
t_{PDZ}	$\overline{OE}$ to driver 3-state delay	See Figure 1		15	ns
t_{PZV}	Driver 3-state to receive delay	See Figure 1	15		ns
t_{PLH} t_{PHL}	V_P, V_M to D+, D– propagation delay	See Figure 4		17	ns
t_{PLH} t_{PHL}	D+, D– to RCV propagation delay	See Figure 3		17	ns
t_{PLH} t_{PHL}	D+, D– to V_P, V_M propagation delay	See Figure 3		10	ns

(1) Specification for packaged product only

TIMING DIAGRAMS

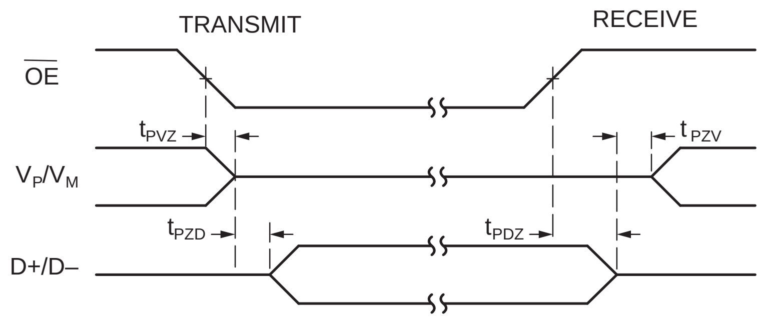


Figure 1. Enable and Disable Times

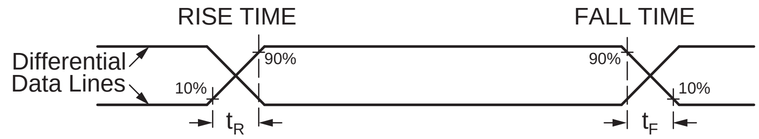


Figure 2. Rise and Fall Times

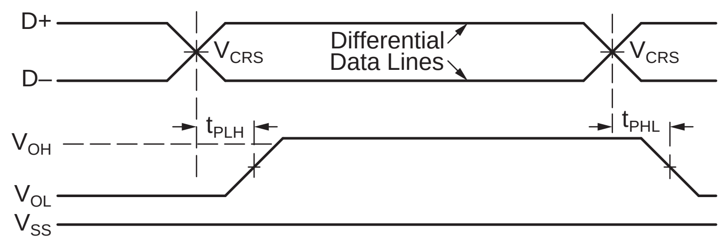


Figure 3. Receiver Propagation Delay

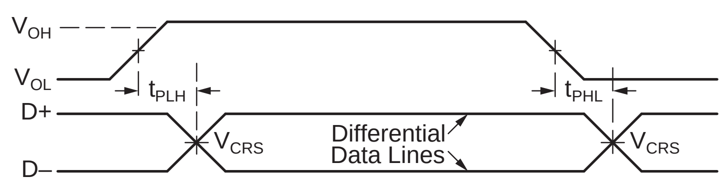


Figure 4. Driver Propagation Delay

TEST CIRCUITS

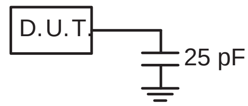


Figure 5. Load for V_P, V_M, RCV

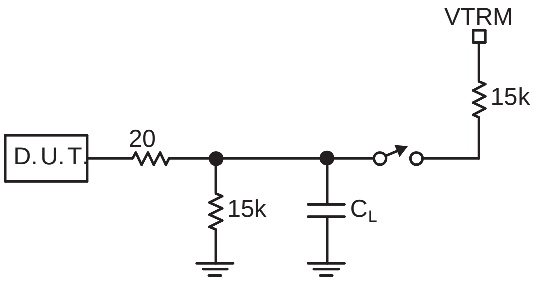


Figure 6. Load for D+, D–

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TUSB2551PW	PREVIEW	TSSOP	PW	14	90	TBD	Call TI	Call TI
TUSB2551PWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI
TUSB2551RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TUSB2551RSVR	PREVIEW	QFN	RSV	16	3000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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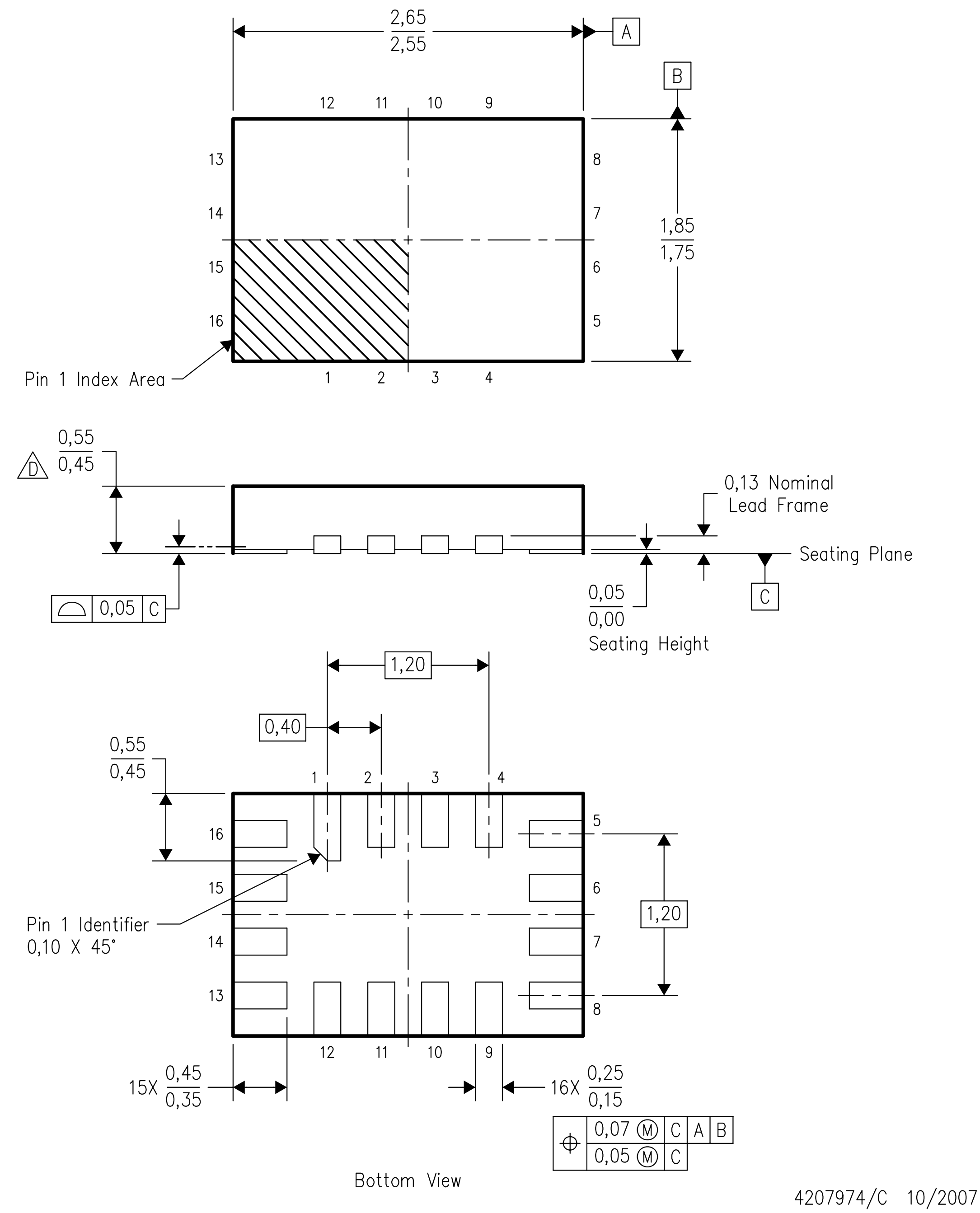
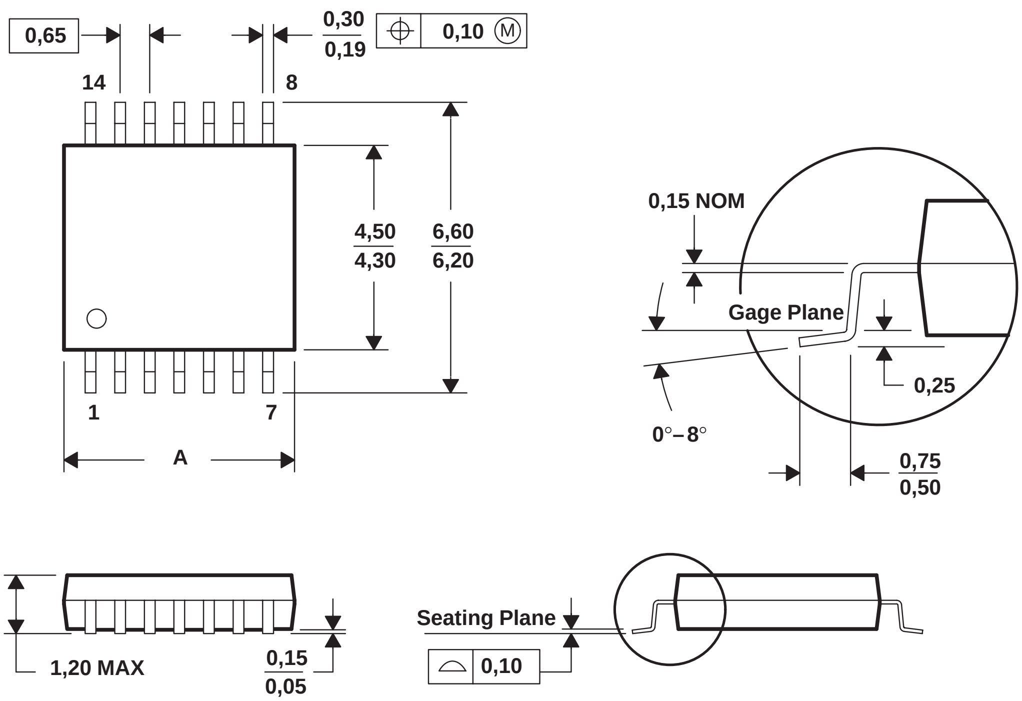
RSV (R-PQFP-N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

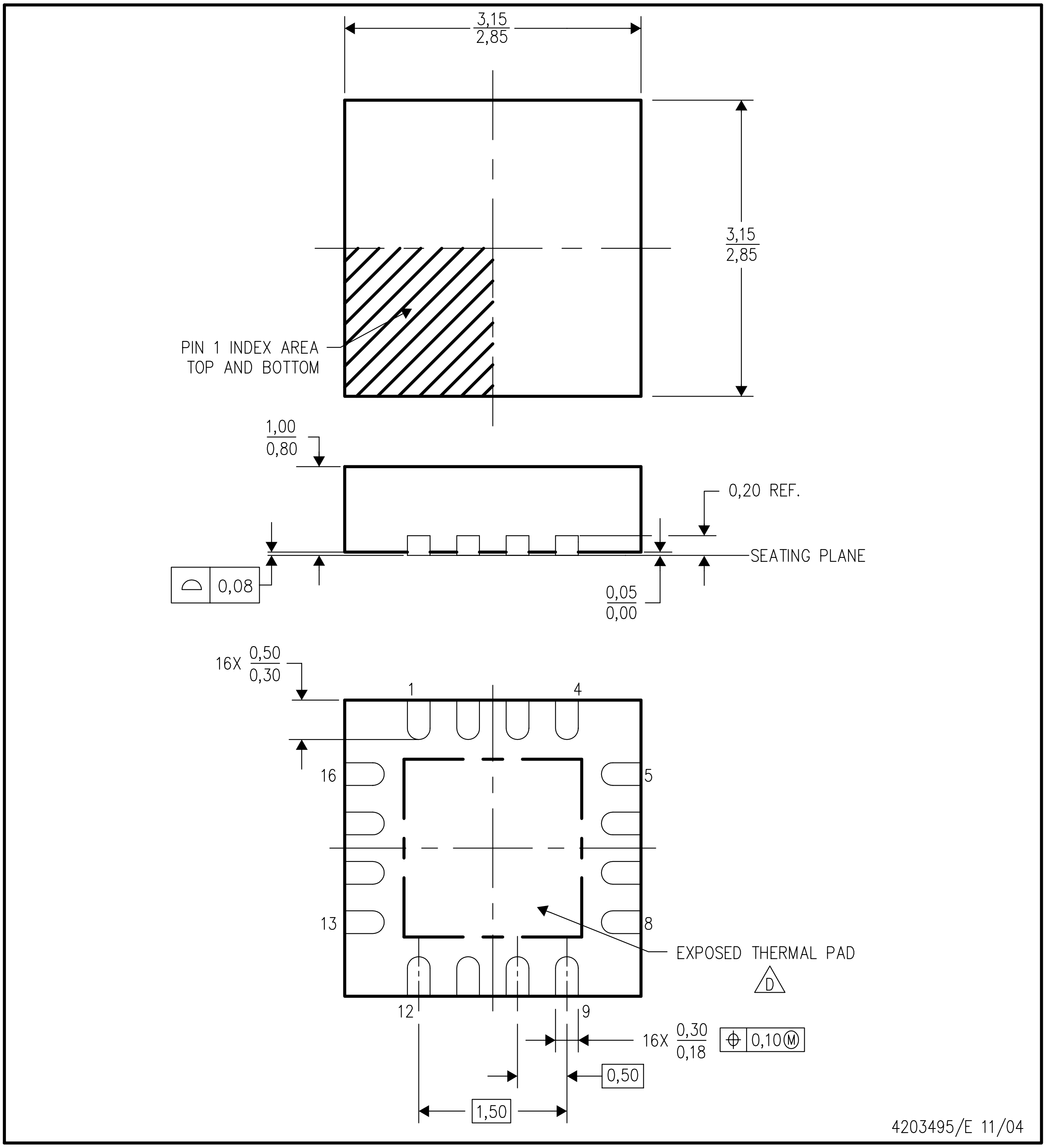


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



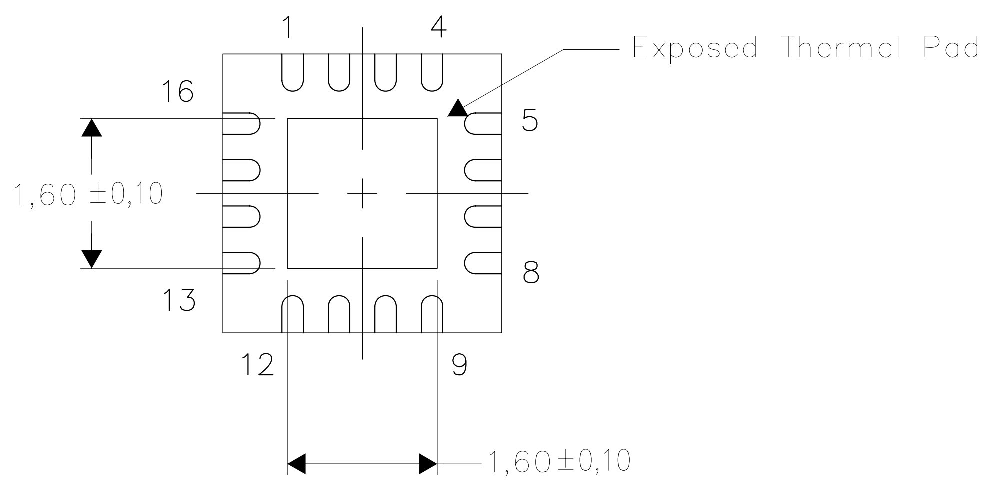
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

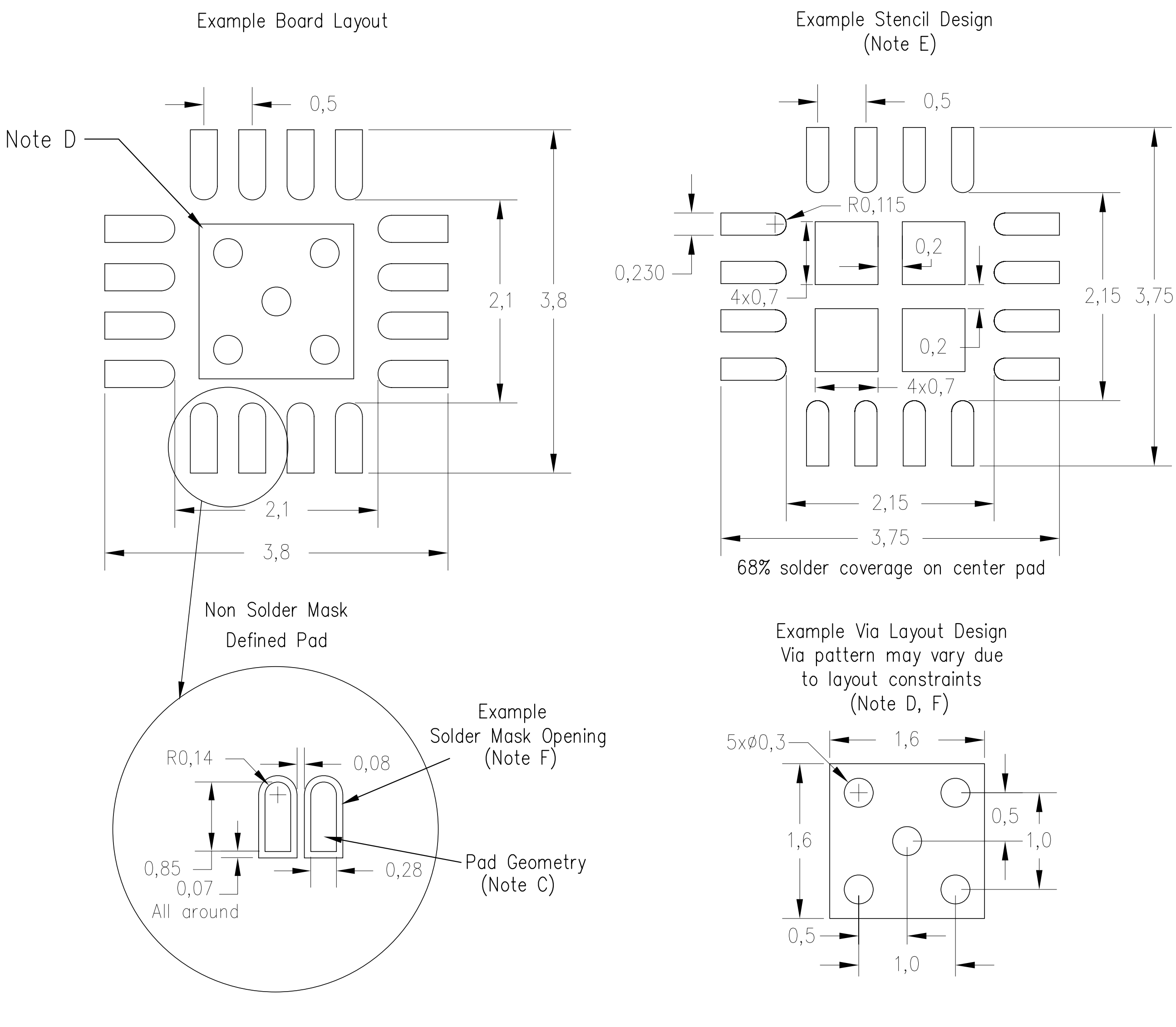


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S-PQFP-N16)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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