

TVGA9000 DATA SHEET

TVGA9000 LOW COST VGA CONTROLLER

Overview

- Single-chip solution for IBM PC/AT, PS/2 and compatibles
- Fully hardware compatible with VGA, EGA, CGA, MDA, and Hercules at the register level
- Requires only two 256Kx4 DRAM chips for VGA solution
- Supports 640x400, 640x480, 800x600 in 256 colors
- Supports 800x600, 1024x768 (interlaced or non-interlaced), and 768x1024 in 16 colors
- Supports 132-column text in 25, 30, 43, or 60 rows
- Supports Edsun CEG™ (Continuous Edge Graphics) DAC
- Supports plasma display
- Built-in data bus transceiver
- Built-in feature connector support
- Only one 32KB EPROM required to achieve 16-bit BIOS operation
- Minimum chip count offers low-cost VGA board level solution (besides DRAM only one EPROM, DAC and clockchip required)
- High-resolution drivers available
- 160 pin, PFP package

General Description

The TRIDENT TVGA9000 is a versatile and full-featured single-chip solution for low cost VGA systems. The TVGA9000 provides register-level compatibility, enhanced graphics and text modes, support for 256Kx4 DRAM, plasma display control, and support for analog VGA, EGA, CGA, and MDA monitors. Register-level compatibility insures compatibility with standard IBM VGA modes and backward compatibility with EGA, CGA, MDA, and Hercules modes. The enhanced graphics modes provide high-resolution displays in 4, 16, and 256 colors. A built-in data bus transceiver and built-in feature connector support save board space and provide cost savings. The TVGA9000 supports both the PC/AT bus and the PS/2 Micro Channel bus.

Software drivers are available to support: AutoCAD, Autoshade, CADkey, Framework, Gem, Lotus, MS Windows, MS Word, P-CAD, Symphony, Ventura, VersaCAD, WordPerfect, Wordstar, OS/2, SCO X-Windows (contact SCO), 8514/AI emulation, and the VESA BIOS extension.

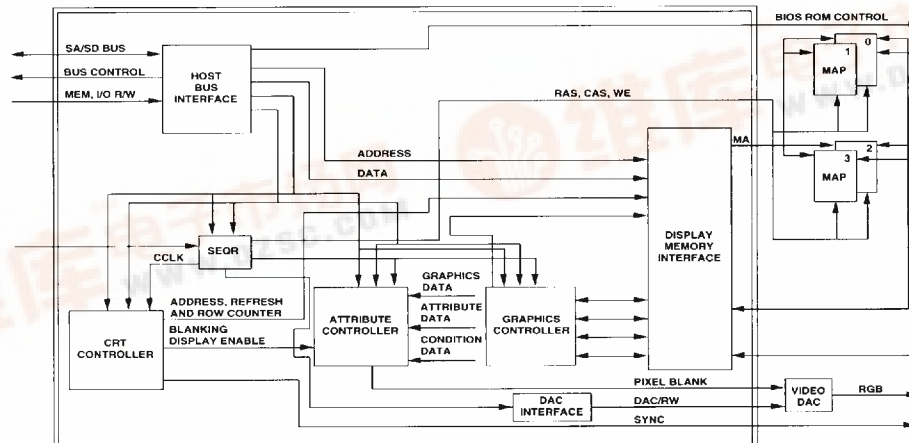


Figure 1. TVGA 9000 Functional Block Diagram





TVGA9000 DATA SHEET

Compatibility

The TVGA9000 is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes, and allows:

- Use of application software that uses any of the above modes
- Emulation of EGA, CGA, MDA, and Hercules modes on a VGA monitor

Extended Graphics and Text Modes

Extended graphics modes supported include:

- 640x400, 640x480 and 800x600 in 256 colors from a palette of 262,144 colors (with 6-bit RAMDAC) or 16 million (with 8-bit RAMDAC)
- 800x600 and 1024x768 (interlaced or non-interlaced) in 16 colors from a palette of 256K/16M
- 1024x768 in 4 colors from a palette of 256K/16M
- Extended text modes offer 132-column text with 25, 30, 43, and 60 rows

Table 1 outlines the amount and speed of Fast Page Mode 256Kx4 DRAM required to implement the 4-, 16-, and 256-color modes.

Hardware Features

The TVGA9000 offers the following special hardware features:

- Source address register to speed memory read/write operations
- Optimized READY Line to speed CPU access
- All TTL included on-board chip
- 16-bit BIOS operation with only one 32KB EPROM

Table 1. 4, 16, and 256-Color DRAM Requirements

Resolution	Colors			DRAM Count		Speed ns
	4	16	256	2	4	100 80
Standard VGA		•		•		•
640x480 (Non-interlaced)			•		•	•
800x600 (Non-interlaced)		•		•		•
800x600 (Interlaced)			•		•	•
800x600 (Non-interlaced)			•		•	•
1024x768 (Interlaced)	•			•		•
1024x768 (Non-interlaced)	•			•		•
1024x768 (Interlaced)		•			•	•
1024x768 (Non-interlaced)		•			•	•

Software Drivers Supported

Extended graphics and text modes are supported by software application drivers developed by Trident. The following applications are supported:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Windows
- MS Word
- P-CAD
- Symphony
- Ventura
- VersaCAD
- WordPerfect
- Wordstar
- OS/2
- SCO X-Windows (call SCO)
- Quattro Pro
- Edsun CEG™ (Windows, AutoCAD, Lotus)

Contact Trident for the latest high-resolution driver releases.

TVGA9000 Applications

The TVGA9000 works with your hardware to let you develop a cost efficient, high performance system. You can use the Trident TCK9002 clock chip to select up to 16 different clock frequencies. Such frequency



selection ability allows you to implement specific applications such as support for high-resolution analog VGA monitors, fixed-frequency VGA monitors, and EGA, CGA, MDA, and Hercules monitors. The TVGA9000 allows you to divide clock input frequencies by one and one half, two, or four. Four chips signals (SC1, SC2, SC3, and FOUT0) can be programmed to select specific clock inputs for the TVGA9000.

A minimum 256K DRAM configuration requires a TVGA9000, Trident Clock Chip, 32KB EPROM, 6-bit RAMDAC, 15-pin connector, jumpers, and miscellaneous ferrite beads, capacitors, resistors.

TVGA9000 Components

The TVGA9000 consists of seven major components: Sequencer, CRT Controller, Graphics Controller, Attribute Controller, DAC Support Logic, Host Bus Interface, and Display Memory Bus Interface. These components are used to generate video output and timing for video memory and the monitor. See Figure 1 on front cover for the TVGA9000 Functional Block Diagram.

Sequencer

The sequencer provides basic memory timing for DRAM interfacing, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 32 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses the video memory. This greatly increases performance over standard CPU access implementations.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller in 4-bit plane format. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the Video DAC. Here it is used as an address into the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.

DAC Support Logic

To simplify the chip hardware design, the TVGA9000 provides a pixel clock and DAC write, DAC read, and blank signals to an off-chip color look-up table/DAC. Both 8- and 6-bit DACs can be supported from one of the TVGA 9000's programmable outputs. The Edsun Laboratories Anti-Aliasing CEG™ DAC is supported with special Trident Drivers.



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Host Bus Interface

The TVGA9000 supports the PC/AT bus and the Micro Channel bus respectively by setting or resetting the configuration bits during the system reset time. Four pins are defined as MEMR, MEMW, SIOR, and SIOW when the TVGA9000 is configured to the PC/AT mode (see Figure 2, page 6). These same four pins can be defined as M/IO, S0, S1, and CMD when the TVGA9000 is part of a Micro Channel board solution (see Figure 3).

The BIOS PROM data width can be configured as 16-bit or 8-bit at system reset time by pulling MD7 high or low, respectively. If the 16-bit mode is turned on, the TVGA9000 will return MCS16 when the PROM is addressed. If the on-board BIOS is not used, the PROM chip(s) can be disabled by pulling MD6 low at system reset time. The TVGA9000 supports a 32KB BIOS, which is located at address hex C0000 to C7FFF. For additional system reset configuration definitions, see "Definitions of MD7-MD0 and RMD7-RMD0 at System Reset" section on this page.

The TVGA9000 can address up to 512KB of video memory depending on the mode (text or graphics). The 16-bit-wide data bus can be activated automatically by BIOS. The TVGA9000 will drive MCS16 when the 16-bit mode is set and video memory is accessed. In order to comply with the Micro Channel specifications, the TVGA9000 supports channel ID (I/O address 100 and 101) as well as the card-enable control bit (bit 0 of I/O port 102). When the video memory or on-board I/O registers are accessed, the TVGA9000 responds with CDSFBK. CDSFBK is generated by decoding the following groups of addresses together with a read/write command:

I/O Read/Write:

- 3BX - excluding 3B6, 3B7, 3BC, 3BD, and 3BE. For monochrome mode only.
- 3DX - excluding 3D6, 3D7, 3DE, and 3DF. For color mode only.
- 3CX - excluding 3CA, 3CB, and 3CD.

Memory Read/Write:

- ROMCS - on-board BIOS EPROM address from C0000 to C7FFF.
- MEMR/W - default display memory address space.

Since there is only the decoding delay for generation of CDSFBK, the signal will look very much like that of a system read/write command. Signal CDSFBK is open-drain output.

Display Memory Bus Interface

The TVGA9000 provides a bus interface for the video display DRAM. The interface provides address multiplexing, data multiplexing, refresh, and RAS, CAS, and write-enable signals. Eighteen address pins (MAA8-MAA0 for Bank A and MAB8-MAB0 for Bank B) and 32 data pins (MD31-MD0) are available for display memory.

Definitions of MD7-MD0 & RMD7-RMD0 at System Reset

Tables 2 and 3 list the values and definitions for MD7-MD0 and RMD7-RMD0, respectively, at system reset.

Table 2. MD7-MD0 Definitions

MD	Logic Value*	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM disable
	1	ROM enable
MD5	0	I/O port at 2xx
	1	I/O port at 3xx
MD4	0	MCA bus
	1	PC bus
MD3-MD0	**	Ext. switch settings

* Set a Logical 1 value by pulling-up to Vcc through a 4.7K-10K resistor. Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.

** Data is read into a 4-bit register. The data values can be used by the BIOS or application software.

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Table 3. RMD7-RMD0 Definitions

RMD	Logic Value *	Definition
RMD7	0	8-bit video memory
	1	16-bit video memory
RMD6	0	One BIOS I/O wait state
	1	Two BIOS I/O wait states
RMD5	0	245Kx4 memory (4 chips)
	1	256Kx4 memory (2 chips)
RMD4	0	Selects 46E8 for port control
	1	Selects 3C3 for port control
RMD3	0	24K BIOS
	1	32K BIOS
RMD2	0	Selects test mode
	1	Normal operation
RMD1	0	Enables BIOS wait state control
	1	Disable BIOS wait state control
RMD0	0	Uses SA lines to decode MCS16
	1	Uses LSA19-17 to decode MCS16

* Set a Logical 1 value by pulling-up to Vcc through a 4.7K-10K resistor.
Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.

Chip Specifications

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typ.	Maximum	Units
Power Supply Voltage	V _{DD}	4.75	5.0	5.25	V
Input Voltage	V _{IN}	GND		V _{DD}	V
Pin Voltage with respect to GND	V _{PIN}	-0.5		V _{DD} + 0.5	V
Operating Temperature	T _{OP}	0		70	°C
Storage Temperature	T _{STO}	-40		100	°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.



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Table 5. DC Specifications

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Low Voltage	V_{IL}	GND	0.8	V	$V_{DD}=5V$
Input High Voltage	V_{IH}	2.0	V_{DD}	V	$V_{DD}=5V$
Input Low Current	I_{IL}	-	-0.5	μA	$V_{IN}=0.0V$
Input High Current	I_{IH}	-	20	μA	$V_{IN}=V_{DD}$
Output Low Voltage	V_{OL}	-	0.4	V	$I_{OL}=6.0mA$ (9mA for MCS16 and READY)
Output High Voltage	V_{OH}	2.4	-	V	$I_{OH}=6.0mA$ (9 mA for MCS16 and READY)
High Impedence Leakage	I_{OZ}	-	10.0	μA	$V_{SS}<V_{OUT}<V_{DD}$
Supply Current	I_{OC}	-	70.0	mA	$V_{DD}=5.25V$ (V_{DD} MAX.)

Table 6. AC Specifications In Nanoseconds (Parameters illustrated in Figures 2 and 3)

SYM	Description	Min	Typ	Max
T1a	$\overline{MCS16}$ active from latched	ADDRESS ¹	valid	10 10 15
T1b	$\overline{MCS16}$ active from unlatched	ADDRESS ²	valid	10 10 15
T2	ALE active from unlatched	ADDRESS	valid	0 5 10
T3	ALE pulse width	NA	NA	5 10 15
T4	DATA read time from	$\overline{COMMAND}$	active	45 50 65
T5	DATA hold time to	$\overline{COMMAND}$	inact.	10 15 20
T6	READY inactive from	$\overline{COMMAND}$	active	10 15 20
T7	$\overline{MCS16}$ hold time to	$\overline{COMMAND}$	inact.	20 25 30
T8	READY hold time before	$\overline{COMMAND}$	inact.	60 120 180
T9	$\overline{MCS16}$ active (low)	from ADDRESS	active	10 15 20
T10	\overline{CDSFBK} active (low)	from ADDRESS	active	10 15 20
T11	READY inactive (low)	from status	active	15 20 25
T12	DATA read time	from READY	active	40 50 60

¹Slow mode. ²Fast mode.

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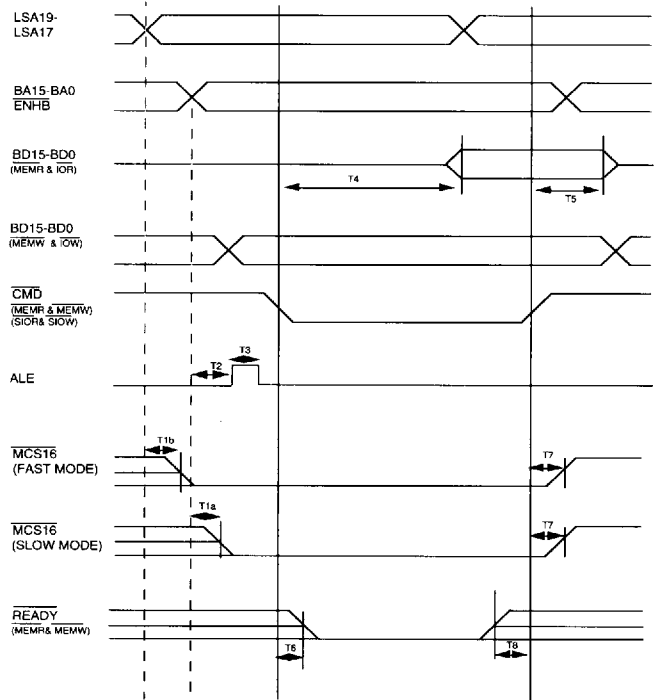


Figure 2. PC/AT Bus Timing

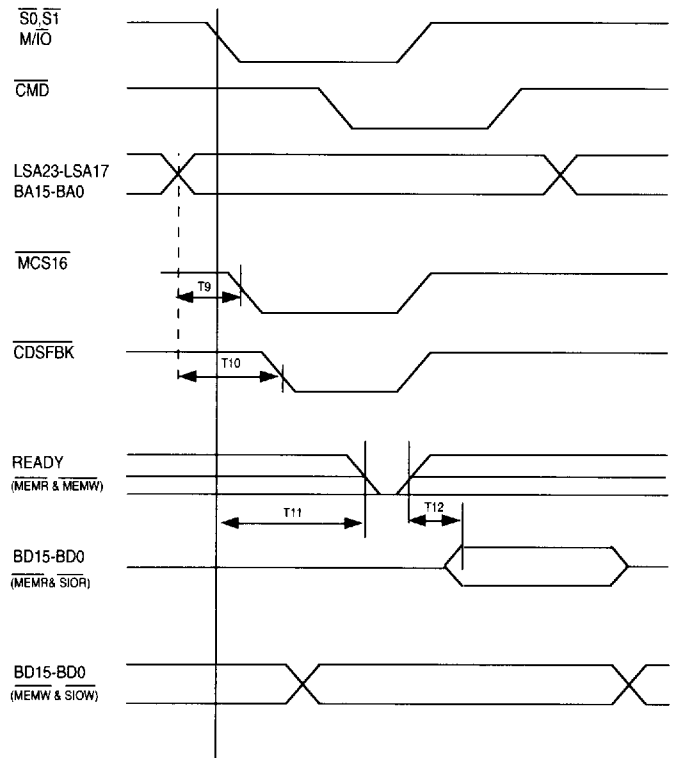


Figure 3. Micro Channel Bus Timing



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Table 7. Vertical and Horizontal Timing

Mode	CLK (MHz)	Type	Display	Max Colors	VERTICAL TIMING (ms)					Polarity	HORIZONTAL TIMING (μs)					Polarity	
					T1	T2	T3	T4	T5		T6	T7	T8	T9	T10		T11
0,1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5B ¹	50.35	APA	800x600	16	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
5C	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	+	6.356	25.422	0.556	1.668	4.131	31.778	-
5D	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.556	1.668	4.131	31.778	-
5E	57.3	APA	800x600 (I)	256	1.073	10.057	0.151	11.130	0.067	-	5.587	27.937	0.139	1.676	3.771	33.524	+
5E	72.0	APA	800x600 (NI)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5F	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	0.204	1.260	3.956	28.151	+
5F	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
5F ¹	75.0	APA	1024x768	16	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024x768(I)	4	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	0.336	1.038	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	+	9.265	17.105	-1.782	4.633	3.956	26.370	+

Based on VESA (Video Electronics Standards Association) proposed standards VS900502 and VS910801.

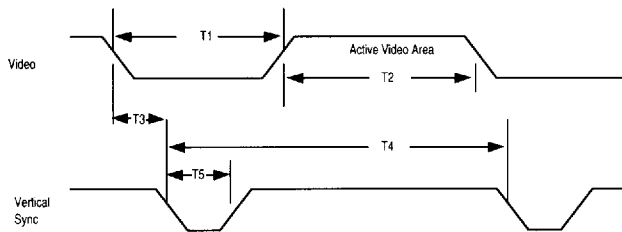


Figure 4-A. Vertical Timing (ms)

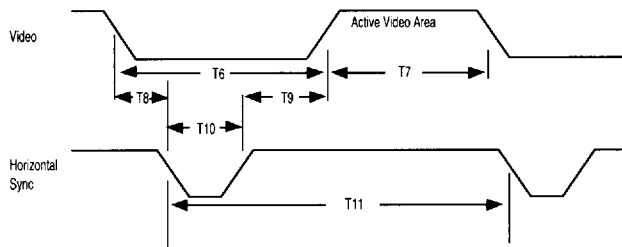
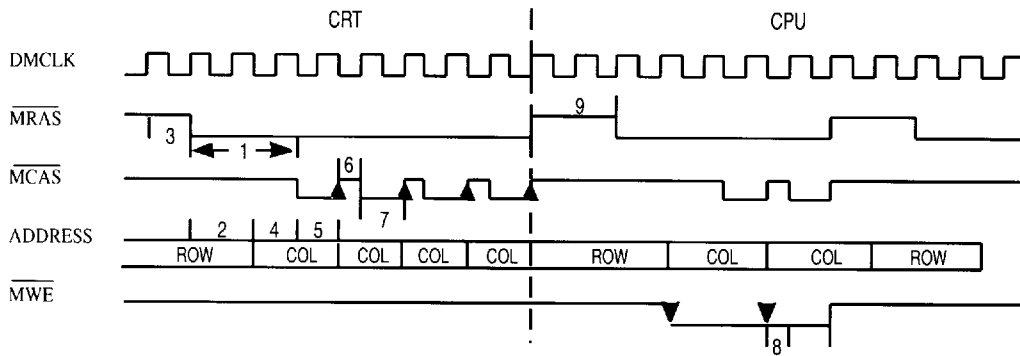


Figure 4-B. Horizontal Timing (μs)

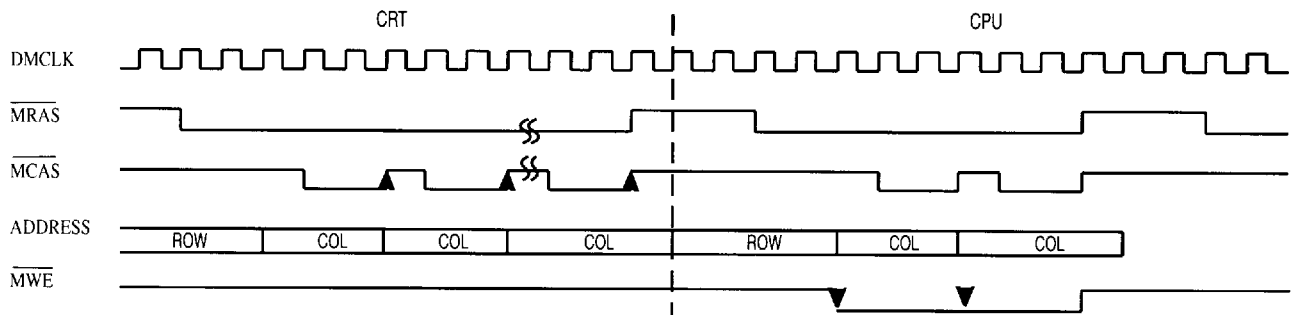
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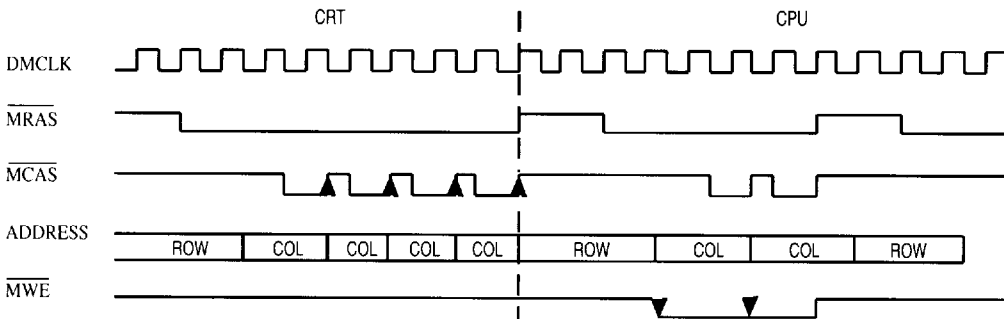
256Kx4 Graphics Mode (Two DRAM)



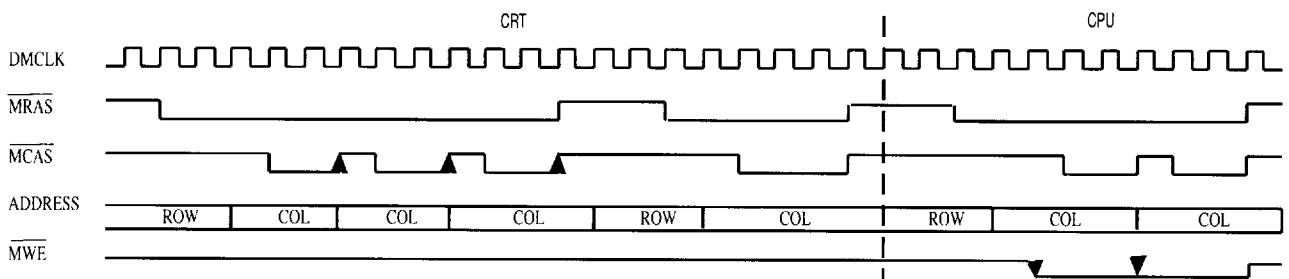
256Kx4 Graphics Mode (Four DRAM)



256Kx4 Text Mode (Two DRAM)



256Kx4 Text Mode (Four DRAM)



NOTES: *ROW refers to Row Address. *COL refers to Column Address. *Above DRAM timings represent worst case. *For each timing diagram, 1st cycle represents a memory read, 2nd cycle (MWE Active) represents a memory write. *▲ indicates when data is ready for a memory read. *▼ indicates when data is ready for a memory write.

Figure 5. Trident TVGA9000 DRAM Timing



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Table 8. Worst Case Memory Timing Parameters*

Parameter	2 DRAM	4 DRAM
T _{rcd} 1	2.5t + 2	3t
T _{rah} 2	1.5t + 3	2t
T _{asr} 3	≥ 0	≥ 0
T _{asc} 4	≥ t	≥ t
T _{cah} 5	t + 6	2t + 10
T _{cp} 6	0.5t + 2	t + 1
T _{cas} 7	t	2t
T _{ds} 8	≥ 0	≥ 0
T _{rp} 9	2t	3t + 10
Test Load	25pf	50pf

*(t=1/DMCLK if VCLK < 40MHz, or t=1/VCLK if VCLK ≥ 40MHz)

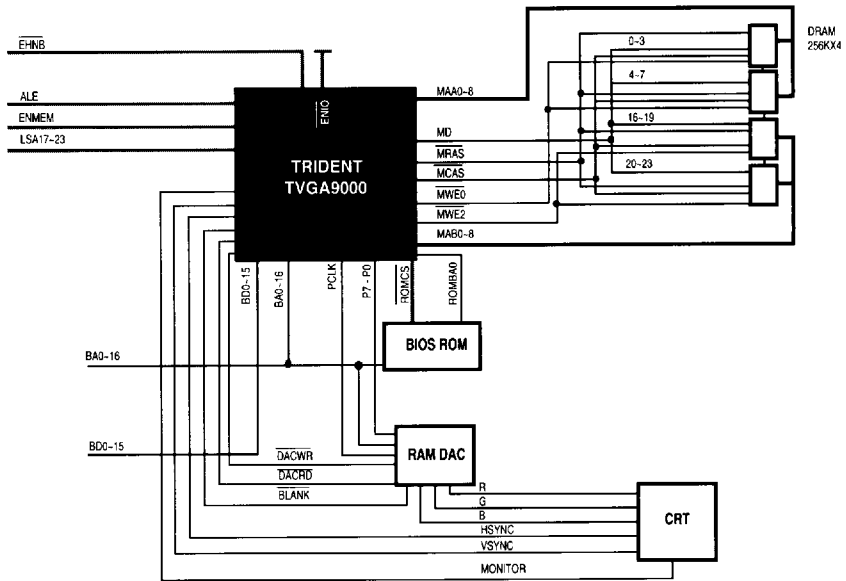


Figure 6-A.
Application For
Four 256Kx4 DRAM

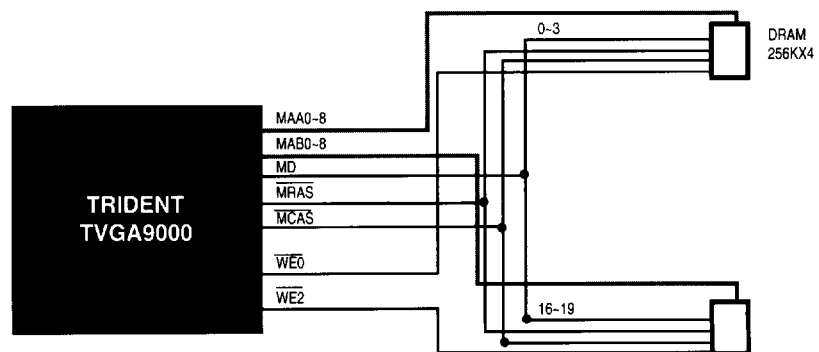


Figure 6-B.
Application For
Two 256Kx4 DRAM

TVGA9000 DATA SHEET



VDD	122	VSS	121	VDD	80	VSS	80
MEMR	119	VSS	122	VSS	79	VSS	79
MEMW	118	MEMR	123	MCAS	78	MCAS	78
BANK	117	SIGS	124	EXEPD	77	EXEPD	77
P1	115	SIOW	125	MAB5	76	MAB5	76
P2	114	LSA23	126	MAB7	75	MAB7	75
P3	113	LSA22	127	MAB6	74	MAB6	74
VSS	112	LSA21	128	MAB5	73	MAB5	73
P4	111	VDD	129	MAB4	72	MAB4	72
P5	109	LSA20	130	MAB3	71	MAB3	71
P6	108	LSA19	131	MAB2	70	MAB2	70
P7	107	LSA18	132	VDD	69	VDD	69
P8	106	SA17	133	VSS	68	VSS	68
P9	105	ATC	134	MAB1	67	MAB1	67
P10	104	BA15	135	MAB0	66	MAB0	66
P11	103	BA14	136	ALE	65	ALE	65
P12	102	BA13	137	HSYNC	64	HSYNC	64
P13	101	BA12	138	VSYNC	63	VSYNC	63
P14	100	BA11	139	MONITOR	62	MONITOR	62
P15	99	BA10	140	MD7	61	MD7	61
P16	98	VDD	141	MD6	60	MD6	60
P17	97	BA9	142	MD5	59	MD5	59
P18	96	BA8	143	VSS	58	VSS	58
P19	95	BA7	144	MD4	57	MD4	57
P20	94	BA6	145	MD3	56	MD3	56
P21	93	BA5	146	MD2	55	MD2	55
P22	92	BA4	147	MD1	54	MD1	54
P23	91	BA3	148	MD0	53	MD0	53
P24	90	BA2	149	MAA6	52	MAA6	52
P25	89	VDD	150	MAA7	51	MAA7	51
P26	88	BA1	151	VDD	50	VDD	50
P27	87	BA0	152	MAA6	49	MAA6	49
P28	86	UACFD	153	MAA5	48	MAA5	48
P29	85	EXCWR	154	MAA4	47	MAA4	47
P30	84	MCSTB	155	MAA3	46	MAA3	46
P31	83	ENHB	156	MAA2	45	MAA2	45
P32	82	CDSFBK	157	MAA1	44	MAA1	44
P33	81	MPAS	158	MAA0	43	MAA0	43
P34	80	VSS	159	VSS	42	VSS	42
P35	79	VSS	160	VSS	41	VSS	41



Figure 7. TVGA9000 Pin-Out

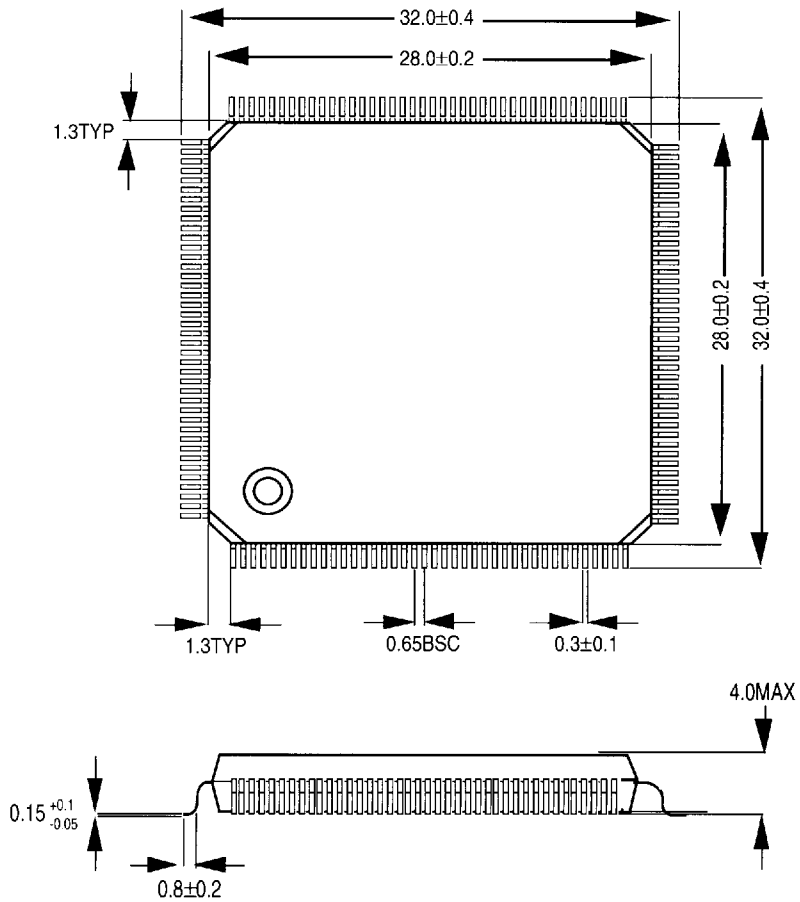


Figure 8. TVGA9000 Packaging PFP 160 Pins



T V G A 9 0 0 0 D A T A S H E E T

Table 9. TVGA9000 Pin Description

Pin	Pin Type	Pin Number	Description
RESET	I	3	System reset (active high); the falling edge latches configuration information into internal registers from memory data lines and AD7-AD0
CLK0	I	104	Video clock input
CLK1/SC3	I/O	103	Video clock input/Clock select output 1
CLK2/SC1	I/O	102	Video clock input/Clock select output 2
CLK3/SC2	I/O	98	Video clock input/Clock select output 3
DMCLK	I	105	DRAM clock
CDSFBK	O	157	Card select feedback, open drain output
ENHB	I	156	Bus high-byte enable
ENIO ²	I	118	Enable on-board IO
ENMEM	I	4	Enable display memory
LSA23-LSA17	I	126-128, 130-133	Unlatched address bus, bit 23 to bit 17
BD15-BD8	I/O	6-8, 10-13, 15	Data bus (high byte), bit 15 to bit 8
BD7-BD0	I/O	16-18, 22-26	Data bus (low byte), bit 7 to bit 0
ROMD7-RMD0	I/O	27-30, 32-35	ROM/DAC data bus, bit 7 to bit 0
BA16-BA10	I/O	134-140	Address Bus
BA9-BA0	I/O	142-152	Address Bus
MEMR ¹	I	119	Memory read strobe
MEMW ¹	I	123	Memory write strobe
SIOR ¹	I	124	I/O read strobe
SIOW ¹	I	125	I/O write strobe
MC516	O	155	Enable 16-bit transfer, open drain output
MD7-MD0	I/O	61-59, 57-53	Memory data bus (bit 7 to bit 0)
MD23-MD15	I/O	94-91, 89-86	Memory data bus (bit 23 to bit 15)
MRA5	O	158	Row address strobe
MCA5	O	78	Column address strobe
MWE0	O	85	Write enable
MWE2	O	84	Write enable
MAA8-MAA0	O	52-51, 49-43	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	76-70, 67-66	Multiplexed address bus of display memory Bank B
P7-P0	O	108-111, 113-116	Video DAC address, bit 7 to bit 0
PCLK	O	97	Pixel clock output
BLANK	O	117	BLANK output
HSYNC	O	64	Horizontal synchronization pulse, polarity programmable
VSYSN	O	63	Vertical synchronization pulse, polarity programmable
DACRD	O	153	DAC read strobe
DACWR	O	154	DAC write strobe
READY	O	106	I/O channel ready, open-drain output
IREQ	O	36	Interrupt request
ROMCS	O	5	BIOS EPROM chip select
ROMBA0	O	95	BIOS EPROM address bit 0
FOU0	O	107	Programmable output 0
MONITOR	I	62	Monitor type detect (analog monitors)
NMI	O	2	Non-maskable interrupt, open-drain output
EXENPD	I	77	External pixel data enable (feature connector)
EXTCLK	I	82	External clock enable (feature connector)
EXSYN	I	83	External sync enable (feature connector)
ALE	I	65	System address latch enable
ROMCLK	I	96	ROM wait state clock
RES4-RES1	NA	99, 39, 38, 19	Reserved pins
VSS	GND	9, 14, 21, 31, 41, 42, 58, 68, 79, 80, 90, 101, 112, 121, 122, 159, 160	Ground
VDD	PWR	1, 20, 37, 40, 50, 69, 81, 100, 120, 129, 141, 150	+5VDC

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¹In Micro Channel Architecture, these four pins are defined as system signals M/IO, S0, S1, and CMD.

²In Micro Channel Architecture, this pin is defined as CDSTP. Definition - 1: normal 0: setup