T835H, T850H

Snubberless™

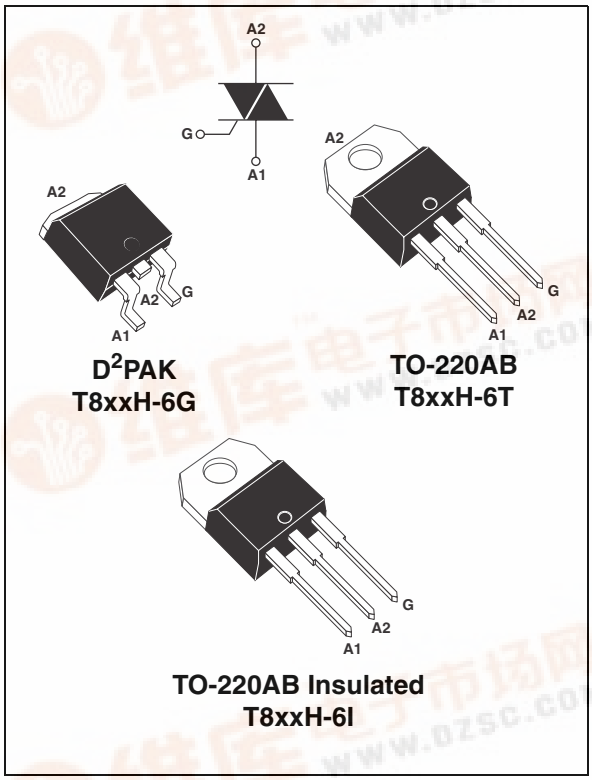
High temperature 8 A Triacs

Main characteristics

Symbol	Value	Unit
$I_{T(RMS)}$	8	A
V_{DRM}/V_{RRM}	600	V
I_{GT}	35 or 50	mA

Features

- Medium current Triac
- 150° C max. T_j turn-off commutation
- Low thermal resistance with clip bonding
- Very high 3 quadrant commutation capability
- Packages are RoHS (2002/95/EC) compliant



Applications

Especially designed to operate in high power density or universal motor applications such as vacuum cleaner and washing machine drum motor, these 8 A triacs provide a very high switching capability up to junction temperatures of 150° C.

The heatsink can be reduced, compared to traditional triacs, according to the high performance at given junction temperatures.

Description

Available in through-hole or surface mount packages, the T835H and T850H triac series are suitable for general purpose mains power AC switching.

Order codes

Part Numbers	Marking
T835H-6G	T835H 6G
T850H-6G	T850H 6G
T835H-6G-TR	T835H 6G
T850H-6G-TR	T850H 6G
T835H-6T	T835H 6T
T850H-6T	T850H 6T
T835H-6I	T835H 6I
T850H-6I	T850H 6I

TM: Snubberless is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	D^2PAK, TO-220AB	T_c = 135° C	8	A
		TO-220AB Ins	T_c = 125° C		
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25° C)	F = 50 Hz	t = 20 ms	80	A
		F = 60 Hz	t = 16.7 ms	84	
I^2t	I^2t Value for fusing	t_p = 10 ms		42	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 2 x I_{GT} , $t_r \leq$ 100 ns	F = 120 Hz	T_j = 150° C	50	A/µs
V_{DSM}/V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25° C	V_{DRM}/V_{RRM} + 100	V
I_{GM}	Peak gate current	t_p = 20 µs	T_j = 150° C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_j = 150° C	1	W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 150	° C

Table 2. Electrical Characteristics (T_j = 25° C, unless otherwise specified)

Symbol	Test Conditions	Quadrant		Value		Unit
				T835H	T850H	
I_{GT} (1)	V_D = 12 V R_L = 33 Ω	I - II - III	MAX.	35	50	mA
V_{GT}		I - II - III	MAX.	1.0		V
V_{GD}	$V_D = V_{DRM}$, R_L = 3.3 kΩ	I - II - III	MIN.	0.15		V
I_H (2)	I_T = 500 mA		MAX.	35	75	mA
I_L	I_G = 1.2 I_{GT}	I - III	MAX.	50	60	mA
		II		80	110	
dV/dt (2)	V_D = 67% V_{DRM}, gate open, T_j = 150° C		MIN.	1000	1500	V/µs
(dI/dt)c (2)	Without snubber, T_j = 150° C		MIN.	11	14	A/ms

1. minimum I_{GT} is guaranted at 20% of I_{GT} max.
2. for both polarities of A2 referenced to A1.

Table 3. Static Characteristics

Symbol	Test Conditions			Value	Unit
V_T (1)	I_{TM} = 11 A, t_p = 380 µs	T_j = 25° C	MAX.	1.5	V
V_{t0} (1)	Threshold voltage	T_j = 150° C	MAX.	0.80	V
R_d (1)	Dynamic resistance	T_j = 150° C	MAX.	52	mΩ
I_{DRM} I_{RRM} (2)	V_{DRM} = V_{RRM}	T_j = 25° C	MAX.	5	µA
		T_j = 150° C	MAX.	3.1	mA
	V_D/V_R = 400 V (at peak mains voltage)	T_j = 150° C	MAX.	2.5	
	V_D/V_R = 200 V (at peak mains voltage)	T_j = 150° C	MAX.	2.0	

1. for both polarities of A2 referenced to A1.
2. t_p = 380 µs.

Table 4. Thermal resistance

Symbol	Parameter			Value	Unit
$R_{th(j-c)}$	Junction to case (AC)		D^2PAK / TO-220AB	1.85	° C/W
			TO-220AB Ins	3.7	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm^2	D^2PAK	45	
			TO-220AB / TO-220AB Ins	60	

Figure 1. Maximum power dissipation versus RMS on-state current (full cycle)

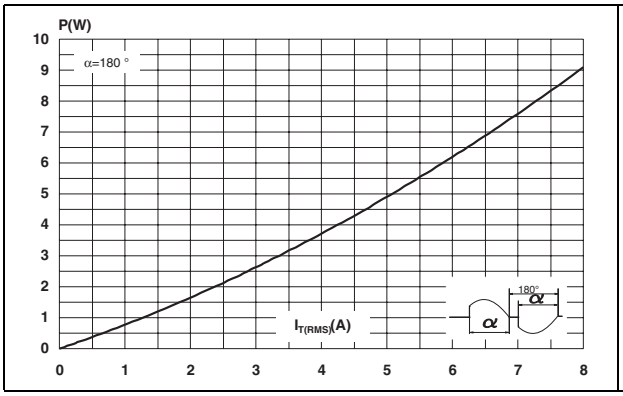


Figure 2. RMS on-state current versus case temperature (full cycle)

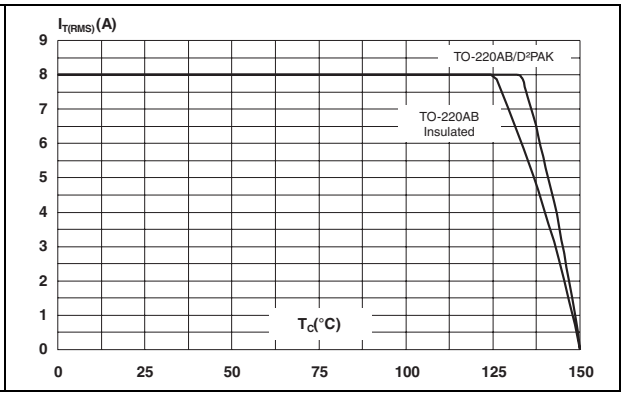


Figure 3. RMS on-state current versus ambient temperature (Epoxy printed circuit board FR4, copper thickness = 35 µm)

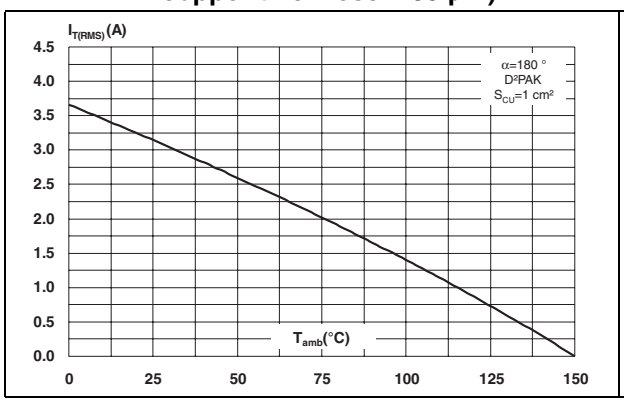


Figure 4. Variation of thermal impedance versus pulse duration

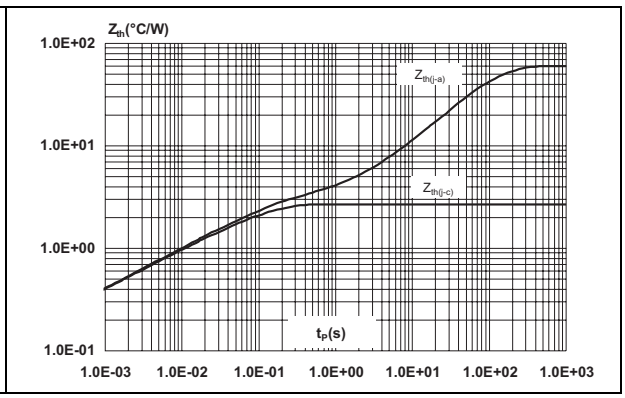


Figure 5. On-state characteristics (maximum values)

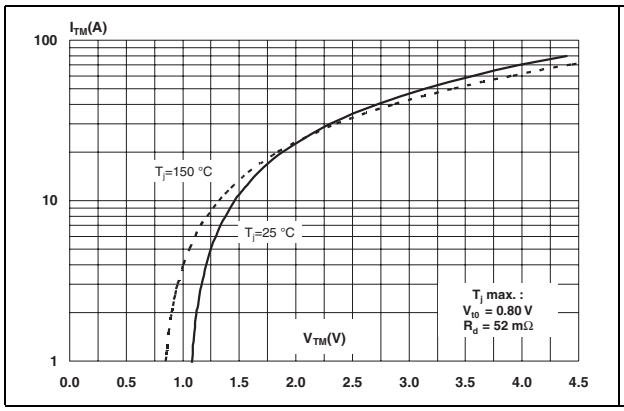


Figure 6. Surge peak on-state current versus number of cycles

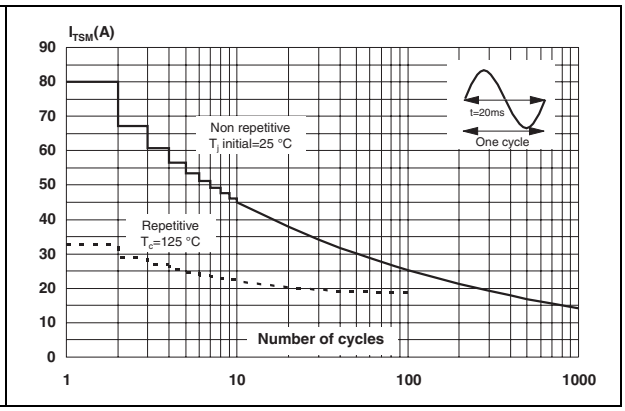


Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms and corresponding value of I^2t

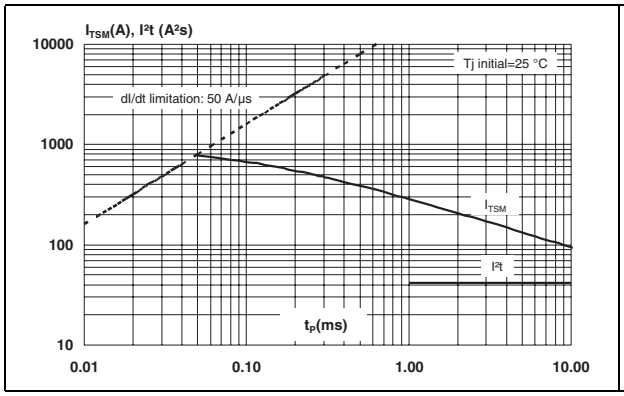


Figure 8. Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

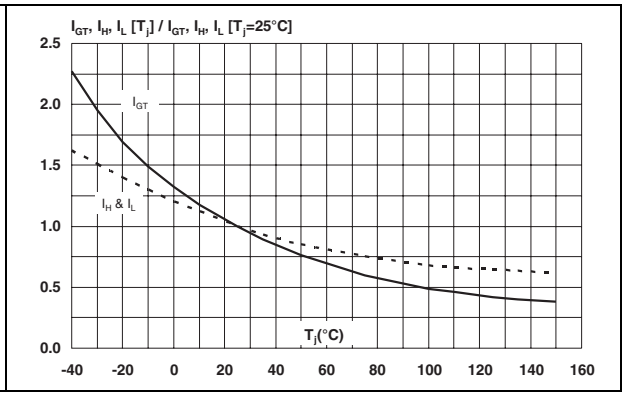


Figure 9. Relative variation of critical rate of decrease of main current (dI/dt)c versus reapplied (dV/dt)c (typical values)

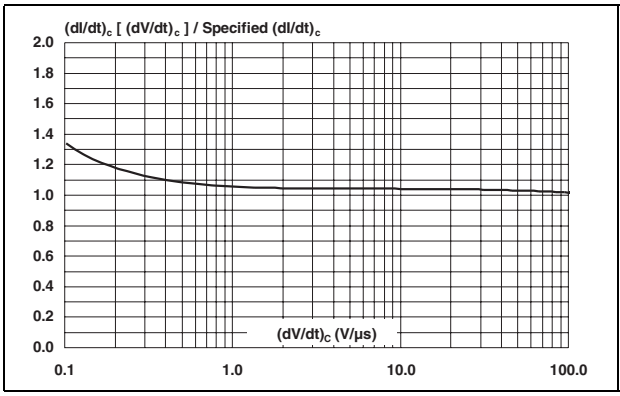


Figure 10. Relative variation of critical rate of decrease of main current versus junction temperature

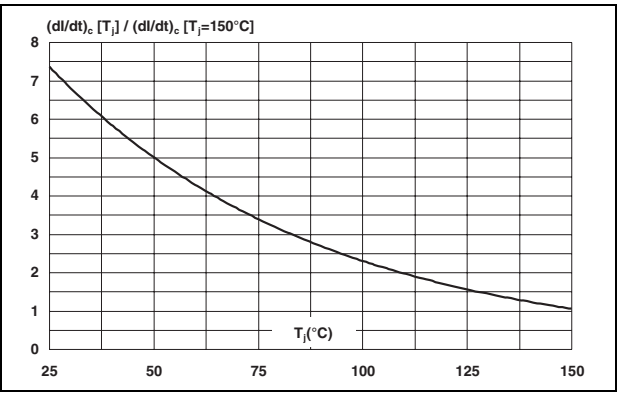


Figure 11. Leakage current versus junction temperature for different values of blocking voltage (typical values)

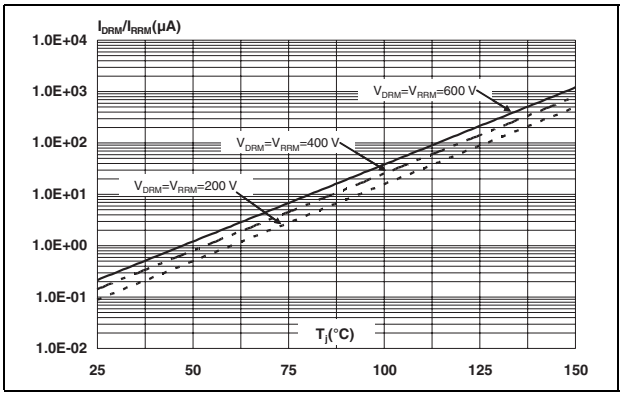
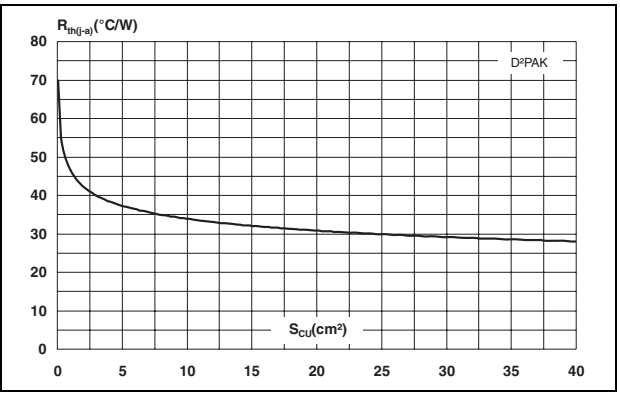
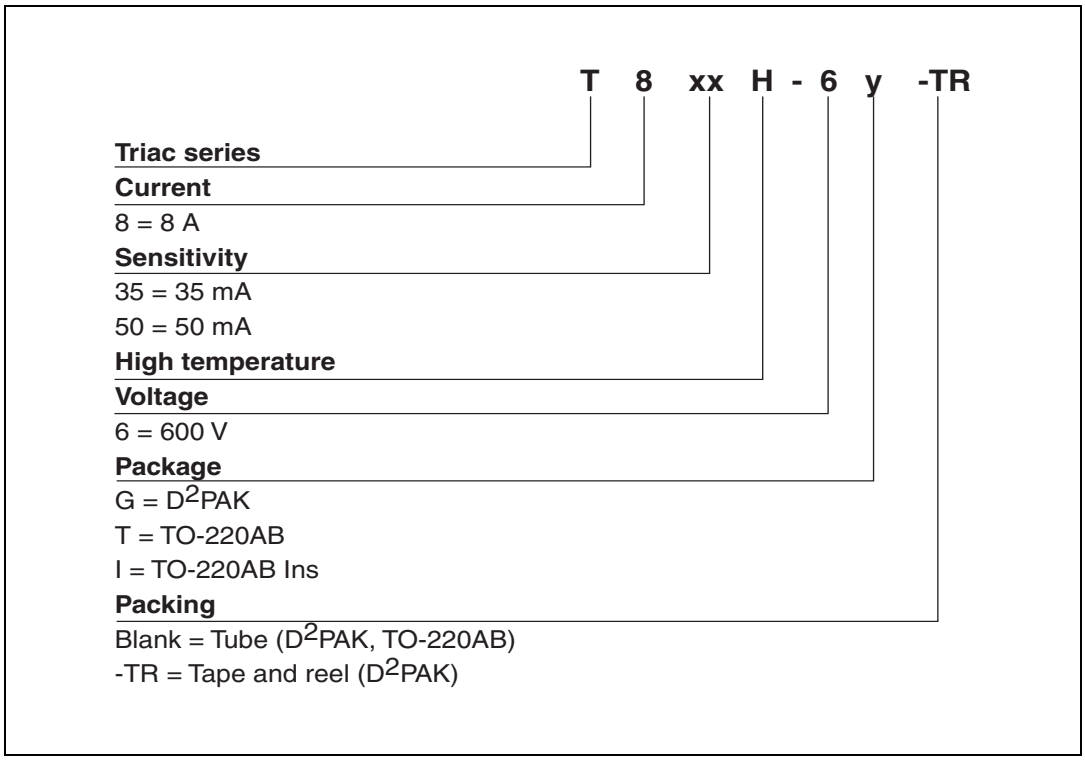


Figure 12. Variation of thermal resistance junction to ambient versus copper surface under tab (Epoxy printed circuit board FR4, copper thickness = 35 µm)



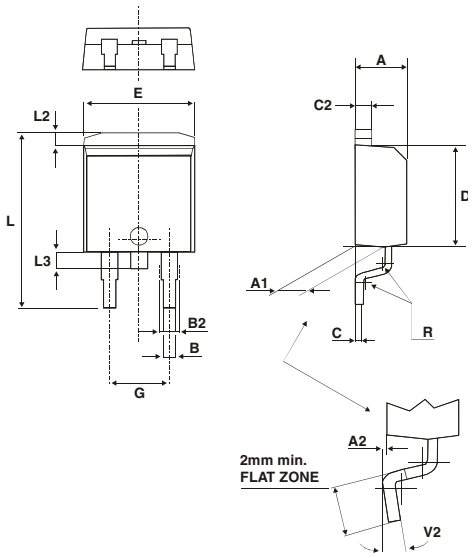
2 Ordering information



3 Package mechanical data

- Epoxy meets UL94, V0
- Recommended torque 0.4 to 0.6 Nm

Table 5. D²PAK dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.169		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.70		0.93	0.027		0.037
B2	1.25	1.40		0.048	0.055	
C	0.45		0.60	0.017		0.024
C2	1.21		1.36	0.047		0.054
D	8.95		9.35	0.352		0.368
E	10.00		10.28	0.393		0.405
G	4.88		5.28	0.192		0.208
L	15.00		15.85	0.590		0.624
L2	1.27		1.40	0.050		0.055
L3	1.40		1.75	0.055		0.069
R	0.40			0.016		
V2	0°		8°	0°		8°

Figure 13. Footprint (dimensions in mm)

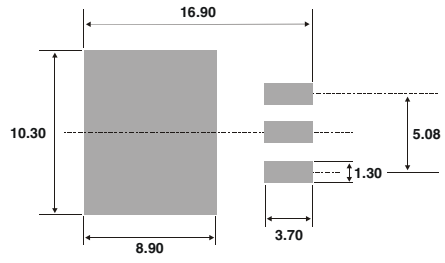
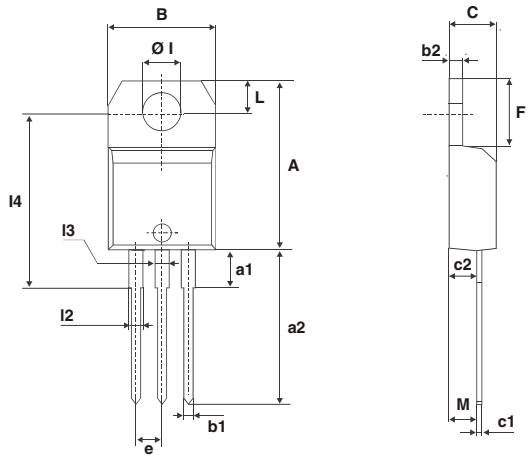


Table 6. TO-220AB and TO-220AB Ins dimensions



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	15.20		15.90	0.598		0.625
a1		3.75			0.147	
a2	13.00		14.00	0.511		0.551
B	10.00		10.40	0.393		0.409
b1	0.61		0.88	0.024		0.034
b2	1.23		1.32	0.048		0.051
C	4.40		4.60	0.173		0.181
c1	0.49		0.70	0.019		0.027
c2	2.40		2.72	0.094		0.107
e	2.40		2.70	0.094		0.106
F	6.20		6.60	0.244		0.259
ØI	3.75		3.85	0.147		0.151
l4	15.80	16.40	16.80	0.622	0.646	0.661
L	2.65		2.95	0.104		0.116
l2	1.14		1.70	0.044		0.066
l3	1.14		1.70	0.044		0.066
M		2.60			0.102	

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
T8xxH-6G	T8xxH 6G	D^2PAK	1.5 g	50	Tube
T8xxH-6G-TR	T8xxH 6G	D^2PAK	1.5 g	1000	Tape and reel
T8xxH-6T	T8xxH 6T	TO-220AB	2.3 g	50	Tube
T8xxH-6I	T8xxH 6I	TO-220AB Ins	2.3 g	50	Tube

5 Revision history

Date	Revision	Description of Changes
17-Apr-2007	1	First issue

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