µA741, µA741Y
GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

SLOS094B – NOVEMBER 1970 – REVISED SEPTEMBER 2000

- **Short-Circuit Protection**
- **Offset-Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **No Frequency Compensation Required**
- **Low Power Consumption**
- **No Latch-Up**
- **Designed to Be Interchangeable With Fairchild µA741**

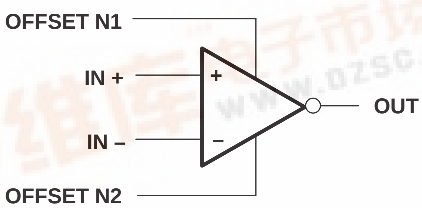
description

The µA741 is a general-purpose operational amplifier featuring offset-voltage null capability.

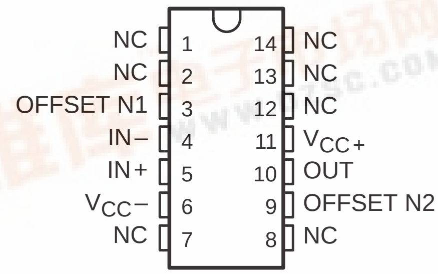
The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in Figure 2.

The µA741C is characterized for operation from 0°C to 70°C. The µA741I is characterized for operation from −40°C to 85°C.The µA741M is characterized for operation over the full military temperature range of –55°C to 125°C.

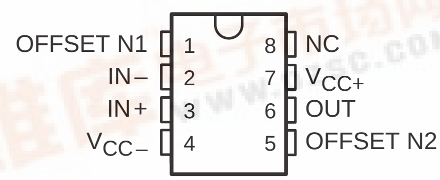
symbol



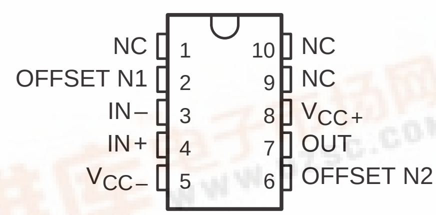
µA741M . . . J PACKAGE
(TOP VIEW)



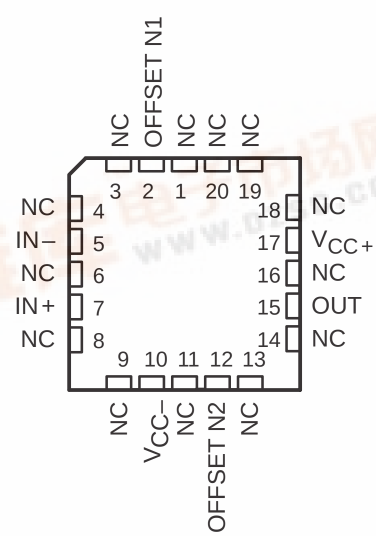
µA741M . . . JG PACKAGE
µA741C, µA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



µA741M . . . U PACKAGE
(TOP VIEW)



µA741M . . . FK PACKAGE
(TOP VIEW)



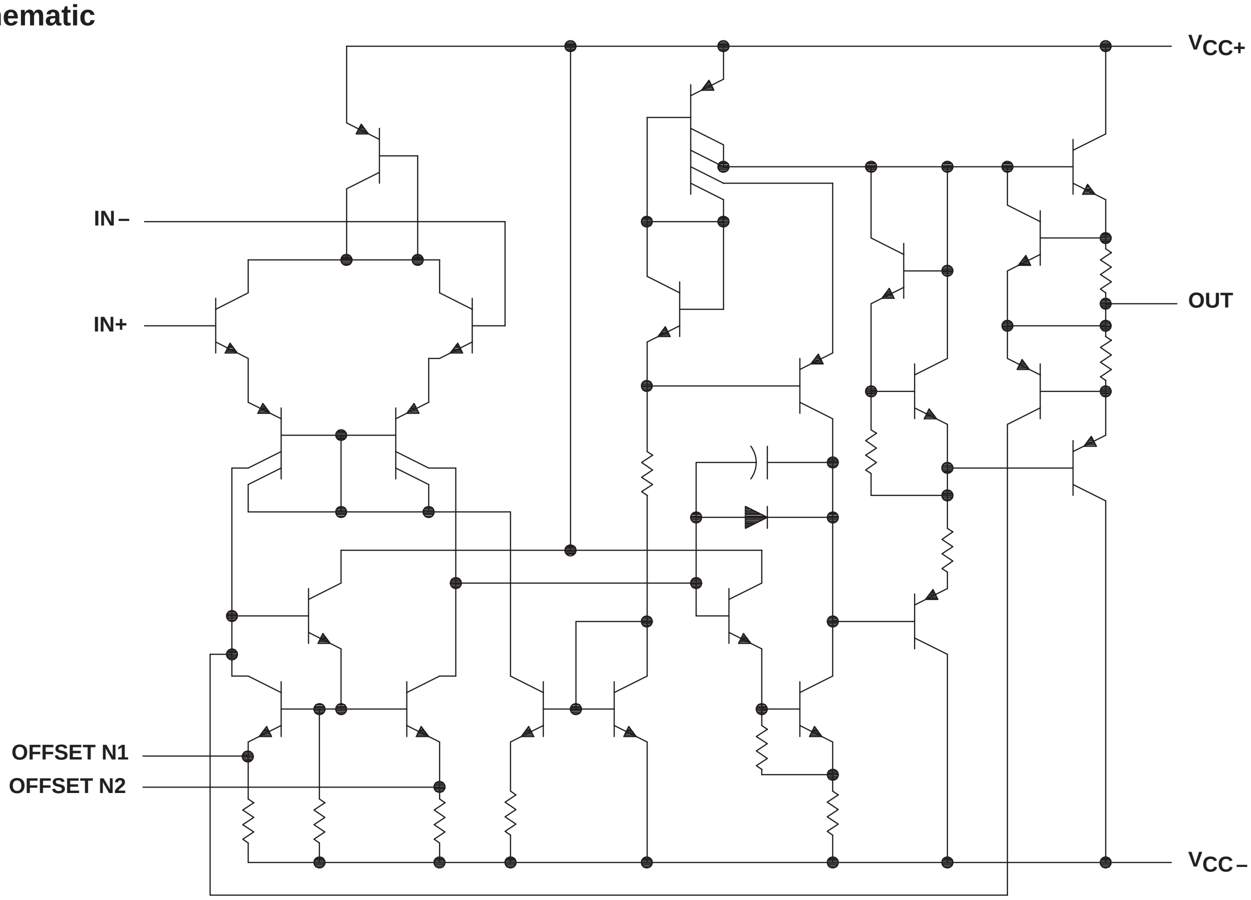
NC – No internal connection

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES							CHIP FORM (Y)
	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	FLAT PACK (U)	
0°C to 70°C	μA741CD				μA741CP	μA741CPW		μA741Y
–40°C to 85°C	μA741ID				μA741IP			
–55°C to 125°C		μA741MFK	μA741MJ	μA741MJG			μA741MU	

The D package is available taped and reeled. Add the suffix R (e.g., μA741CDR).

schematic

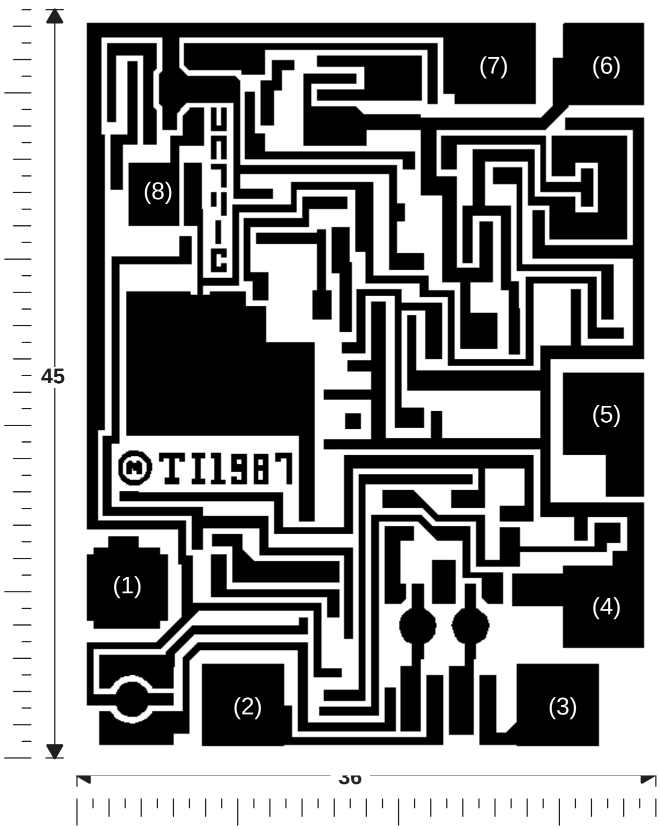


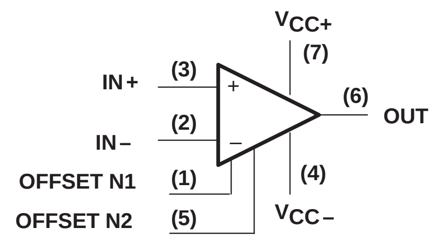
Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

µA741Y chip information

This chip, when properly assembled, displays characteristics similar to the µA741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C.

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

		µA741C	µA741I	µA741M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	22	22	V
Supply voltage, V_{CC-} (see Note 1)		–18	–22	–22	V
Differential input voltage, V_{ID} (see Note 2)		±15	±30	±30	V
Input voltage, V_I any input (see Notes 1 and 3)		±15	±15	±15	V
Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-}		±15	±0.5	±0.5	V
Duration of output short circuit (see Note 4)		unlimited	unlimited	unlimited	
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature range, T_A		0 to 70	–40 to 85	–55 to 125	°C
Storage temperature range		–65 to 150	–65 to 150	–65 to 150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package			300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D, P, or PW package	260	260		°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply. For the µA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PW	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

electrical characteristics at specified free-air temperature, $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	µA741C			µA741I, µA741M			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$	25°C		1	6		1	5	mV
			Full range			7.5			6	
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$	25°C		±15			±15		mV
I_{IO}	Input offset current	$V_O = 0$	25°C		20	200		20	200	nA
			Full range			300			500	
I_{IB}	Input bias current	$V_O = 0$	25°C		80	500		80	500	nA
			Full range			800			1500	
V_{ICR}	Common-mode input voltage range		25°C	±12	±13		±12	±13		V
			Full range	±12			±12			
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±14		±12	±14		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L = 2 kΩ	25°C	±10	±13		±10	±13		
		R_L ≥ 2 kΩ	Full range	±10			±10			
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ	25°C	20	200		50	200		V/mV
		V_O = ±10 V	Full range	15			25			
r_i	Input resistance		25°C	0.3	2		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5	25°C		75			75		Ω
C_i	Input capacitance		25°C		1.4			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	V_{CC} = ±9 V to ±15 V	25°C		30	150		30	150	µV/V
			Full range			150			150	
I_{OS}	Short-circuit output current		25°C		±25	±40		±25	±40	mA
I_{CC}	Supply current	$V_O = 0$, No load	25°C		1.7	2.8		1.7	2.8	mA
			Full range			3.3			3.3	
P_D	Total power dissipation	$V_O = 0$, No load	25°C		50	85		50	85	mW
			Full range			100			100	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the µA741C is 0°C to 70°C, the µA741I is –40°C to 85°C, and the µA741M is –55°C to 125°C.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	µA741C			µA741I, µA741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	V_I = 20 mV, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.3			0.3		µs
	Overshoot factor			5%			5%		
SR	Slew rate at unity gain	V_I = 10 V, R_L = 2 kΩ, C_L = 100 pF, See Figure 1		0.5			0.5		V/µs

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$		1	6	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$		±15		mV
I_{IO}	Input offset current	$V_O = 0$		20	200	nA
I_{IB}	Input bias current	$V_O = 0$		80	500	nA
V_{ICR}	Common-mode input voltage range		±12	±13		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	±12	±14		V
		$R_L = 2\ k\Omega$	±10	±13		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2\ k\Omega$	20	200		V/mV
r_i	Input resistance		0.3	2		MΩ
r_o	Output resistance	$V_O = 0$, See Note 5		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ±15 V		30	150	μV/V
I_{OS}	Short-circuit output current			±25	±40	mA
I_{CC}	Supply current	$V_O = 0$, No load		1.7	2.8	mA
P_D	Total power dissipation	$V_O = 0$, No load		50	85	mW

† All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified.

NOTE 5: This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	μA741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.3		μs
	Overshoot factor			5%		
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2\ k\Omega$, $C_L = 100$ pF, See Figure 1		0.5		V/μs

PARAMETER MEASUREMENT INFORMATION

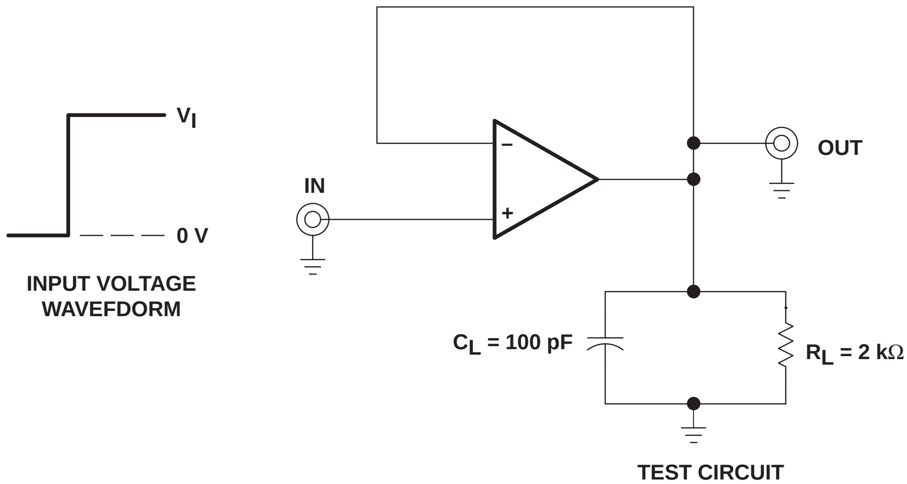


Figure 1. Rise Time, Overshoot, and Slew Rate

APPLICATION INFORMATION

Figure 2 shows a diagram for an input offset voltage null circuit.

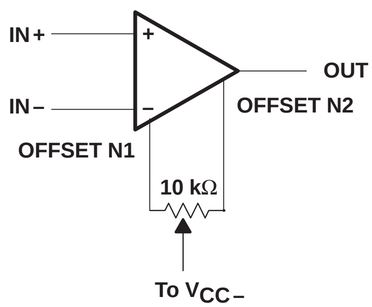


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS†

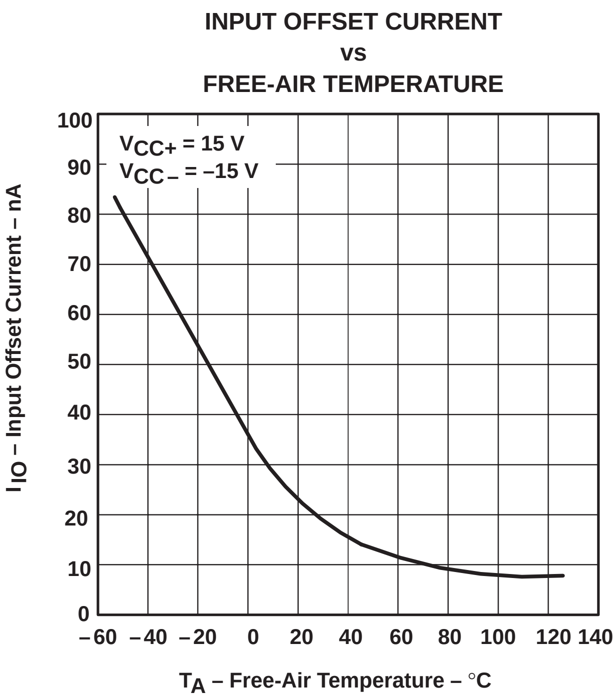


Figure 3

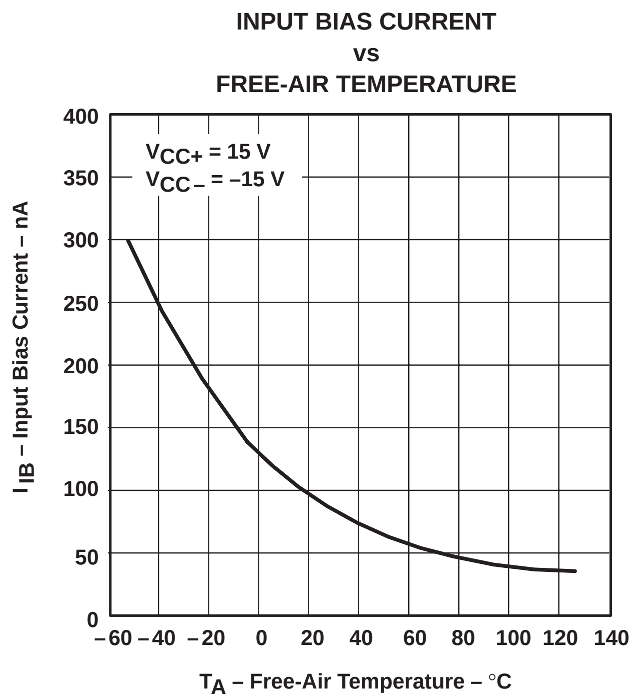


Figure 4

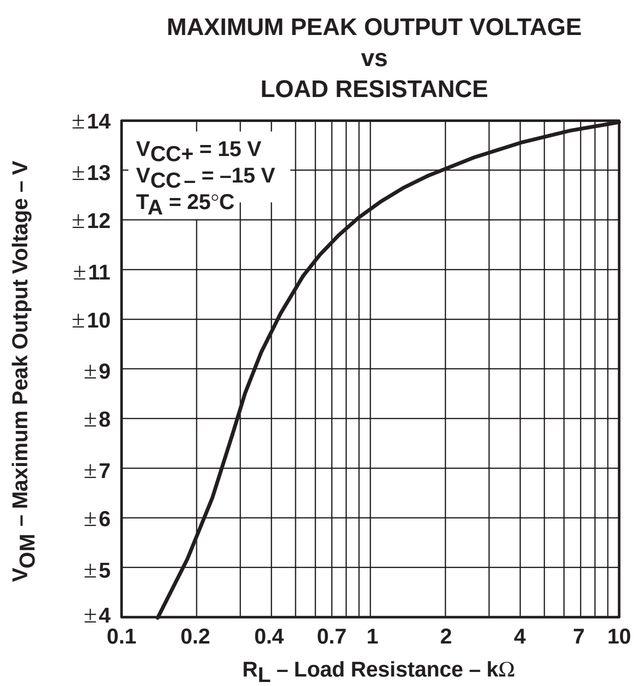


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

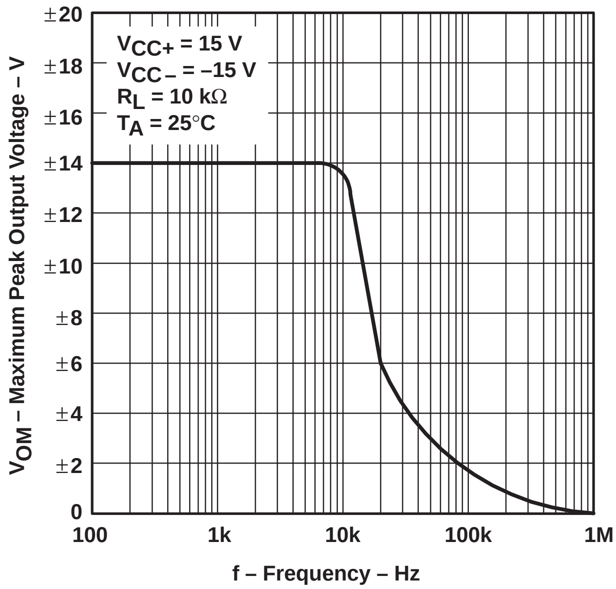


Figure 6

OPEN-LOOP SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

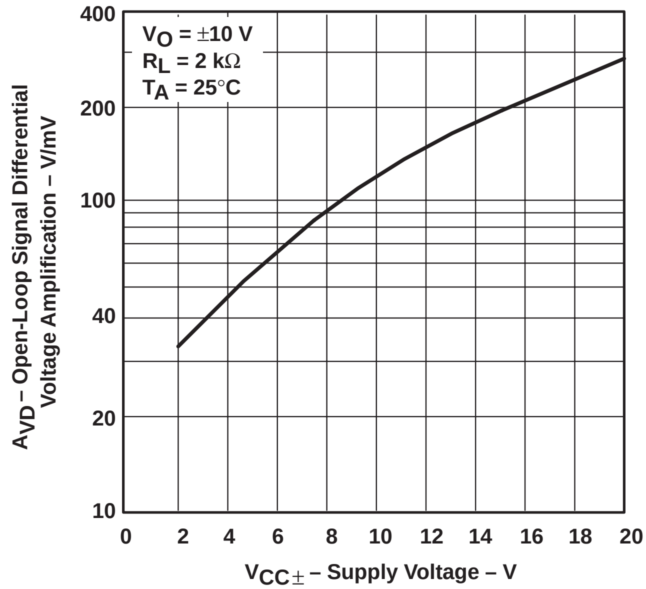
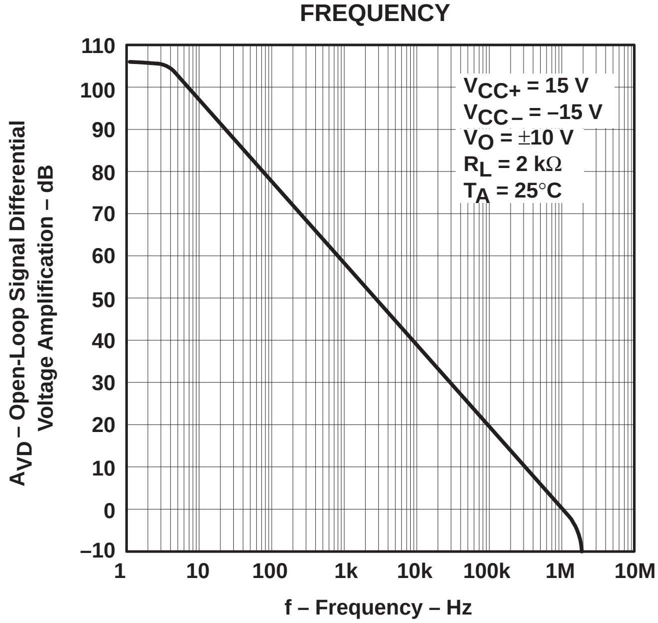


Figure 7

OPEN-LOOP LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREQUENCY



TYPICAL CHARACTERISTICS

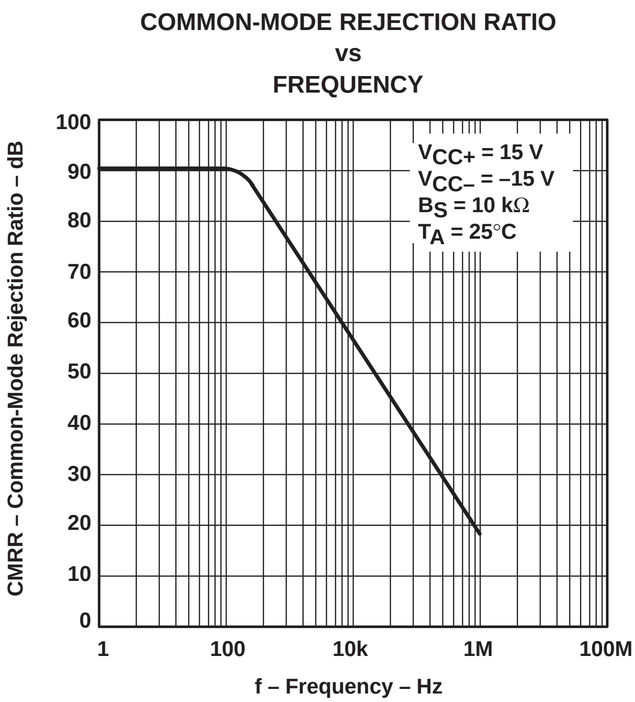


Figure 8

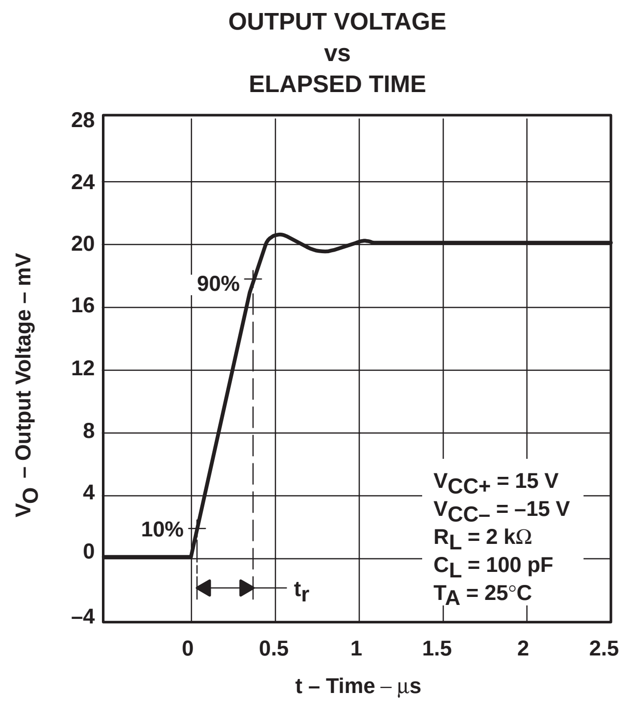


Figure 9

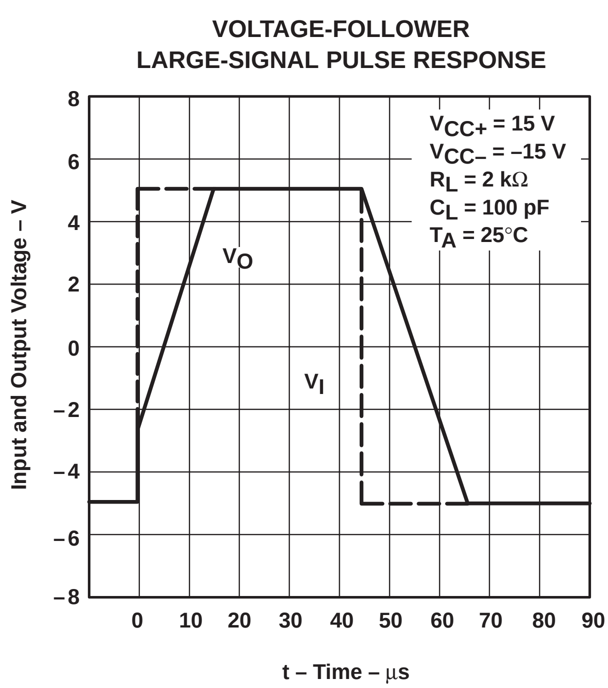


Figure 10

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UA741CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UA741CJG4	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UA741CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA741CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
UA741CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UA741MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
UA741MJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
UA741MJB	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
UA741MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
UA741MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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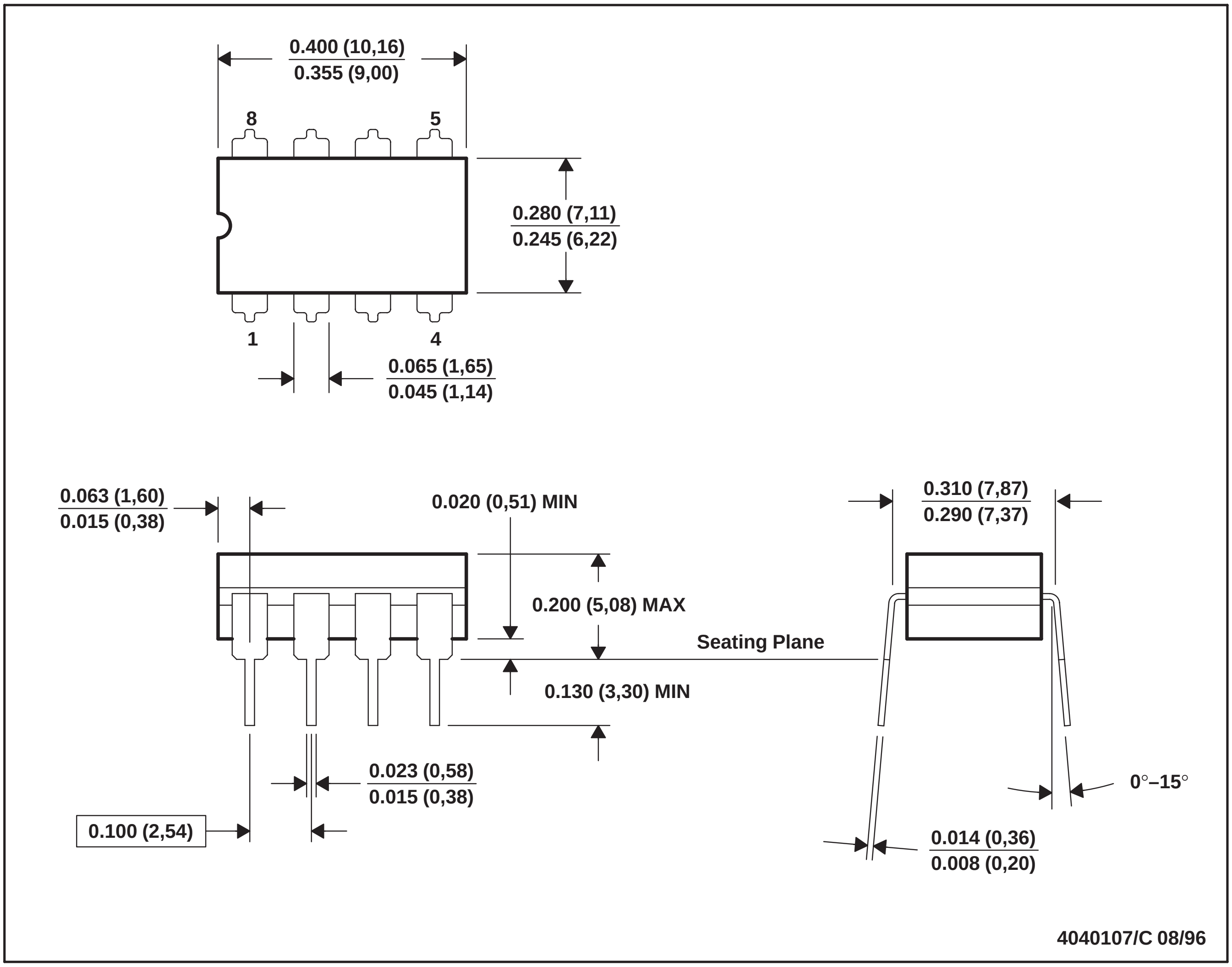
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

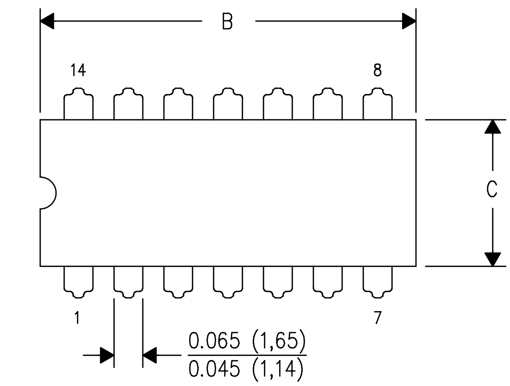
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



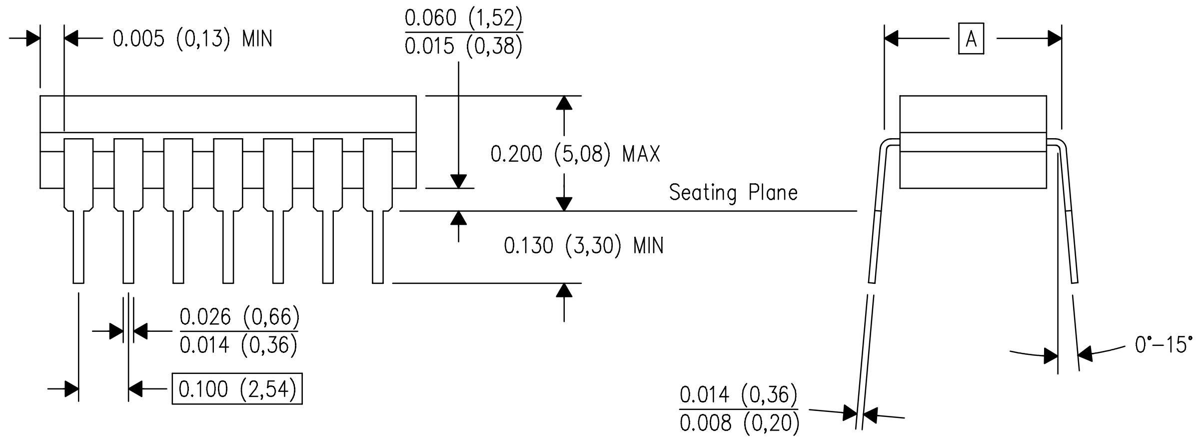
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

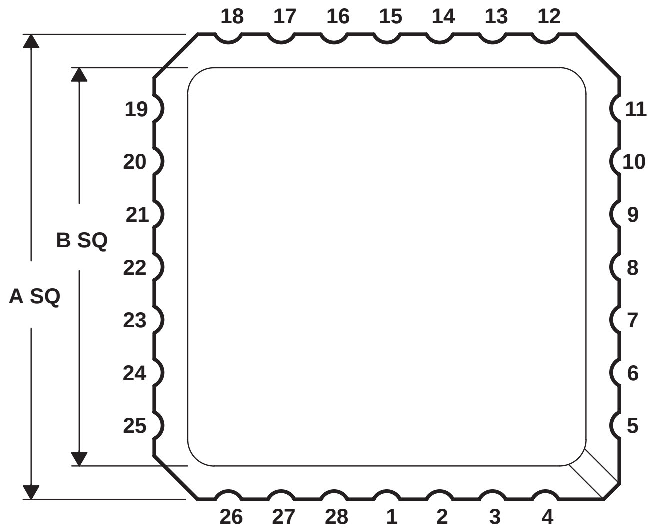


4040083/F 03/03

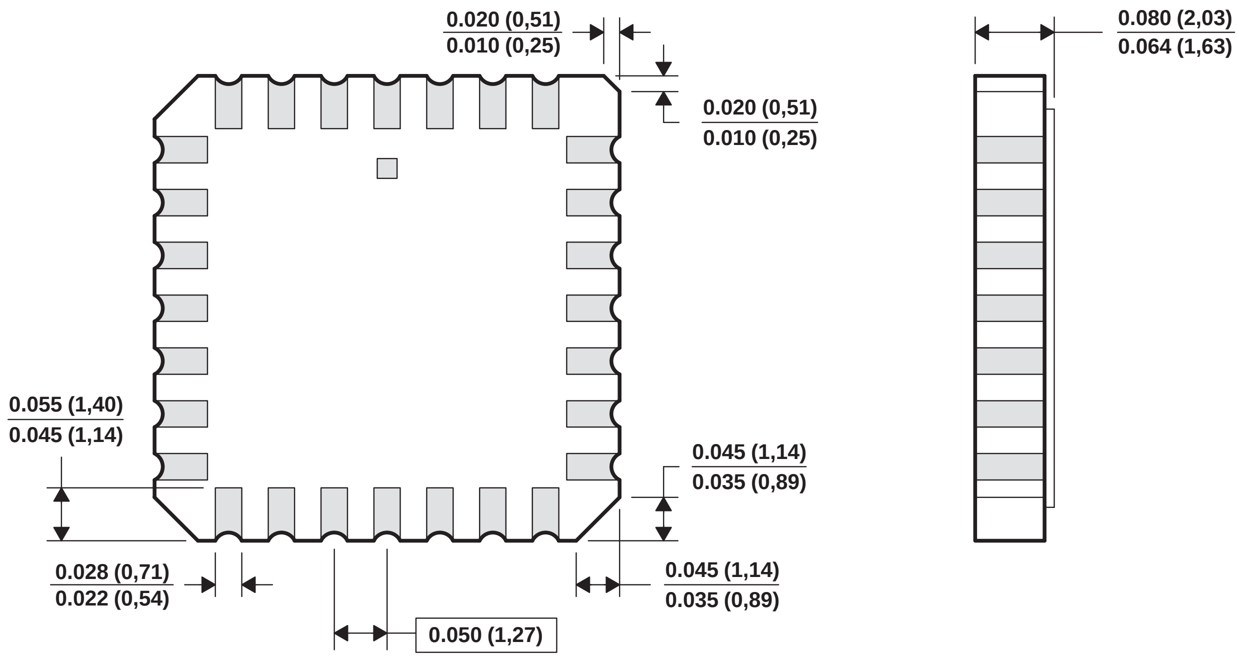
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N)** — **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



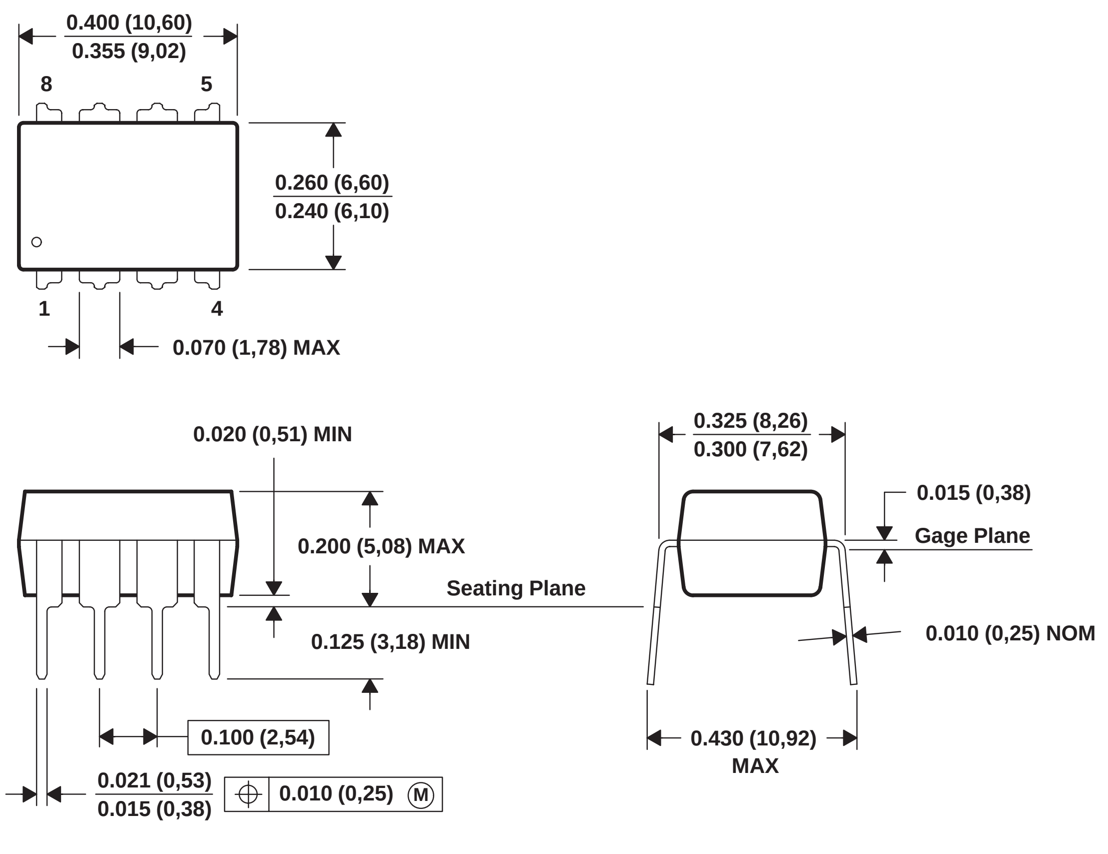
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

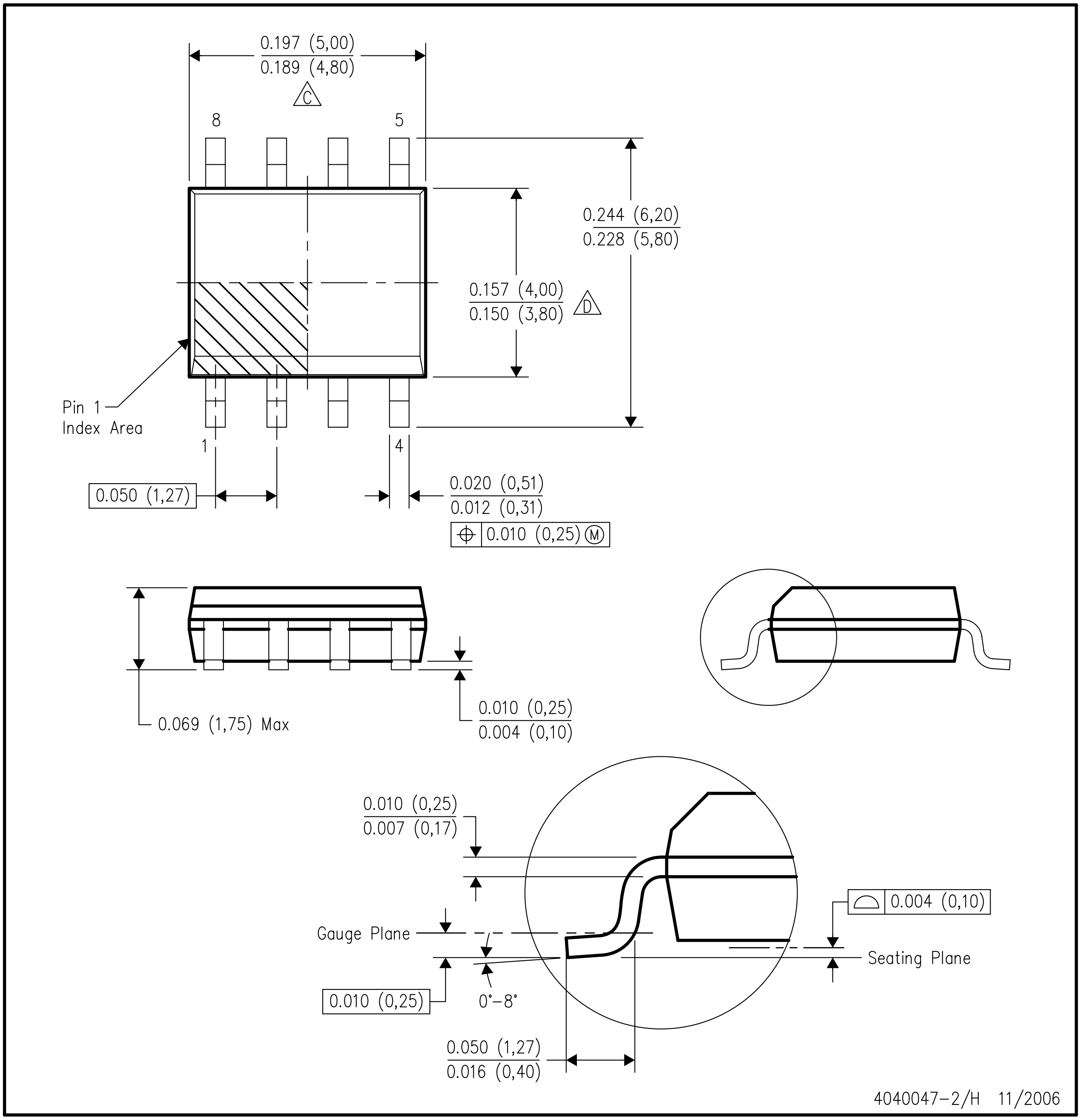
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**

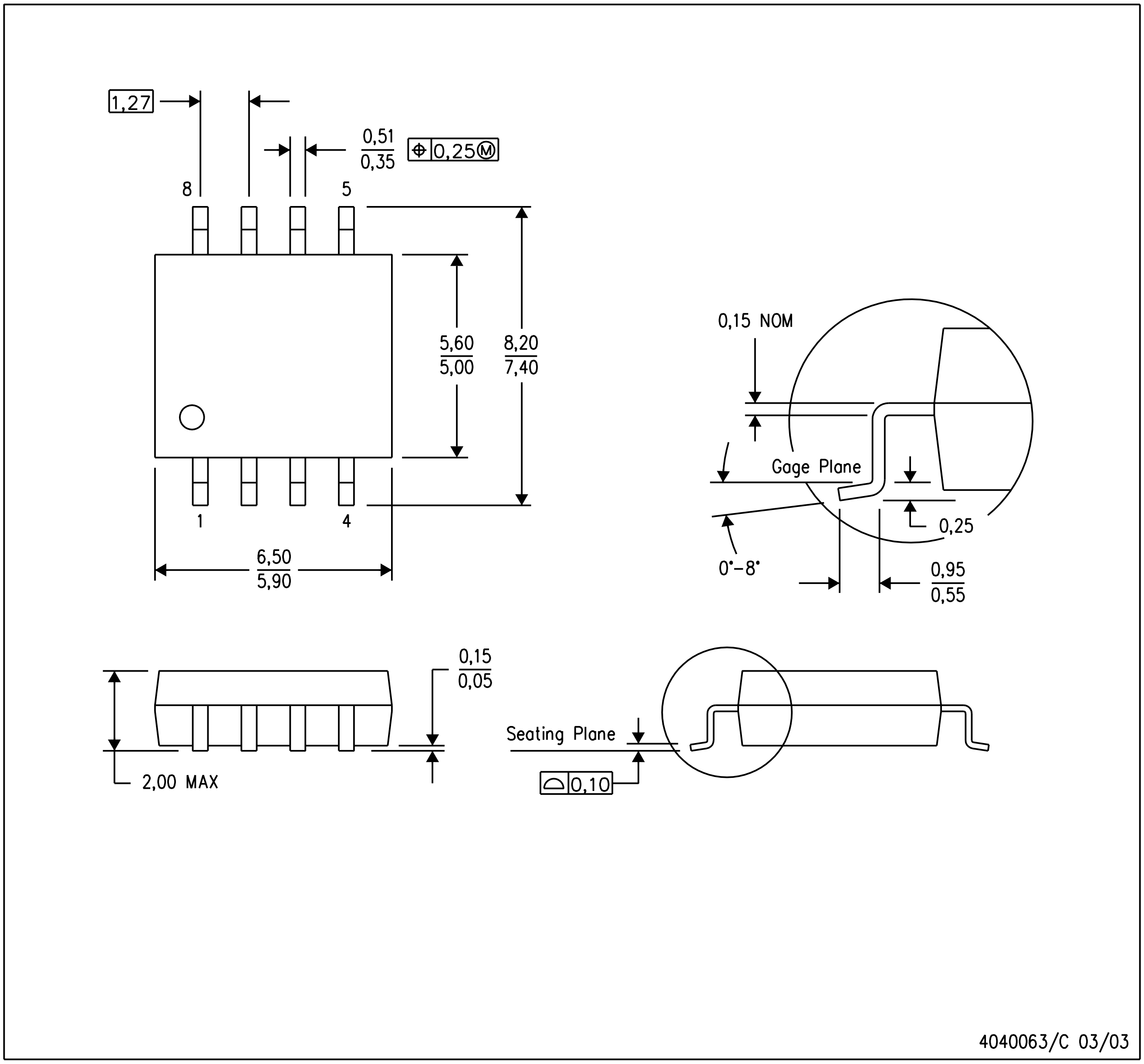


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS–012 variation AA.



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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		Video & Imaging	www.ti.com/video
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