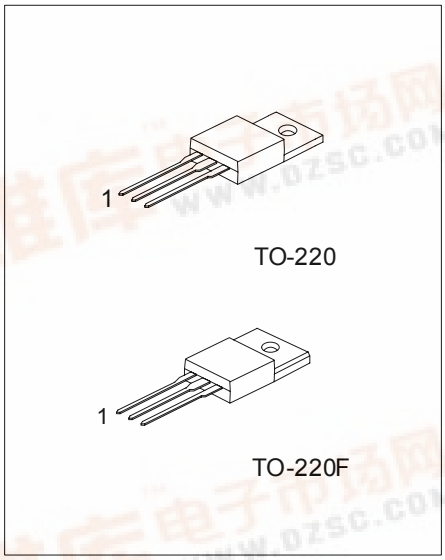
9A, 200V, 0.4Ω , N-CHANNEL POWER MOSFETS



*Pb-free plating product number: UF630L

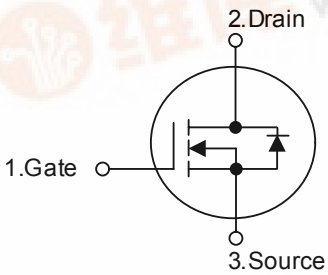
■ DESCRIPTION

The N-Channel enhancement mode silicon gate power MOSFET is designed for high voltage, high speed power switching applications such as switching regulators, switching converters, solenoid, motor drivers, relay drivers.

■ FEATURES

* 9A, 200V, Low $R_{DS(ON)}$(0.4Ω)
* Single Pulse Avalanche Energy Rated
* Rugged - SOA is Power Dissipation Limited
* Fast Switching Speeds
* Linear Transfer Characteristics
* High Input Impedance

■ SYMBOL



■ ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UF630-TA3-T	UF630L-TA3-T	TO-220	G	D	S	Tube
UF630-TF3-T	UF630L-TF3-T	TO-220F	G	D	S	Tube

UF630L-TA3-T
(1)Packing Type
(2)Package Type
(3)Lead Plating

(1) T: Tube
(2) TA3: TO-220, TF3: TO-220F
(3) L: Lead Free Plating Blank: Pb/Sn

■ ABSOLUTE MAXIMUM RATINGS (Tc = 25°C, Unless Otherwise Specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain to Source Voltage (T_J =25°C~125°C)		V_{DS}	200	V
Drain to Gate Voltage (R_{GS} = 20kΩ, T_J =25°C~125°C)		V_{DGR}	200	V
Gate to Source Voltage		V_{GS}	±20	V
Drain Current	Continuous	I_D	9	A
	Ta = 100°C		6	A
	Pulsed	I_{DM}	36	A
Maximum Power Dissipation (Ta = 25°C) Derating above 25°C		P_D	75 0.6	W W/℃
Single Pulse Avalanche Energy Rating (V_{DD}=20V, starting T_J =25°C, L=3.37mH, R_G=50Ω, peak I_{AS} = 9A)		E_{AS}	150	mJ
Operation and Storage Temperature		T_J, T_{STG}	-40 ~ +150	℃

Note: 1.Signified recommend operating range that indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits.
2.Absolute maximum ratings indicate limits beyond which damage to the device may occur.

■ ELECTRICAL SPECIFICATIONS (T_C =25°C, unless otherwise specified.)

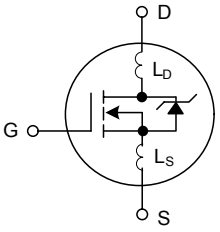
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 16)	200			V
Gate to Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
On-State Drain Current (Note 1)	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)MAX}$, V_{GS} = 10V	9			A
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V			25	μA
		V_{DS}=0.8xRated BV_{DSS},V_{GS}=0V,T_J= 125°C			250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V			±100	nA
Drain to Source On Resistance (Note 1)	$R_{DS(ON)}$	I_D = 5A, V_{GS} = 10V (Figure 14, 15)		0.25	0.85	Ω
Forward Transconductance (Note 1)	g_{FS}	V_{DS} > $I_{D(ON)}$ x $R_{DS(ON)MAX}$, I_D = 5A (Figure 18)	3	4.8		S
Turn-On Delay Time	$t_{DLY(ON)}$	V_{DD} = 90V, I_D≈9A, R_{GS} = 9.1Ω, V_{GS} = 10V R_L = 9.6Ω (Note 2)			30	ns
Rise Time	t_R				50	ns
Turn-Off Delay Time	$t_{DLY(OFF)}$				50	ns
Fall Time	t_F				40	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10V, I_D = 9A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{g(REF)}$ = 1.5mA (Figure 20) (Note 3)		19	30	nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain “Miller” Charge	Q_{GD}			9		nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz (Figure 17)		600		pF
Output Capacitance	C_{OSS}			250		pF
Reverse - Transfer Capacitance	C_{RSS}			80		pF

NOTE : 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.
2. MOSFET Switching Times are Essentially Independent of Operating Temperature.
3. Gate Charge is Essentially Independent of Operating Temperature.

■ INTERNAL PACKAGE INDUCTANCE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Internal Drain Inductance Measured from the contact screw on tab to center of die Measured from the drain lead(6mm from package) to center of die	L_D		 3.5 4.5		 nH nH
Internal Source Inductance Measured from the source lead(6mm from header) to source bond pad	L_S		 7.5		 nH

Remark: Modified MOSFET symbol showing the internal devices inductances as below.



■ THERMAL DATA

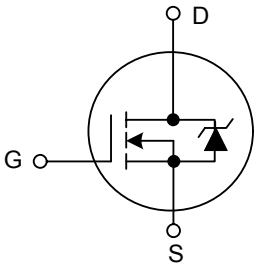
PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction-Ambient	θ_{JA}	80	°C/W
Thermal Resistance Junction-Case	θ_{Jc}	1.67	

■ SOURCE TO DRAIN DIODE SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Source to Drain Diode Voltage (Note 1)	V_{SD}	T_J = 25°C, I_{SD} = 9.0A, V_{GS} =0V (Figure 19)			2	V
Continuous Source to Drain Current	I_{SD}	Note 2			8	A
Pulse Source to Drain Current	I_{SDM}				36	A
Reverse Recovery Time	t_{RR}	T_J = 150°C, I_{SD} = 9.0A, dI_{SD}/dt = 100A/μs		450		ns
Reverse Recovery Charge	Q_{RR}	T_J = 150°C, I_{SD} = 9.0A, dI_{SD}/dt = 100A/μs		3		μC

NOTE : 1. Pulse Test: Pulse width≤300μs, Duty Cycle≤2%.

2. Modified MOSFET symbol showing the integral reverse P-N junction diode as below.



■ TEST CIRCUITS AND WAVEFORMS

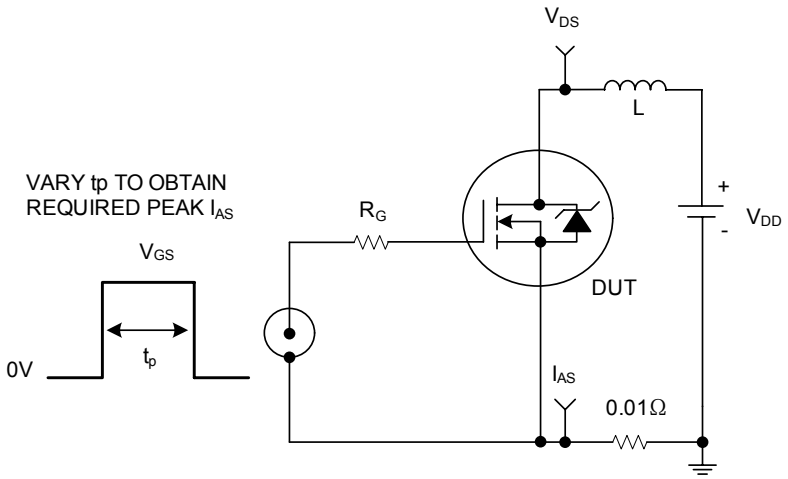


FIGURE 1. UNCLAMPED ENERGY TEST CIRCUIT

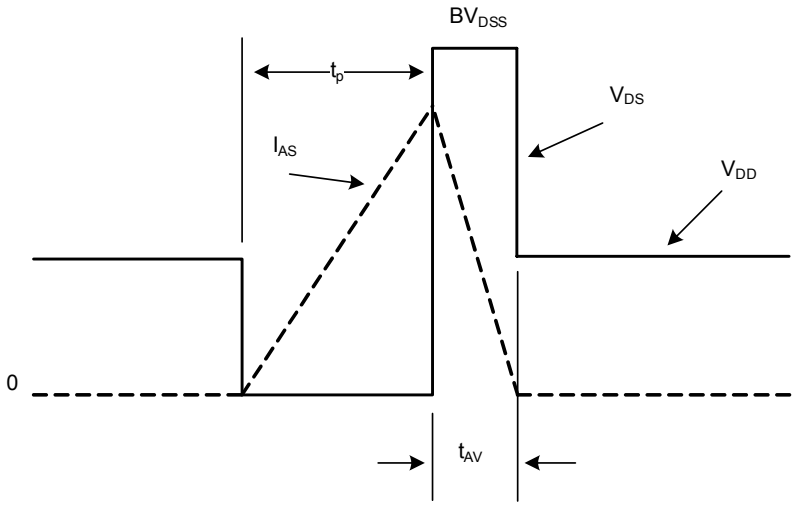


FIGURE 2. UNCLAMPED ENERGY WAVEFORMS

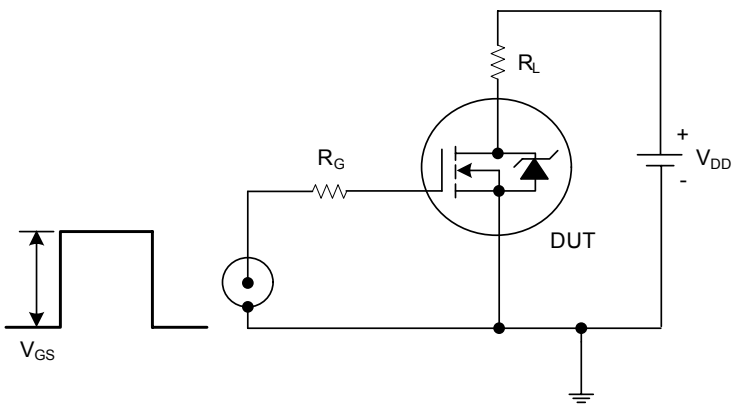


FIGURE 3. SWITCHING TIME TEST CIRCUIT

■ TEST CIRCUITS AND WAVEFORMS(cont.)

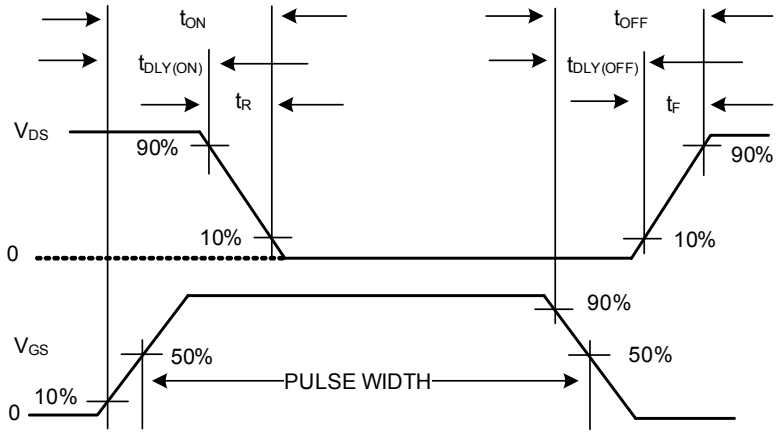


FIGURE 4. RESISTIVE SWITCHING WAVEFORMS

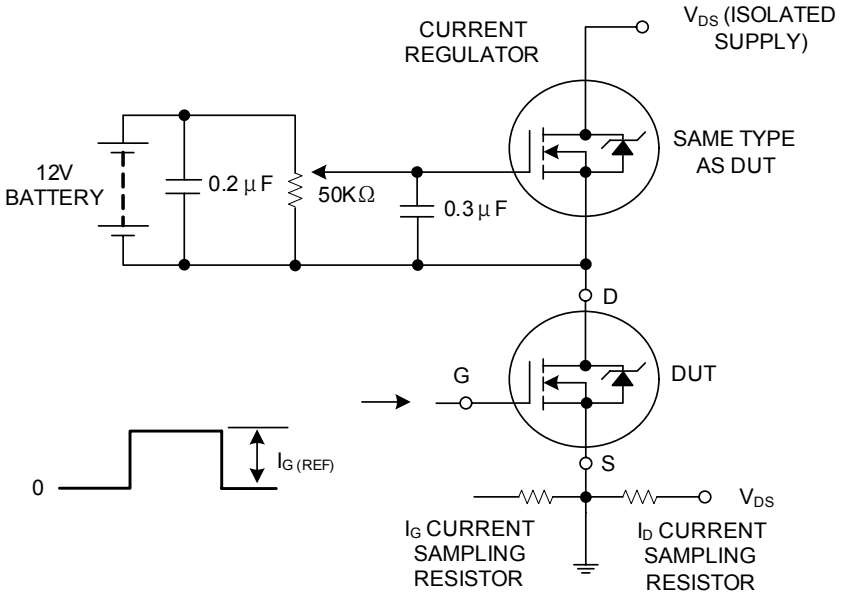


FIGURE 5. GATE CHARGE TEST CIRCUIT

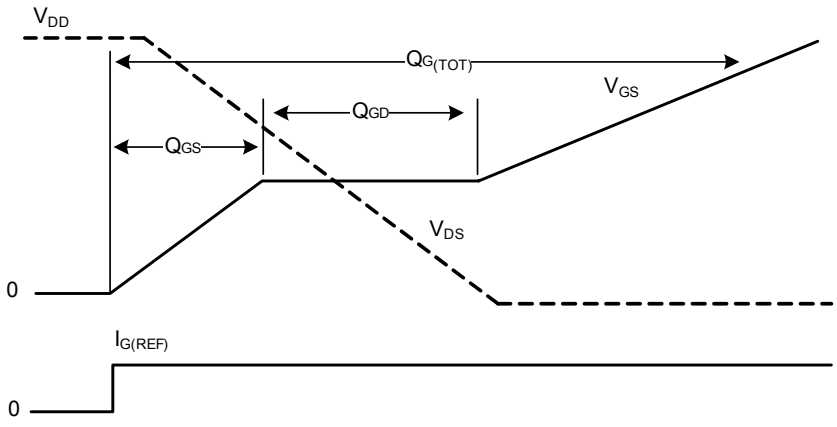


FIGURE 6. GATE CHARGE WAVEFORMS

■ TYPICAL CHARACTERISTICS

FIGURE 7. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

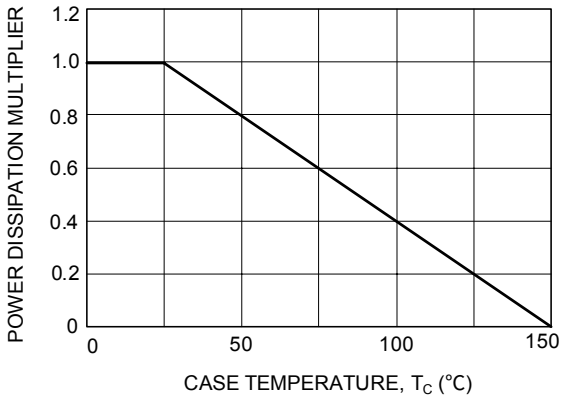


FIGURE 8. MAXIMUM CONTIONUOUS DRAIN CURRENT vs CASE TEMPERATURE

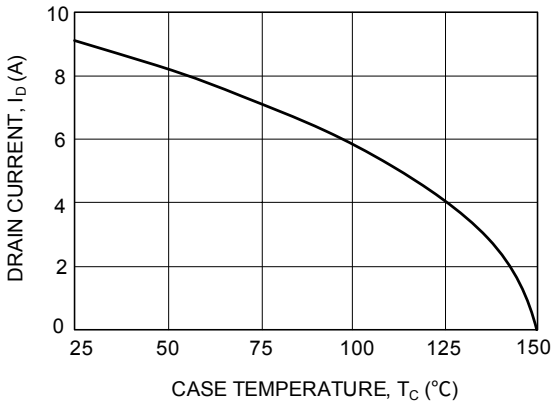


FIGURE 9. NORMALIZED TRANSIENT THERMAL IMPEDANCE

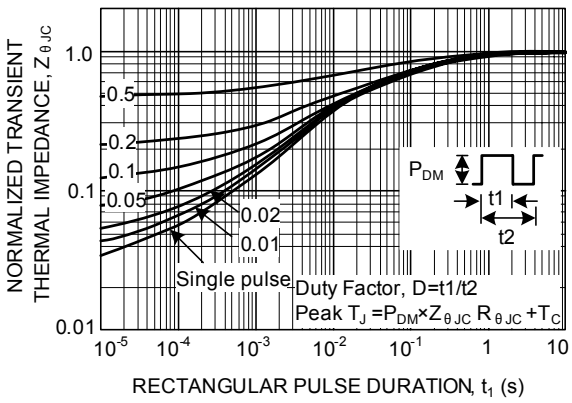


FIGURE 10. FORWARD BIAS SAFE OPERATING AREA

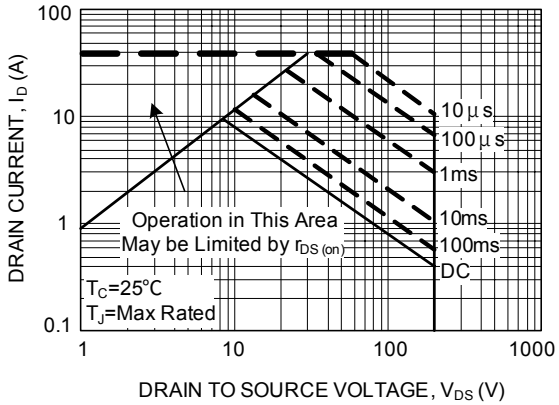


FIGURE 11. OUTPUT CHARACTERISTICS

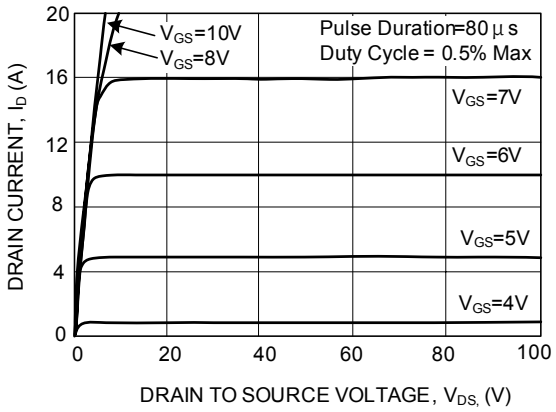
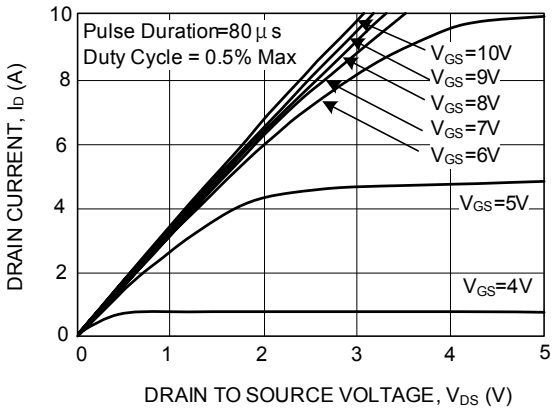


FIGURE 12. SATURATION CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (cont.)

FIGURE 13. TRANSFER CHARACTERISTICS

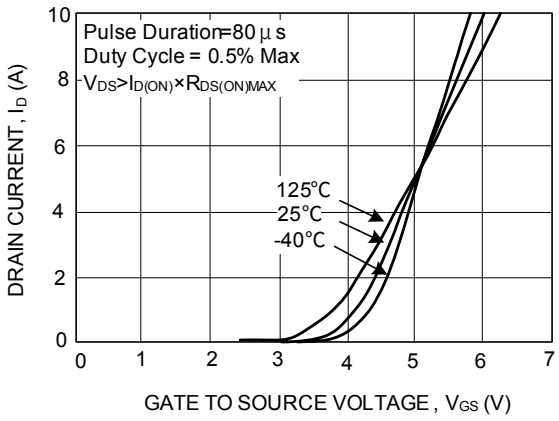


FIGURE 14. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

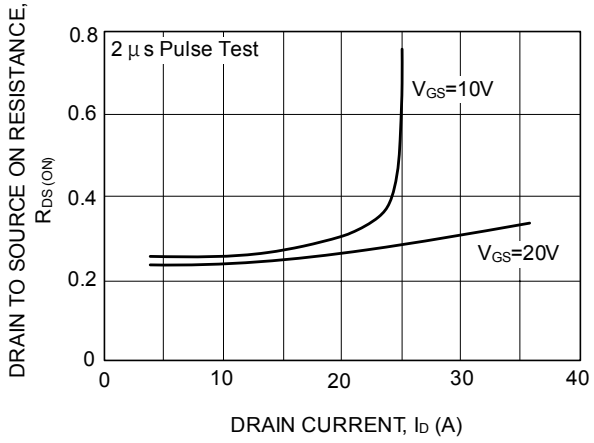


FIGURE 15. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

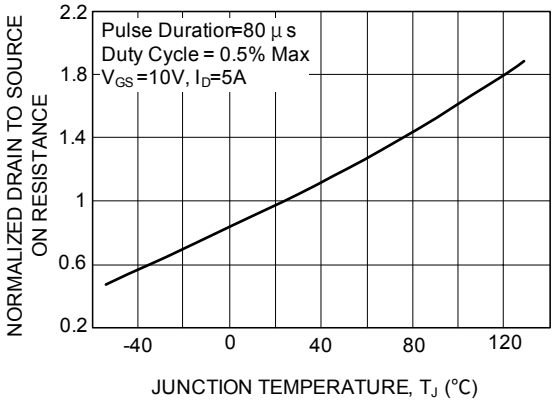


FIGURE 16. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

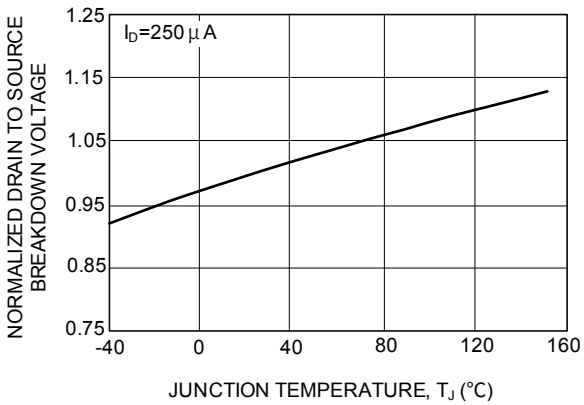


FIGURE 17. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

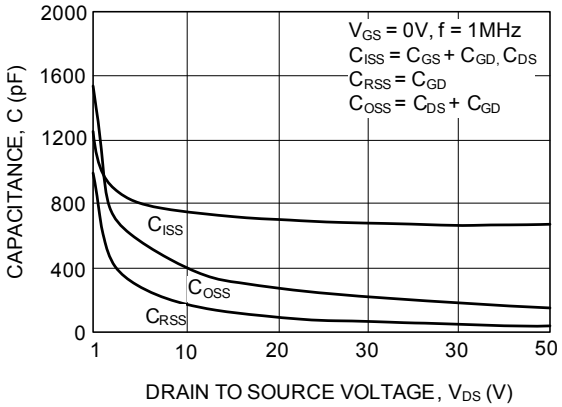
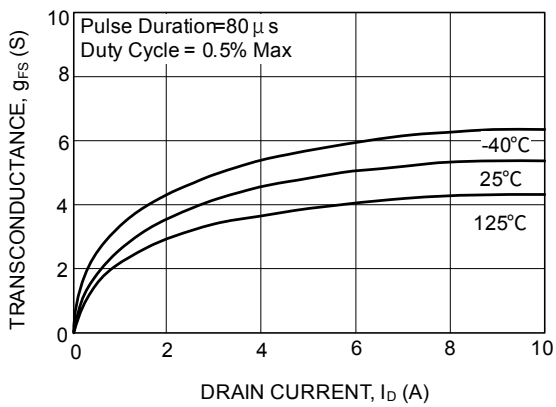


FIGURE 18. TRANSCONDUCTANCE vs DRAIN CURRENT



■ TYPICAL CHARACTERISTICS (cont.)

FIGURE 19. SOURCE TO DRAIN DIODE VOLTAGE

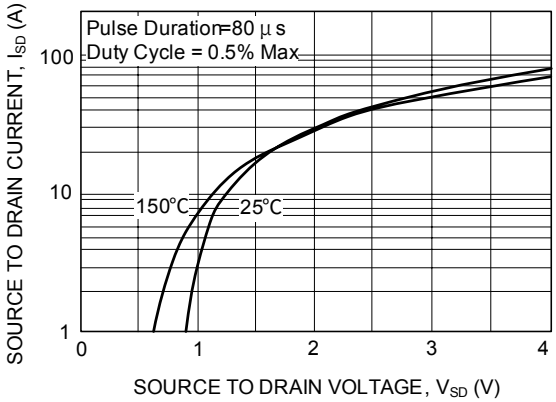


FIGURE 20. GATE TO SOURCE VOLTAGE vs GATE CHARGE