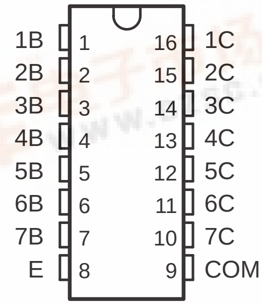
ULQ2003A-Q1, ULQ2004A-Q1, HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAY

SGLS148B − DECEMBER 2002 − REVISED JUNE 2006

- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **ESD Protection Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**

† Contact Texas Instruments for details. Q100 qualification data available on request.

D PACKAGE
(TOP VIEW)



description

The ULQ2003A and ULQ2004A are high-voltage high-current Darlington transistor arrays. Each consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULQ2003A has a 2.7-kΩ series base resistor for each Darlington pair, for operation directly with TTL or 5-V CMOS devices. The ULQ2004A has a 10.5-kΩ series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULQ2004A is below that of the ULQ2003A.

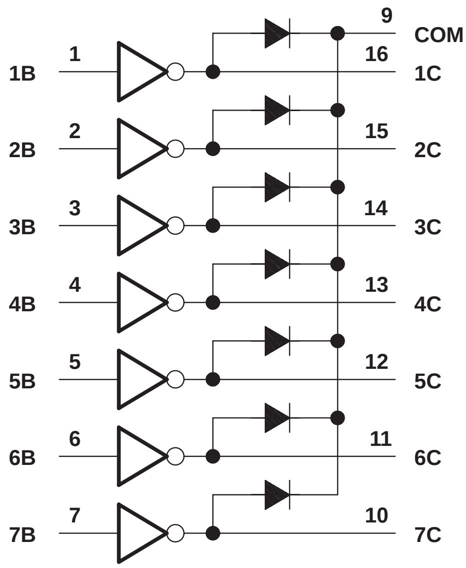
AVAILABLE OPTIONS

T_A	D PACKAGES† SMALL OUTLINE
−40°C to 105°C	ULQ2003ATDQ1 ULQ2003ATDRQ1
	ULQ2004ATDQ1‡ ULQ2004ATDRQ1
−40°C to 125°C	ULQ2003AQDRQ1

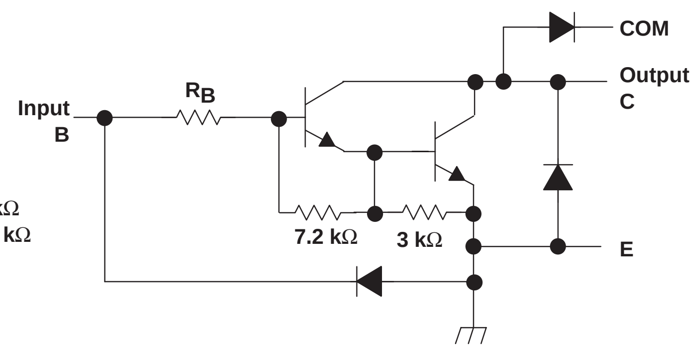
† The D package is available taped and reeled. Add the suffix R to device type (e.g., ULQ2003TDADRQ1).
‡ ULQ2004ATDQ1 is Product Preview only.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage	50 V
Clamp diode reverse voltage (see Note 1)	50 V
Input voltage, V_I (see Note 1)	30 V
Peak collector current (see Figure 14)	500 mA
Output clamp current, I_{OK}	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 2)	73°C/W
Operating free-air temperature range, T_A,	−40°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A = 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 105°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW	190 mW

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		ULQ2003AT			ULQ2003AQ			ULQ2004A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$	On-state input voltage, See Figure 6	$V_{CE} = 2$ V	$I_C = 125$ mA									5	V
			$I_C = 200$ mA			2.7			2.7			6	
			$I_C = 250$ mA			2.9			2.9				
			$I_C = 275$ mA									7	
			$I_C = 300$ mA			3			3				
			$I_C = 350$ mA									8	
$V_{CE(sat)}$	Collector-emitter saturation voltage, See Figure 5	$I_I = 250$ µA,	$I_C = 100$ mA		0.9	1.2		1	1.3		0.9	1.1	V
		$I_I = 350$ µA,	$I_C = 200$ mA		1	1.4		1	1.5		1	1.3	
		$I_I = 500$ µA,	$I_C = 350$ mA		1.2	1.7		1.2	1.8		1.2	1.6	
I_{CEX}	Collector cutoff current	$V_{CE} = 50$ V, $I_I = 0$, See Figure 1				100			110			50	µA
		$V_{CE} = 50$ V, See Figure 2	$I_I = 0$									100	
			$V_I = 1$ V									500	
V_F	Clamp forward voltage, See Figure 8	$I_F = 350$ mA			1.7	2.2		1.7	2.2		1.7	2.1	V
$I_{I(off)}$	Off-state input current, See Figure 3	$V_{CE} = 50$ V,	$I_C = 500$ µA	30	65		30	65		50	65		µA
I_I	Input current, see Figure 4	$V_I = 3.85$ V			0.93	1.35		0.93	1.35				mA
		$V_I = 5$ V									0.35	0.5	
		$V_I = 12$ V									1	1.45	
I_R	Clamp reverse current, See Figure 7	$V_R = 50$ V,	$T_A = 25°C$			100			100			50	µA
		$V_R = 50$ V				100			100			100	
C_i	Input capacitance	$V_I = 0$,	f = 1 MHz		15	25		15	25		15	25	pF

switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ULQ2003A, ULQ2004A			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high level output	See Figure 9		1	10	µs
t_{PHL}	Propagation delay time, high-to-low level output	See Figure 9		1	10	µs
V_{OH}	High-level output voltage after switching	$V_S = 50$ V, $I_O \approx 300$ mA, See Figure 10	$V_S - 500$			mV

PARAMETER MEASUREMENT INFORMATION

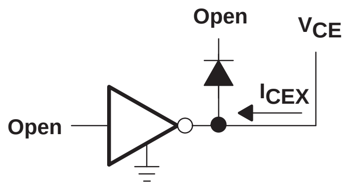


Figure 1. I_{CEX} Test Circuit

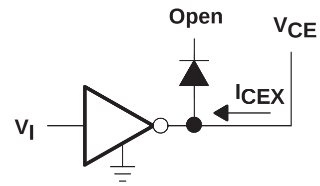


Figure 2. I_{CEX} Test Circuit

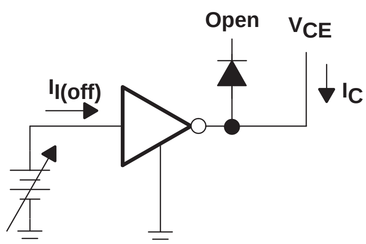


Figure 3. $I_{I(off)}$ Test Circuit

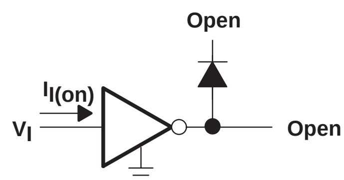
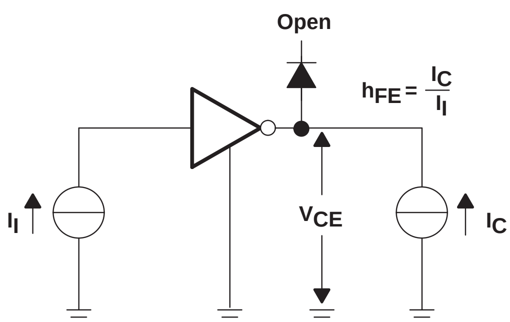


Figure 4. I_I Test Circuit



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

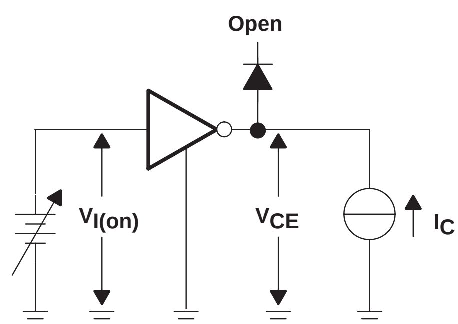


Figure 6. $V_{I(on)}$ Test Circuit

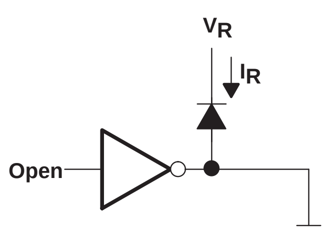


Figure 7. I_R Test Circuit

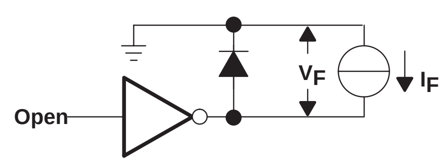


Figure 8. V_F Test Circuit

PARAMETER MEASUREMENT INFORMATION

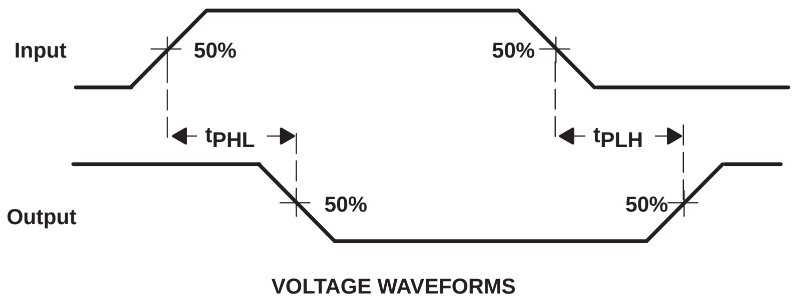
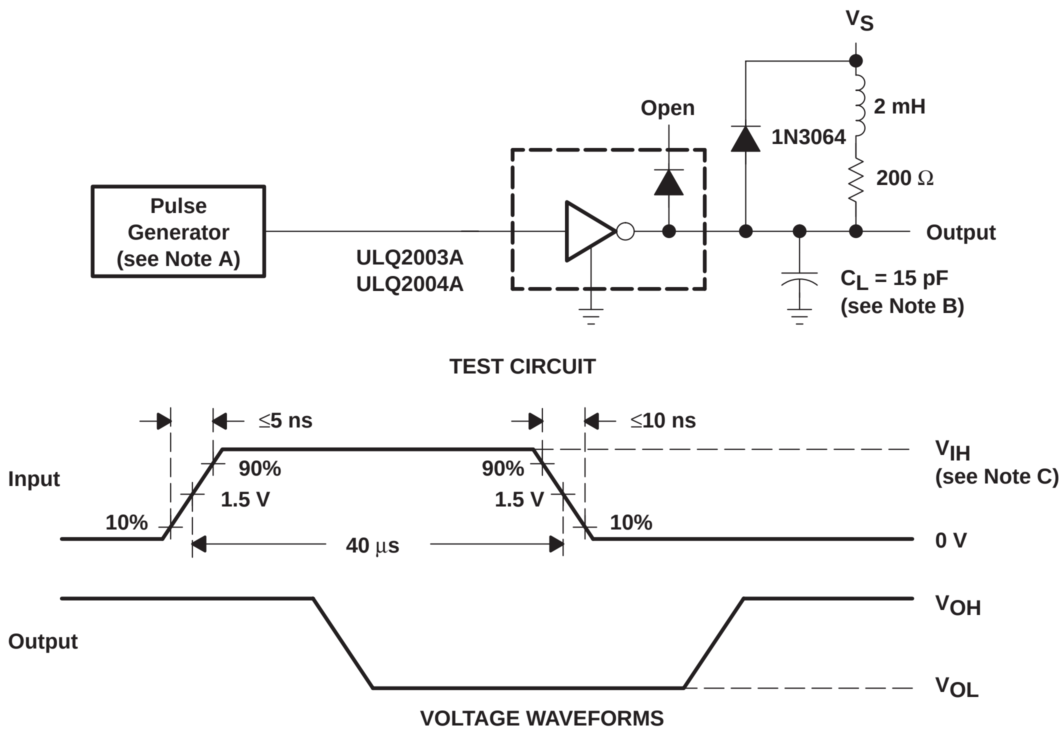


Figure 9. Propagation Delay-Time Waveforms



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULQ2003A, V_{IH} = 3 V; for the ULQ2004A, V_{IH} = 8 V.

Figure 10. Latch-Up Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

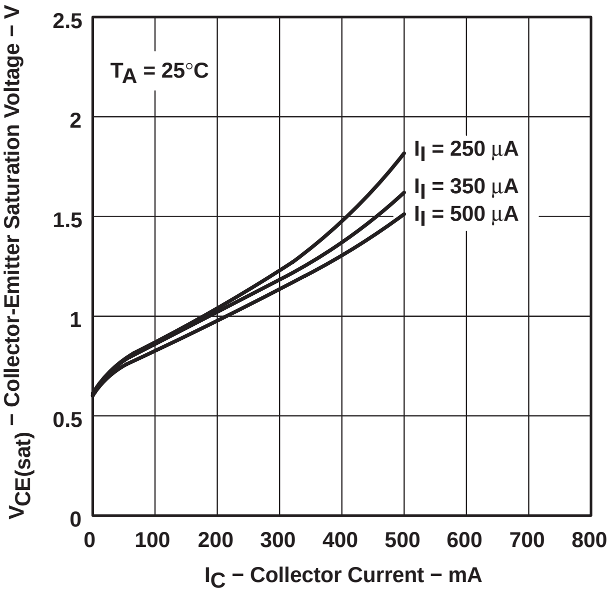


Figure 11

COLLECTOR-EMITTER SATURATION VOLTAGE vs TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)

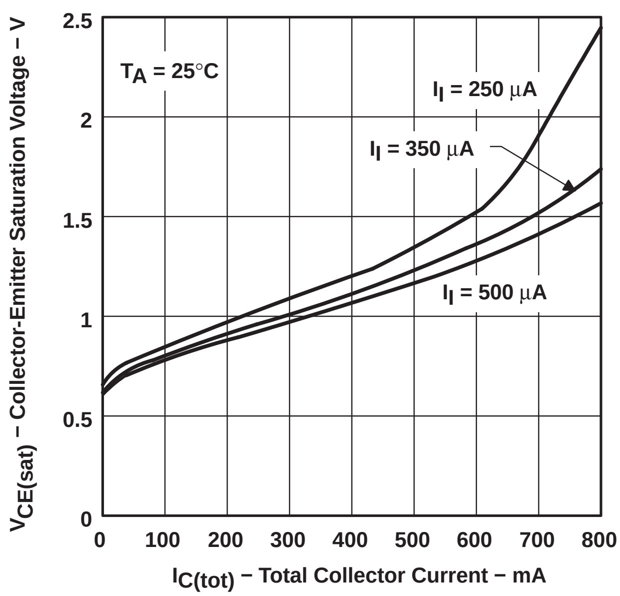


Figure 12

COLLECTOR CURRENT vs INPUT CURRENT

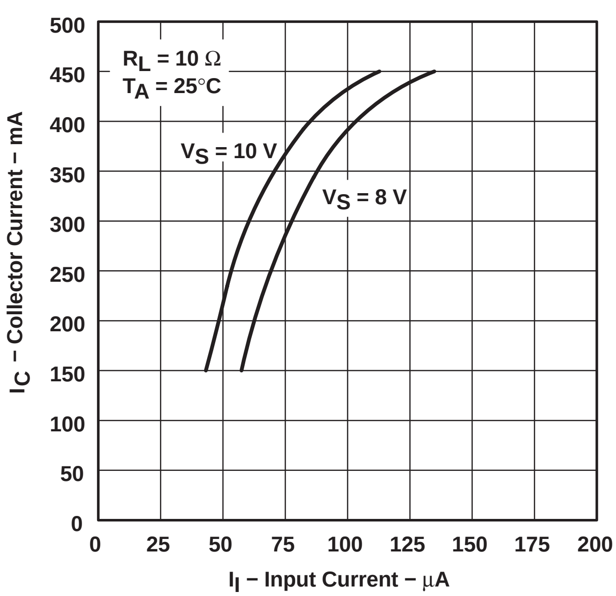


Figure 13

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

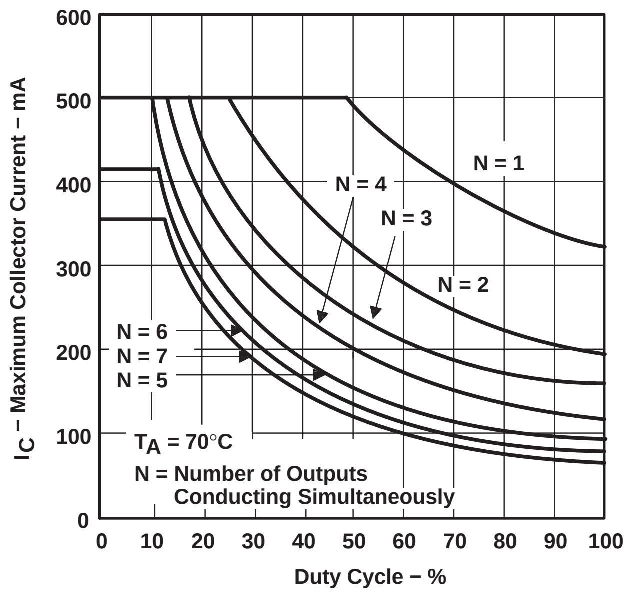


Figure 14

APPLICATION INFORMATION

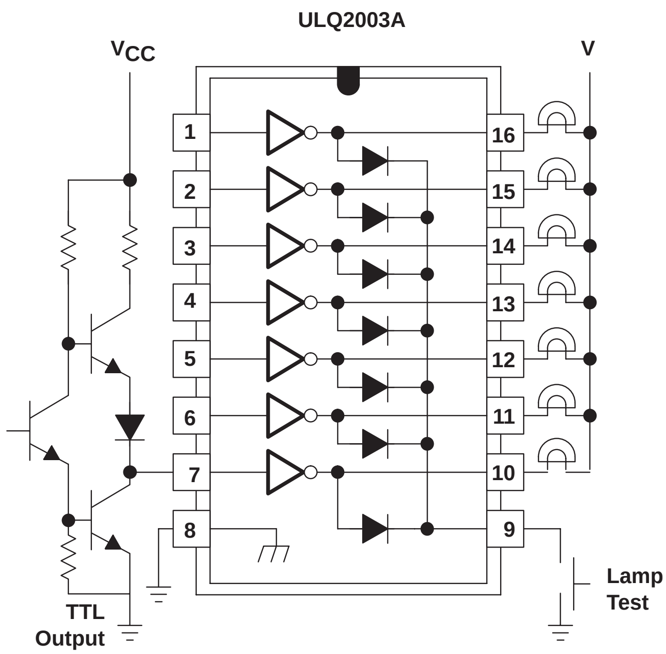


Figure 15. TTL to Load

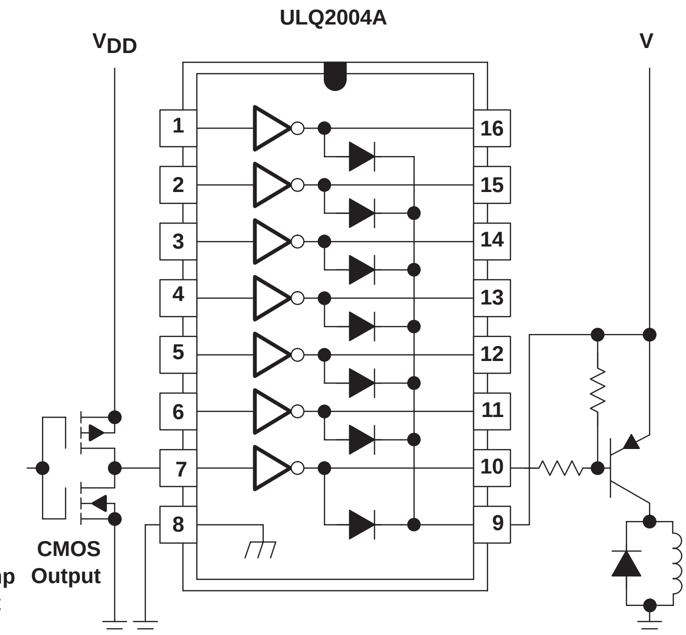


Figure 16. Buffer for Higher Current Loads

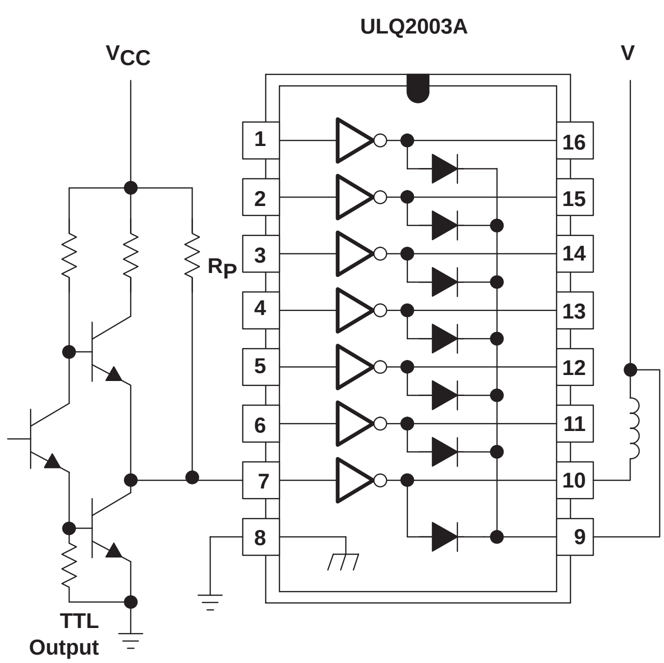


Figure 17. Use of Pullup Resistors
to Increase Drive Current

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
ULQ2003AQDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ULQ2003ATDQ1	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2003ATDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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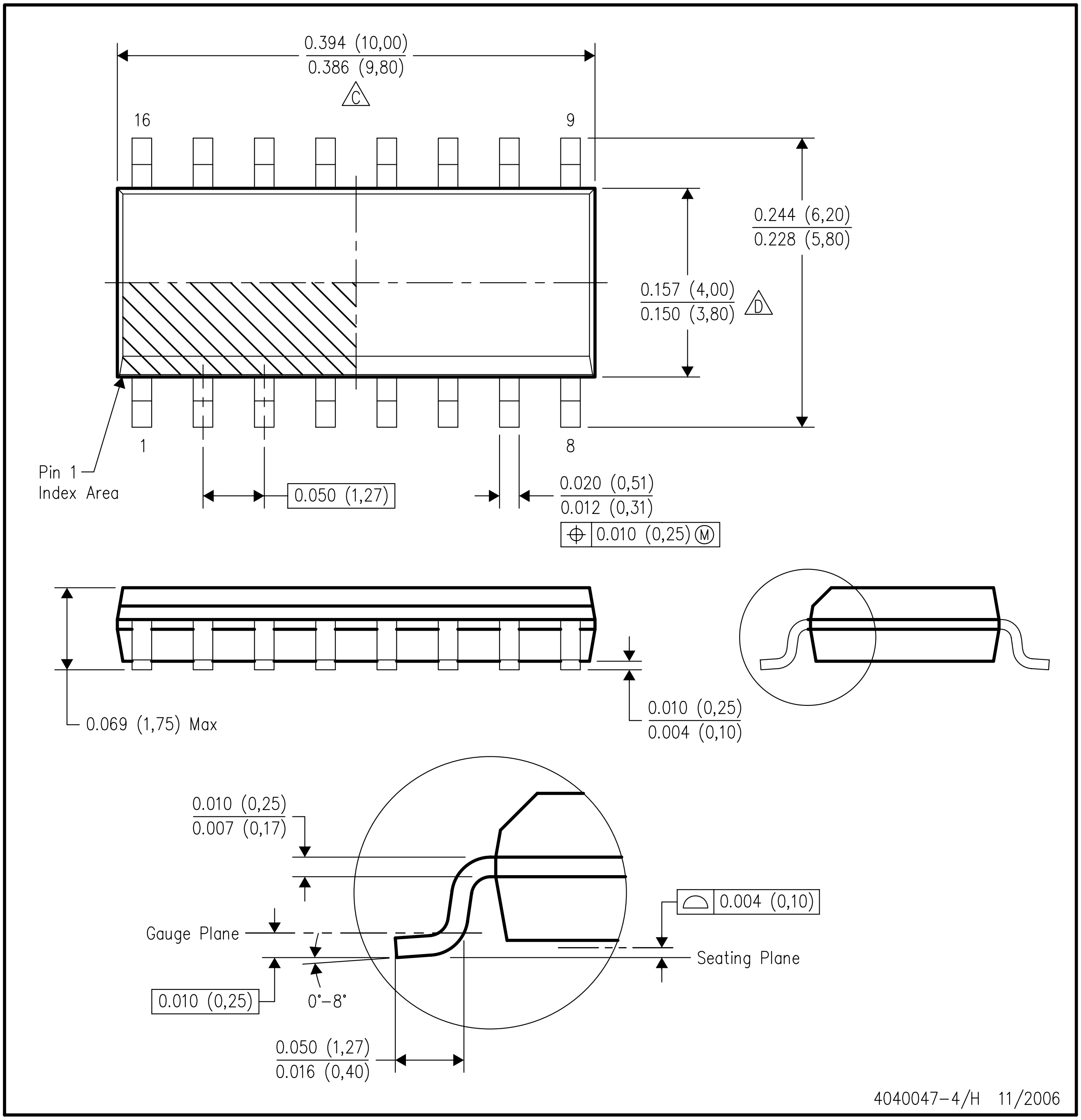
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AC.

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