UMC

UMC

UM6164 Series

PRELIMINARY

8K × 8 High Speed CMOS SRAM

Features

- Single +5 volt power supply
- Access times: 20/25/30 ns (max.)
- Current:
  - Standard version: Operating: 170 mA (max.)
    Standby: 2 mA (max.)
  - Low power version: Operating: 170 mA (max.)
    Standby: 100 μA (max.)
- Fully static operation, no clock or refreshing required
- Directly TTL compatible: All inputs and outputs
- Common I/O using three-state output
- Output enable and two chip select inputs for easy application
- Data retention voltage: 2V (min.) for low power version
- Available in 28 pin SOP, or Skinny DIP packages (See ordering information)

General Description

The UM6164 is a high speed, low-power 8,192-word by 8-bit CMOS static RAM. It is fabricated using UMC's high performance CMOS double metal technology. This highly reliable process coupled with innovative circuit design techniques yields access times as fast as 20 ns.

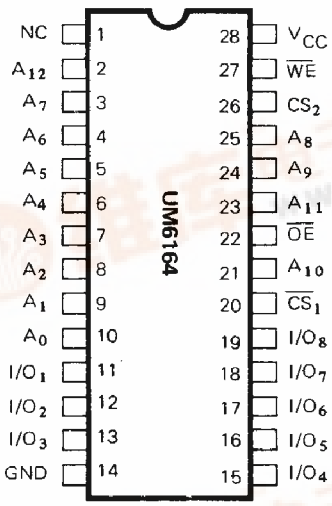
When $\overline{CS}_1$ is high or CS_2 is low (de-select), the device assumes a standby mode at which the power dissipation can be reduced to 25 μW (typical) at CMOS input levels.

Easy memory expansion is provided by using two Chip Select inputs $\overline{CS}_1$ and CS_2. The active low Write Enable controls both writing and reading of the memory.

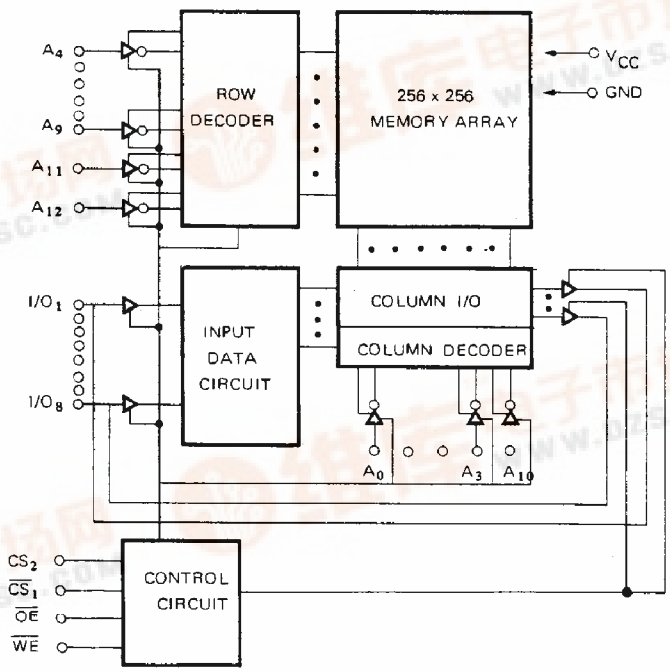
The UM6164 is pin compatible with 2764 type EPROM's and other 8K x 8 SRAM's.

High Speed SRAM

Pin Configuration



Block Diagram



Truth Table

Mode	$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O Operation	V_{CC} Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disabled	L	H	H	H	High Z	I_{CC}, I_{CC1}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X : H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}*	Input Capacitance		5	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		7	pF	$V_{I/O}$ = 0V

* This parameter is sampled and not 100% tested.

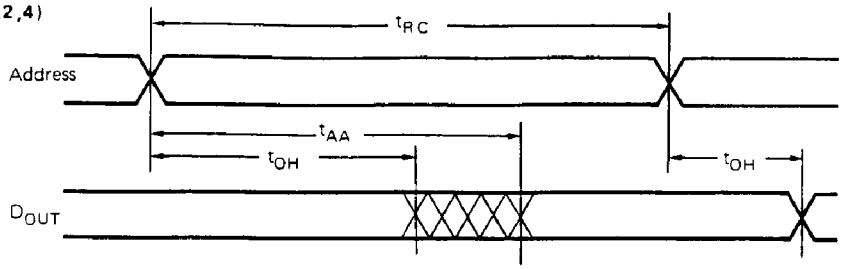
AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter		UM6164-20/20L Min.	UM6164-20/20L Max.	UM6164-25/25L Min.	UM6164-25/25L Max.	UM6164-30/30L Min.	UM6164-30/30L Max.	Unit
Read Cycle									
t_{RC}	Read Cycle Time		20	–	25	–	30	–	ns
t_{AA}	Address Access Time		–	20	–	25	–	30	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS_1}$	–	20	–	25	–	30	ns
t_{ACS2}		CS_2	–	20	–	25	–	30	ns
t_{OE}	Output Enable to Output Valid		–	7	–	9	–	12	ns
t_{CLZ1}	Chip Selection to Output in Low Z	$\overline{CS_1}$	3	–	3	–	3	–	ns
t_{CLZ2}		CS_2	3	–	3	–	3	–	ns
t_{OLZ}	Output Enable to Output in Low Z		0	–	0	–	0	–	ns
t_{CHZ1}	Chip Deselection to Output in High Z	$\overline{CS_1}$	0	10	0	12	0	15	ns
t_{CHZ2}		CS_2	0	10	0	12	0	15	ns
t_{OHZ}	Output Disable to Output in High Z		0	10	0	12	0	15	ns
t_{OH}	Output Hold from Address Change		3	–	3	–	3	–	ns
Write Cycle									
t_{WC}	Write Cycle Time		20	–	25	–	30	–	ns
t_{CW}	Chip Selection to End of Write		17	–	22	–	25	–	ns
t_{AS}	Address Set-up Time		0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write		15	–	22	–	25	–	ns
t_{WP}	Write Pulse Width		12	–	15	–	18	–	ns
t_{WR}	Write Recovery Time		0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High Z		0	10	0	12	0	15	ns
t_{DW}	Data to Write Time Overlap		10	–	12	–	15	–	ns
t_{DH}	Data Hold from Write Time		0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High Z		0	10	0	12	0	15	ns
t_{OW}	Output Active from End of Write		0	–	0	–	0	–	ns

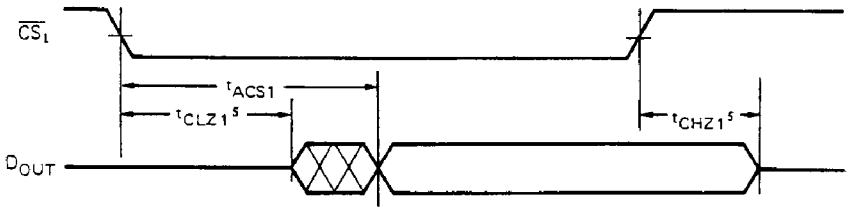
Note: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

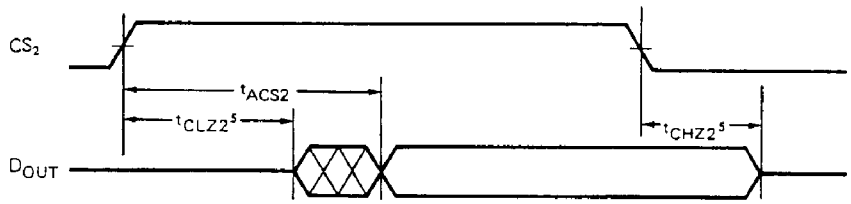
Read Cycle 1 (1,2,4)



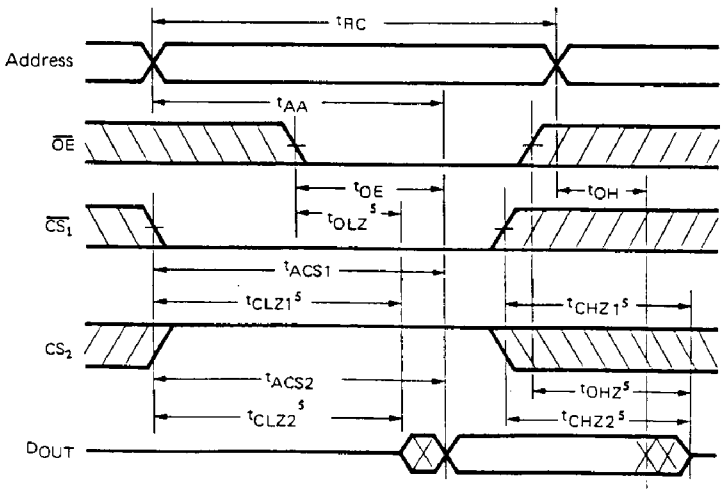
Read Cycle 2 (1,3,4,6)



Read Cycle 3 (1,4,7,8)



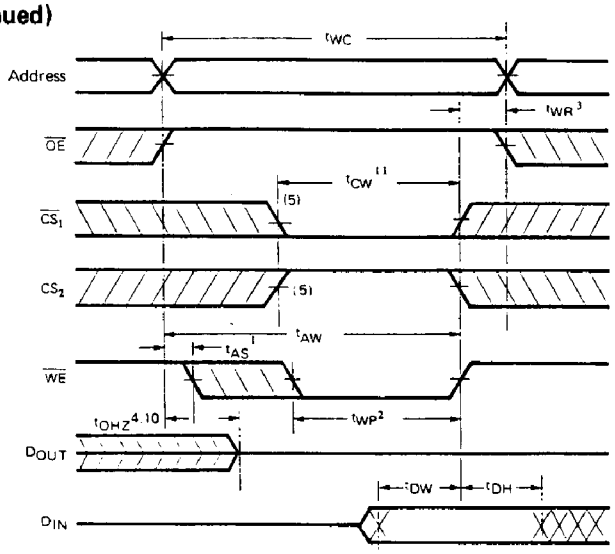
Read Cycle 4 (1)



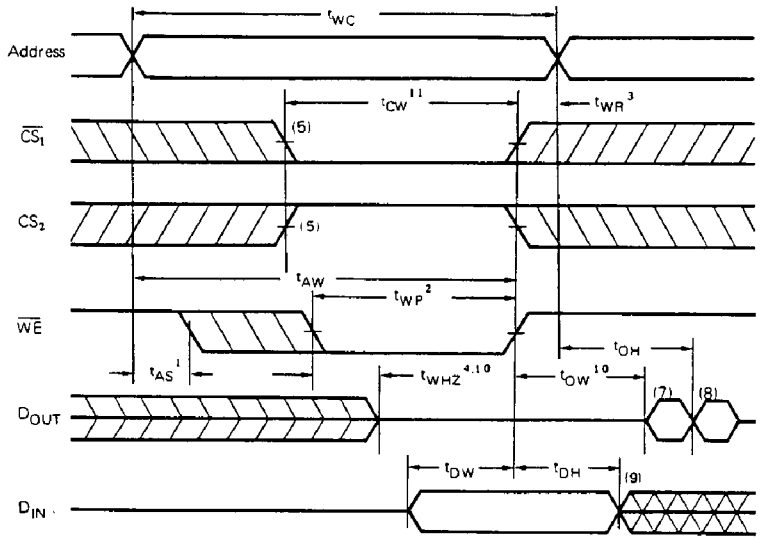
Notes: 1. $\overline{WE}$ is high for READ cycle.
2. Device is continuously selected $\overline{CS_1} = V_{IL}$ and $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.
8. Address valid prior to or coincident with CS_2 transition high.

Timing Waveforms (Continued)

Write Cycle 1



Write Cycle 2 (6)



Notes:
1. t_{AS} is measured from the address valid to the beginning of write.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to I/O pins.
10. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

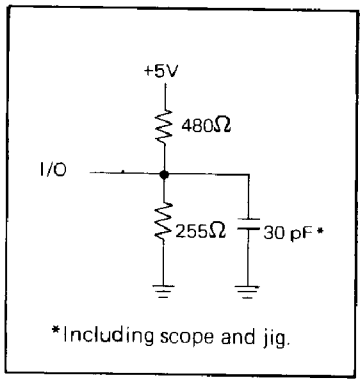


Figure 1. Output Load

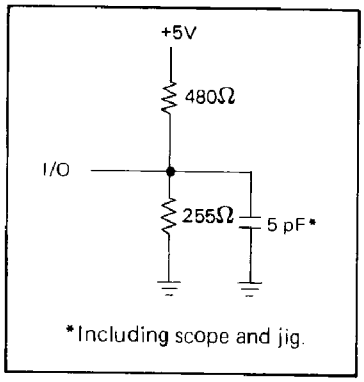


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0 to +70°C; L version only)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{DR_1}	V_{CC} for Data Retention	2.0	–	V	$\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ or $CS_2 \leq 0.2V$
V_{DR_2}		2.0	–	V	$CS_2 \leq 0.2V$
I_{CCDR_1}	Data Retention Current	–	100	μA	V_{CC} = 3.0V, $\overline{CS_1} \geq V_{CC} - 0.2V$, $CS_2 \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
I_{CCDR_2}		–	100	μA	$\overline{CS_1} \leq 0.2V$, $CS_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Deselect to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	–	ns	

*t_{RC} = Read Cycle Time