

**SWITCHING**  
**DUAL P-CHANNEL POWER MOS FET**  
**INDUSTRIAL USE**

**DESCRIPTION**

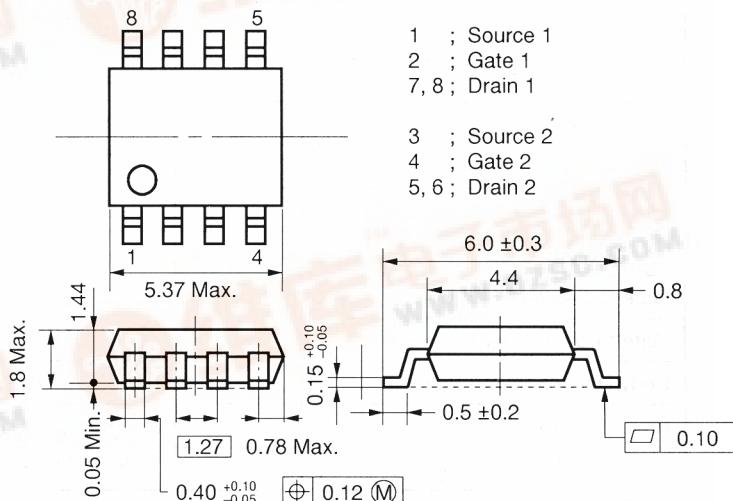
This product is Dual P-Channel MOS Field Effect Transistor designed for power management switch applications of notebook computers and cellphones.

**FEATURES**

- Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance  
 $R_{DS(on)1} = 0.09 \Omega$  Max. ( $V_{GS} = -10$  V,  $I_D = -1.8$  A)  
 $R_{DS(on)2} = 0.18 \Omega$  Max. ( $V_{GS} = -4$  V,  $I_D = -1.8$  A)
- Low  $C_{iss}$   $C_{iss} = 540$  pF Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

**PACKAGE DIMENSIONS**

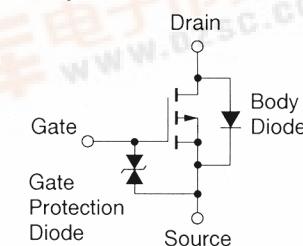
(in millimeter)

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, all terminals are connected.)**

Drain to Source Voltage	V <sub>DSS</sub>	-20	V
Gate to Source Voltage	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±3.5	A
Drain Current (pulse)*	I <sub>D(pulse)</sub>	±14	A
Total Power Dissipation (1 unit)**	P <sub>T</sub>	1.7	W
Total Power Dissipation (2 unit)**	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

\* PW ≤ 10  $\mu$ s, Duty Cycle ≤ 1 %

\*\* T<sub>A</sub> = 25 °C, Mounted on ceramic substrate of 2 000 mm<sup>2</sup> × 1.1 mm



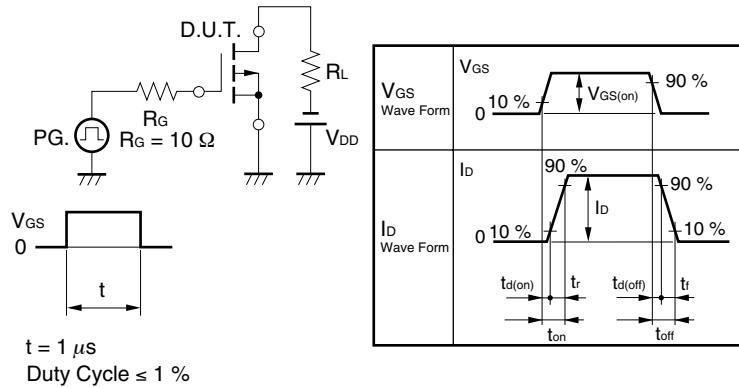
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

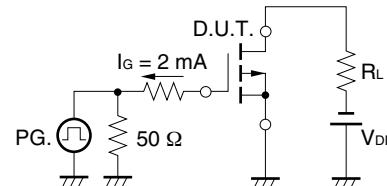
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , all terminals are connected.)

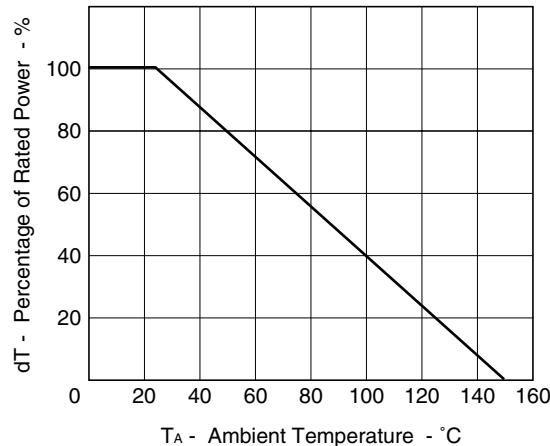
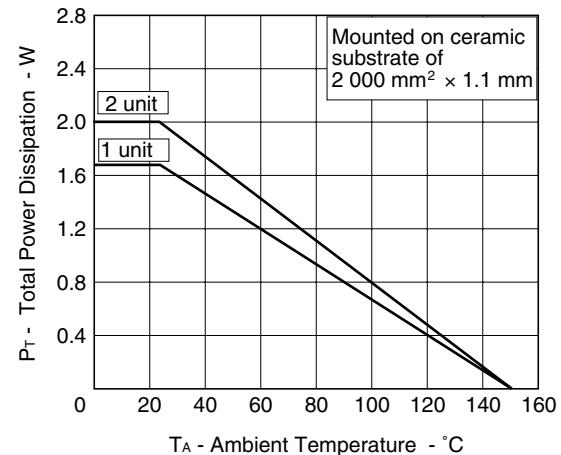
Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain to Source On-state Resistance	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}$ , $I_D = -1.8\text{ A}$		0.065	0.090	$\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4\text{ V}$ , $I_D = -1.8\text{ A}$		0.125	0.180	$\Omega$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}$ , $I_D = -1\text{ mA}$	-1.0	-1.7	-2.5	$\text{V}$
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = -10\text{ V}$ , $I_D = -1.8\text{ A}$	2.0	4.4		$\text{S}$
Drain Leakage Current	$I_{DSS}$	$V_{DS} = -20\text{ V}$ , $V_{GS} = 0$			-10	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0$			$\pm 10$	$\mu\text{A}$
Input Capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}$ $V_{GS} = 0$ $f = 1\text{ MHz}$		540		$\text{pF}$
Output Capacitance	$C_{oss}$			385		$\text{pF}$
Reverse Transfer Capacitance	$C_{rss}$			105		$\text{pF}$
Turn-On Delay Time	$t_{d(on)}$	$I_D = -1.8\text{ A}$		10		$\text{ns}$
Rise Time	$t_r$	$V_{GS(on)} = -10\text{ V}$		110		$\text{ns}$
Turn-off Delay Time	$t_{d(off)}$	$V_{DD} = -10\text{ V}$		340		$\text{ns}$
Fall Time	$t_f$	$R_G = 10\Omega$		230		$\text{ns}$
Total Gate Charge	$Q_G$	$I_D = -3.5\text{ A}$		18		$\text{nC}$
Gate to Source Charge	$Q_{GS}$	$V_{DD} = -16\text{ V}$		2.0		$\text{nC}$
Gate to Drain Charge	$Q_{GD}$	$V_{GS} = -10\text{ V}$		5.1		$\text{nC}$
Body Diode Forward Voltage	$V_{F(S-D)}$	$I_F = 3.5\text{ A}$ , $V_{GS} = 0$		0.8		$\text{V}$
Reverse Recovery Time	$t_{rr}$	$I_F = 3.5\text{ A}$ , $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$		160		$\text{ns}$
Reverse Recovery Charge	$Q_{rr}$			310		$\text{nC}$

Test Circuit 1 Switching Time

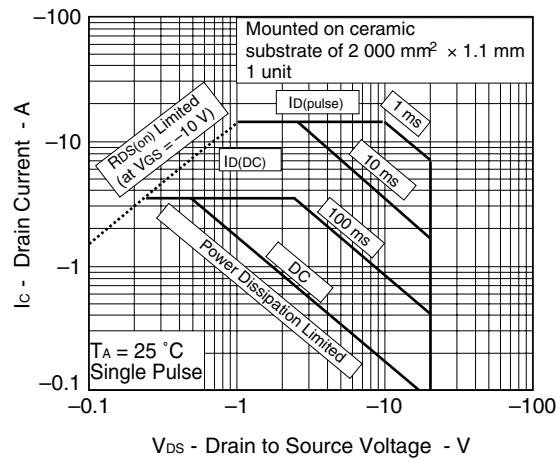
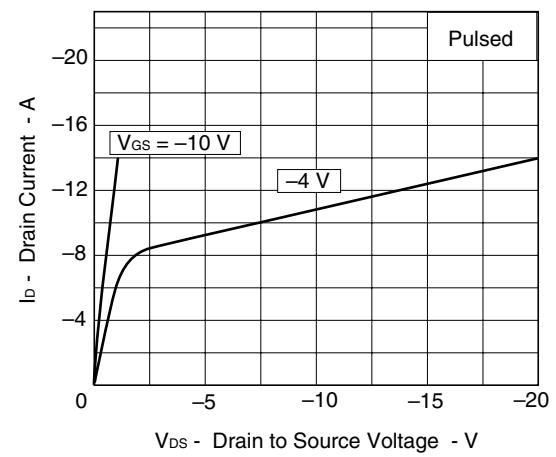


Test Circuit 2 Gate Charge

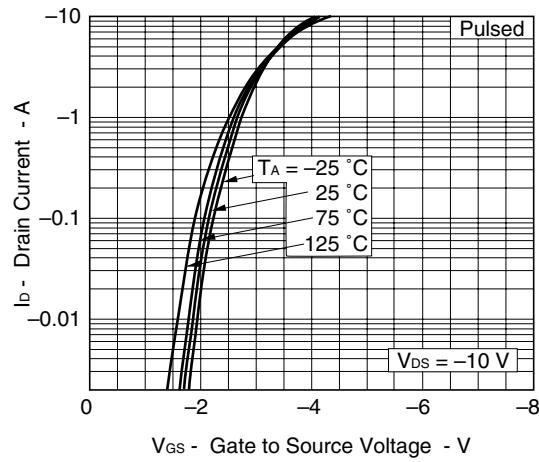


DERATING FACTOR OF FORWARD BIAS  
SAFE OPERATING AREATOTAL POWER DISSIPATION vs.  
AMBIENT TEMPERATURE

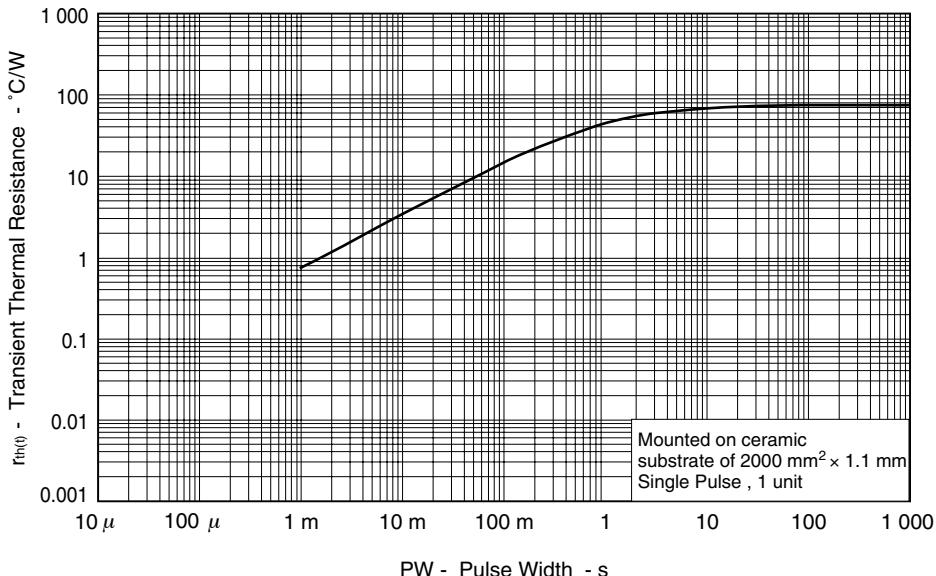
FORWARD BIAS SAFE OPERATING AREA

DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE

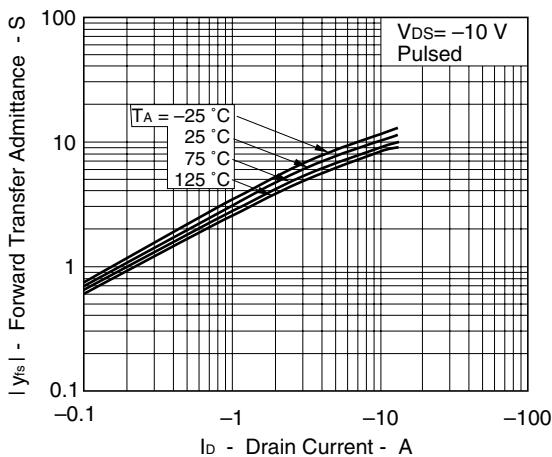
FORWARD TRANSFER CHARACTERISTICS



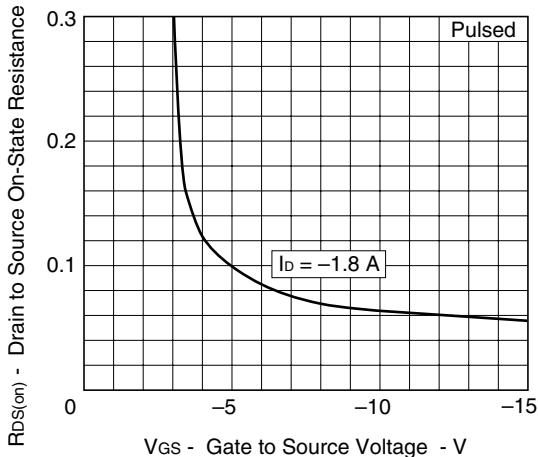
## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



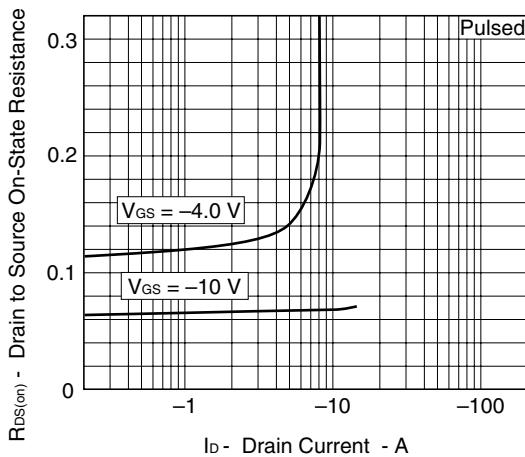
## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



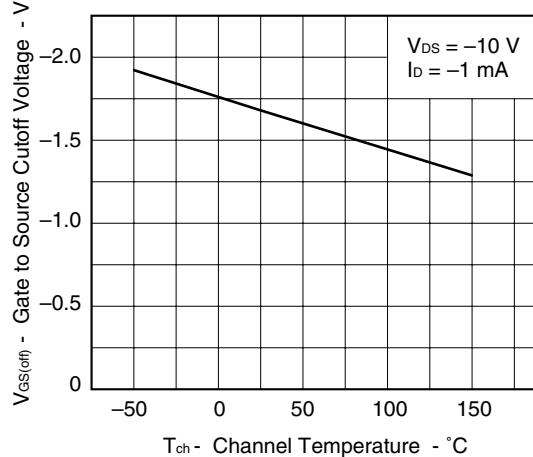
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

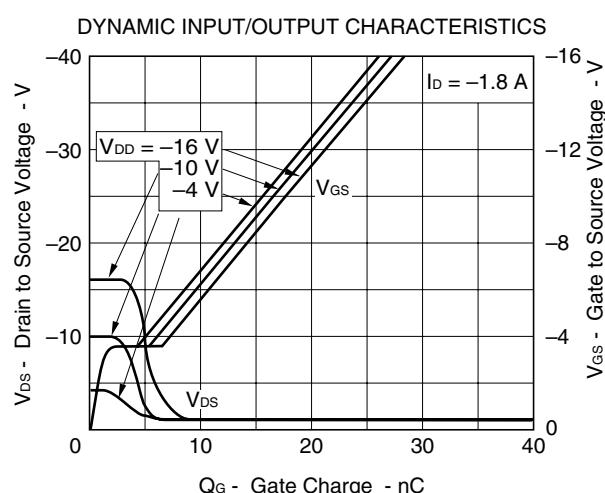
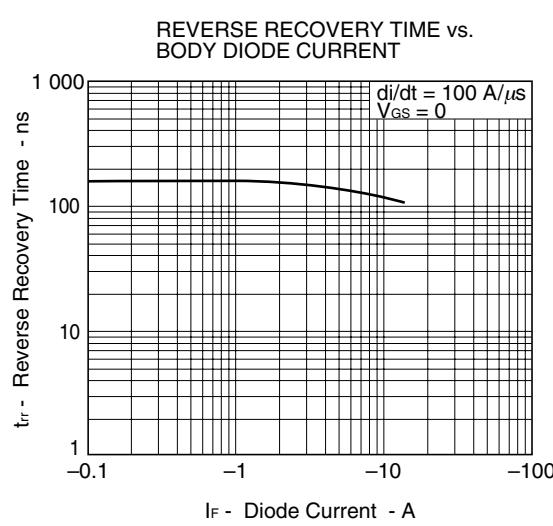
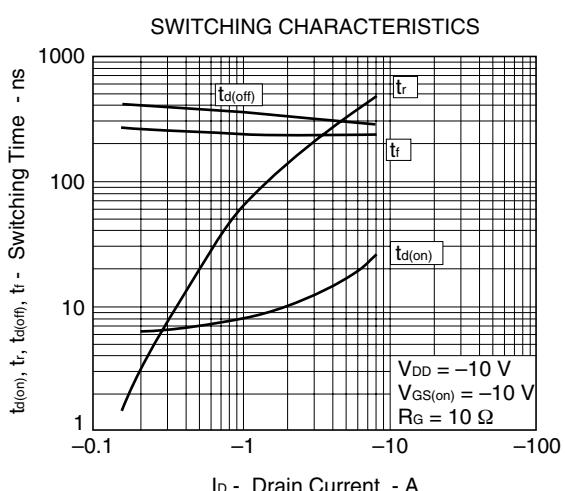
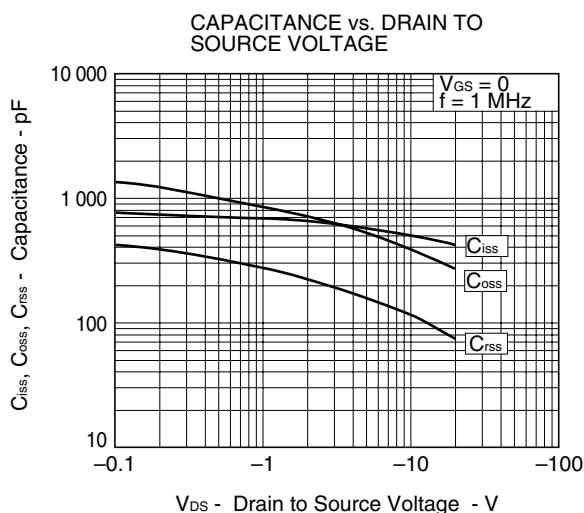
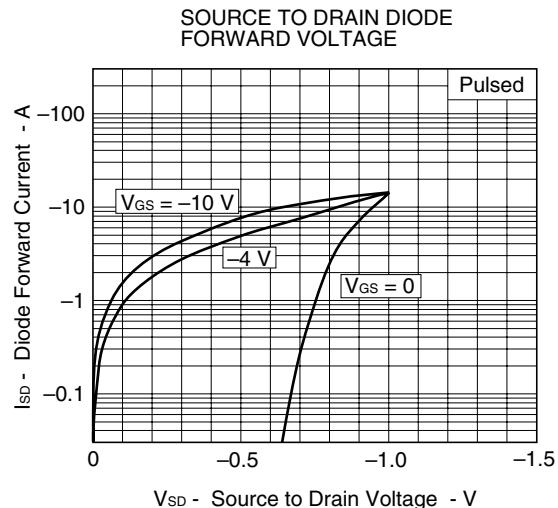
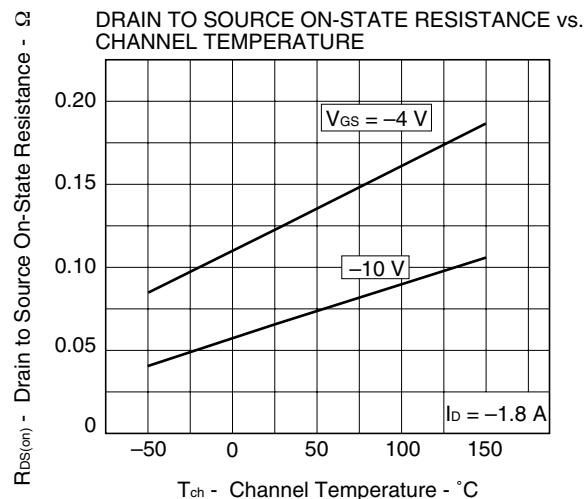


## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



## GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.