DATA SHEET

NEC

MOS FIELD EFFECT POWER TRANSISTORS

μPA1750

SWITCHING
DUAL P-CHANNEL POWER MOS FET
INDUSTRIAL USE

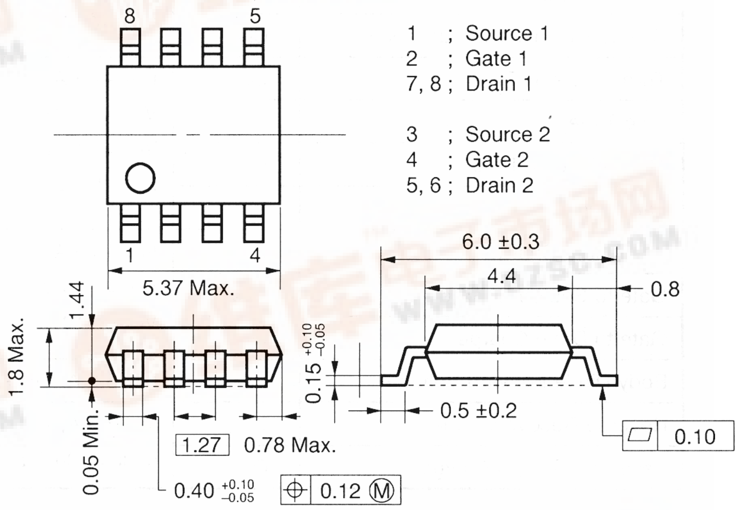
DESCRIPTION

This product is Dual P-Channel MOS Field Effect Transistor designed for power management switch applications of notebook computers and cellur phones.

FEATURES

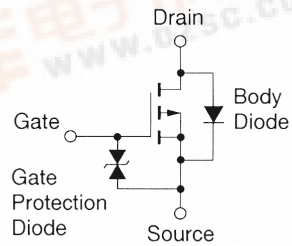
- Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance
  $R_{DS(on)1}$ = 0.09 Ω Max. (V_{GS} = –10 V, I_D = –1.8 A)
  $R_{DS(on)2}$ = 0.18 Ω Max. (V_{GS} = –4 V, I_D = –1.8 A)
- Low C_{iss} C_{iss} = 540 pF Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS
(in millimeter)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, all terminals are connected.)

Drain to Source Voltage	V_{DSS}	–20	V
Gate to Source Voltage	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓3.5	A
Drain Current (pulse)*	$I_{D(pulse)}$	∓14	A
Total Power Dissipation (1 unit)**	P_T	1.7	W
Total Power Dissipation (2 unit)**	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C



* PW ≤ 10 μs, Duty Cycle ≤ 1 %

** T_A = 25 °C, Mounted on ceramic substrate of 2 000 mm^2 × 1.1 mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

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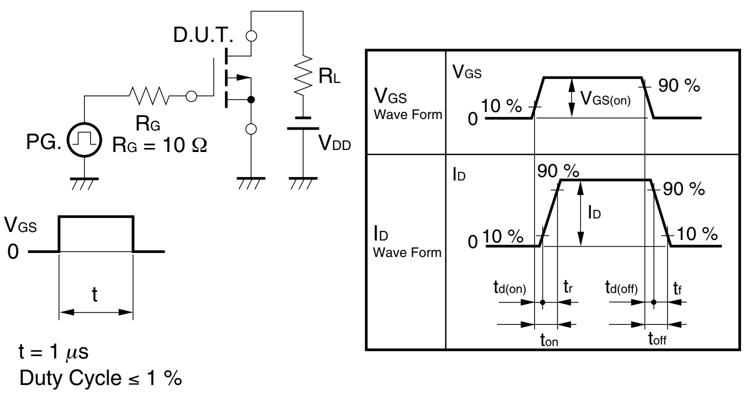
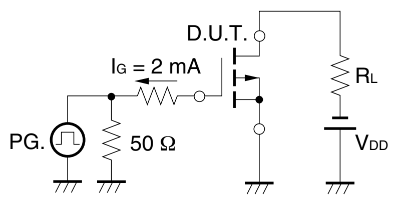
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, all terminals are connected.)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –1.8 A		0.065	0.090	Ω
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –1.8 A		0.125	0.180	Ω
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.7	–2.5	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = –10 V, I_D = –1.8 A	2.0	4.4		S
Drain Leakage Current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0			–10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0			∓10	μA
Input Capacitance	C_{iss}	V_{DS} = –10 V V_{GS} = 0 f = 1 MHz		540		pF
Output Capacitance	C_{oss}			385		pF
Reverse Transfer Capacitance	C_{rss}			105		pF
Turn-On Delay Time	$t_{d(on)}$	I_D = –1.8 A $V_{GS(on)}$ = –10 V V_{DD} = –10 V R_G = 10 Ω		10		ns
Rise Time	t_r			110		ns
Turn-off Delay Time	$t_{d(off)}$			340		ns
Fall Time	t_f			230		ns
Total Gate Charge	Q_G	I_D = –3.5 A V_{DD} = –16 V V_{GS} = –10 V		18		nC
Gate to Source Charge	Q_{GS}			2.0		nC
Gate to Drain Charge	Q_{GD}			5.1		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.5 A, V_{GS} = 0		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 3.5 A, V_{GS} = 0 di/dt = 100 A/μs		160		ns
Reverse Recovery Charge	Q_{rr}			310		nC

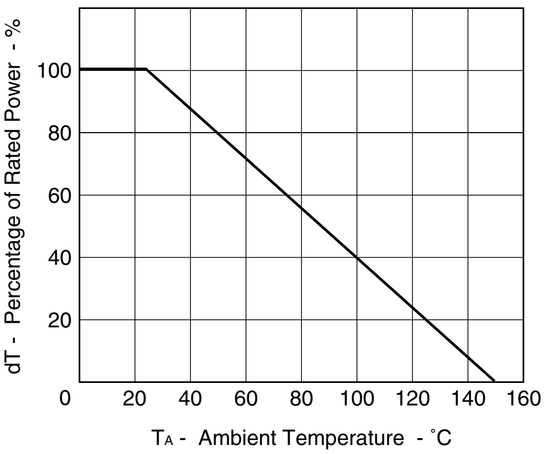
Test Circuit 1 Switching Time



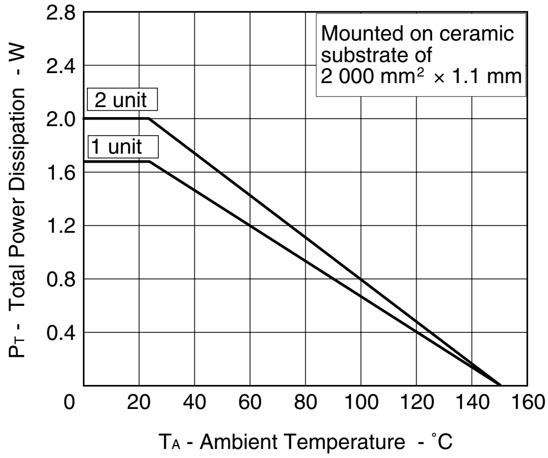
Test Circuit 2 Gate Charge



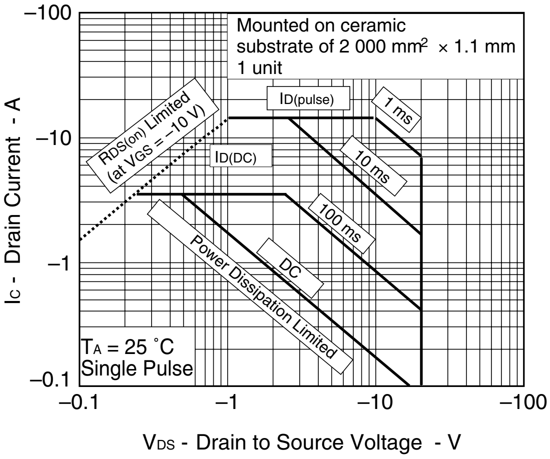
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



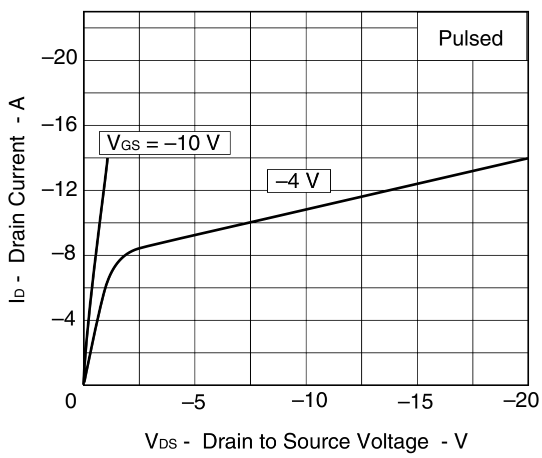
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



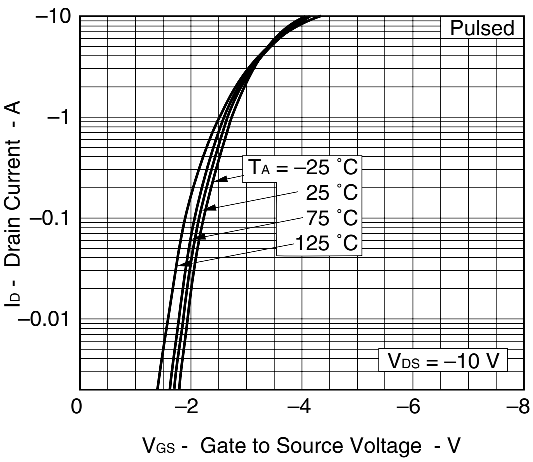
FORWARD BIAS SAFE OPERATING AREA



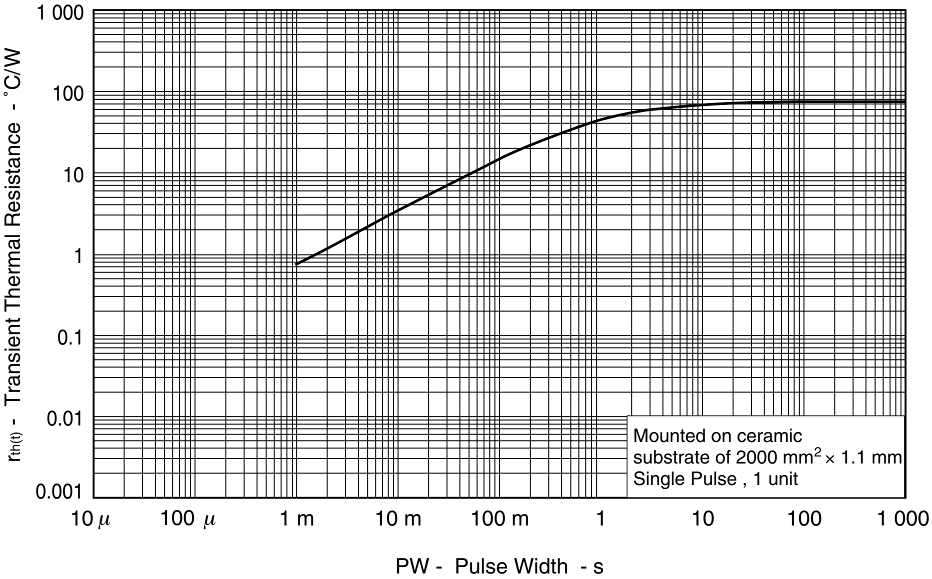
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



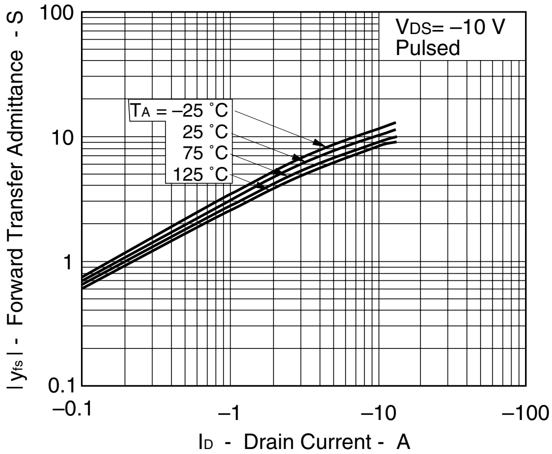
FORWARD TRANSFER CHARACTERISTICS



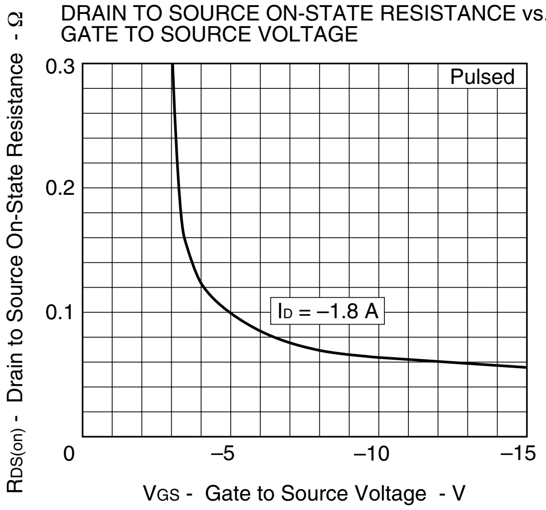
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



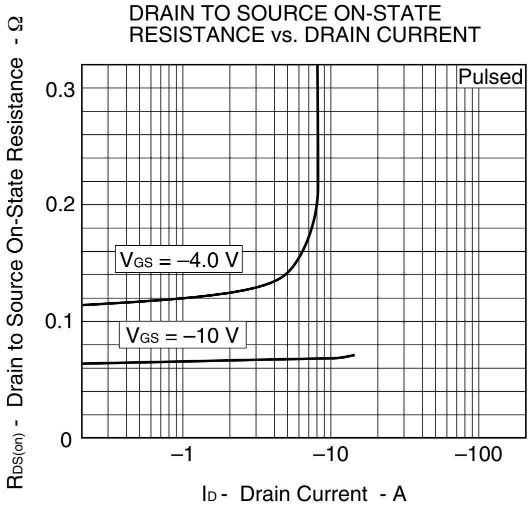
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



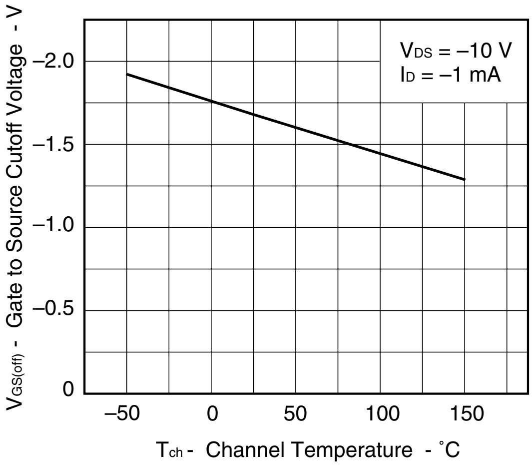
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



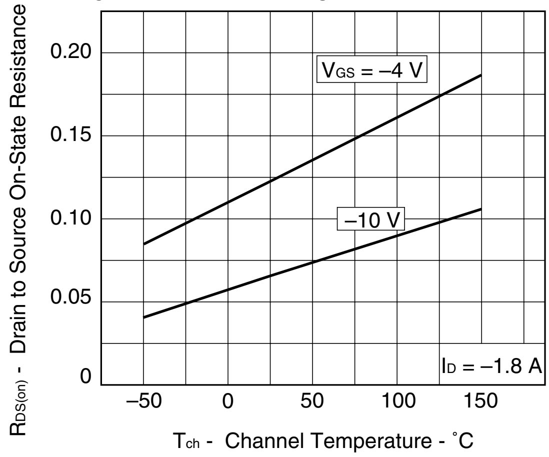
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



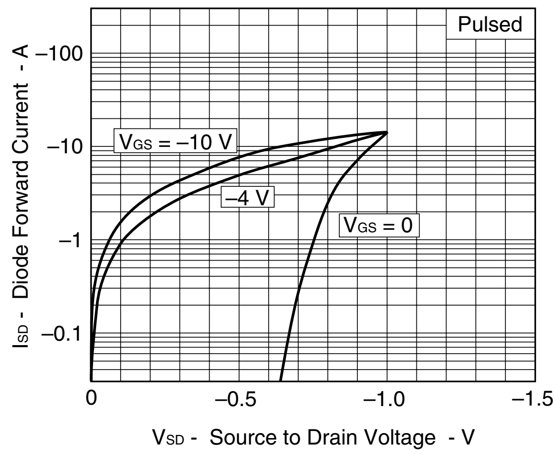
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



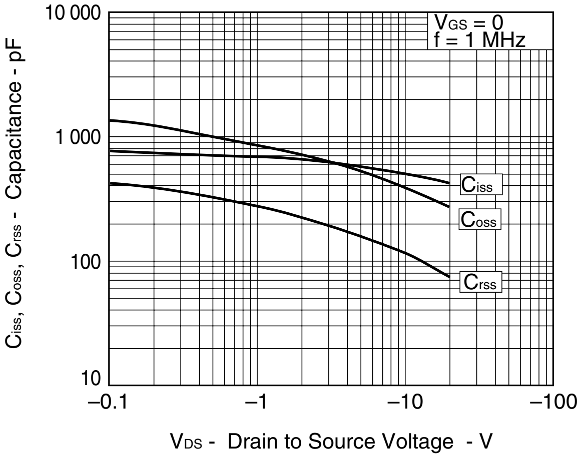
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



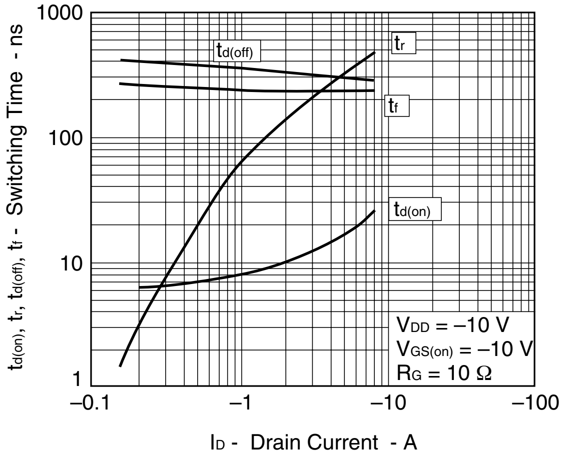
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



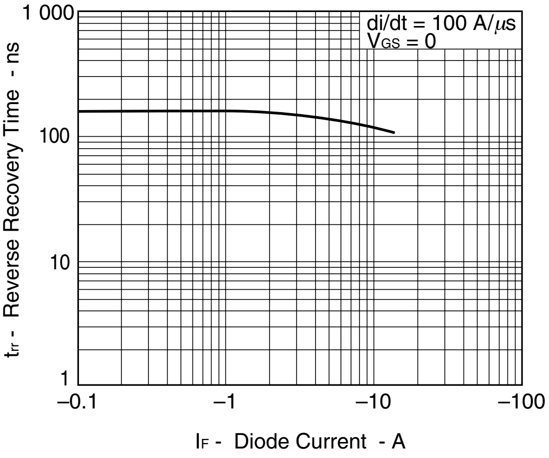
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



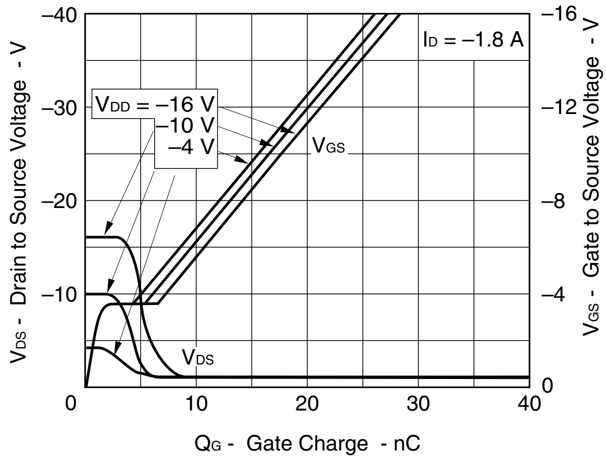
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. BODY DIODE CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E
Power MOS FET features and application switching power supply	TEA-1034
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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