NEC Electronics Inc.

μPB8284A
CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

Description

The μPB8284 is a clock generator and driver for the 8086 and 8088 microprocessors. This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

Features

- ☐ Generates system clock for the 8086 and 8088
- ☐ Frequency source can be a crystal or a TTL signal
- ☐ MOS level output for the processor
- ☐ TTL level output for the peripheral devices
- ☐ Power-up reset for the processor
- ☐ READY synchronization
- ☐ +5 V supply

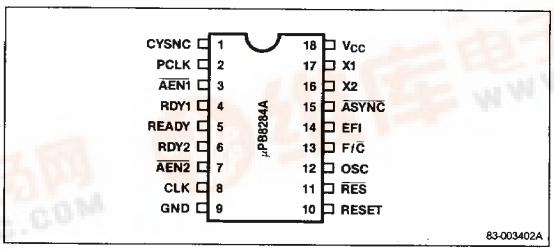
Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPB8284AD	18-Pin cerdip	25 MHz ÷ 3

Pin Identification

No.	Symbol	Function
1	CSYNC	Clock synchronization
2	PCLK	Peripheral clock
3, 7	$\overline{AEN1}$, $\overline{AEN2}$	Address enable
4, 6	RDY1, RDY2	Bus ready
5	READY	Ready
8	CLK	Processor clock
9	GND	Ground
10	RESET	Reset
11	$\overline{RES}$	Reset in
12	OSC	Oscillator output
13	F/C	Frequency crystal select
14	EFI	External frequency in
15	$\overline{ASYNC}$	Asynchronous input
16, 17	X1, X2	Crystal in
18	V_{CC}	V_{CC}

Pin Configuration



Pin Functions

Clock Synchronization

An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count, and when high, the counters are reset. CYSNC should be grounded when the internal oscillator is used.

Peripheral Clock

A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.

Address Enable

This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.

Bus Ready

This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.

Ready

The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.

Processor Clock

This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.

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Ground

Ground.

Reset

This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.

Reset In

The Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.

Oscillator Output

This TTL level clock is the output of the oscillator circuit running at the crystal frequency.

Frequency Crystal Select

F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A high is for the EFI input, and a low is for the crystal.

External Frequency In

A square wave in at three times the CLK output. A TTL level clock to generate CLK.

Asynchronous Input

Ready Synchronization Select. $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.

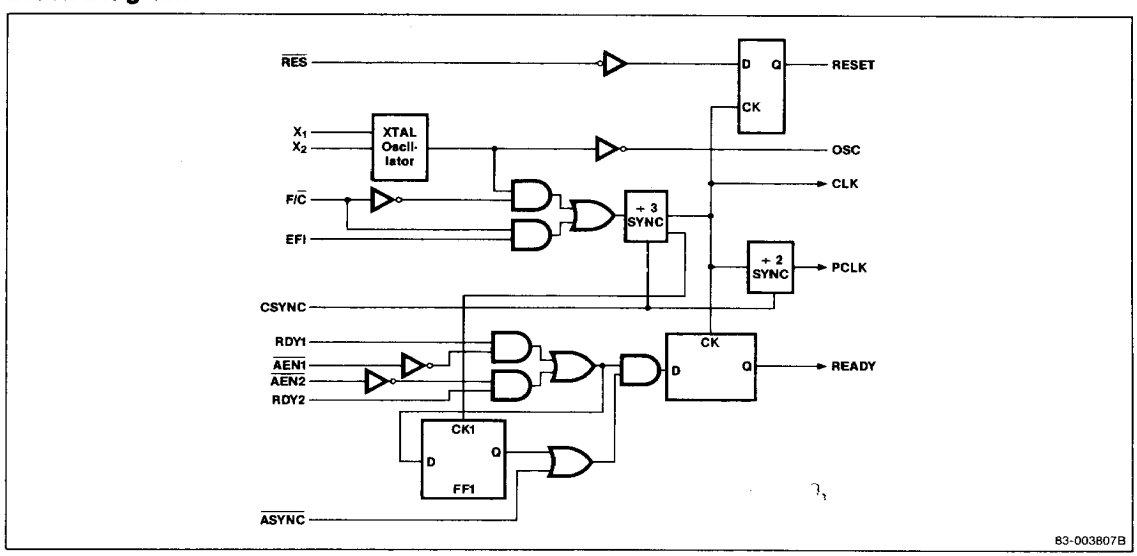
Crystal In

A crystal is connected to these inputs to generate the processor clock. The crystal frequency is three times the desired CLK output.

V_{CC} Supply Voltage

+5 V supply.

Block Diagram



Functional Description

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide-by-three counter which receives its input from either the crystal or TTL source (EFI pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one-half of the processor clock speed.

Reset timing is provided by a Schmitt trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.5 V to +7 V
Input voltage, V_I	−1.0 V to +5.5 V
Output supply voltage, V_O	−0.5 V to +7 V
Operating temperature, T_{OPT}	−0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5 V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}			+0.8	V	$V_{CC} = 5.0 V$
Input voltage high	V_{IH}	2			V	$V_{CC} = 5.0 V$
Output voltage low	V_{OL}			+0.45	V	$5 mA = I_{OL}$
Output voltage high (CLK)	V_{OH}	4			V	$-1 mA = I_{OH}$
(Other outputs)		2.4			V	$-1 mA = I_{OH}$
Forward input current ($\overline{ASYNC}$)	I_F			−1.3	mA	$V_F = 0.45 V$
(Other inputs)				−0.5	mA	$V_F = 0.45 V$
Reverse input current	I_R			50	μA	$V_R = 5.25 V$
Input forward clamp voltage	V_C			−1.0	V	$I_C = -5 mA$
Reset input high voltage	V_{IHR}	2.6			V	$V_{CC} = 5.0 V$
$\overline{RES}$ input hysteresis	$V_{IHR} - V_{ILR}$	0.25			V	$V_{CC} = 5.0 V$
Power supply current	I_{CC}			140	mA	

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284A synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5 V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Timing Requirements						
External frequency time high	t_{EHEL}	13			ns	90%–90% V_{IN}
External frequency time low	t_{ELEH}	13			ns	10%–10% V_{IN}
EFI period	t_{ELEL}	(5)			ns	(Note 1)
XTAL frequency		12		25	MHz	
RDY1, RDY2 set-up to CLK	t_{R1VCL}	35			ns	
RDY1, RDY2 hold to CLK	t_{CLR1X}	0			ns	
$\overline{AEN1}$, $\overline{AEN2}$ set-up to RDY1, RDY2	t_{A1VR1V}	15			ns	
$\overline{AEN1}$, $\overline{AEN2}$ hold to CLK	t_{CLA1X}	0			ns	
CSYNC set-up to EFI	t_{YHEH}	20			ns	
CSYNC hold to EFI	t_{EHYL}	10			ns	
CSYNC width	t_{YHYL}	$2t_{ELEL}$			ns	
$\overline{RES}$ set-up to CLK	t_{I1HCL}	65			ns	(Note 2)
$\overline{RES}$ hold to CLK	t_{CLI1H}	20			ns	(Note 2)
RDY1, RDY2 active set-up to CLK	t_{R1VCH}	35			ns	$\overline{ASYNC}$ = Low
RDY1, RDY2 inactive set-up to CLK	t_{R1VCL}	35			ns	
$\overline{ASYNC}$ set-up to CLK	t_{AYVCL}	50			ns	
$\overline{ASYNC}$ hold to CLK	t_{CLAYX}	0			ns	
Input rise time	t_{ILIH}			20	ns	From 0.8 V to 2.0 V
Input fall time	t_{ILIL}			12	ns	From 2.0 V to 0.8 V

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AC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Timing Responses						
CLK cycle period	t_{CLCL}	125			ns	
CLK time high	t_{CHCL}	(6)			ns	Figure 1 and figure 2
CLK time low	t_{CLCH}	(7)			ns	Figure 1 and figure 2
CLK rise and fall time	t_{CH1CH2}, t_{CL2CL1}			10	ns	1.0 V to 3.5 V
PCLK time high	t_{PHPL}	(8)			ns	
PCLK time low	t_{PLPH}	(8)			ns	
Ready inactive to CLK	t_{RYLCL}	−8			ns	Figure 3 and figure 4, (Note 4)
Ready active to CLK	t_{RYHCH}	(7)			ns	Figure 3 and figure 4, (Note 3)
CLK to reset delay	t_{CLIL}			40	ns	
CLK to PCLK high delay	t_{CLPH}			22	ns	
CLK to PCLK low delay	t_{CLPL}			22	ns	
OSC to CLK high delay	t_{OLCH}	−5		12	ns	
OSC to CLK low delay	t_{OLCL}	2		22	ns	
Output rise time (except CLK)	t_{OLOH}			20	ns	From 0.8 V to 2.0 V
Output fall time (except CLK)	t_{OHOL}			12	ns	From 2.0 V to 0.8 V

Note:

(1) δ = EFI rise (5 ns max) + EFI fall (5 ns max).

(2) Set-up and hold only necessary to guarantee recognition at next clock.

(3) Applies only to T3 and TW states.

(4) Applies only to T2 states.

(5) $t_{EHEL} + t_{ELEH} + \delta$

(6) $(1/3\ t_{CLCL}) + 2.0$

(7) $(2/3\ t_{CLCL}) - 15.0$

(8) $t_{CLCL} - 20$

AC Test Circuits

Figure 1. Clock High and Low Time

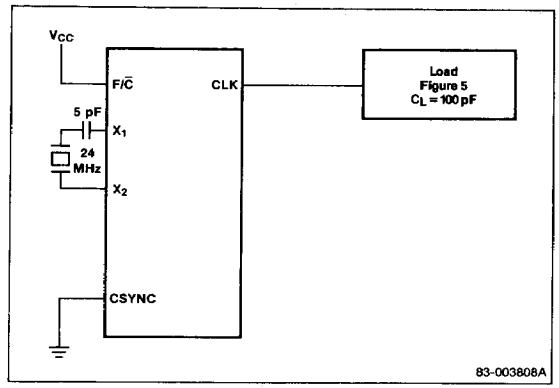


Figure 2. Clock High and Low Time

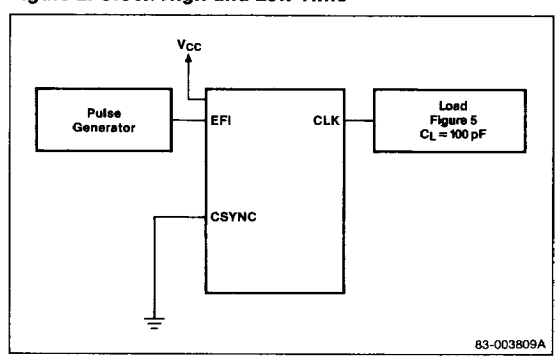


Figure 3. Ready to CLK

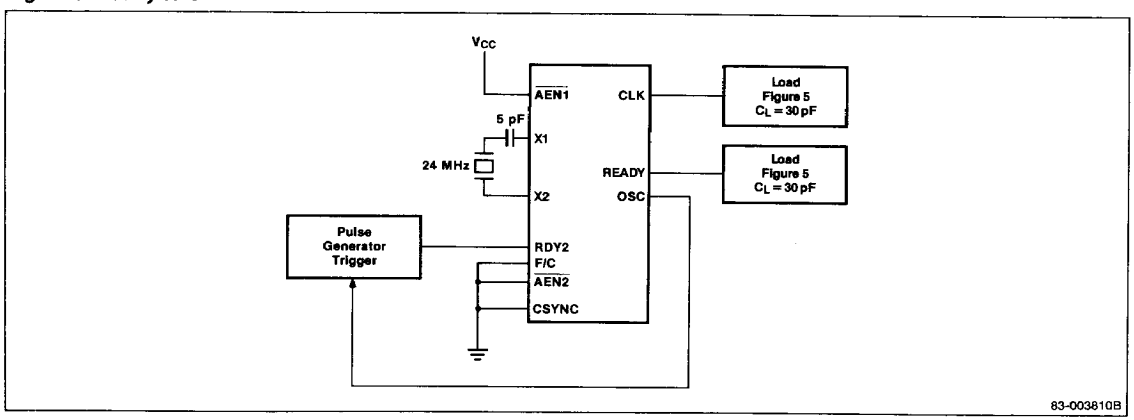


Figure 4. Ready to CLK Output

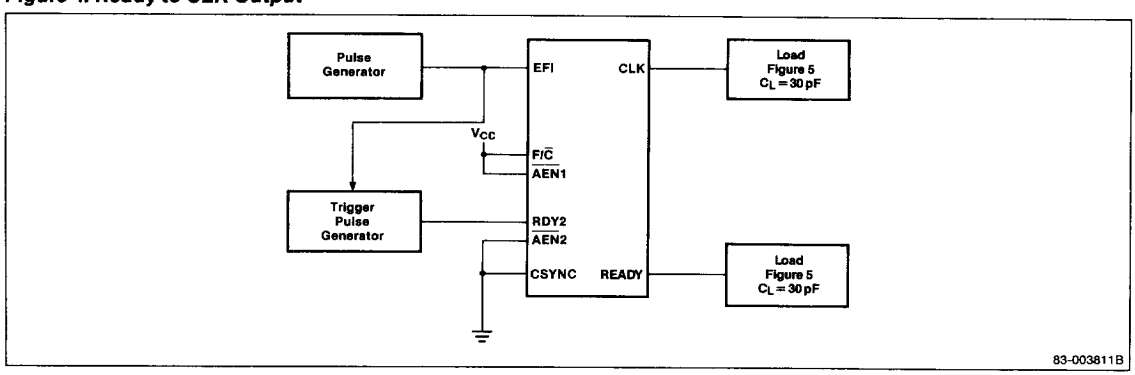


Figure 5. AC Load

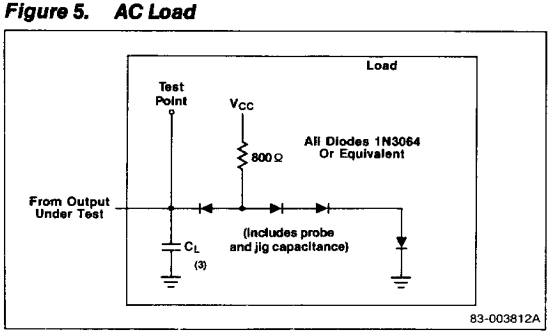
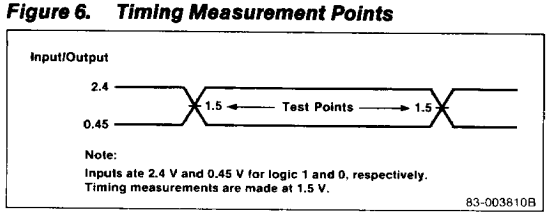


Figure 6. Timing Measurement Points



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Timing Waveform