DATA SHEET

NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC4091

J-FET INPUT LOW-OFFSET OPERATIONAL AMPLIFIER

The μPC4091 operational amplifier offers high input impedance, low offset voltage, high slew rate, and stable AC operating characteristics. NEC's unique high-speed PNP transistor (f_T = 300 MHz) in the output stage solves the oscillation problem of current sinking with a large capacitive load. Zener-zap resistor trimming in the input stage produces excellent offset voltage and temperature drift characteristics.

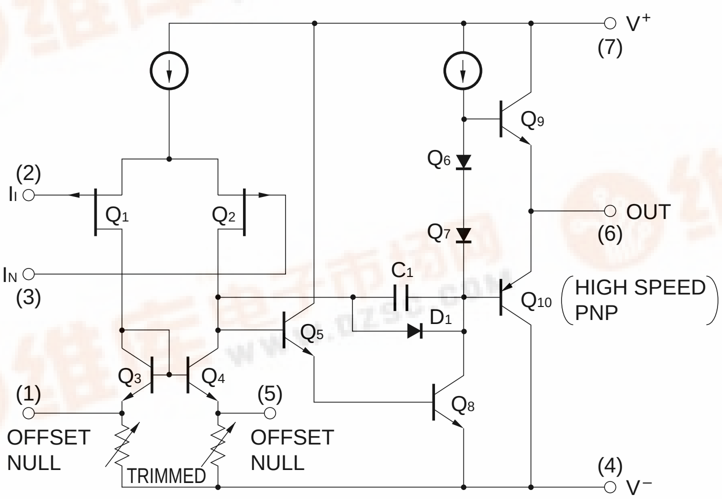
FEATURES

- Stable operation with 10000 pF capacitive load
- Low input offset voltage and offset voltage null capability
  - ±2.5 mV (MAX.)
  - ±7 μV/°C (TYP.) temperature drift
- Very low input bias and offset currents
- Low noise : e_n = 19 nV/ $\sqrt{Hz}$ (TYP.)
- Output short circuit protection
- High input impedance ... J-FET Input Stage
- Internal frequency compensation
- High slew rate: 15 V/μs (TYP.)

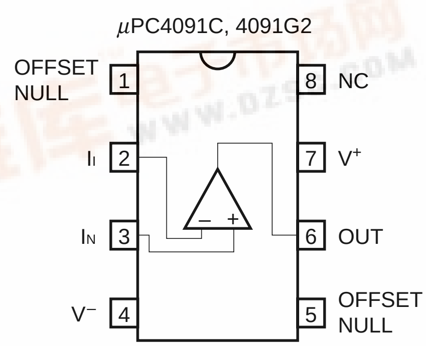
ORDERING INFORMATION

Part Number	Package
μPC4091C	8-pin plastic DIP (300 mil)
μPC4091G2	8-pin plastic SOP (225 mil)

EQUIVALENT CIRCUIT



PIN CONFIGURATION (Top View)



Remark NC : No Connection

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter		Symbol	Ratings	Unit
Voltage between V^+ and V^- Note 1		$V^+ - V^-$	–0.3 to +36	V
Differential Input Voltage		V_{ID}	±30	V
Input Voltage Note 2		V_I	V^-–0.3 to V^+ +0.3	V
Output Voltage Note 3		V_O	V^-–0.3 to V^+ +0.3	V
Power Dissipation	C Package Note 4	P_T	350	mW
	G2 Package Note 5		440	mW
Output Short Circuit Duration Note 6			Indefinite	sec
Operating Ambient Temperature		T_A	–20 to +80	°C
Storage Temperature		T_{stg}	–55 to +125	°C

Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

4. Thermal derating factor is –5.0 mV/°C when operating ambient temperature is higher than 55 °C.

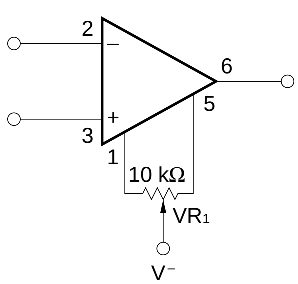
5. Thermal derating factor is –4.4 mV/°C when operating ambient temperature is higher than 25 °C.

6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	$V^{\pm}$	±5		±16	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1, R_f = 0 Ω)	C_L			10000	pF

OFFSET VOLTAGE NULL CIRCUIT



Remark The OFFSET NULL pins should be left open or connected to V^- via a resistor as shown in the left figure. Don't connect to any lines other than V^-, otherwise mulfunction, degradation, or failure may occur.

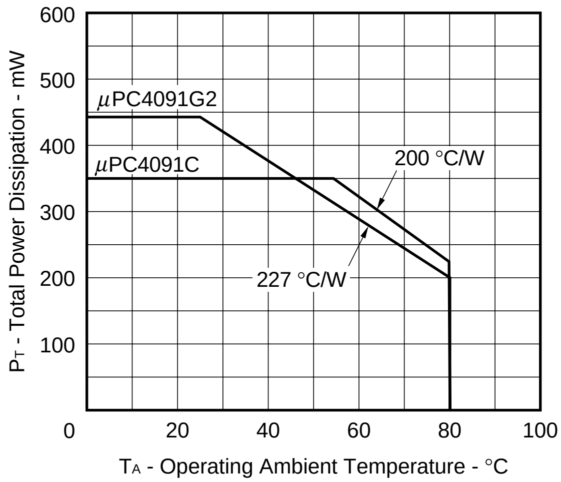
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		±1	±2.5	mV
Input Offset Current[Note 7]	I_{IO}			±25	±100	pA
Input Bias Current[Note 7]	I_B			50	200	pA
Large Signal Voltage Gain	A_V	$R_L \geq 2$ kΩ , V_O = ±10 V	25000	200000		
Supply Current	I_{CC}	I_O = 0 A		2.5	3.4	mA
Common Mode Rejection Ratio	CMR		70	100		dB
Supply Voltage Rejection Ratio	SVR		70	100		dB
Output Voltage Swing	V_{om}	$R_L \geq 10$ kΩ	±12	+14.0 –13.3		V
		$R_L \geq 2$ kΩ	±10	+13.5 –12.8		V
Common Model Input Voltage Range	V_{ICM}		±11	+14 –12		V
Slew Rate	SR	A_V = 1		15		V/μs
Unity Gain Frequency	f_{unity}			4		MHz
Input Equivalent Noise Voltage Density	e_n	R_S = 100 Ω, f = 1 kHz		19		nV/$\sqrt{Hz}$
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$, T_A = –20 to +70 °C			±5	mV
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$	T_A = –20 to +70 °C		±7		μV/°C
Input Offset Current[Note 7]	I_{IO}	T_A = –20 to +70 °C			±2	nA
Input Bias Current[Note 7]	I_B	T_A = –20 to +70 °C			7	nA

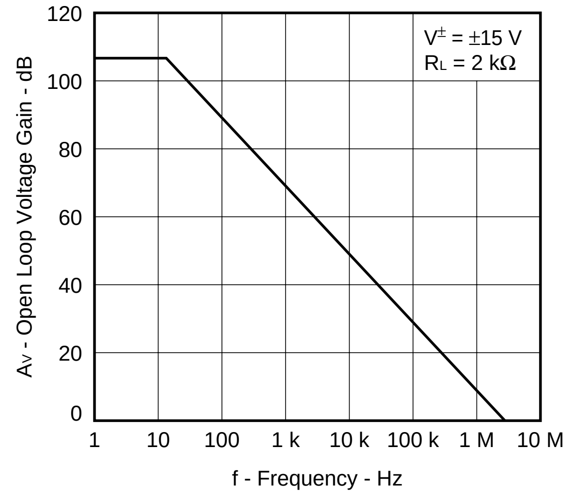
Notes 7. Input bias currents flow into IC. Because each currents are gate leak current of P-channel J-FET on input stage. And that are temperature sensitive. Short time measuring method is recommendable to maintain the junction temperature close to the operating ambient temperature.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25 °C, TYP.)

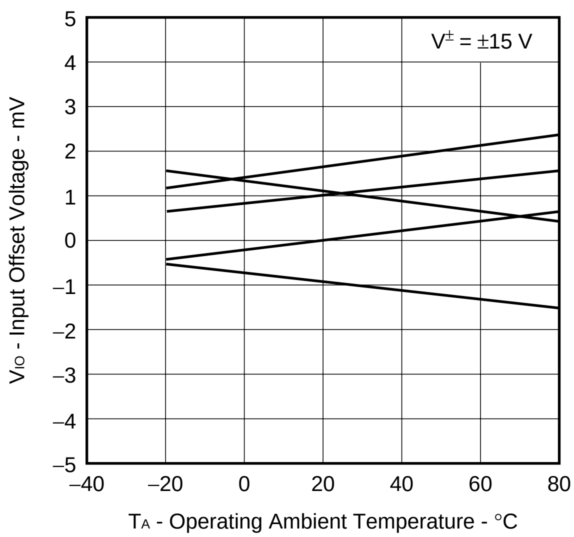
POWER DISSIPATION



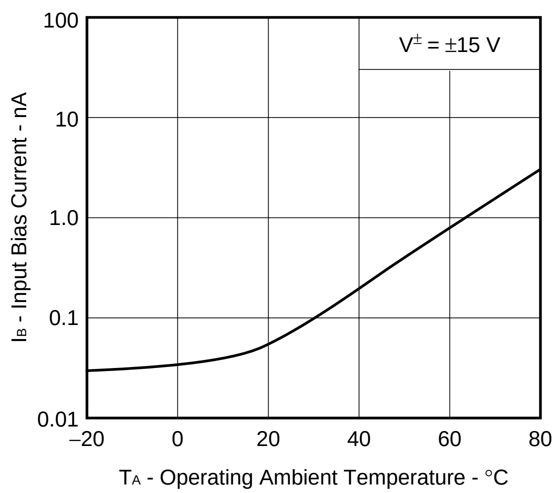
OPEN LOOP FREQUENCY RESPONSE



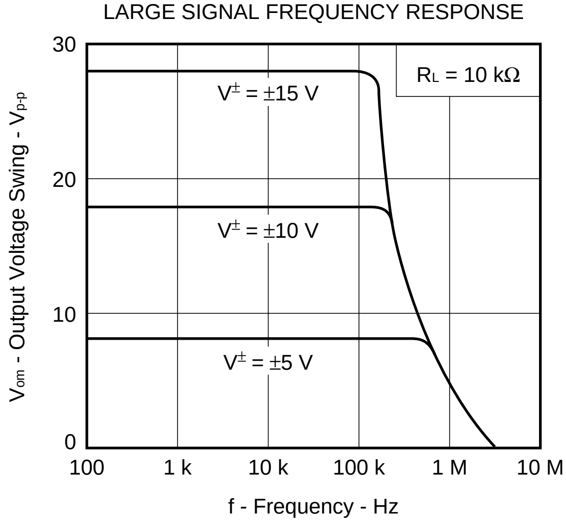
INPUT OFFSET VOLTAGE



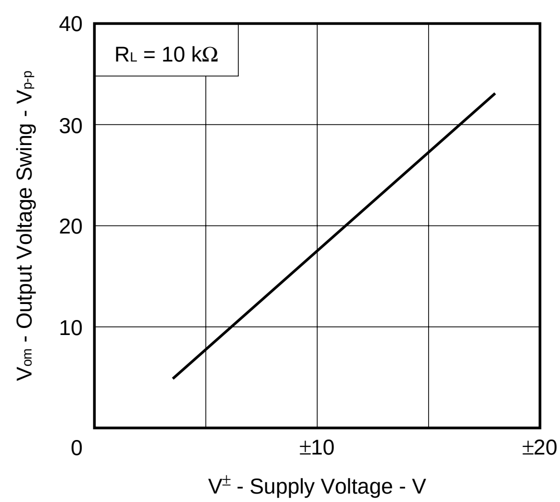
INPUT BIAS CURRENT



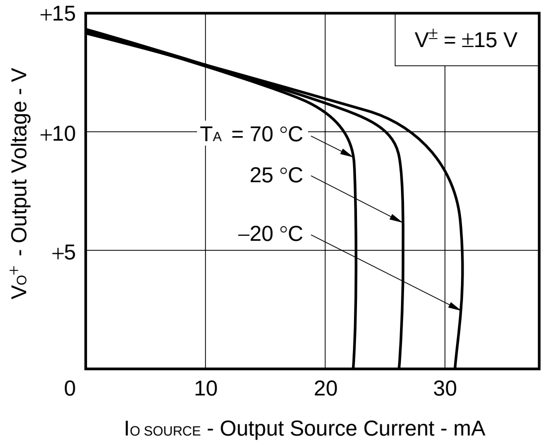
LARGE SIGNAL FREQUENCY RESPONSE



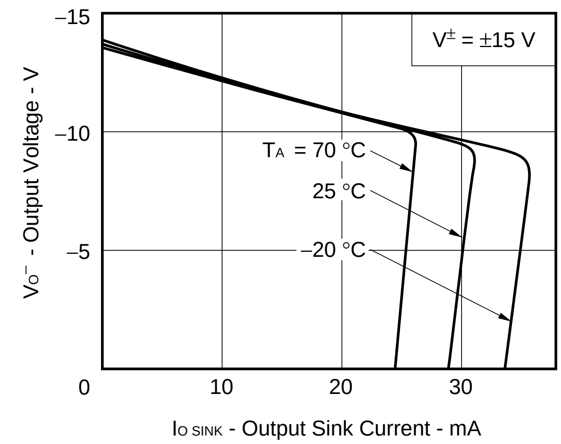
OUTPUT VOLTAGE SWING



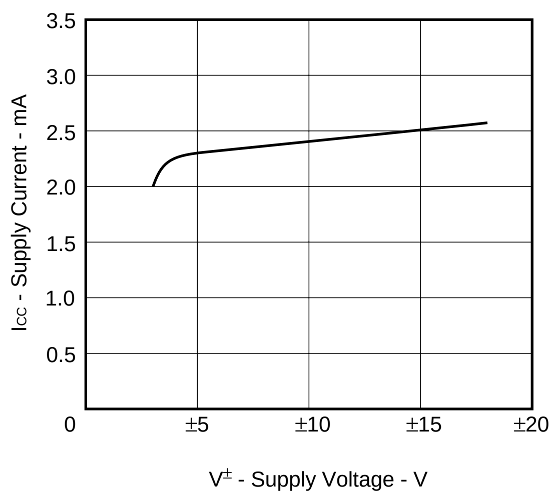
OUTPUT SOURCE CURRENT LIMIT



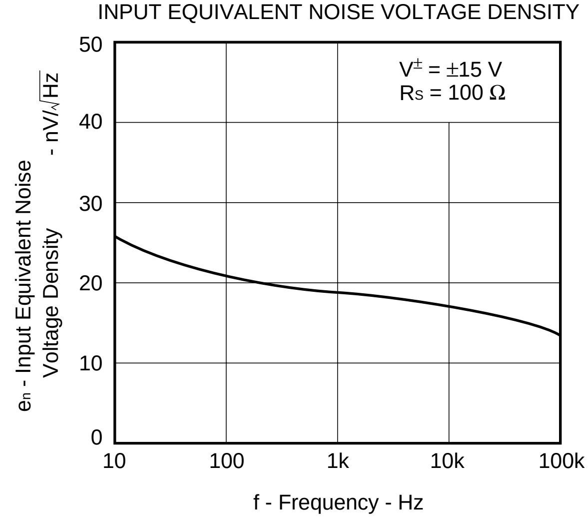
OUTPUT SINK CURRENT LIMIT



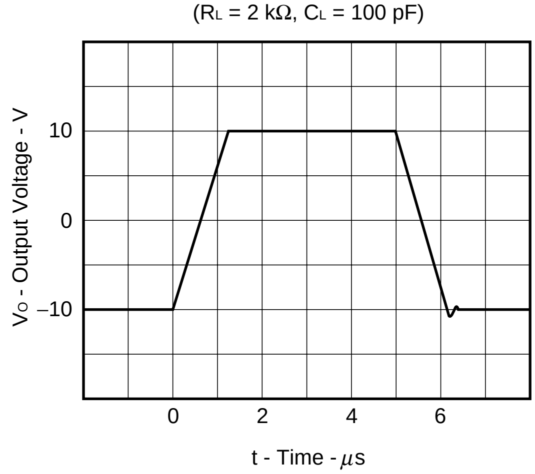
SUPPLY CURRENT



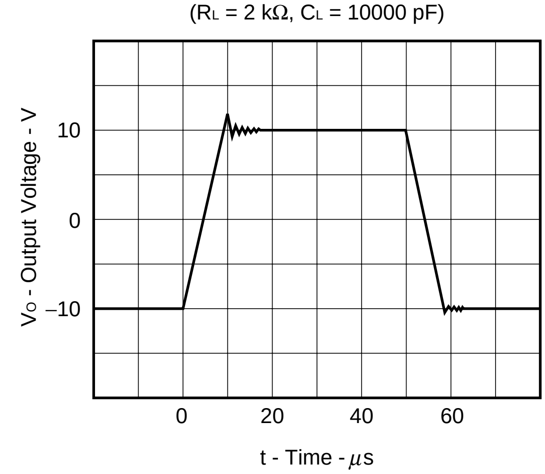
INPUT EQUIVALENT NOISE VOLTAGE DENSITY



VOLTAGE FOLLOWER PULSE RESPONSE 1
($V^{\pm}$ = ±15 V, A_V = +1)
(R_L = 2 kΩ, C_L = 100 pF)

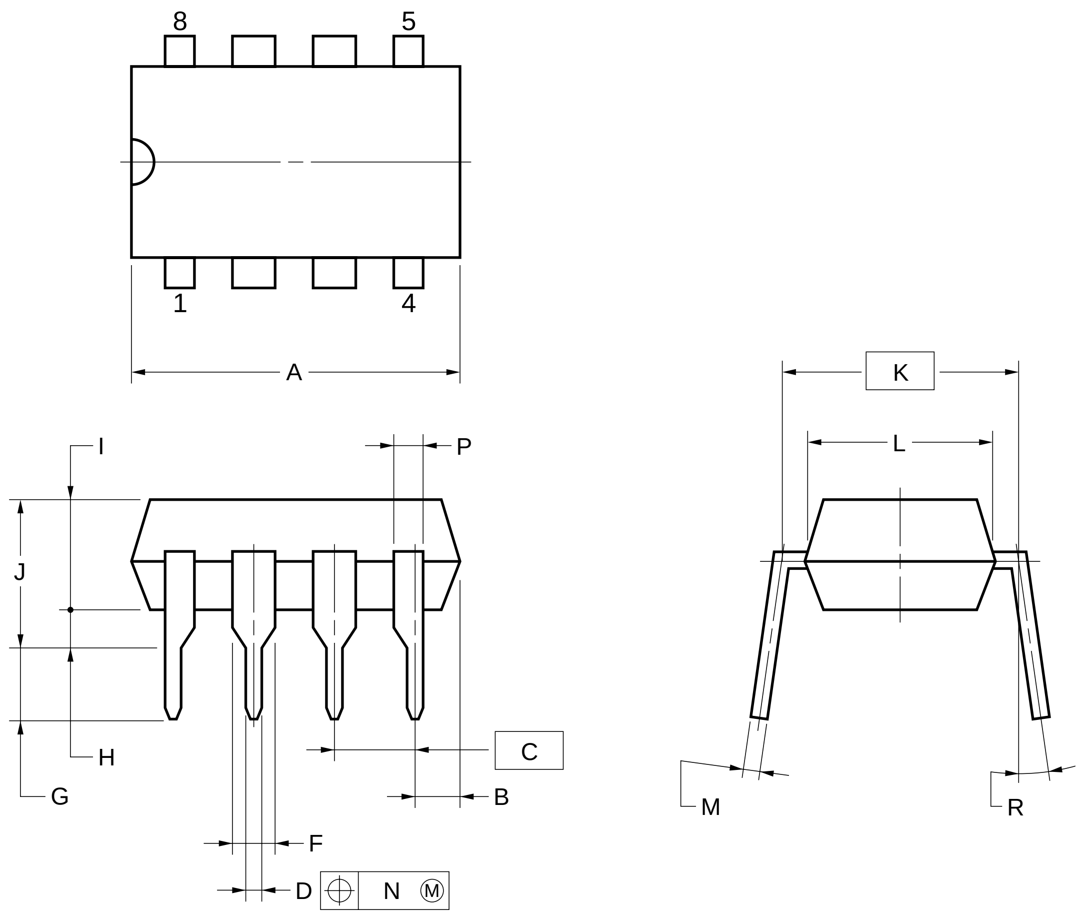


VOLTAGE FOLLOWER PULSE RESPONSE 2
($V^{\pm}$ = ±15 V, A_V = +1)
(R_L = 2 kΩ, C_L = 10000 pF)



PACKAGE DRAWINGS

8PIN PLASTIC DIP (300 mil)



NOTES

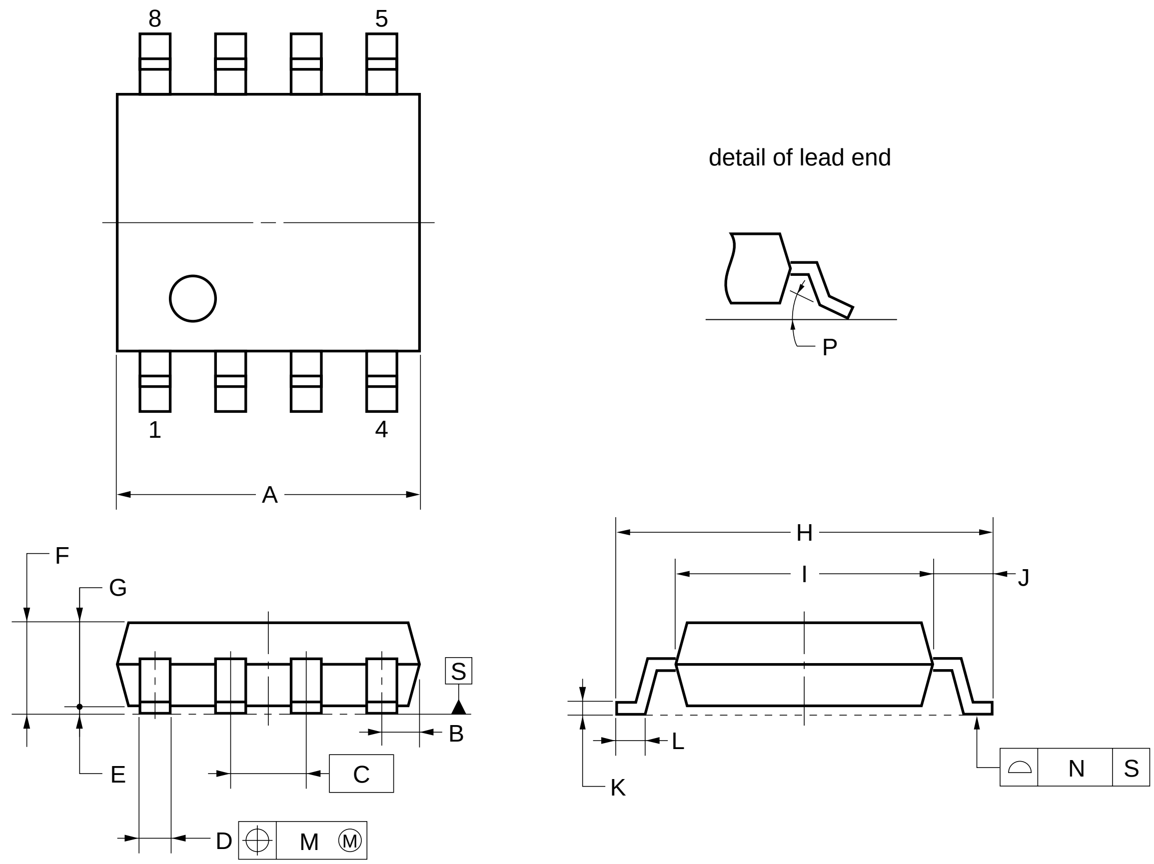
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	10.16 MAX.	0.400 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	1.4 MIN.	0.055 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.9 MIN.	0.035 MIN.
R	0~15°	0~15°

P8C-100-300B,C-1

8 PIN PLASTIC SOP (225 mil)



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$5.2^{+0.17}_{-0.20}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3°^{+7°}_{-3°}$

S8GM-50-225B-5

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document "**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL"(C10535E)**.

Type of Surface Mount Device

μPC4091G2: 8-pin plastic SOP (225 mil)

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Type of Through-hole Device

μPC4091C: 8-pin plastic DIP (300 mil)

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

REFERENCE DOCUMENTS

QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL	C10535E
NEC IC PACKAGE MANUAL (CD-ROM)	C13388E
GUIDE TO QUALITY ASSURANCE FOR SEMICONDUCTOR DEVICES	MEI-1202
SEMICONDUCTORS SELECTION GUIDE	X10679E
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM (STANDARD LINEAR IC)	IEI-1212

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The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.