NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC8104GR

UP CONVERTER + QUADRATURE MODULATOR IC FOR DIGITAL MOBILE COMMUNICATION SYSTEMS

DESCRIPTION

The μPC8104GR is a silicon monolithic integrated circuit designed as quadrature modulator for digital mobile communication systems. This modulator consists of 1.9 GHz up-converter and 400 MHz quadrature modulator which are packaged in 20 pin SSOP. The device has power save function and can operate 2.7 to 5.5 V supply voltage, therefore, it can contribute to make RF block small, high performance and low power consumption.

FEATURES

- 20 pin SSOP suitable for high density surface mounting.
- High linearity up converter is incorporated; $P_{RFout(sat)}$ = –6 dBm TYP.
- Low phase difference due to digital phase shifter is adopted.
- Wide operating frequency range. Up converter; f_{RFout} = 800 MHz to 1.9 GHz
  Modulator ; f_{MODout} = 100 MHz to 400 MHz, $f_{I/Q}$ = DC to 10 MHz
- External IF filter can be applied between modulator output and up converter input terminal.
- Supply voltage: V_{CC} = 2.7 to 5.5 V
- Equipped with power save function.

APPLICATION

- Digital cordless phones
- Digital cellular phones

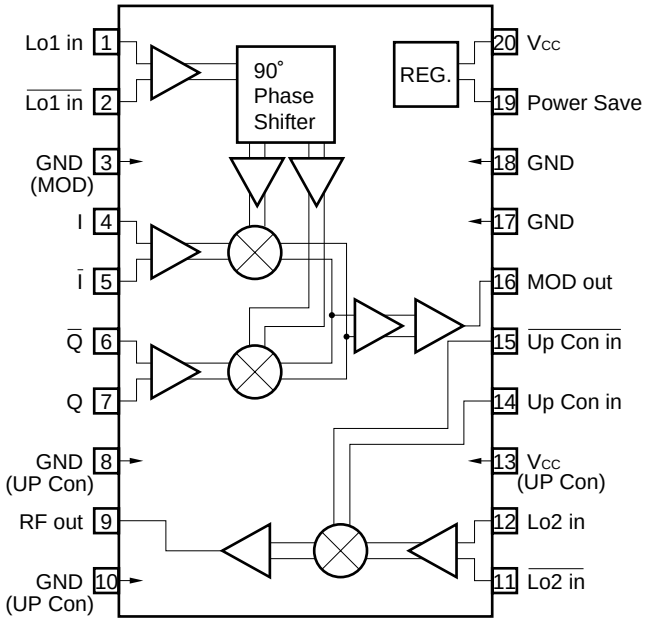
ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μPC8104GR-E1	20 pin plastic SSOP	Embossed tape 12 mm wide. QTY 2.5 kp/Reel. Pin 1 indicates pull-out direction of tape.

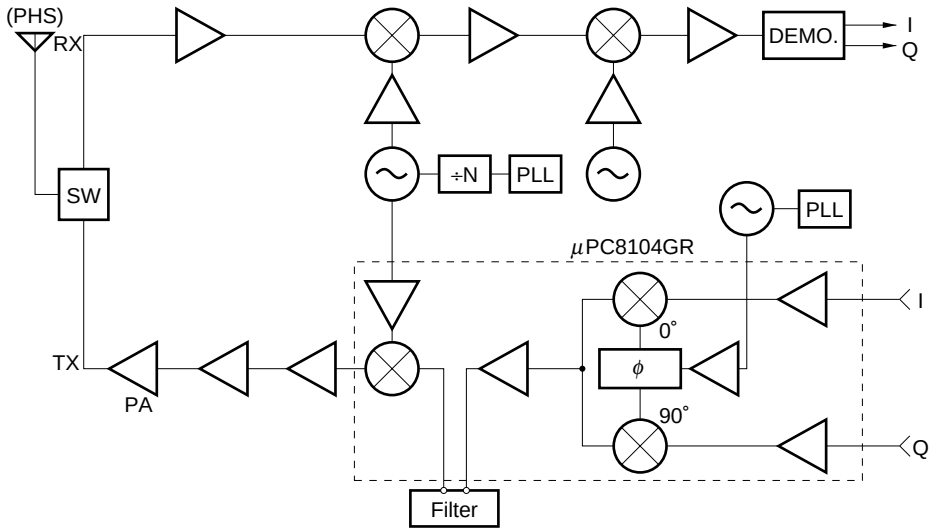
* For evaluation sample order, please contact your local NEC sales office. (Order number: μPC8104GR)

Caution electro-static sensitive device

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)



APPLICATION EXAMPLE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITION
Supply Voltage	V_{CC}	6.0	V	T_A = +25 °C
Power Save Voltage	V_{PS}	6.0	V	T_A = +25 °C
Power Dissipation	P_D	430	mW	T_A = +85 °C Note1
Operating Temperature	T_A	–40 to +85	°C	
Storage Temperature	T_{stg}	–55 to +150	°C	

Note 1: Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	2.7	3.0	5.5	V	
Operating Temperature	T_A	–40	+25	+85	°C	
Up Converter RF Frequency	f_{RFout}	0.8		1.9	GHz	
Up Converter Input Freq.	$f_{UpConin}$	100		400	MHz	
Modulator Output Frequency	f_{MODout}					
Lo1 Input Frequency	f_{Lo1in}					P_{Lo1in} = –10 dBm
Lo2 Input Frequency	f_{Lo2in}	800		1800	MHz	P_{Lo2in} = –10 dBm
I/Q Input Frequency	$f_{I/Qin}$	DC		10	MHz	$P_{I/Qin}$ = 600 mV_{p-p} MAX (Single ended)

ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified V_{PS} ≥ 1.8 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
UP CONVERTER + QUADRATURE MODULATOR TOTAL						
Total Circuit Current	$I_{ccTOTAL}$	18	28	37	mA	No input signal
Total Circuit Current at Power-Save Mode	$I_{cc(PS)TOTAL}$		0.1	10	μA	V_{PS} ≤ 1.0 V
Total Output Power	P_{RFout}	–18.5	–13.5	–8.5	dBm	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended)
Lo Carrier Leak Note2	LOL		–40	–30	dBc	
Image Rejection (Side Band Leak)	ImR		–40	–30	dBc	

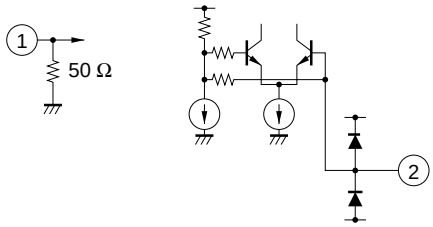
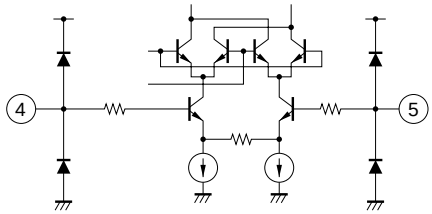
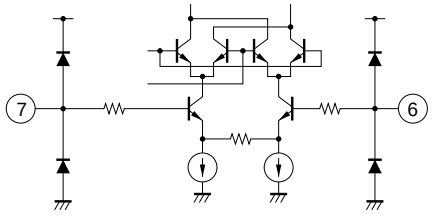
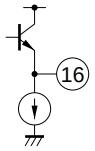
Note 2: Lo1 + Lo2

STANDARD CHARACTERISTICS FOR REFERENCE

(T_A = +25 °C, V_{CC} = 3.0 V, Unless Otherwise Specified V_{PS} ≥ 1.8 V)

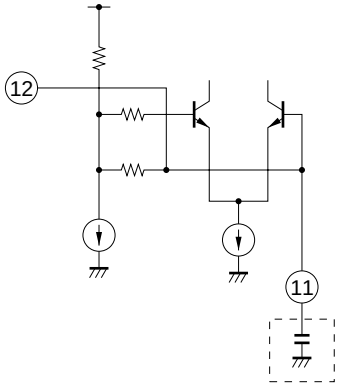
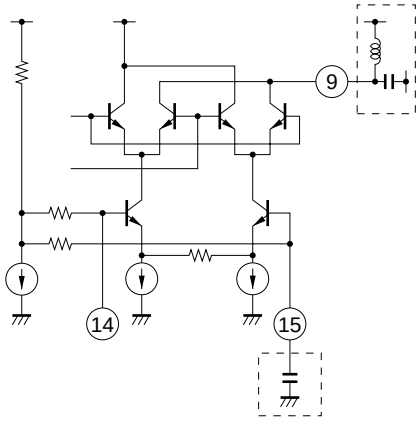
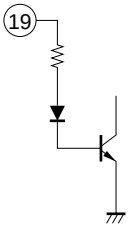
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
UP CONVERTER BLOCK						
Up Con. Circuit Current	$I_{ccUpCon}$		12		mA	No input signal
Up Con. Circuit Current at Power-Save Mode	$I_{cc(PS)UpCon}$			5	μA	V_{PS} ≤ 1.0 V
Conversion Gain	CG		4		dB	f_{RFout} = 1.9 GHz $f_{UpConin}$ = 240.0 MHz/240.2 MHz
Maximum Output Power	$P_{RF(sat)}$		–6		dBm	
Output Intercept Point	OIP3		0		dBm	
QUADRATURE MODULATOR BLOCK						
MOD. Circuit Current	I_{ccMOD}	10	16	21	mA	No input signal
MOD. Circuit Current at Power-Save Mode	$I_{cc(PS)MOD}$			5	μA	V_{PS} ≤ 1.0 V
Output Power	P_{MODout}		–16.5		dBm	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended)
Lo1 Carrier Leak	LOL		–40	–30	dBc	
Image Rejection (Side Band Leak)	ImR		–40	–30	dBc	
I/Q 3rd Order Intermodulation Distortion	$I_{M3I/Q}$		–50	–30	dBc	
I/Q Input Impedance	$Z_{I/Q}$		20		kΩ	I/Q DC = 1.5 V $P_{I/Qin}$ = 500 mV_{p-p} (Single ended) (I → $\overline{I}$, Q → $\overline{Q}$)
I/Q Bias Current	$I_{I/Q}$		5		μA	
Lo1 Input VSWR	Z_{Lo1}		1.2:1		X:1	
Power Save Rise Time	$T_{PS(RISE)}$		2.0	5.0	μs	$V_{PS(OFF)}$ → $V_{PS(ON)}$
Power Save Fall Time	$T_{PS(FALL)}$		2.0	5.0	μs	$V_{PS(ON)}$ → $V_{PS(OFF)}$

PIN EXPLANATION

<table>
<tr><th>PIN NO.</th><th>ASSIGN-MENT</th><th>SUPPLY VOL. (V)</th><th>PIN VOL.(V)</th><th>FUNCTION AND APPLICATION</th><th>EQUIPMENT CIRCUIT</th></tr>
<tr><td>1</td><td>Lo1in</td><td>–</td><td>0</td><td>Lo1 input for phase shifter.
This input impedance is 50 Ω matched internally.</td><td rowspan="2">  </td></tr>
<tr><td>2</td><td>$\overline{\text{Lo1in}}$</td><td>–</td><td>2.4</td><td>Bypass of Lo1 input.
This pin is grounded through internal capacitor.
Open in case of single ended.</td></tr>
<tr><td>3</td><td>GND for modulator</td><td>0</td><td>–</td><td>Connect to the ground with minimum inductance.
Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>4</td><td>I</td><td>Vcc/2</td><td>–</td><td>Input for I signal. This input impedance is larger than 20 kΩ.
Relations between amplitude and Vcc/2 bias of input signal are following.
<table><tr><th>Vcc/2 (v)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥ 1.35</td><td>400</td></tr><tr><td>≥ 1.5</td><td>600</td></tr><tr><td>≥ 1.75</td><td>1000</td></tr></table>Note</td><td rowspan="2">  </td></tr>
<tr><td>5</td><td>$\overline{\text{I}}$</td><td>Vcc/2</td><td>–</td><td>Input for I signal. This input impedance is larger than 20 kΩ.
Vcc/2 biased DC signal should be input.</td></tr>
<tr><td>6</td><td>$\overline{\text{Q}}$</td><td>Vcc/2</td><td>–</td><td>Input for Q signal. This input impedance is larger than 20 kΩ.
Vcc/2 biased DC signal should be input.</td><td rowspan="2">  </td></tr>
<tr><td>7</td><td>Q</td><td>Vcc/2</td><td>–</td><td>Input for Q signal. This input impedance is larger than 20 kΩ.
Relations between amplitude and Vcc/2 bias of input signal are following.
<table><tr><th>Vcc/2 (v)</th><th>Amp. (mVp-p)</th></tr><tr><td>≥ 1.35</td><td>400</td></tr><tr><td>≥ 1.5</td><td>600</td></tr><tr><td>≥ 1.75</td><td>1000</td></tr></table>Note</td></tr>
<tr><td>16</td><td>MODout</td><td>–</td><td>1.5</td><td>Output from modulator.
This is emitter follower output.</td><td>  </td></tr>
</table>

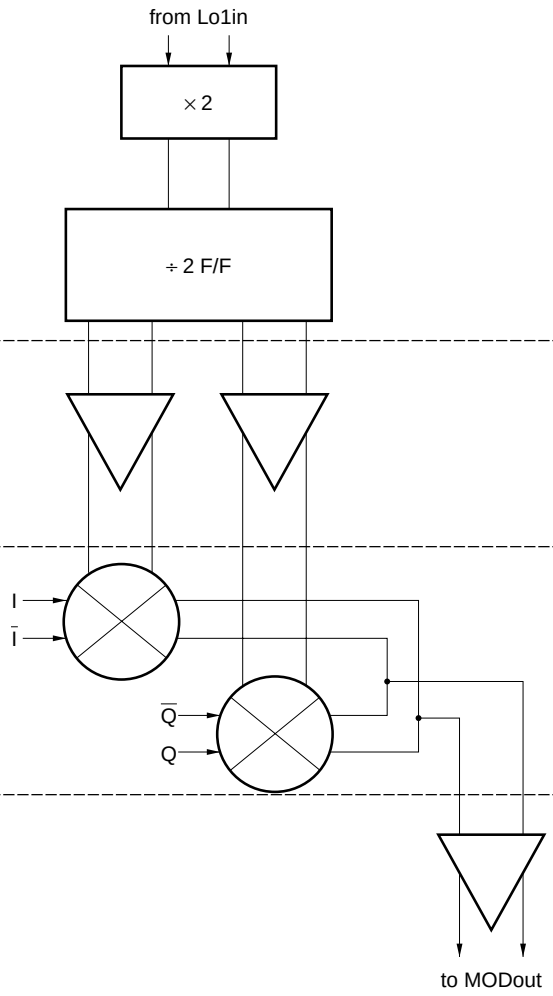
Note In case of that I/Q input signals are single ended.
Of course, I/Q signal inputs can be used either single endedly or differentially with proper terminations.

PIN EXPLANATION

PIN NO.	ASSIGN-MENT	SUPPLY VOL. (V)	PIN VOL.(V)	FUNCTION AND APPLICATION	EQUIPMENT CIRCUIT
8 10	GND for Up-converter	0	–	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
11	$\overline{\text{Lo2in}}$	–	2.0	Bypass of Lo2 input. Grounded through external capacitor.	
12	Lo2in	–	0	Lo2 input of Up-converter. This pin is high impedance input.	
13	V_{CC} for Up-converter	2.7 to 5.5	–	Supply voltage pin for Up-converter.	
9	RFout	V_{CC}	–	RF output from Up-Converter. This pin is open collector output.	
14	UpConin	–	2.0	IF input for Up-converter. This pin is high impedance input.	
15	$\overline{\text{UpConin}}$	–	2.0	Bypass of IF input. Grounded through external capacitor.	
17 18	GND	0	–	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
19	Power Save	$V_{P/S}$	–	Power save control pin can be controlled ON/SLEEP state with bias as follows; $V_{P/S}$ (V): 1.8 to 5.5 – STATE: ON $V_{P/S}$ (V): 0 to 1.0 – STATE: SLEEP	
20	V_{CC} for Modulator	2.7 to 5.5	–	Supply voltage pin for modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V_{CC}.	

: Externally

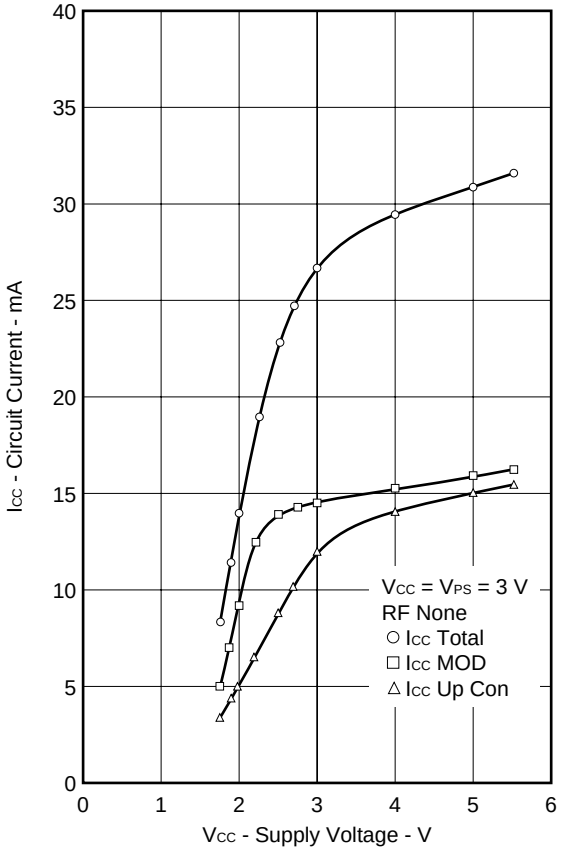
EXPLANATION OF INTERNAL FUNCTION

BLOCK	FUNCTION/OPERATION	BLOCK DIAGRAM
90° PHASE SHIFTER	Input signal from Lo1 is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as Lo1 input and that have quadrature phase shift, 0°, 90°, 180°, 270°. These circuits have function of self phase correction to make correctly quadrature signals.	
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	

TYPICAL CHARACTERISTICS (T_A = +25 °C)

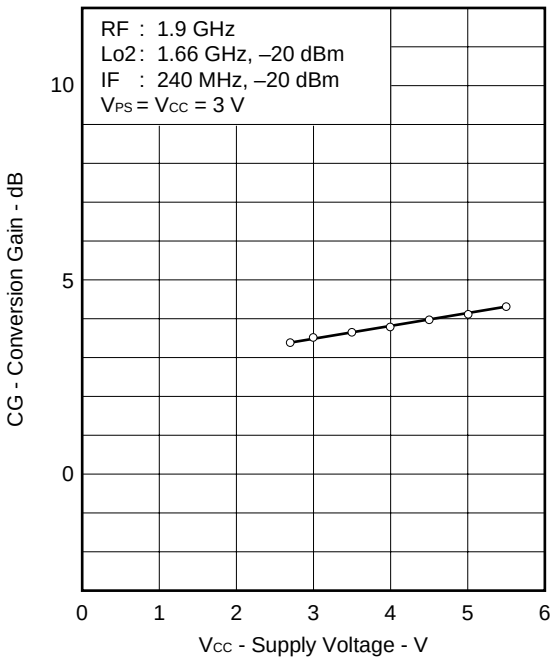
Unless otherwise specified V_{CC} = V_{PS} = 3 V, I/Q DC offset = $\overline{I}/\overline{Q}$ DC offset = 1.5 V, I/Q Input Signal = 500 mV_{p-p} (single ended), P_{Lo1in} = –10 dBm, P_{Lo2in} = –10 dBm, (continuous wave)

SUPPLY VOLTAGE vs CIRCUIT CURRENT



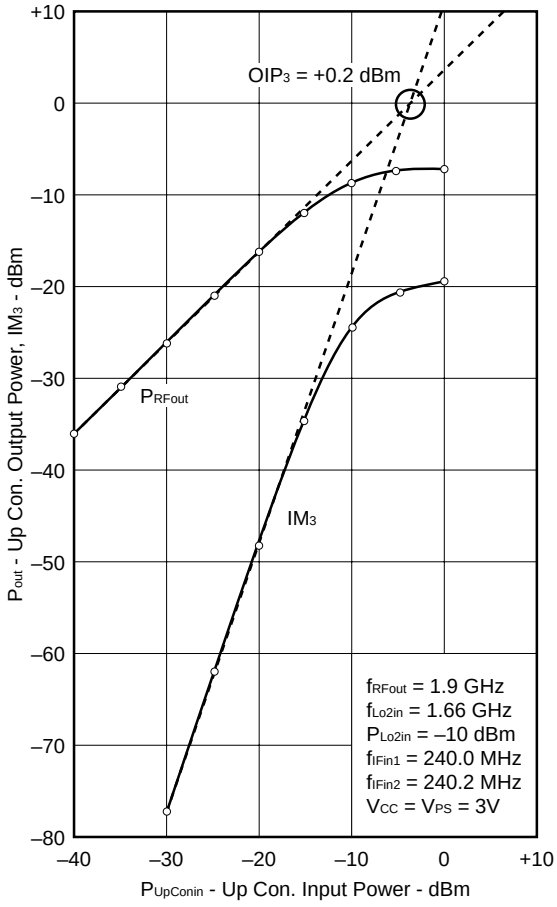
[UP CONVERTER BLOCK]

SUPPLY VOLTAGE vs CONVERSION GAIN



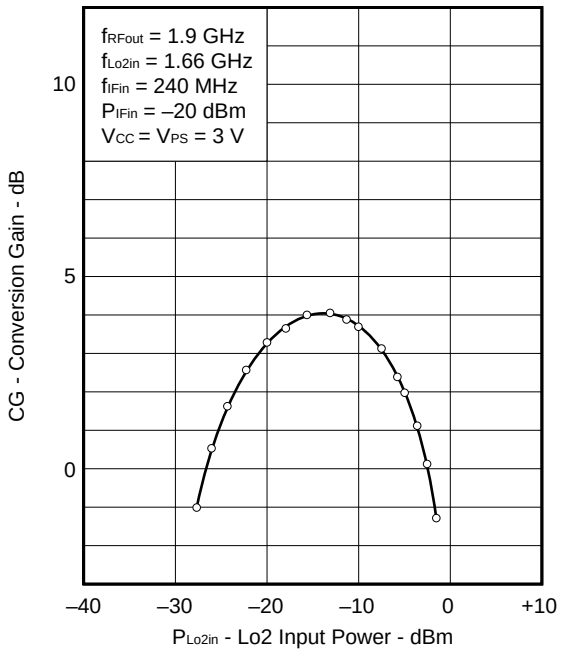
[UP CONVERTER BLOCK]

INPUT POWER vs OUTPUT POWER, IM_3



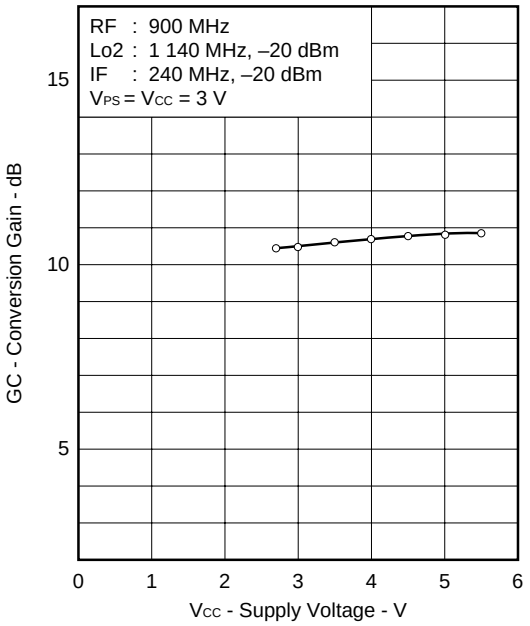
[UP CONVERTER BLOCK]

Lo2 INPUT POWER vs CONVERSION GAIN



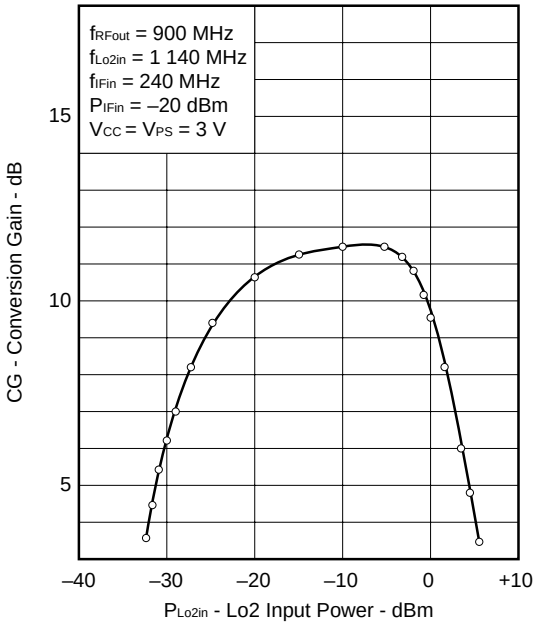
[UP CONVERTER BLOCK]

SUPPLY VOLTAGE vs CONVERSION GAIN



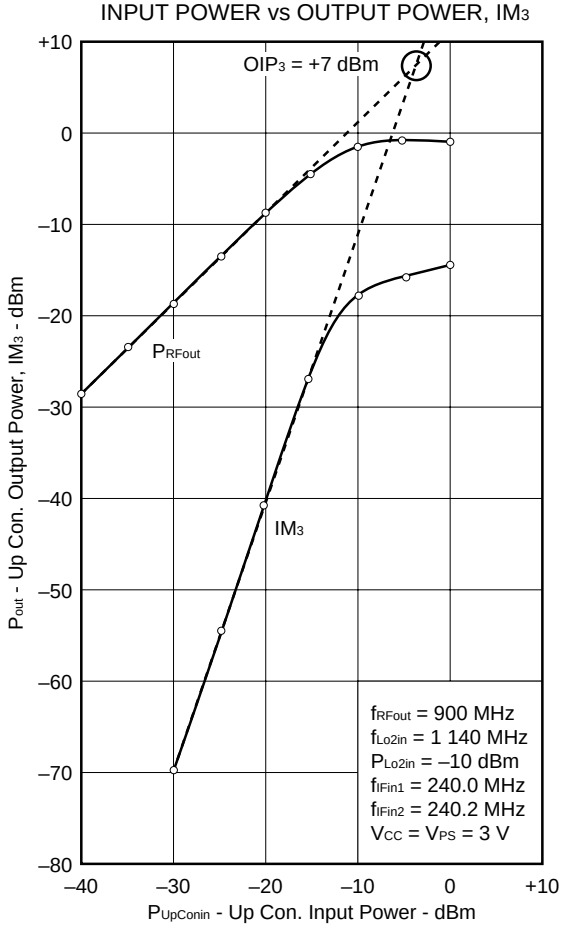
[UP CONVERTER BLOCK]

Lo2 INPUT POWER vs CONVERSION GAIN



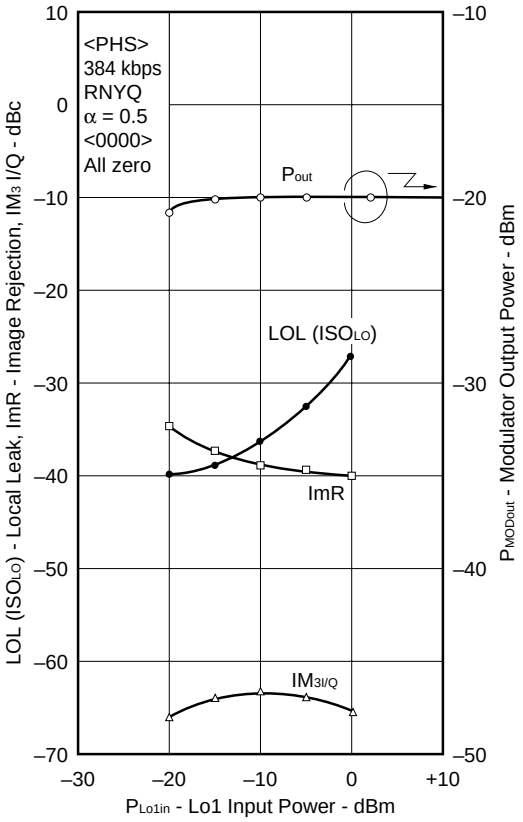
[UP CONVERTER BLOCK]

INPUT POWER vs OUTPUT POWER, IM3



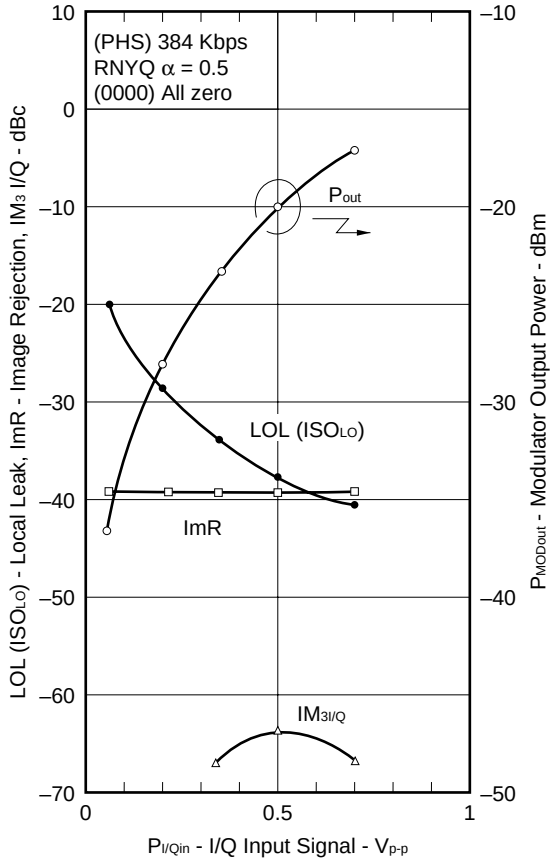
[MODULATOR BLOCK]

Lo1 INPUT POWER vs OUTPUT POWER, LOCAL LEAK, IMAGE REJECTION, I/Q 3RD ORDER INTERMODULATION DISTORTION



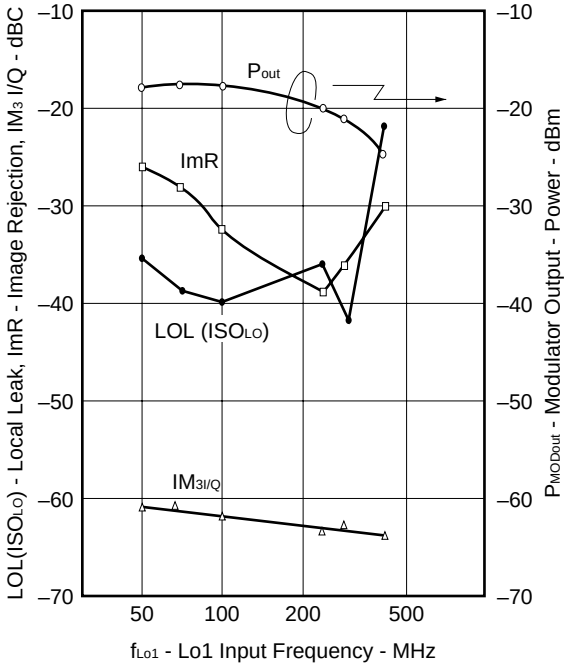
[MODULATOR BLOCK]

I/Q INPUT SIGNAL vs OUTPUT POWER,
LOCAL LEAK, IMAGE REJECTION,
I/Q 3RD ORDER INTERMODULATION
DISTORTION



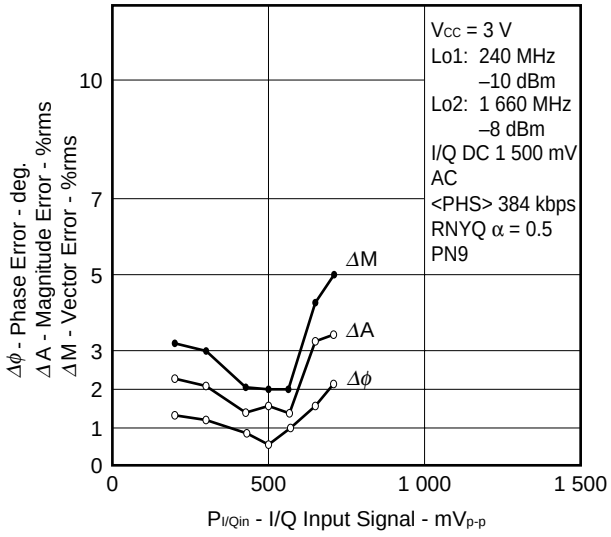
[MODULATOR BLOCK]

Lo1 INPUT FREQUENCY vs OUTPUT POWER,
LOCAL LEAK, IMAGE REJECTION, I/Q 3RD,
ORDER INTERMODULATION DISTORTION



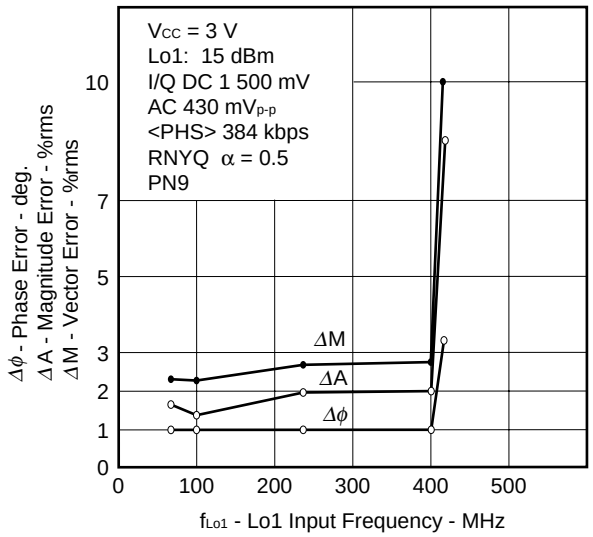
[MODULATOR + UP CONVERTER]

I/Q INPUT SIGNAL vs VECTOR ERROR,
MAGNITUDE ERROR, PHASE ERROR



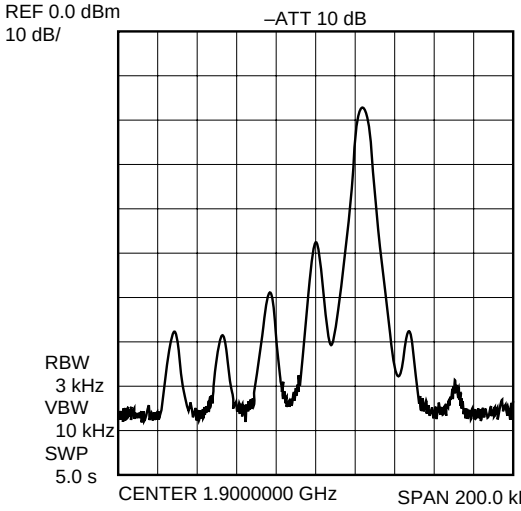
[MODULATOR BLOCK]

Lo1 INPUT FREQUENCY vs VECTOR ERROR,
MAGNITUDE ERROR, PHASE ERROR



[MODULATOR + UP CONVERTER]

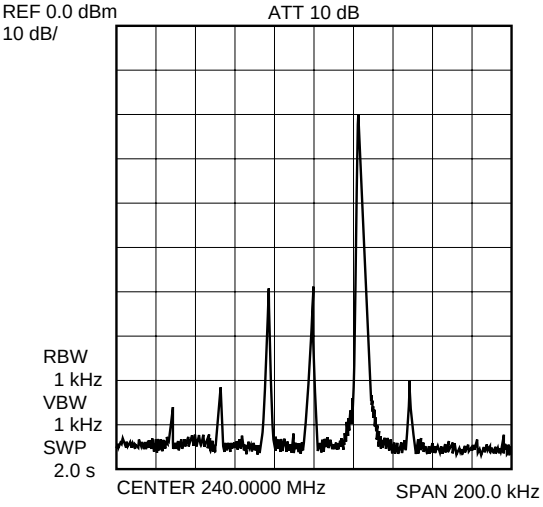
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



<PHS> 384 Kbps, RNYQ α = 0.5, MOD Pattern (0000), all zero.

[MODULATOR BLOCK]

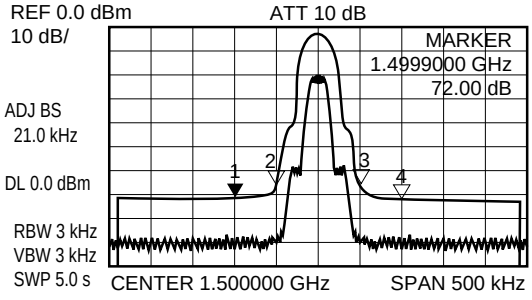
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM



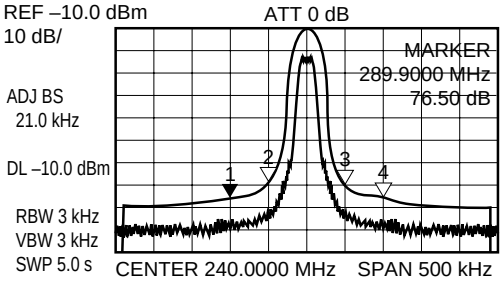
[MODULATOR + UP CONVERTER]

[MODULATOR BLOCK]

TYPICAL π/4 DQPSK MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ α = 0.5, MOD Pattern <PN9>



*** Multi Marker List ***
No. 1: 1.4999000 GHz –72.00 dB
No. 2: 1.4999500 GHz –66.00 dB
No. 3: 1.5000500 GHz –68.75 dB
No. 4: 1.5001000 GHz –72.00 dB

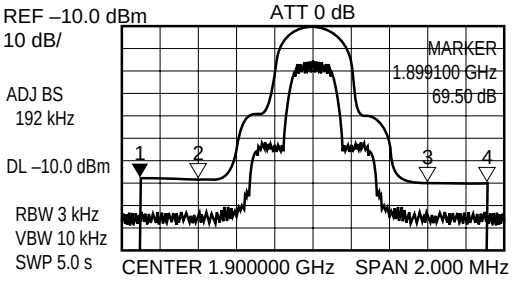


*** Multi Marker List ***
No. 1: 239.9000 MHz –76.50 dB
No. 2: 239.9500 MHz –70.50 dB
No. 3: 240.0500 MHz –71.00 dB
No. 4: 240.1000 MHz –75.75 dB

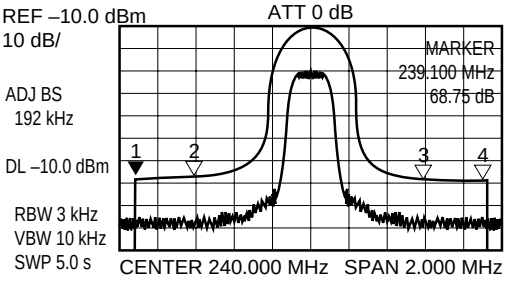
[MODULATOR + UP CONVERTER]

[MODULATOR BLOCK]

TYPICAL π/4 DQPSK MODULATION OUTPUT SPECTRUM
<PHS> 384 kbps, RNYQ α = 0.5, MOD Pattern (PN9)

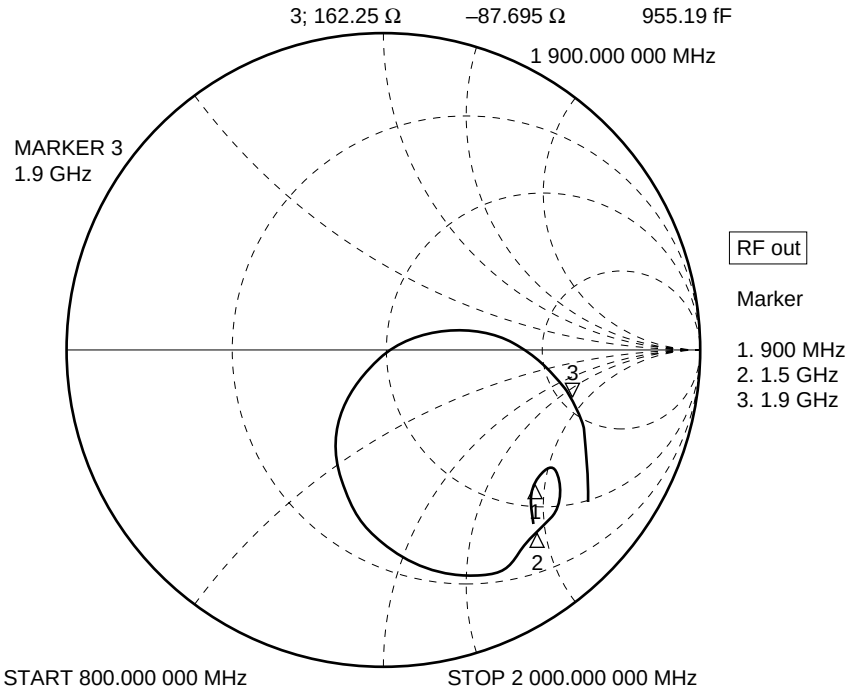


*** Multi Marker List ***
No. 1: 1.899100 GHz –69.50 dB
No. 2: 1.899400 GHz –69.00 dB
No. 3: 1.900600 GHz –69.00 dB
No. 4: 1.900900 GHz –69.50 dB

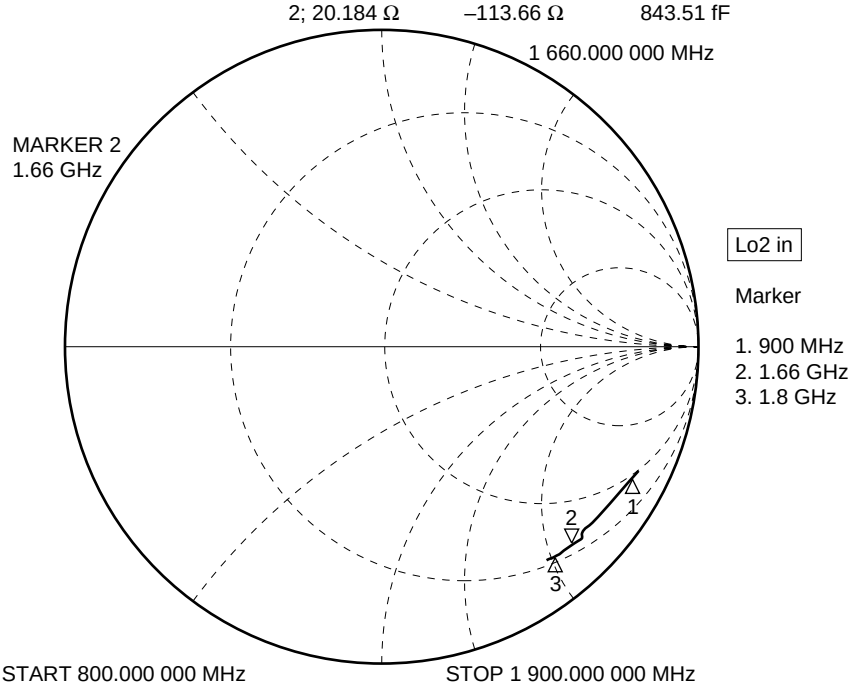


*** Multi Marker List ***
No. 1: 239.100 MHz –68.75 dB
No. 2: 239.400 MHz –68.25 dB
No. 3: 240.600 MHz –68.25 dB
No. 4: 240.900 MHz –69.00 dB

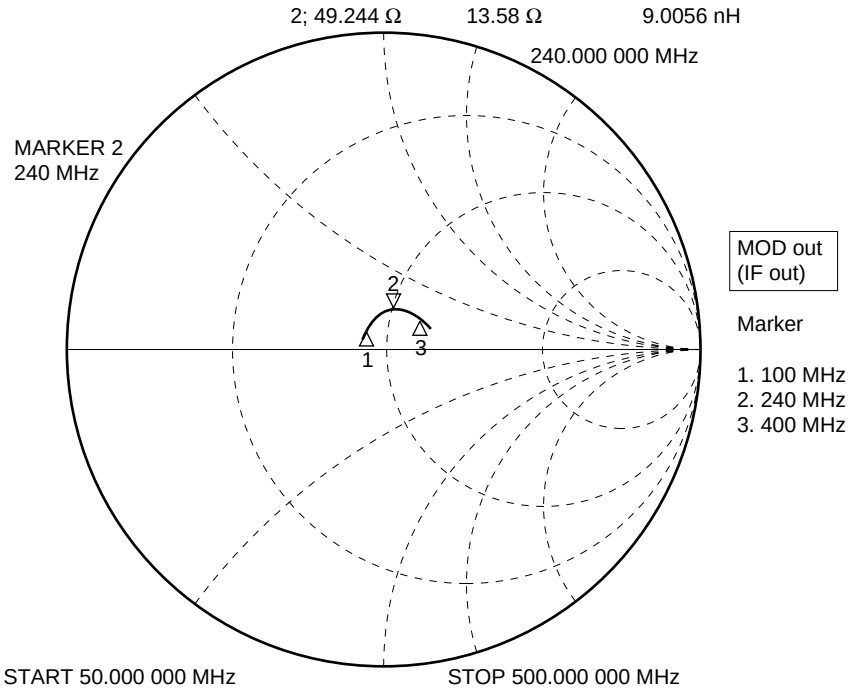
RFout OUTPUT IMPEDANCE



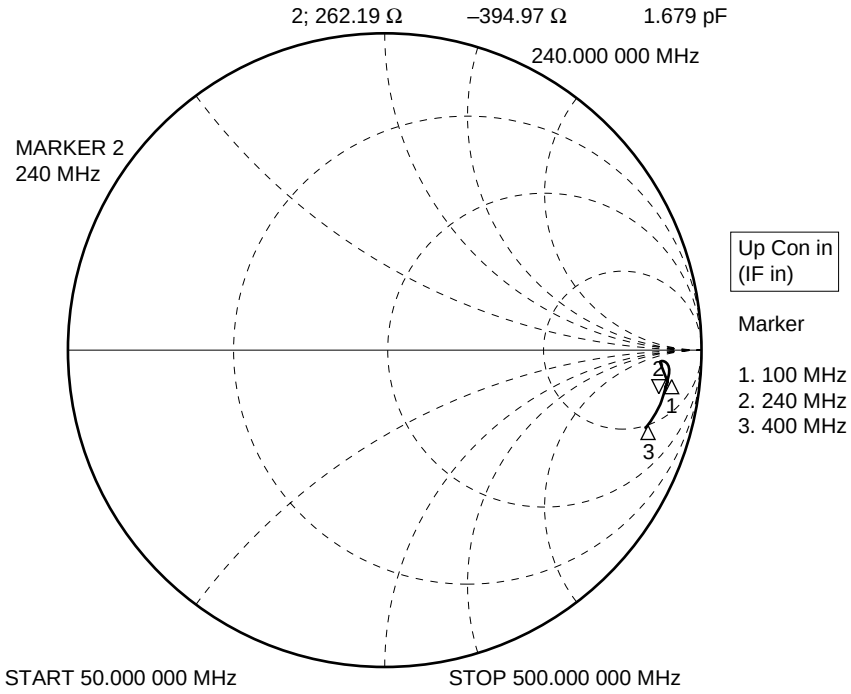
Lo2in INPUT IMPEDANCE



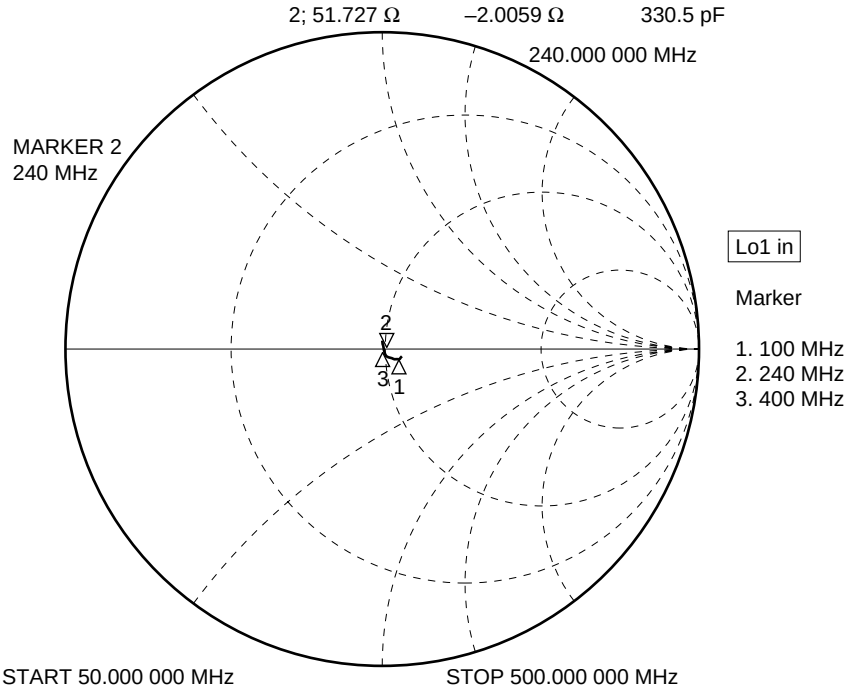
MODout OUTPUT IMPEDANCE



UP CON. in INPUT IMPEDANCE

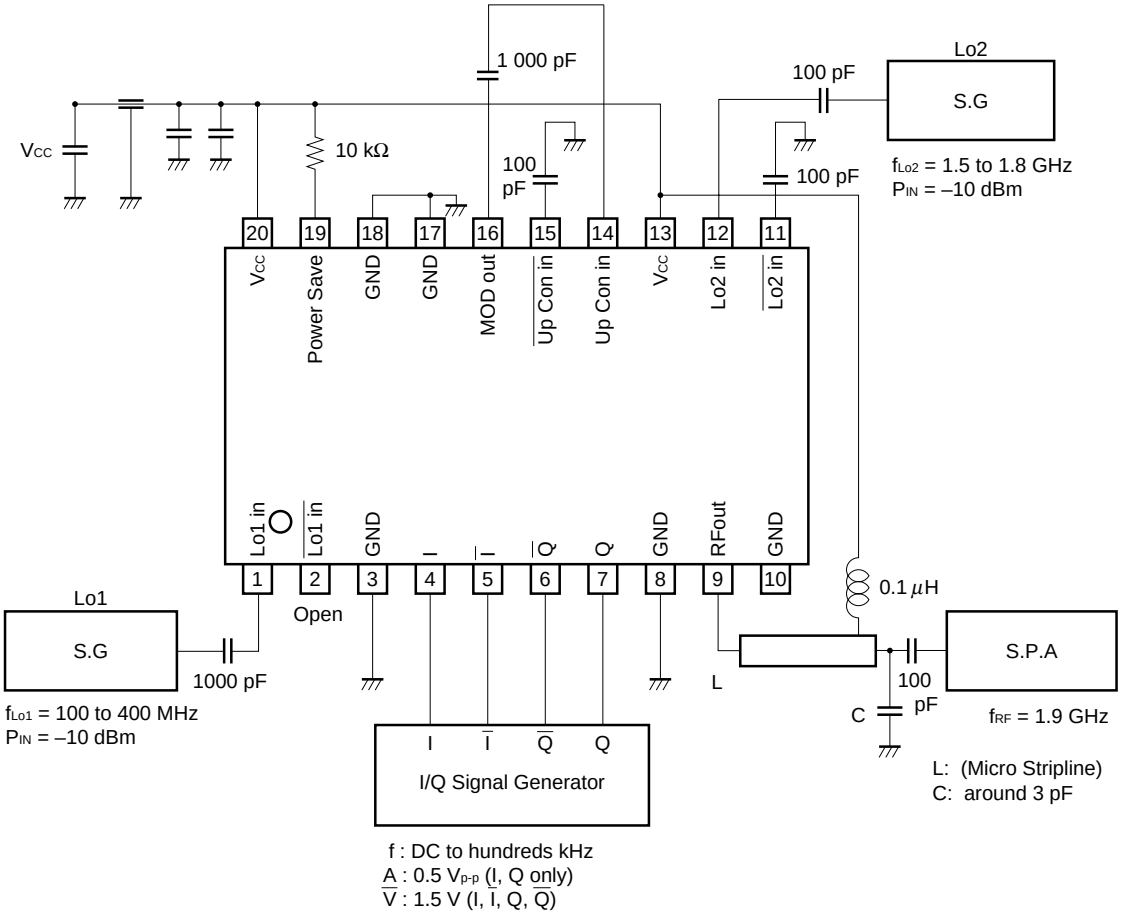


Lo1in INPUT IMPEDANCE

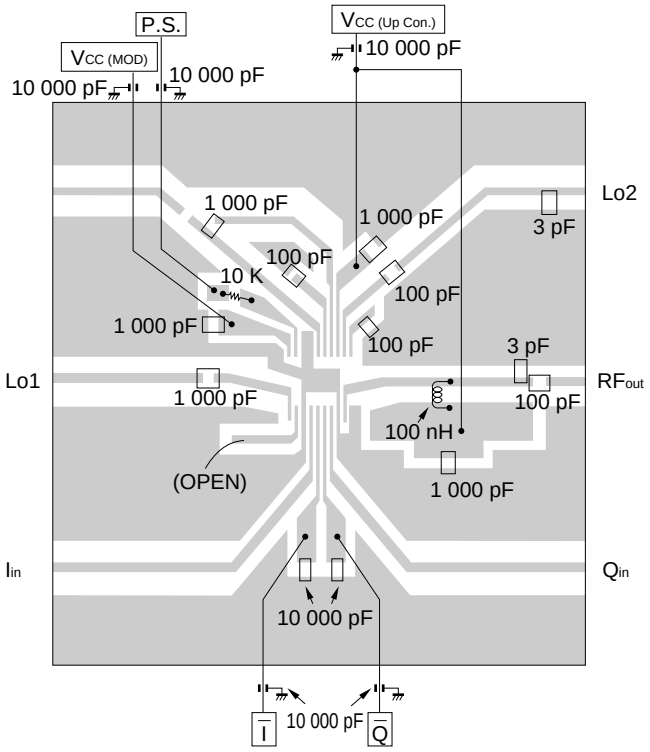


TEST CIRCUIT

(f_{RF} = 1.9 GHz)



TEST BOARD



In case of this test board, the output signal from MOD. is directly connected to the up converter input port through 1000 pF, which is DC coupling.

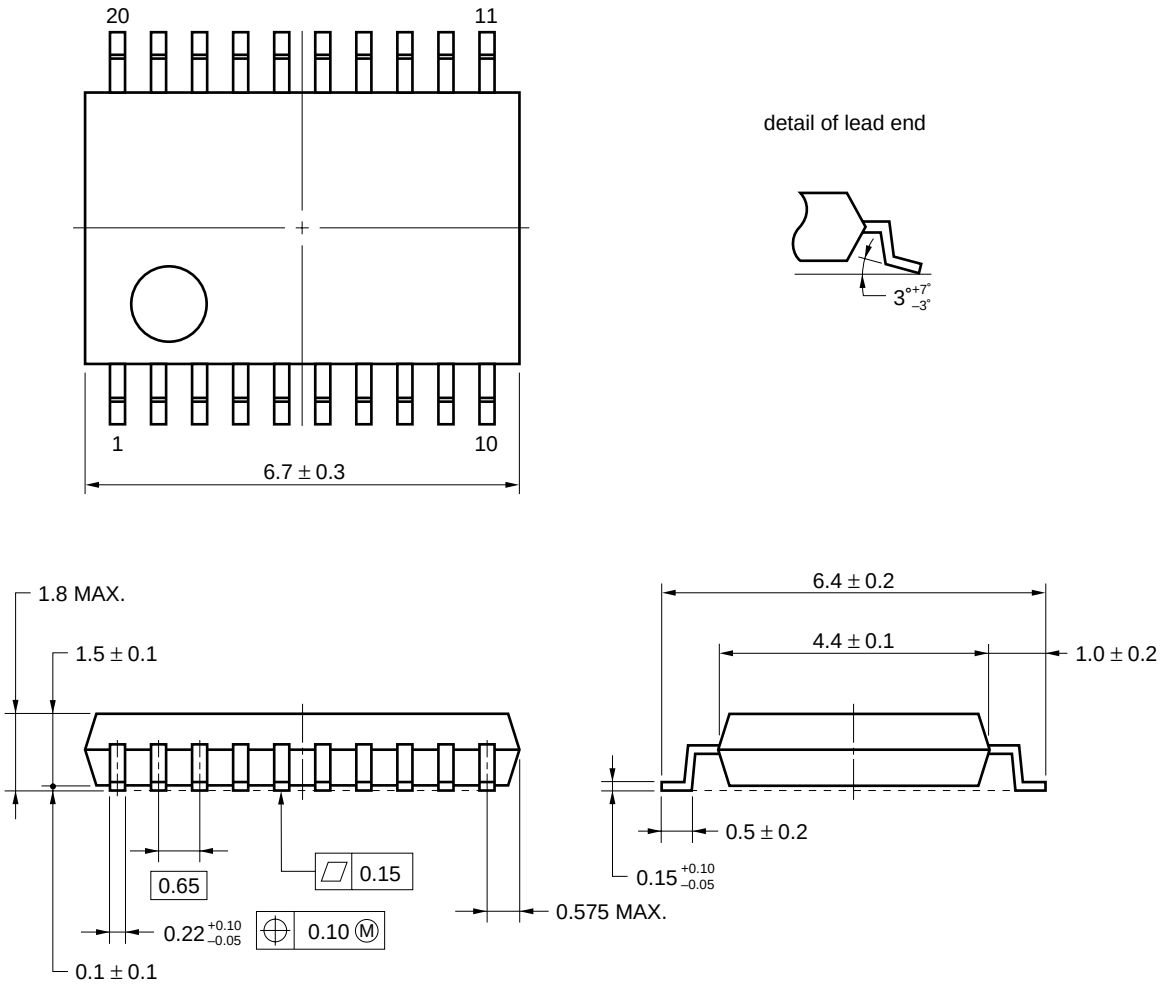
We recommend to insert a low pass filter between MOD output and up converter input port to reject harmonics of the Lo1 signal and to avoid saturation of the up converter.

GND

f_{RF} = 1.9 GHz
f_{Lo2} = 1.66 GHz
f_{Lo1} = 240 MHz

PACKAGE DIMENSIONS

★ **20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)**



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

(1) Observe precautions for handling because of electrostatic sensitive devices.
(2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
(3) Keep the track length of the ground pins as short as possible.
(4) Connect a bypass capacitor (e.g. 1 000 pF) to the V_{CC} pin.
(5) $\overline{I}$, $\overline{Q}$ DC offset voltage should be same as the I, Q DC offset voltage (to prevent changing the local leak level with power save control.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8104GR

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit[Note]: None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below Flow time: 10 seconds or below, Number of reflow process: 1, Exposure limit[Note]: None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below Flow time: 3 seconds/pin or below, Exposure limit[Note]: None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Apply only a single process at once, except for "Partial heating method".
For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

[MEMO]

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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