

NEC**BIPOLAR ANALOG INTEGRATED CIRCUIT**
 μ PC8110GR**1 GHz DIRECT QUADRATURE MODULATOR
FOR DIGITAL MOBILE COMMUNICATION****DESCRIPTION**

The μ PC8110GR is a silicon monolithic integrated circuit designed as 1 GHz direct quadrature modulator for digital mobile communication systems. This modulator housed in a 20 pin plastic SSOP that easy to install and contributes to miniaturizing the system.

The device has power save function and can operates 2.7 to 3.6 V supply voltage to realize low power consumption.

FEATURES

- Direct modulation range : 800 MHz to 1 GHz
- Supply voltage range : $V_{CC} = 2.7$ to 3.6 V
- Low operation current : $I_{CC} = 24$ mA typical @ $V_{CC} = 3$ V
- Low phase difference due to digital phase shifter is adopted.
- 20 pin SSOP suitable for high density surface mounting.
- Low current sleep mode

APPLICATION

- Digital cellular phone (PDC, IS-54/IS-136, GSM etc..)

ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING FORM
μ PC8110GR-E1	20 pin plastic SSOP	Carrier tape width 12 mm. Q'ty 2.5 kp/Reel Pin 1 indicated pull-out direction of tape.

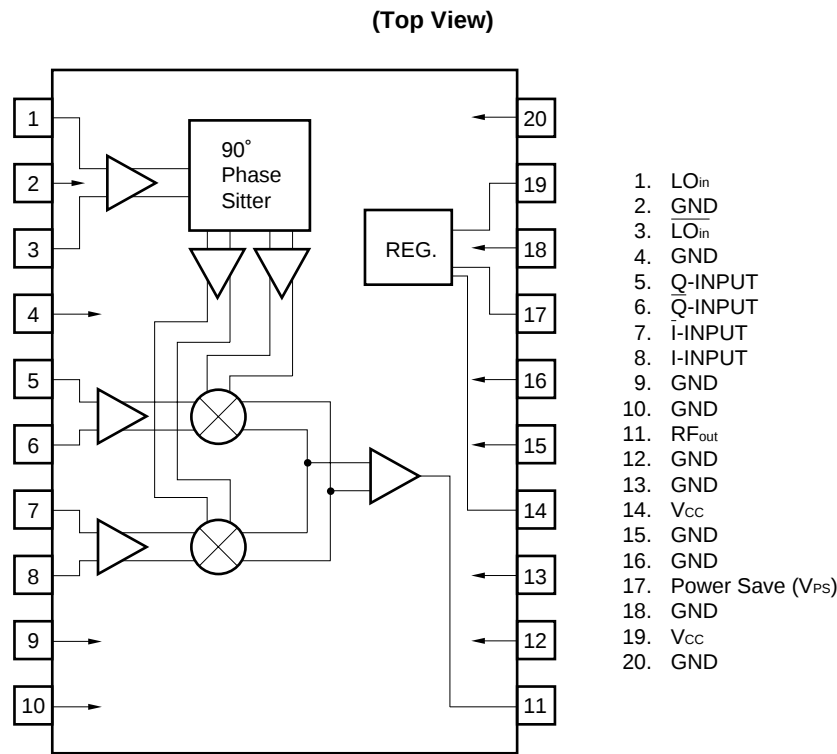
Remark For evaluation sample order, please contact your local NEC sales office. (Order number: μ PC8110GR)

Caution electro-static sensitive device

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS



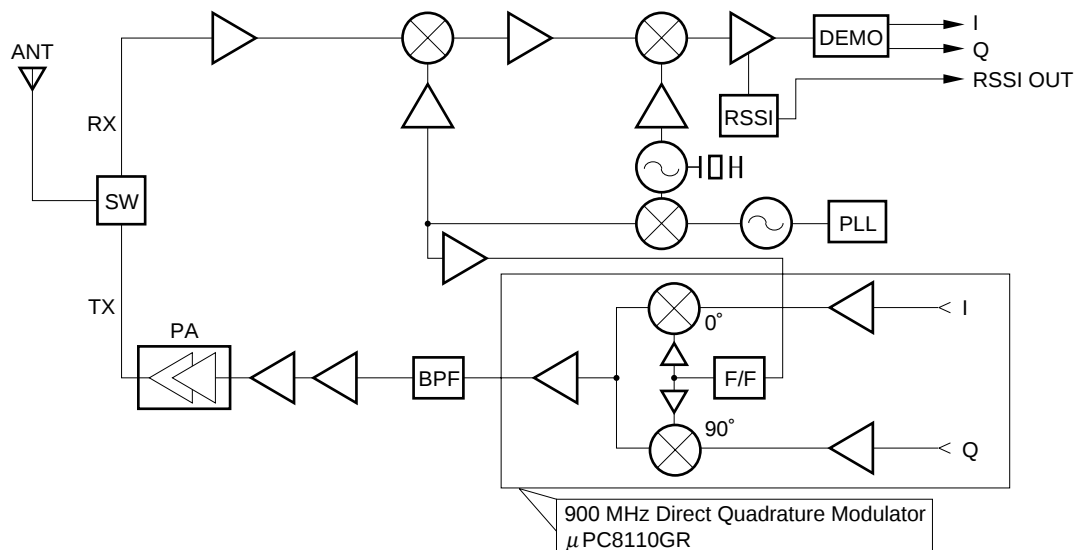
SERIES PRODUCTS

SERIES TYPE	PART NUMBER	f LO _{1in} (MHz)	f MOD _{out} (MHz)	f I/Q (MHz)	Up-Converter f RF _{out} (MHz)	APPLICATION
150 MHz Quadrature MOD	μPC8101GR	100 to 300	50 to 150	DC to 0.5	External	CT2, Digital Comm.
Up-Con+Quadrature MOD	μPC8104GR	100 to 400		DC to 10	900 to 1900	PHS, PDC etc..
400 MHz Quadrature MOD	μPC8105GR	100 to 400		DC to 10	External	PDC, IS-136, GSM, PHS
1 GHz direct Quad MOD	μPC8110GR	800 to 1000		DC to 10	Direct	PDC, IS-136, GSM etc.

Remark As for detail information of series products, please refer to each data sheet.

APPLICATION EXAMPLE

PDC 900 MHz (Direct Modulation Type)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	TEST CONDITIONS
Supply Voltage	V _{CC}	4.0	V	T _A = +25 °C
Power Save Voltage	V _{PS}	4.0	V	T _A = +25 °C
Power Dissipation	P _D	430	mW	T _A = +85 °C ^{Note 1}
Operating Temperature	T _{opt}	−40 to +85	°C	
Storage Temperature	T _{stg}	−55 to +150	°C	

Note 1. Mounted on 50 × 50 × 1.6 mm double copper clad epoxy glass board

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Voltage	V _{CC}	2.7	3.0	3.6	V	
Operating Temperature	T _{opt}	−40	+25	+85	°C	
L _O Input Frequency	f _{LOin}	800	900	1000	MHz	
L _O Input Power Level	PL _{Oin}	−15	−10	−7	dBm	
I/Q Input Frequency	f _{I/Qin}	DC		10	MHz	
I/Q Input Voltage	V _{I/Qin}			500	mV _{p-p}	Single ended input
				250		Differential input

ELECTRICAL CHARACTERISTICS (TA = 25 °C, VCC = 3.0 V, Unless Otherwise Specified VPS ≥ 2.2 V (High))

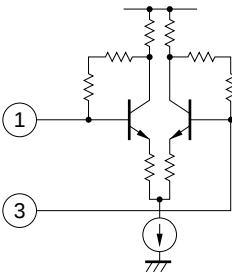
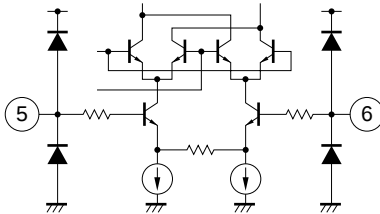
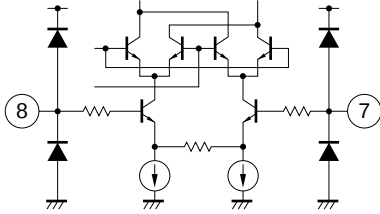
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	ICC	20	24	33	mA	No input signal
Circuit Current at Power Save Mode	ICC(PS)			10	μA	VPS ≤ 0.5 V (Low)
Maximum Output Power	PO(sat)	-13	-10		dBm	fLOin = 948 MHz PLOin = -10 dBm fIQ = 2.625 kHz I/Q (DC) = VCC/2 VI/Qin = 500 mVp-p (Single ended)
Lo Carrier Leak	LoL		-35	-30	dBc	
Image Rejection (Side Band Leak)	ImR		-40	-30	dBc	
I/Q 3rd Order Intermodulation Distortion	IM3I/Q		-45	-30	dBc	
Power Save Rise Time	TPS(RISE)		3	5	μs	VPS: Low → High
Power Save Fall Time	TPS(FALL)		2	5	μs	VPS: High → Low

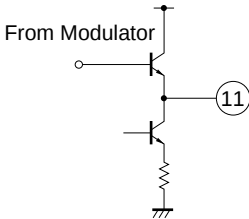
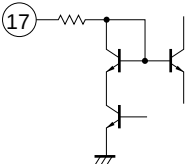
STANDARD CHARACTERISTICS FOR REFERENCE

(TA = +25 °C, VCC = 3.0 V, Unless Otherwise Specified VPS ≥ 2.2 V (High))

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
I/Q Input Impeadance	ZI/Qin		150		kΩ	fIQ = DC to 10 MHz
Lo Input VSWR	VSWR (Lo)		1.5 : 1		—	fLO = 948 MHz
RF Output VSWR	VSWR (RF)		1.5 : 1		—	fLO = 948 MHz

PIN EXPLANATION

Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	L _o in	—	2.6	L _o input for phase shifter. Connect around 50 Ω between 1 and 3 pin to match to 50 Ω.	
2	GND (for Local Amp. Block)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	
18					
3	L _o in	—	2.6	Bypass of L _o input. This pin is grounded through around 33 pF capacitor.	
5	Q	V _{cc} /2	—	Input for Q signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. Note 2	
6	Q̄	V _{cc} /2	—	Input for Q signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, V _{cc} /2 biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. Note 2	
7	Ī	V _{cc} /2	—	Input for I signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, V _{cc} /2 biased DC signal should be input. In case of that I/Q input signals are differential, amplitude of the signal is 250 mVp-p max. Note 2	
8	I	V _{cc} /2	—	Input for I signal. This input impedance is 150 kΩ. In case of that I/Q input signals are single ended, amplitude of the signal is 500 mVp-p max. Note 2	
9	GND (for Quadrature Modulator Block)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—
13					
16					

Pin No.	ASSIGNMENT	SUPPLY VOL. (V)	PIN VOL. (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT						
11	RF _{out}	—	1.6	Output from modulator. This is single-end push-pull amplifier. So this output impedance is Low.							
12	GND (for Output Push-pull Amplifier)	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.							
14	V _{CC} (for Output Amplifier of Modulator)	2.7 to 3.6	—	Supply voltage pin for Output Amplifier of modulator. Internal regulator can be kept stable condition of supply bias against the variable temperature or V _{CC} .							
17	Power Save	V _{P/S}	—	Power save control pin can be controlled ON/SLEEP state with bias as follows; <table border="1" data-bbox="693 932 950 1073"><thead><tr><th>V_{P/S}</th><th>STATE</th></tr></thead><tbody><tr><td>2.2 to 3.6</td><td>ON</td></tr><tr><td>0 to 0.5</td><td>SLEEP</td></tr></tbody></table>	V _{P/S}	STATE	2.2 to 3.6	ON	0 to 0.5	SLEEP	
V _{P/S}	STATE										
2.2 to 3.6	ON										
0 to 0.5	SLEEP										
19	V _{CC}	2.7 to 3.6	—	Supply voltage pin for modulator except output Amplifier. Internal regulator can be kept stable condition of supply bias against the variable temperature or V _{CC} .	—						
4	GND	0	—	Connect to the ground with minimum inductance. Track length should be kept as short as possible.	—						
10											
15											
20											

Note 2. Relations between amplitude and V_{cc}/2 bias of input signal are following.

Supply Voltage V _{cc} (V)	I/Q DC Voltage (V) V _{cc} /2 = I = $\bar{I}$ = Q = $\bar{Q}$	P _{I/Qin} - I/Q Input Signal - mVp-p	
		Single ended input I = Q	Differential input I = $\bar{I}$ = Q = $\bar{Q}$
2.7 to 3.6	1.35 to 1.8	≤ 500	≤ 250

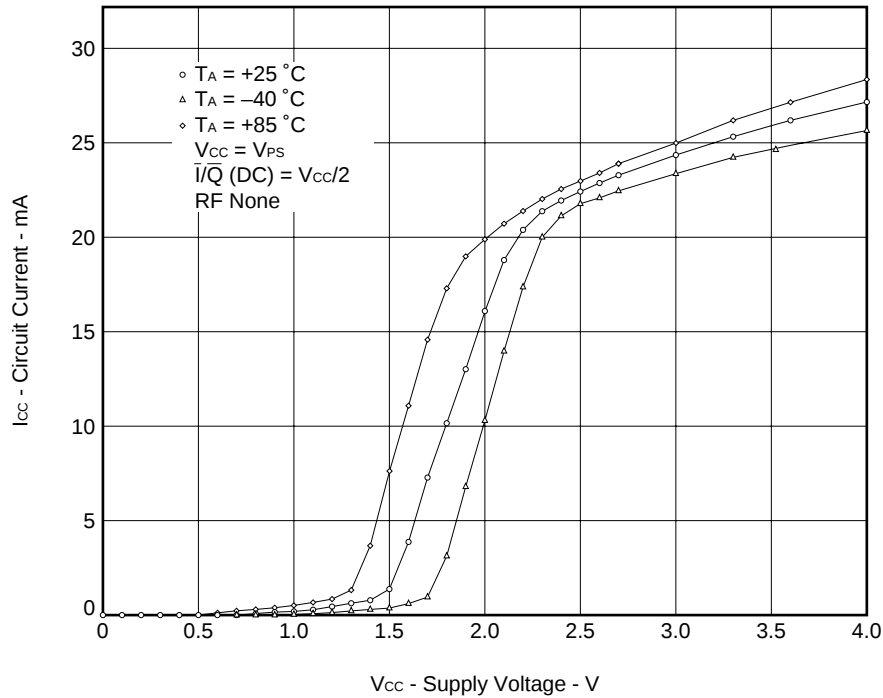
EXPLANATION OF INTERNAL FUNCTION

BLOCK	FUNCTION/OPERATION	BLOCK DIAGRAM
90 ° PHASE SHIFTER	Input signal from L _o is send to digital circuit of T-type flip-flop through frequency doubler. Output signal from T-type F/F is changed to same frequency as L _o input and that have quadrature phase shift, 0 °, 90 °, 180 °, 270 °. These circuits have function of self phase correction to make correctly quadrature signals.	The block diagram illustrates the internal signal processing. It begins with an input 'from LO_{in}' which enters a frequency doubler block labeled '× 2'. The output of this block goes into a T-type flip-flop block labeled '÷ 2 F/F'. From the flip-flop, two signals emerge, each passing through a buffer amplifier (represented by a triangle pointing downwards). These buffered signals then enter two mixers, represented by circles with an 'X' inside. The first mixer also receives an external input 'I' and produces an output 'I'. The second mixer receives an external input 'Q' and produces an output 'Q'. The outputs of both mixers are connected to an adder block (represented by a triangle pointing upwards). The final output of the adder is labeled 'to MOD_{out}'.
BUFFER AMP.	Buffer amplifiers for each phase signals to send to each mixers.	
MIXER	Each signals from buffer amp. are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to good performance for image rejection.	
ADDER	Output signals from each mixers are added with adder and send to final amplifier.	

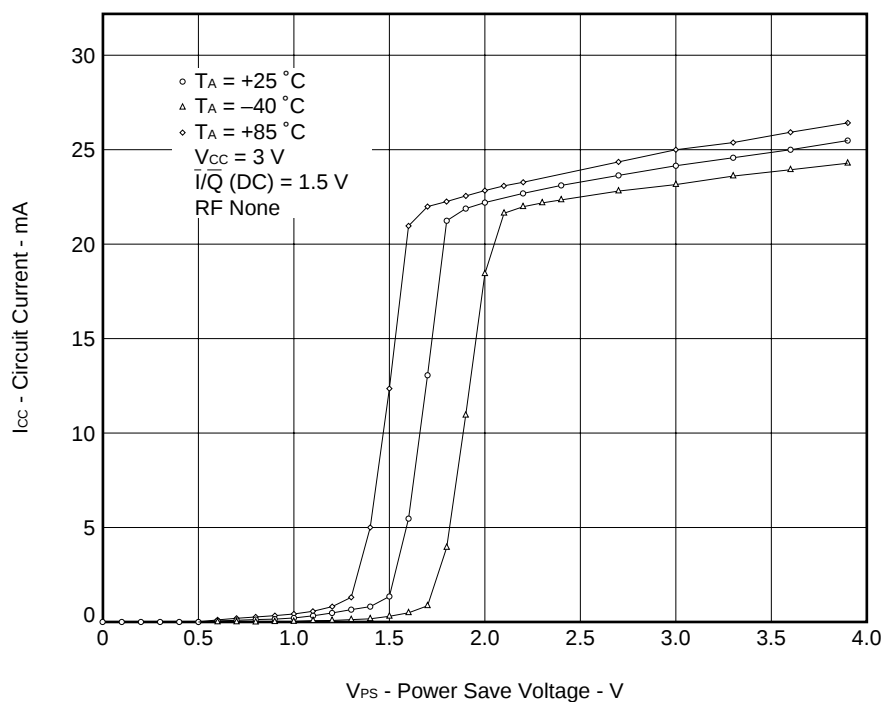
TYPICAL CHARACTERISTICS

Unless otherwise specified $T_A = +25\text{ }^{\circ}\text{C}$, $V_{CC} = V_{PS} = 3\text{ V}$, $I/Q\text{ DC}/\text{offset} = \overline{I/Q}\text{ DC offset} = 1.5\text{ V}$, $I/Q\text{ Input signal} = 500\text{ mV}_{p-p}$ (Single ended), $f_{I/Q} = 2.625\text{ kHz}$, $f_{LOin} = 948\text{ MHz}$, $P_{LOin} = -10\text{ dBm}$, $\langle PDC \rangle$ Transmission speed: 42 kbps, RNYQ: $a = 0.5$.

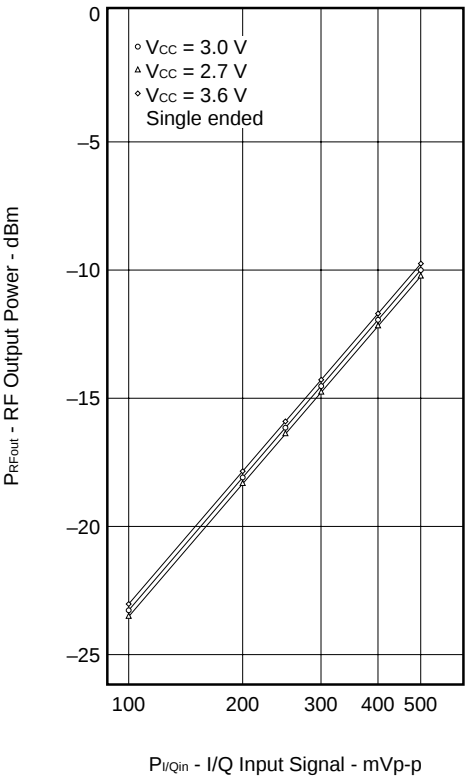
CIRCUIT CURRENT vs SUPPLY VOLTAGE



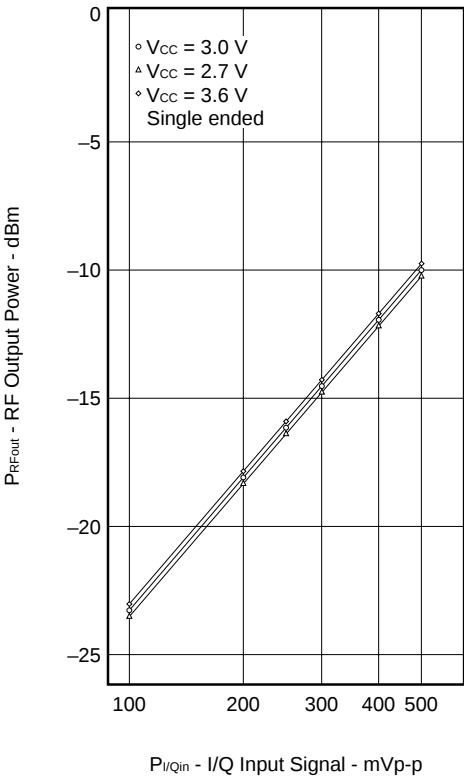
CIRCUIT CURRENT vs POWER SAVE VOLTAGE



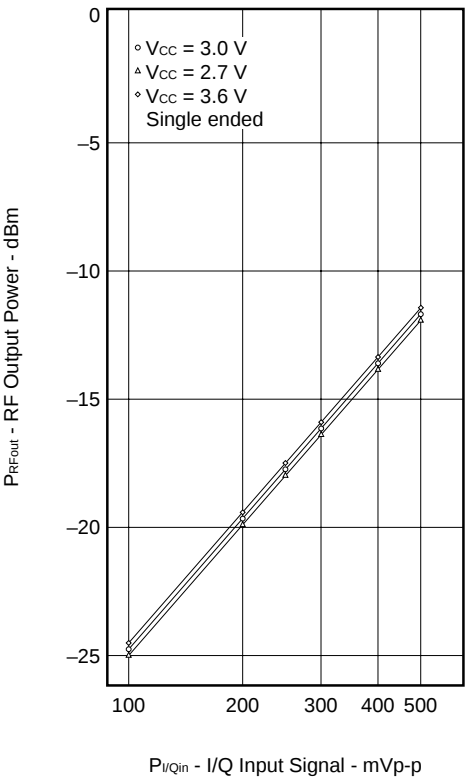
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = -40 °C)



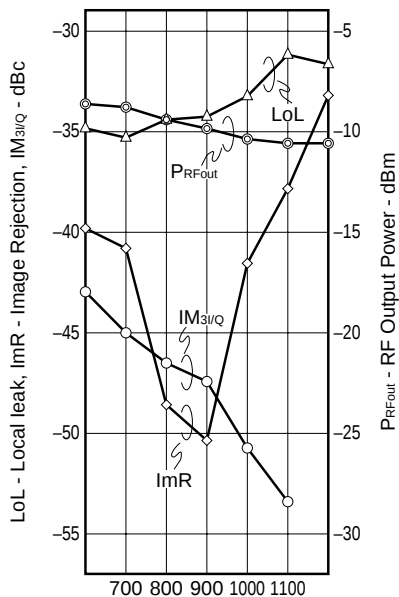
RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = +25 °C)



RF OUTPUT POWER vs I/Q INPUT SIGNAL
(at T_A = +85 °C)

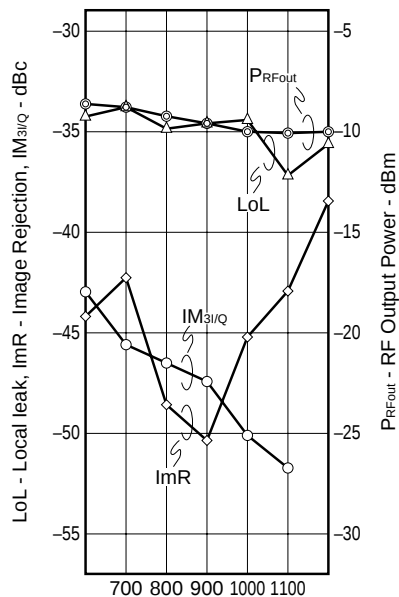


Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 2.7 V, T_A = -40 °C)



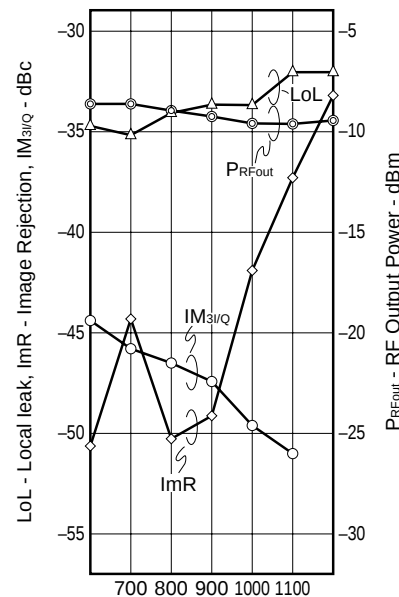
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.0 V, T_A = -40 °C)



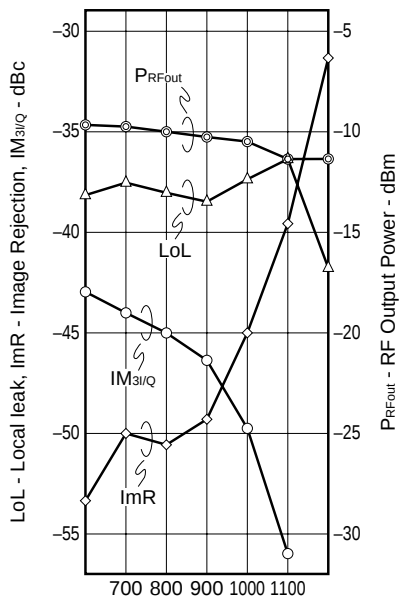
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.6 V, T_A = -40 °C)



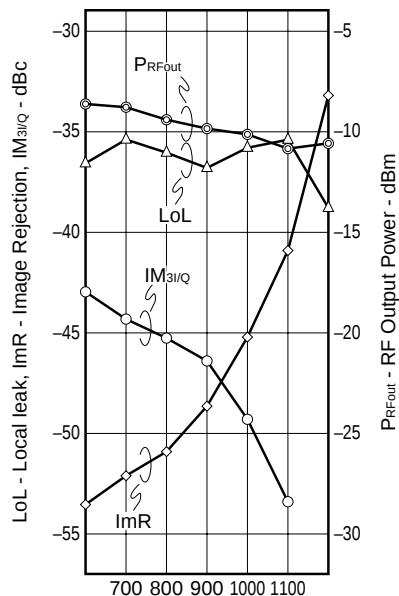
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 2.7 V, T_A = +25 °C)



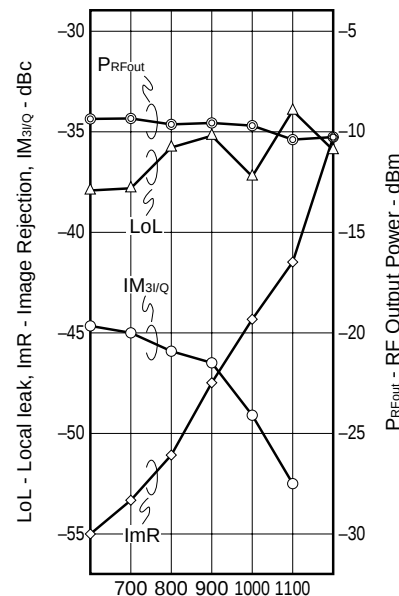
f_{LO} - Local Input Frequency - MHz

Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.0 V, T_A = +25 °C)

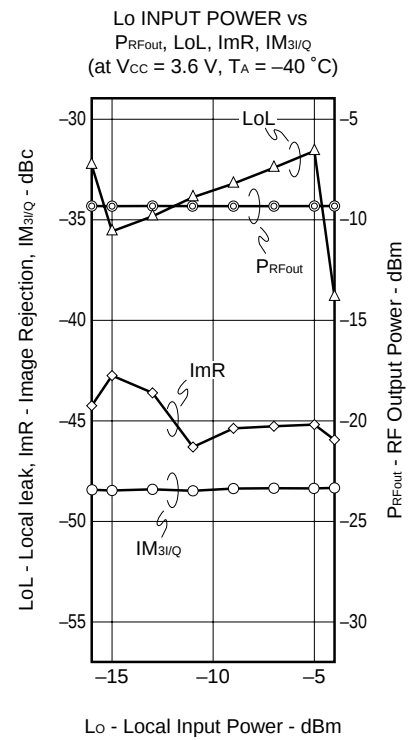
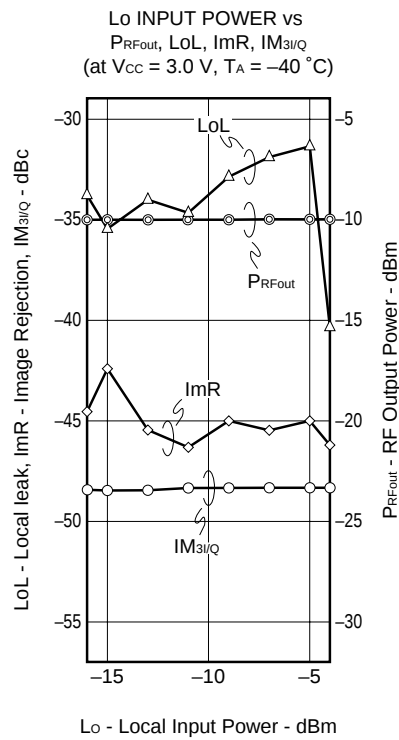
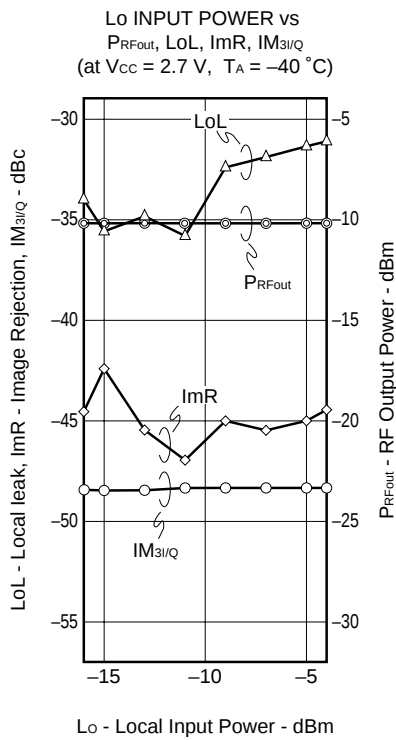
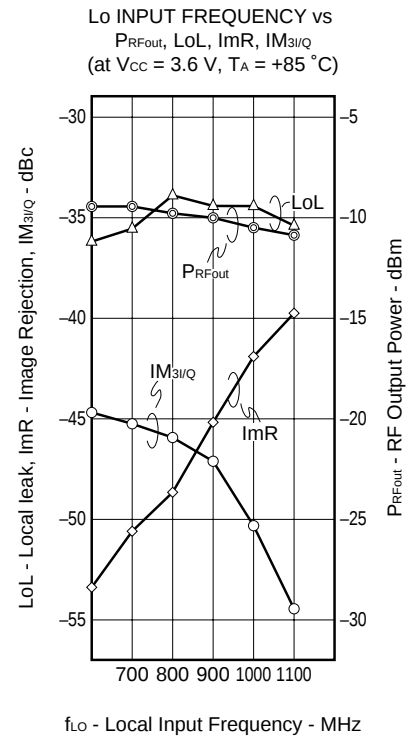
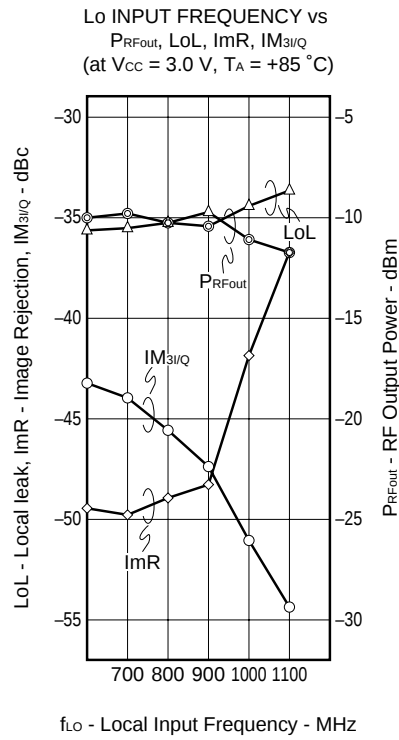
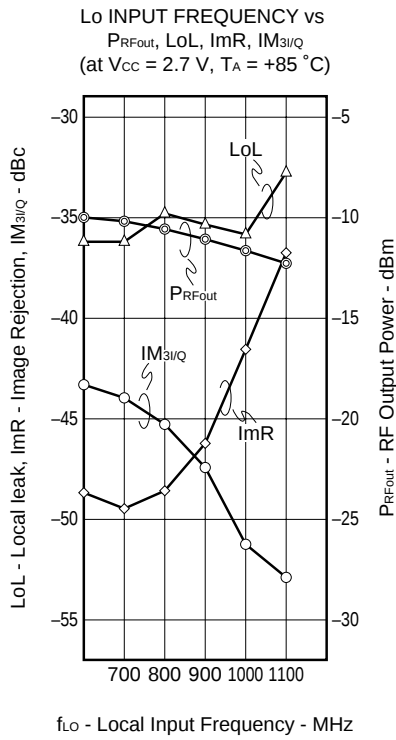


f_{LO} - Local Input Frequency - MHz

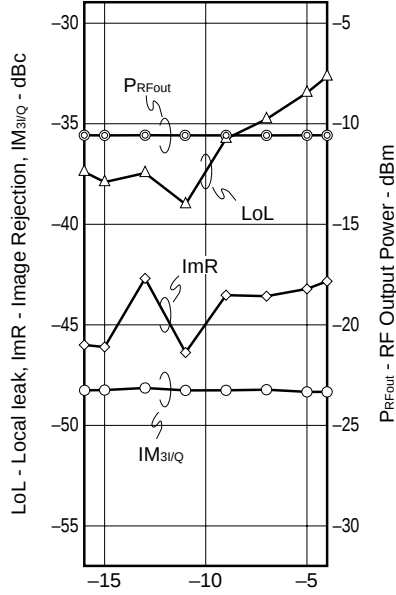
Lo INPUT FREQUENCY vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.6 V, T_A = +25 °C)



f_{LO} - Local Input Frequency - MHz

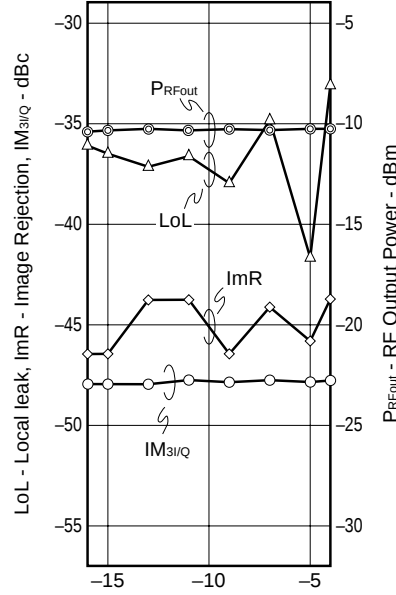


Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 2.7 V, T_A = +25 °C)



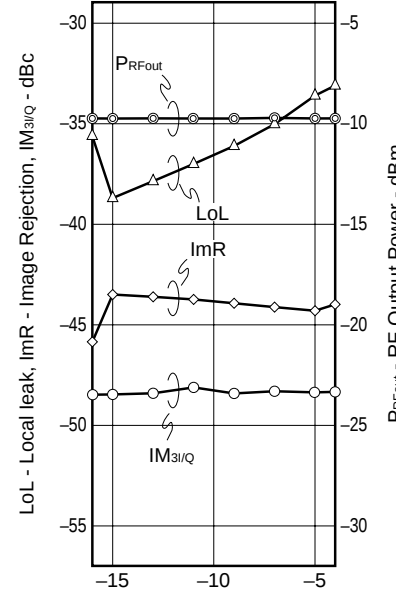
Lo - Local Input Power - dBm

Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.0 V, T_A = +25 °C)



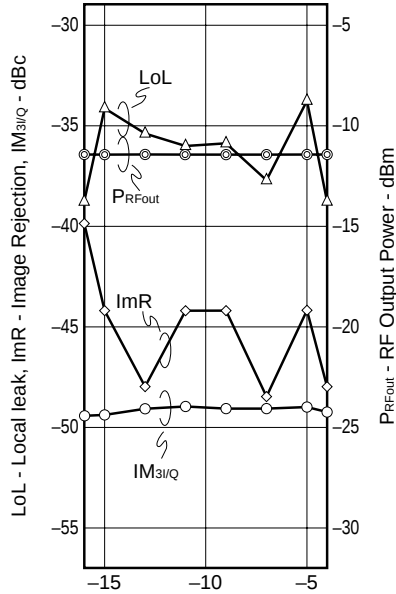
Lo - Local Input Power - dBm

Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.6 V, T_A = +25 °C)



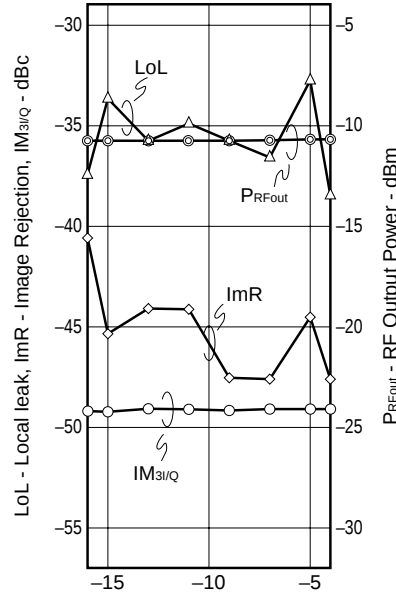
Lo - Local Input Power - dBm

Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 2.7 V, T_A = +85 °C)



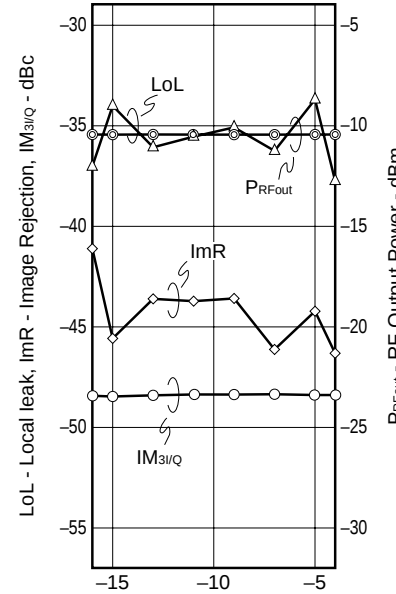
Lo - Local Input Power - dBm

Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.0 V, T_A = +85 °C)

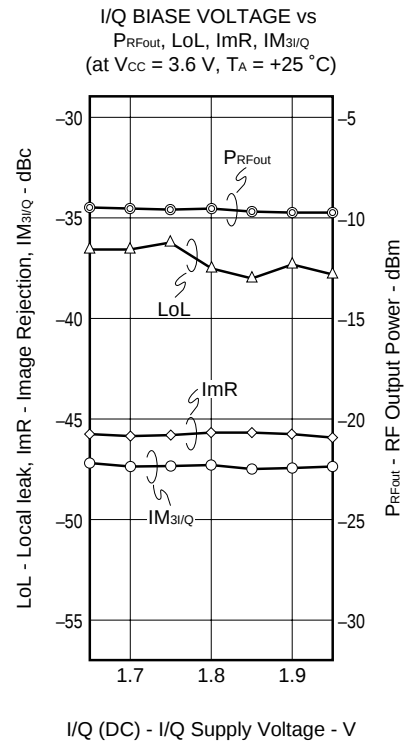
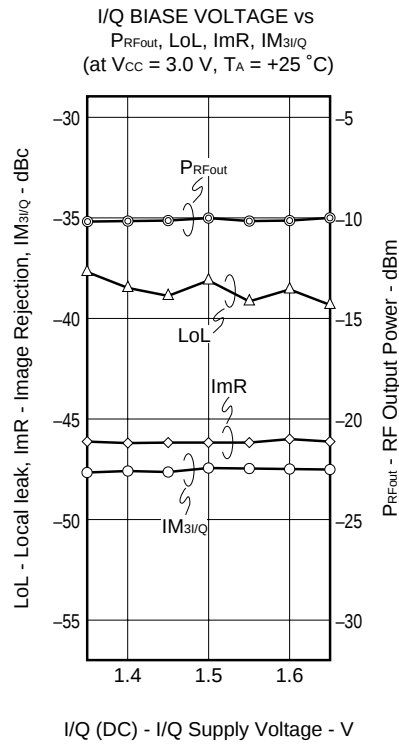
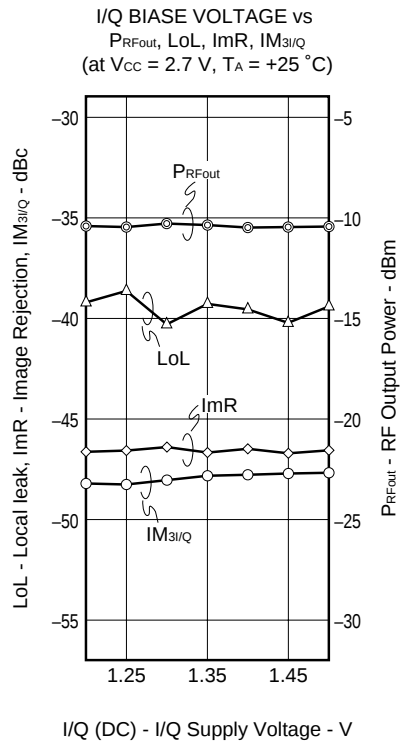
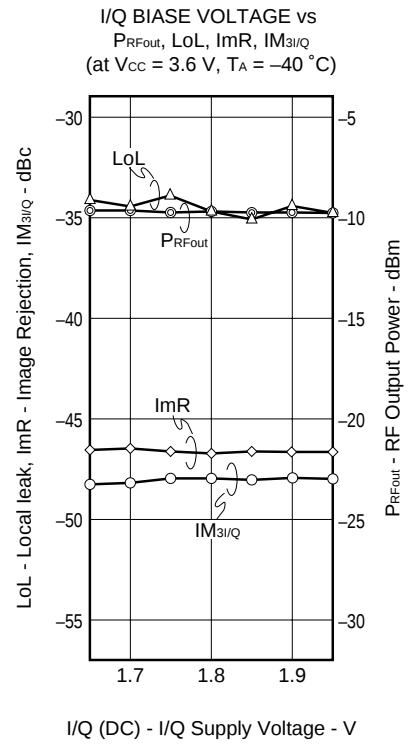
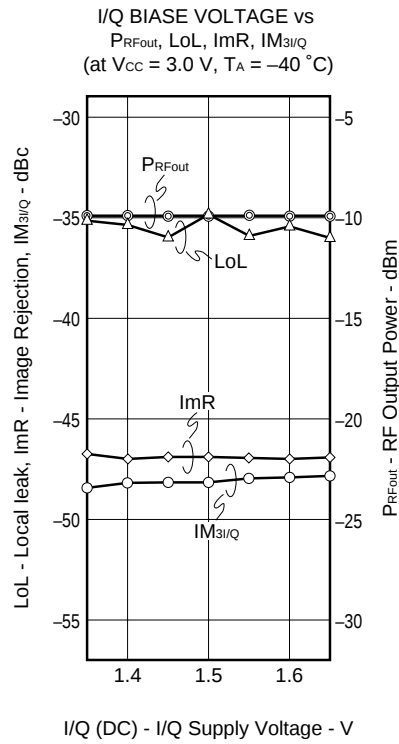
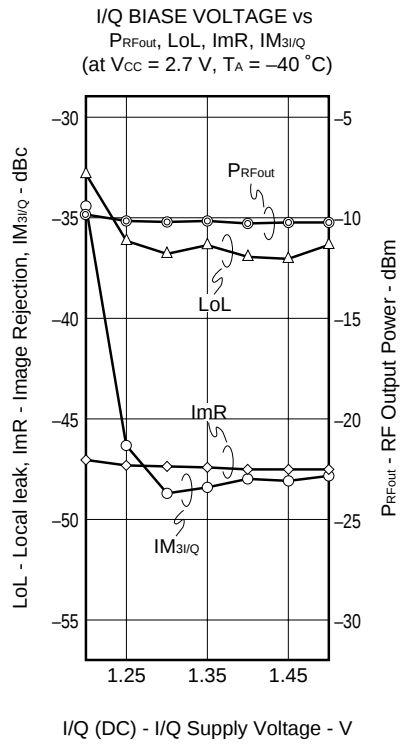


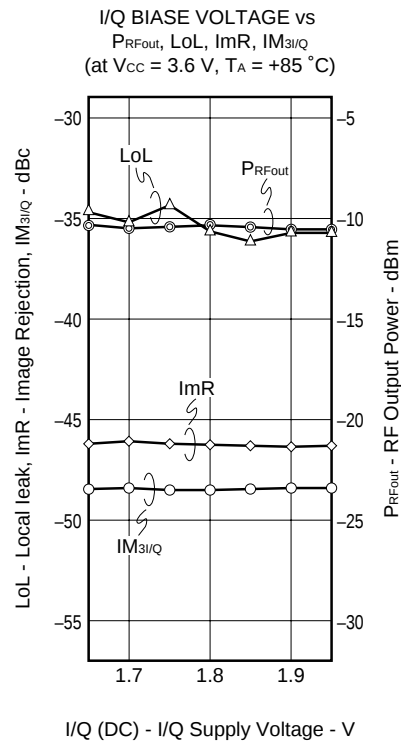
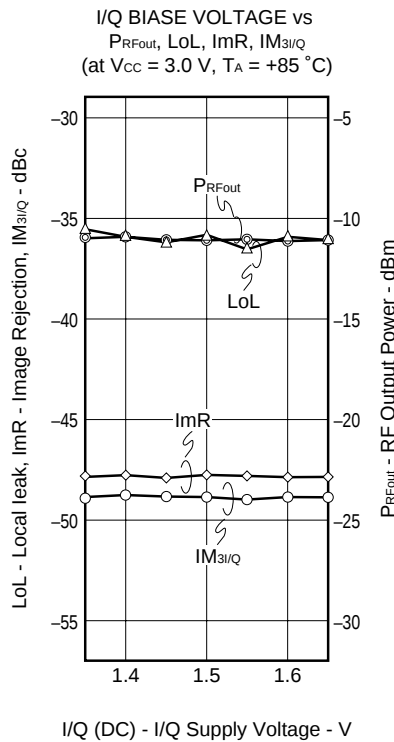
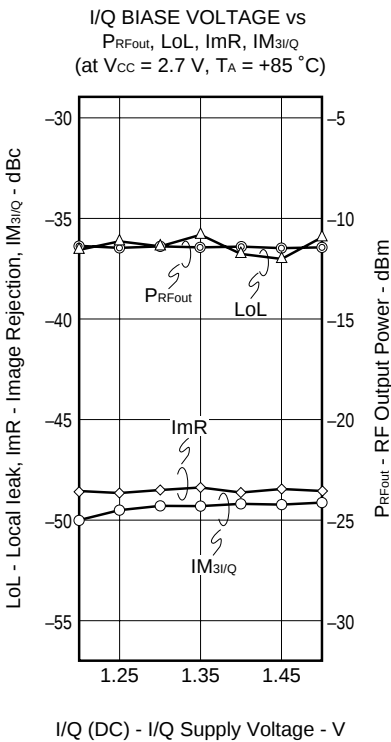
Lo - Local Input Power - dBm

Lo INPUT POWER vs
P_{RFout}, LoL, ImR, IM_{3/1Q}
(at V_{CC} = 3.6 V, T_A = +85 °C)

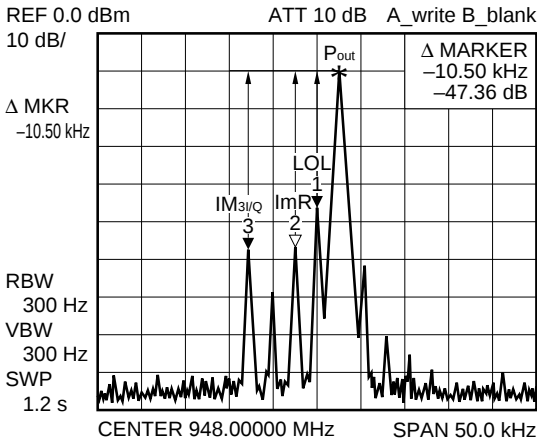


Lo - Local Input Power - dBm

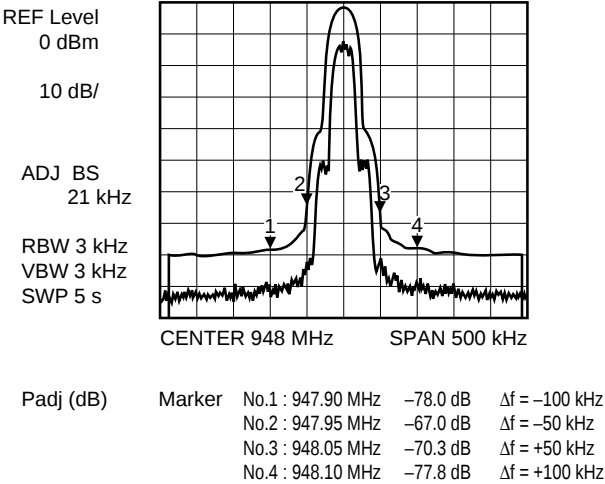




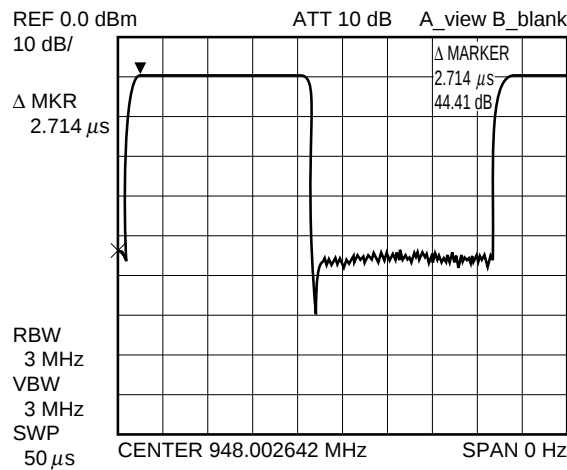
TYPICAL SINE WAVE MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ α = 0.5, MOD Pattern [0000]



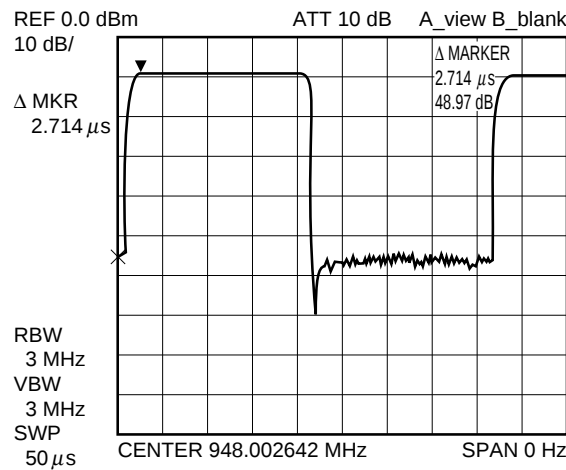
TYPICAL π/4DQPSK MODULATION OUTPUT SPECTRUM
<PDC> 42 kbps, RNYQ α = 0.5, MOD Pattern [PN9]



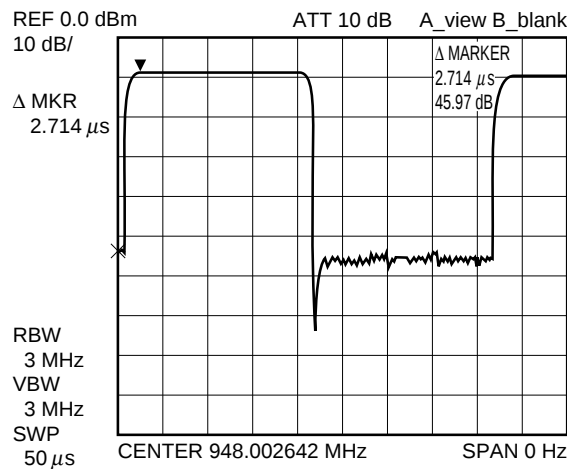
POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 2.7\text{ V}$)



POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.0\text{ V}$)

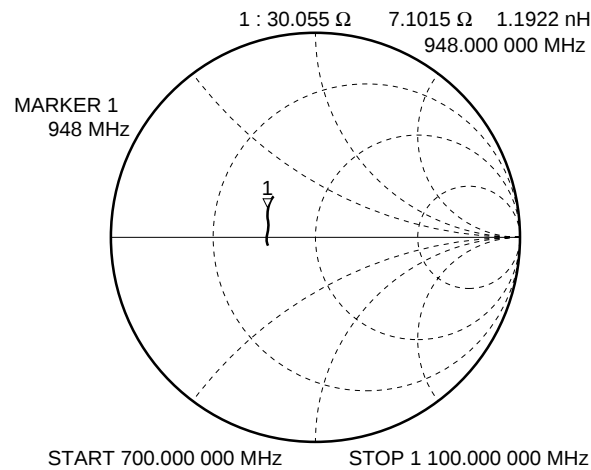


POWER SAVE RESPONSE
(at $V_{CC} = V_{PS} = 3.6\text{ V}$)

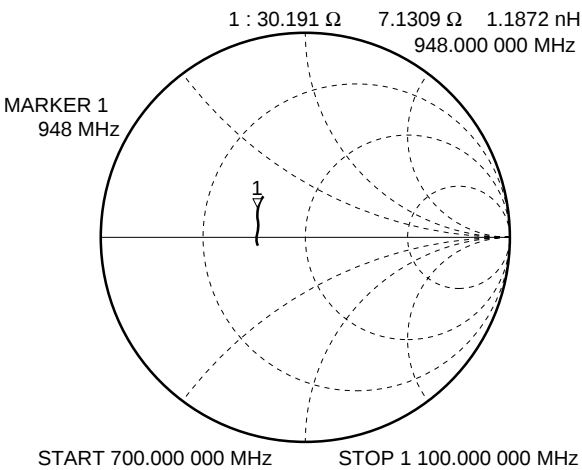


Lo INPUT (LoIn) IMPEDANCE

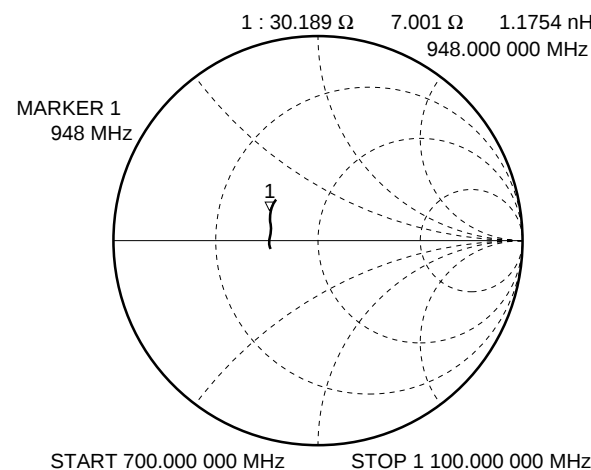
$V_{CC} = V_{PS} = 2.7\text{ V}$



$V_{CC} = V_{PS} = 3.0\text{ V}$

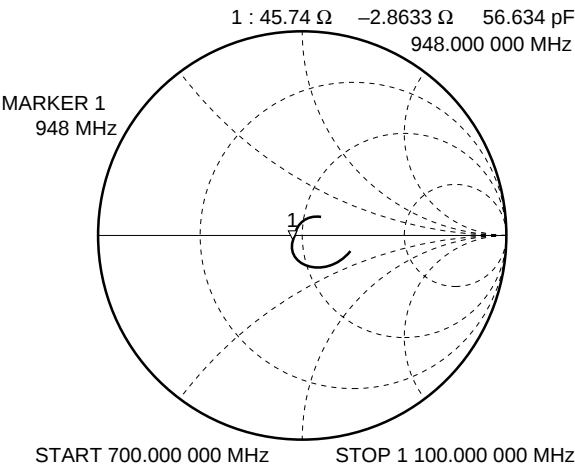


$V_{CC} = V_{PS} = 3.6\text{ V}$

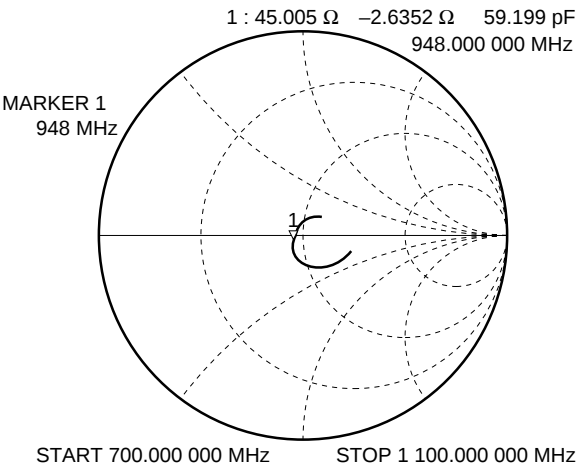


RF OUTPUT (RF_{out}) IMPEDANCE

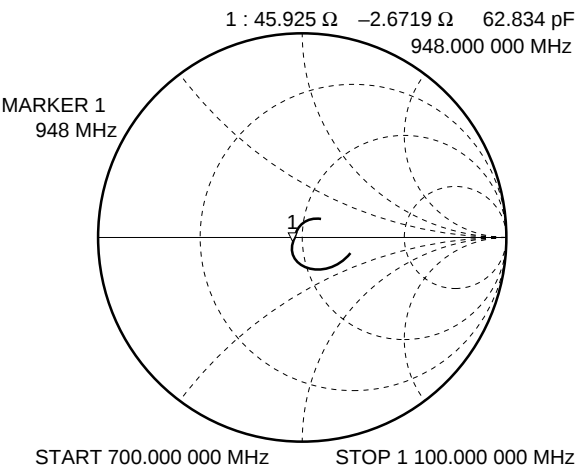
$V_{CC} = V_{PS} = 2.7\text{ V}$



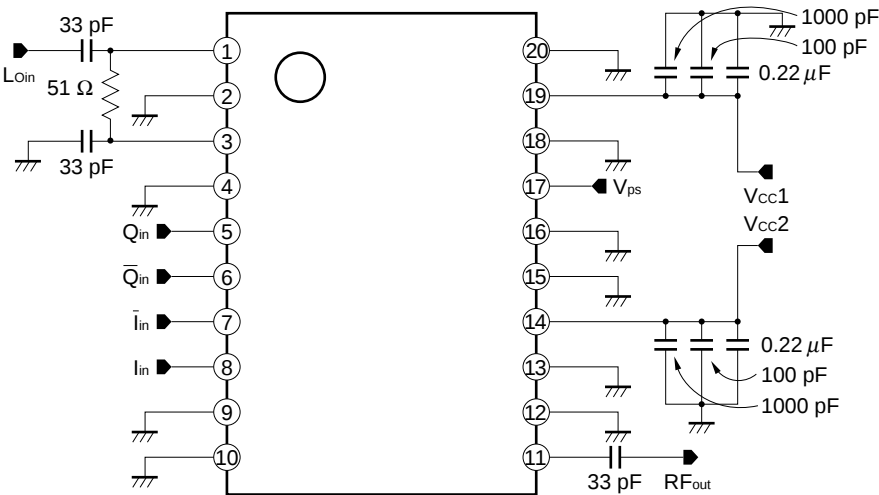
$V_{CC} = V_{PS} = 3.0\text{ V}$



$V_{CC} = V_{PS} = 3.6\text{ V}$

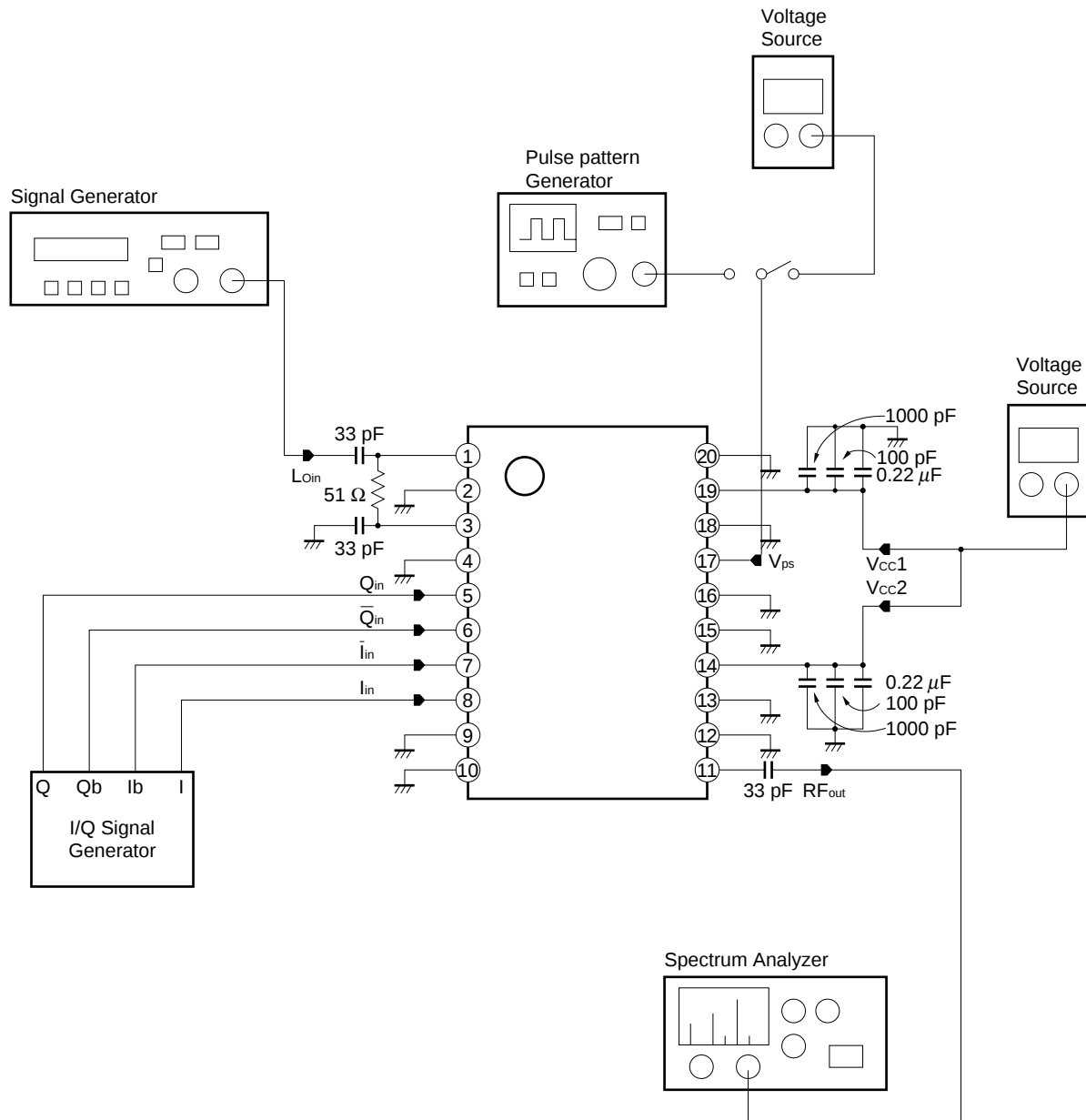


TEST CIRCUIT



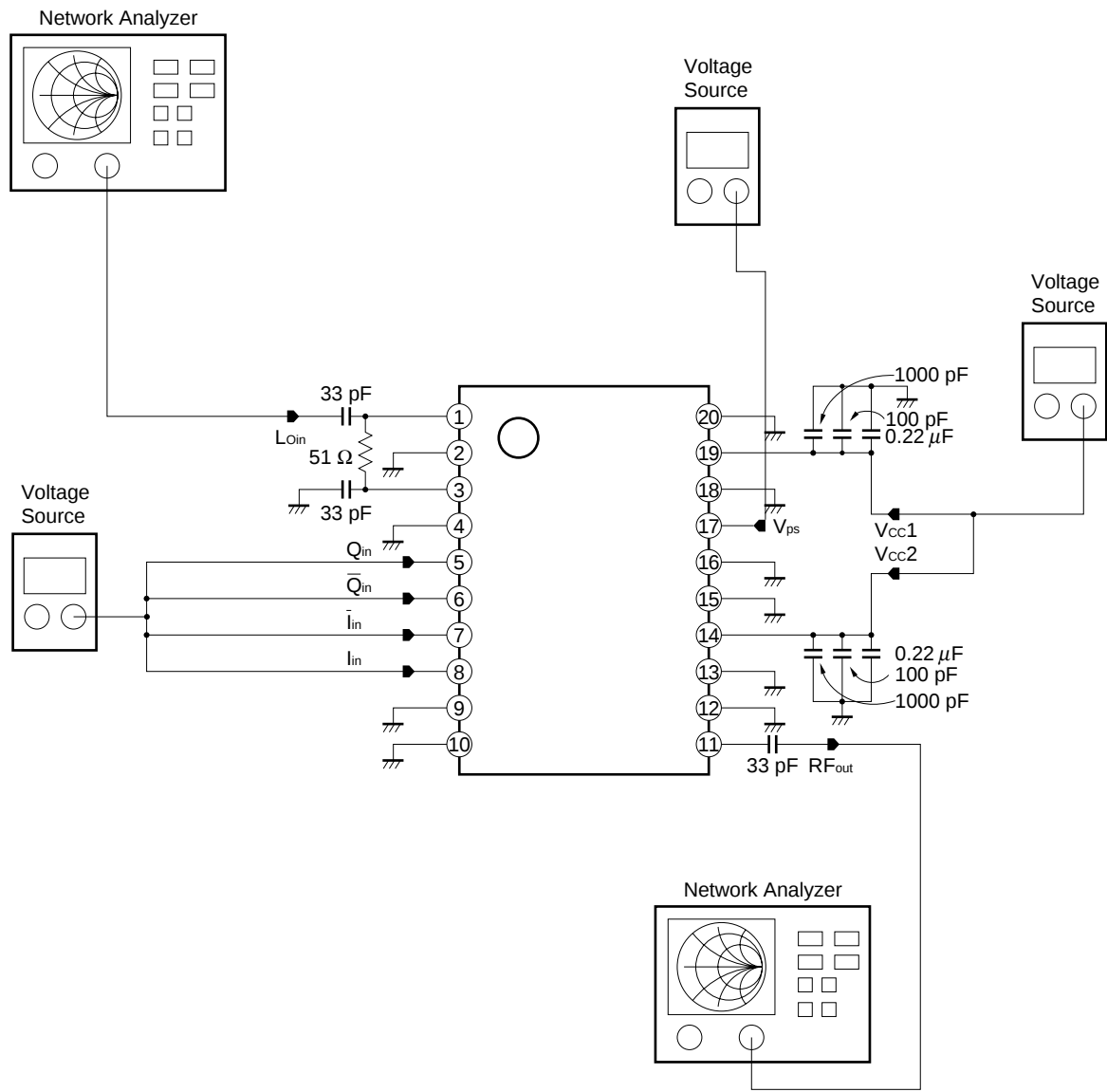
MEASUREMENT BLOCK DIAGRAM 1

(RF Output Power, Local Carrier Leak, Image Rejection, I/Q 3rd Order Intermodulation Distortion and Power Save Rise and Fall Time)

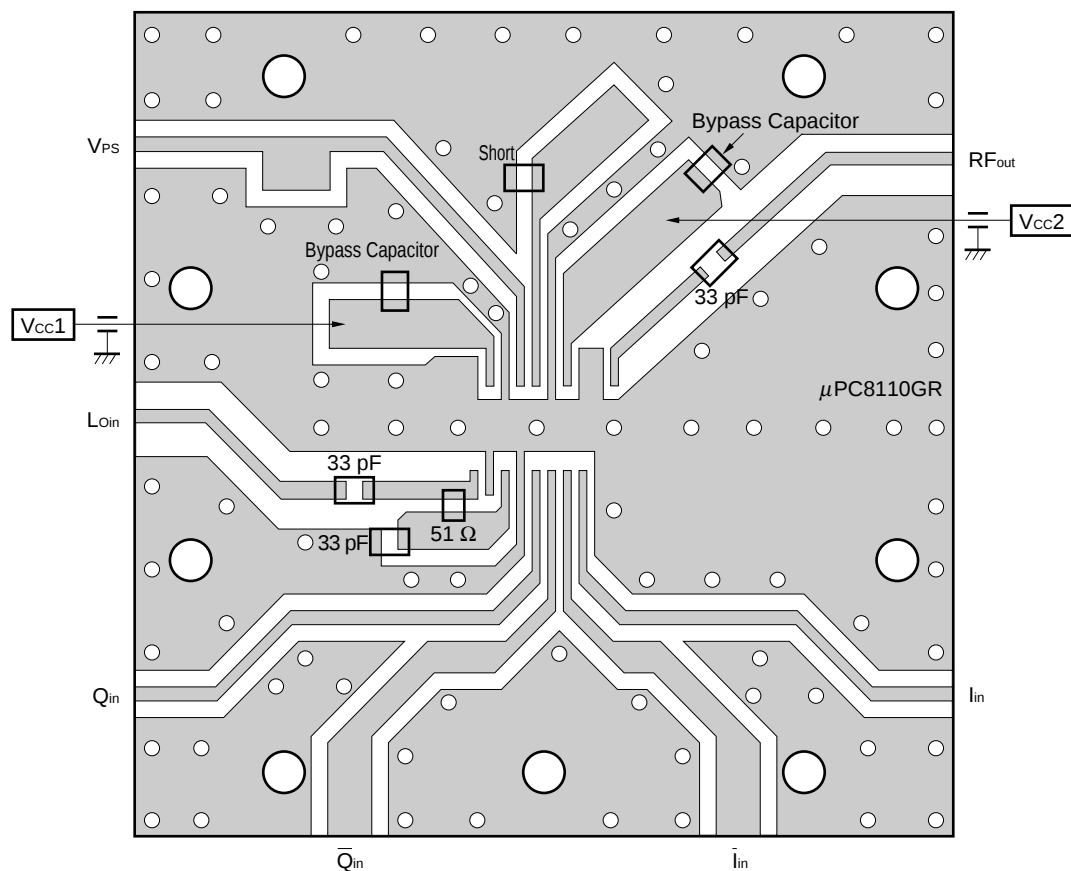


MEASUREMENT BLOCK DIAGRAM 2

(Local Input VSWR and RF Output VSWR)



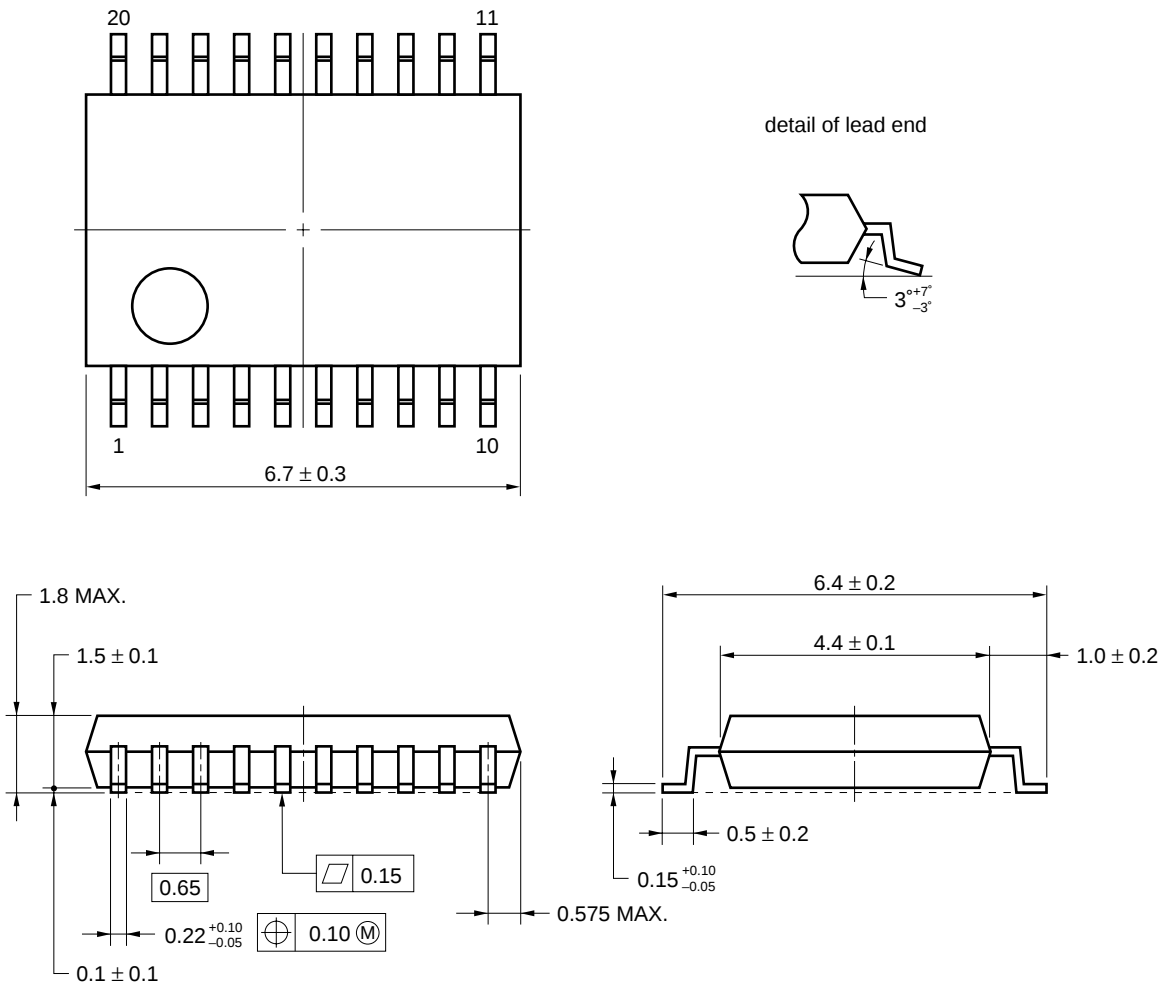
TEST BOARD



- Notes
1. Double-sided patterning with 35 μ m thick copper on polyimide board sizing 50 × 50 × 0.4 mm.
 2. GND pattern on backside.
 3. Solder coating over patterns.
 4. ○, ○ indicate through-holes.

PACKAGE DIMENSIONS

★ 20 PIN PLASTIC SSOP (225 mil) (UNIT: mm)



NOTE Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electrostatic sensitive devices.
- (2) Form a ground pattern as wide as possible to keep the minimum ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.x. 1 000 pF) to the V_{CC} pin.
- (5) I, Q DC offset voltage should be same as the I, Q DC offset voltage (to prevent changing the local leak level with power save control.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering method and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC8110GR

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit ^{Note} : None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit ^{Note} : None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit ^{Note} : None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 3 seconds/pin or below, Exposure limit ^{Note} : None	

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Apply only a single process at once, except for "Partial heating method".

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

[MEMO]

[MEMO]

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