

NEC**BIPOLAR ANALOG INTEGRATED CIRCUITS** **μ PC8130TA, μ PC8131TA****-15 dBm INPUT, VARIABLE GAIN AMPLIFIER SILICON MMIC
FOR TRANSMITTER AGC OF DIGITAL CELLULAR TELEPHONE****DESCRIPTION**

The μ PC8130TA and μ PC8131TA are silicon monolithic integrated circuits designed as variable gain amplifier. Due to 800 MHz to 1.5 GHz operation, these ICs are suitable for RF transmitter AGC stage of digital cellular telephone. These ICs are lower distortion than conventional μ PC8119T and μ PC8120T so that -15 dBm input level can be applied. These ICs also available in two types of gain control so you can choose either IC in accordance with your system design. 3 V supply voltage and minimold package contribute to make your system lower voltage, decreased space and fewer components.

The μ PC8130TA and μ PC8131TA are manufactured using NEC's 20 GHz fr NESAT™III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Recommended operating frequency: $f = 800 \text{ MHz to } 1.5 \text{ GHz}$
- Low distortion : $P_{adj} \leq -60 \text{ dBc MAX. @ } P_{in} = -15 \text{ dBm, } \Delta f = \pm 50 \text{ kHz, } V_{CC} = 3.0 \text{ V, } T_A = +25^\circ \text{C}$
- Supply voltage : $V_{CC} = 2.7 \text{ to } 3.3 \text{ V}$
- Low current consumption : $I_{CC} = 11 \text{ mA TYP. @ } V_{CC} = 3.0 \text{ V}$
- Gain control voltage : $V_{AGC} = 0 \text{ to } 2.4 \text{ V (recommended)}$
- Two types of gain control : μ PC8130TA = V_{AGC} up vs. Gain up (Reverse control)
 μ PC8131TA = V_{AGC} up vs. Gain down (Forward control)
- AGC control can be constructed by external control circuit.
- High-density surface mounting : 6 pin minimold package

APPLICATION

- 800 MHz to 900 MHz or 1.5 GHz Digital cellular telephone (PDC800M, PDC1.5G and so on)

ORDERING INFORMATION

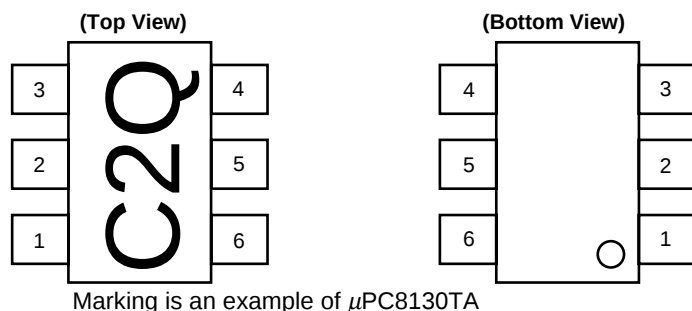
Part Number	Package	Marking	Supplying Form	Gain Control Type
μ PC8130TA-E3	6-pin minimold	C2Q	Embossed tape 8 mm wide. 1, 2, 3 pins face to perforation side of the tape. Qty 3 kp/reel.	Reverse control
μ PC8131TA-E3		C2R		Forward control

Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μ PC8130TA, μ PC8131TA)

Caution Electro-static sensitive devices.



PIN CONNECTIONS



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	V _{CC}
6	V _{AGC}

GAIN CONTROL AMPLIFIER PRODUCT LINE-UP

Part No.	V _{CC} (V)	I _{CC} (mA)	V _{AGC} (V)	V _{AGC} up vs. Gain	f (GHz)	P _O (1 dB)	P _{in} (dBm)	Features
μ PC2723T	4.5 to 5.5	15	3.3 to 5.0	down	up to 1.1	-4	-	
μ PC8119T	2.7 to 3.3	11	0.6 to 2.4	down	0.1 to 1.92	+3	≤ -18	PHS, PDC
μ PC8120T	2.7 to 3.3	11	0.6 to 2.4	up	0.1 to 1.92	+3	≤ -18	PHS, PDC
μ PC8130TA	2.7 to 3.3	11	0.6 to 2.4	up	0.8 to 1.5	+5	≤ -15	PDC 800 M, PDC 1.5 G
μ PC8131TA	2.7 to 3.3	11	0 to 2.4	down	0.8 to 1.5	+5	≤ -15	PDC 800 M, PDC 1.5 G

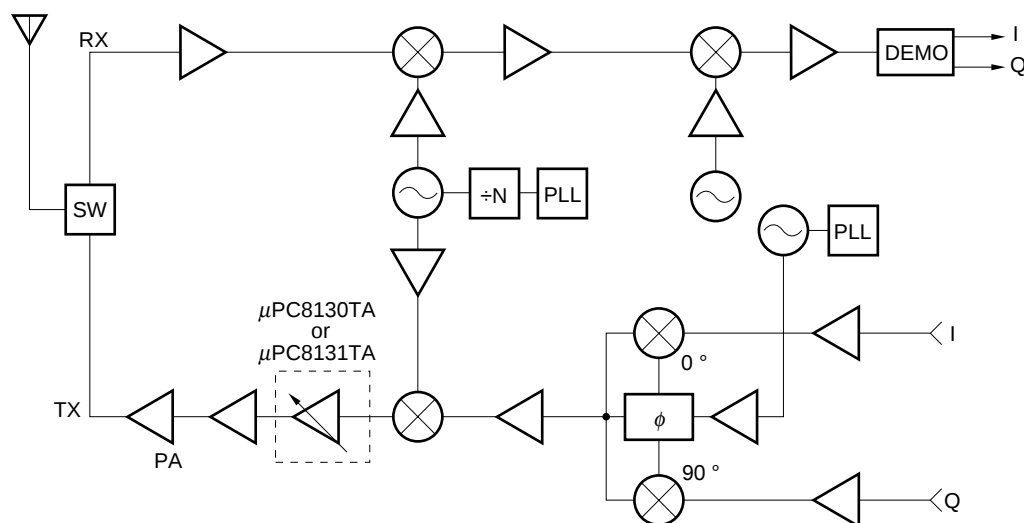
Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

To know the associated product, please refer to each latest data sheet.

SYSTEM APPLICATION EXAMPLE

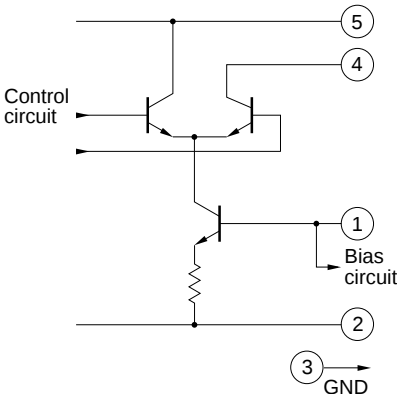
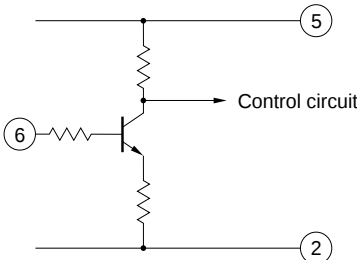
This block diagram is an example of IF modulation digital cellular system.

The μ PC8130TA and μ PC8131TA are applicable for not only IF modulation system but also RF modulation system. This diagram is intended to show the μ PC8130TA and μ PC8131TA location in the systems.



This document is to be specified for μ PC8130TA and μ PC8131TA only. For the other part number mentioned in this document, please refer to the latest data sheet of each part number.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage V	Pin Voltage V ^{Note}	Function and Applications	Internal Equivalent Circuit						
1	IN	—	1.4	RF input pin. This pin should be coupled with capacitor (eg 1000 pF) for DC cut. Input return loss can be improved with external impedance matching circuit.							
2 3	GND	0	—	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. Ground pins must be connected together with wide ground pattern to decrease impedance difference.							
4	OUT	voltage as same as V _{CC} through external inductor	—	RF output pin. This pin is designed as open collector of high impedance. This pin must be externally equipped with matching circuits.							
5	V _{CC}	2.7 to 3.3	—	Supply voltage pin. This pin must be equipped with bypass capacitor (eg 1000 pF) to minimize its RF impedance.							
6	V _{AGC}	0 to 3.3	—	Gain control pin. The relation between product number and control performance is shown below; <table border="1" data-bbox="693 1344 1040 1484"><thead><tr><th>Part No.</th><th>V_{AGC} up vs. Gain</th></tr></thead><tbody><tr><td>μPC8130TA</td><td>up</td></tr><tr><td>μPC8131TA</td><td>down</td></tr></tbody></table>	Part No.	V _{AGC} up vs. Gain	μPC8130TA	up	μPC8131TA	down	
Part No.	V _{AGC} up vs. Gain										
μPC8130TA	up										
μPC8131TA	down										

Note Pin voltage is measured at V_{CC} = 3.0 V.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	$T_A = +25\text{ }^{\circ}\text{C}$, Pin 4 and 5	3.6	V
Total Circuit Current	I_{CC}	$T_A = +25\text{ }^{\circ}\text{C}$, Pin 4 and 5	30	mA
Input Power	P_{in}	$T_A = +25\text{ }^{\circ}\text{C}$	+10	dBm
Gain Control Voltage	V_{AGC}	$T_A = +25\text{ }^{\circ}\text{C}$	3.6	V
Operating Ambient Temperature	T_A		–25 to +85	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		–55 to +150	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V_{CC}	2.7	3.0	3.3	V	Same voltage should be applied to 4 and 5 pins.
Gain Control Voltage	V_{AGC}	0	–	2.4	V	$-0.5 \leq I_{AGC} \leq 0.1\text{ mA}$
Input Level	P_{in}	–	–	–15	dBm	$P_{adj} \leq -60\text{ dBc}$ @ $\Delta f = \pm 50\text{ kHz}$ ^{Note}
Operating Ambient Temperature	T_A	–25	+25	+85	$^{\circ}\text{C}$	
Operating Frequency	f	800	–	1500	MHz	With external output-matching
AGC Pin Drive Current	I_{AGC}	0.5	–	–	mA	$V_{AGC} \leq 3.3\text{ V}$

Note Adjacent Channel Interference (P_{adj}) wave form condition: $\pi/4$ DQPSK modulation signal, data rate = 42 kbps, rolloff ratio = 0.5, PN9 bits (pseudorandom pattern)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = V_{out} = 3.0\text{ V}$, $Z_S = Z_L = 50\text{ }\Omega$, External matched output port)

Parameter	Symbol	Test Conditions	μ PC8130TA			μ PC8131TA			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Circuit Current	I_{CC}	No signal, $I_{CC} = I_{VCC} + I_{out}$	8.5	11	15	8.5	11	15	mA
Maximum Power Gain	G_{PMAX}	$f = 950\text{ MHz}$, $P_{in} = -20\text{ dBm}$	10	12.5	15	9.5	12	14.5	dB
		$f = 1440\text{ MHz}$, $P_{in} = -20\text{ dBm}$	8	11	14	8	11	14	
Gain Control Range ^{Note1}	GCR	$f = 950\text{ MHz}$, $P_{in} = -20\text{ dBm}$	40	50	–	40	45	–	dB
		$f = 1440\text{ MHz}$, $P_{in} = -20\text{ dBm}$	35	41	–	35	39	–	
Minimum Power Gain	G_{PMIN}	$f = 950\text{ MHz}$, $P_{in} = -20\text{ dBm}$	–	–37	–	–	–33	–	dB
		$f = 1440\text{ MHz}$, $P_{in} = -20\text{ dBm}$	–	–30	–	–	–28	–	
Adjacent Channel Interference (@ $\Delta f = \pm 50\text{ kHz}$ ^{Note2})	P_{adj}	$f = 950\text{ MHz}$, $P_{in} = -15\text{ dBm}$	–	–65	–60	–	–65	–60	dB
		$f = 1440\text{ MHz}$, $P_{in} = -15\text{ dBm}$	–	–65	–60	–	–65	–60	
Isolation	ISL	$f = 950\text{ MHz}$, G_{PMAX}	17	20	–	20	25	–	dB
		$f = 1440\text{ MHz}$, G_{PMAX}	20	25	–	25	30	–	
1 dB Compression Output Power	$P_O (1\text{ dB})$	$f = 950\text{ MHz}$, G_{PMAX}	+2	+5	–	+2	+5	–	dBm
		$f = 1440\text{ MHz}$, G_{PMAX}	+2	+5	–	+1	+4	–	
Input Return Loss	RL_{in}	$f = 950\text{ MHz}$, G_{PMAX}	3.5	6.5	–	6	9	–	dB
		$f = 1440\text{ MHz}$, G_{PMAX}	6.5	10	–	7	10.5	–	
Noise Figure	NF	$f = 950\text{ MHz}$, G_{PMAX}	–	11	14	–	11	14	dB
		$f = 1440\text{ MHz}$, G_{PMAX}	–	8.5	11.5	–	8	11	

Notes 1. Gain Control Range (GCR) specification: $GCR = G_{PMAX} - G_{PMIN}$ (dB)

Conditions μ PC8130TA: $G_{PMAX}@ V_{AGC} = V_{CC}$, $G_{PMIN}@ V_{AGC} = 0\text{ V}$

μ PC8131TA: $G_{PMAX}@ V_{AGC} = 0\text{ V}$, $G_{PMIN}@ V_{AGC} = V_{CC}$

2. Adjacent Channel Interference (P_{adj}) wave form condition: $\pi/4$ DQPSK modulation signal, data rate = 42 kbps, rolloff ratio = 0.5, PN9 bits (pseudorandom pattern)

Remark Measured on TEST CIRCUIT 1 and 2

TEST CIRCUIT1 (f = 950 MHz, both products in common)

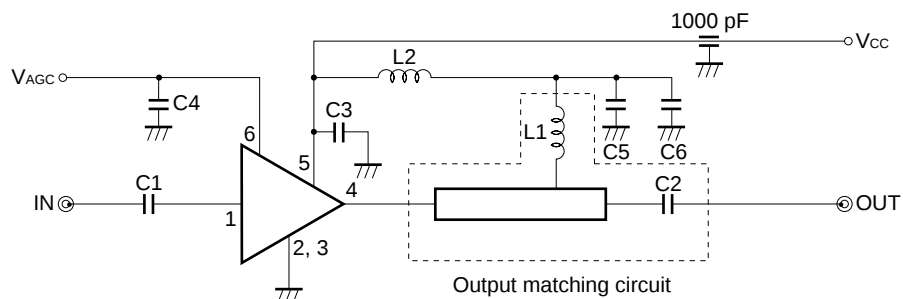
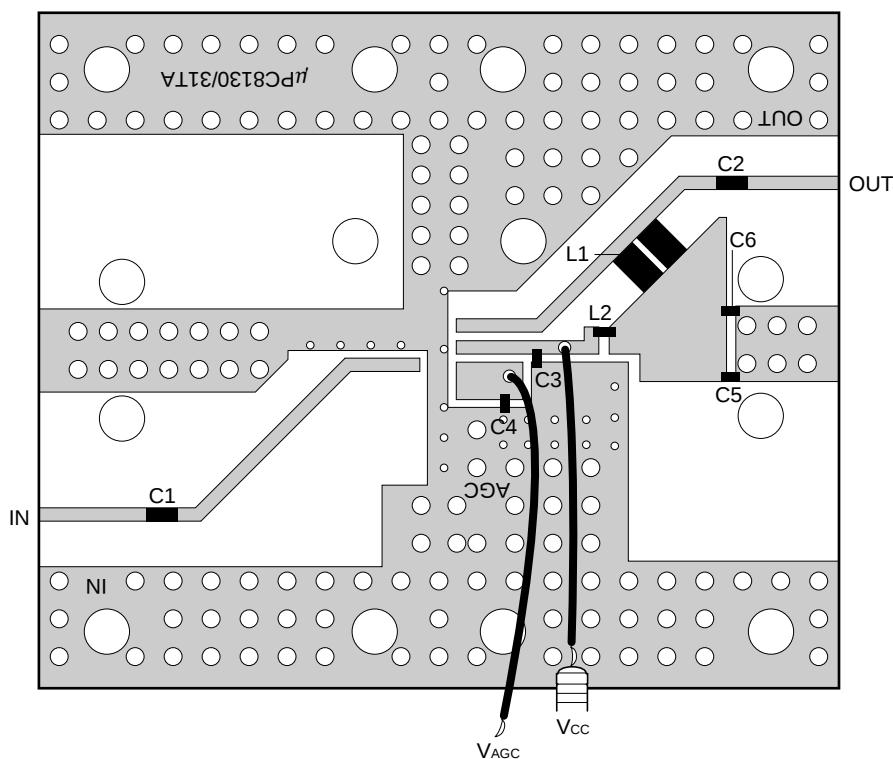


ILLUSTRATION OF TEST CIRCUIT1 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

Form	Symbol	Value	Makers	Product Name
Chip capacitor	C1, C3 to C6	1000 pF	Murata Mfg. Co., Ltd.	GRM39 series
	C2	1.5 pF	Murata Mfg. Co., Ltd.	GRM39 series
Chip inductor	L1	4.5 nH (10 nH, 8.2 nH, parallel)	Toko Co., Ltd.	LL1608-F
	L2	270 nH	Toko Co., Ltd.	LL2012-F

Caution Test circuit or print pattern in this sheet is for testing IC characteristics.

In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

TEST CIRCUIT2 (f = 1440 MHz, both products in common)

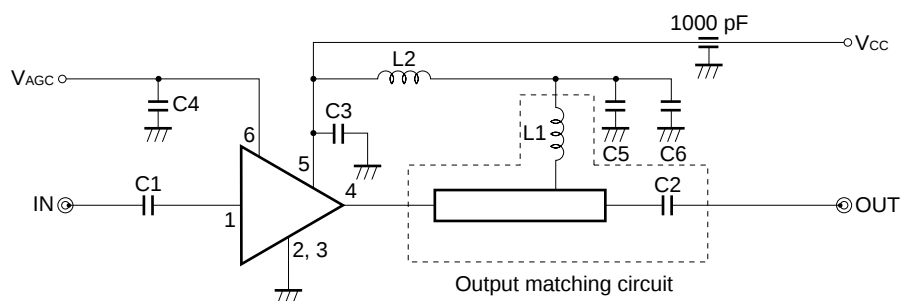
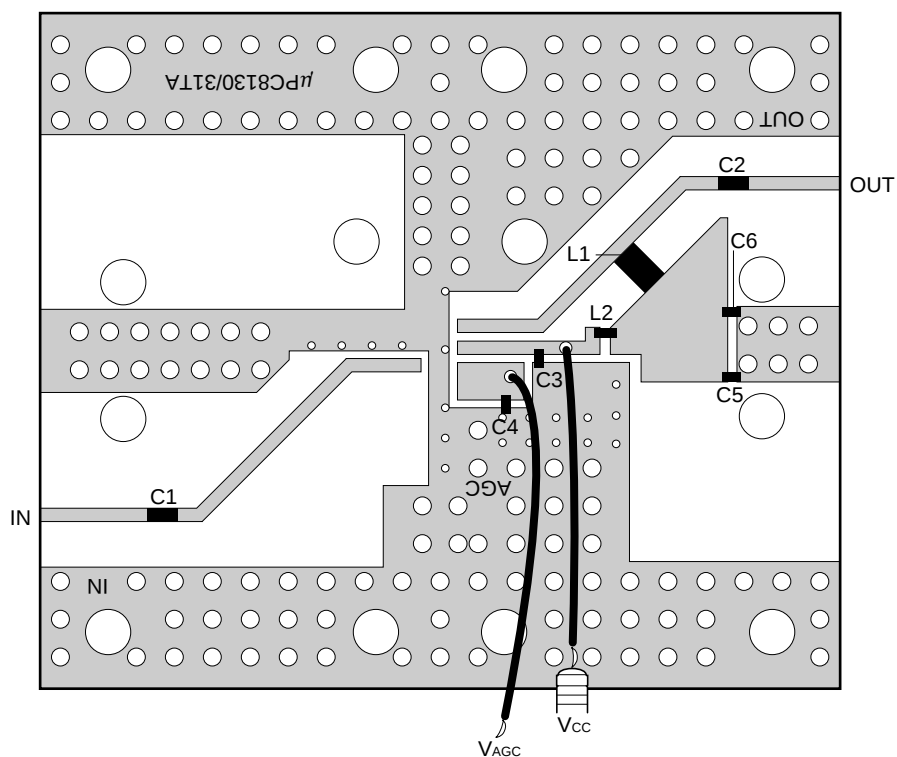


ILLUSTRATION OF TEST CIRCUIT2 ASSEMBLED ON EVALUATION BOARD



COMPONENT LIST

Form	Symbol	Value	Makers	Product Name
Chip capacitor	C1, C3 to C6	1000 pF	Murata Mfg. Co., Ltd.	GRM39 series
	C2	1.5 pF	Murata Mfg. Co., Ltd.	GRM39 series
Chip inductor	L1	1.2 nH	Toko Co., Ltd.	LL1608-F
	L2	270 nH	Toko Co., Ltd.	LL2012-F

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In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

APPLICATION EXPLANATION

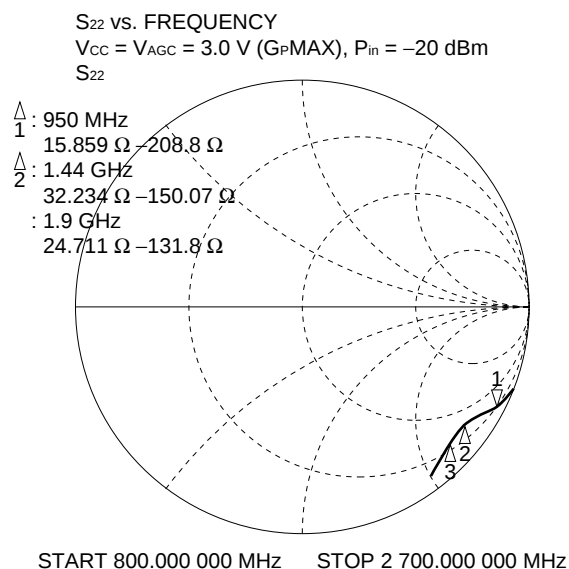
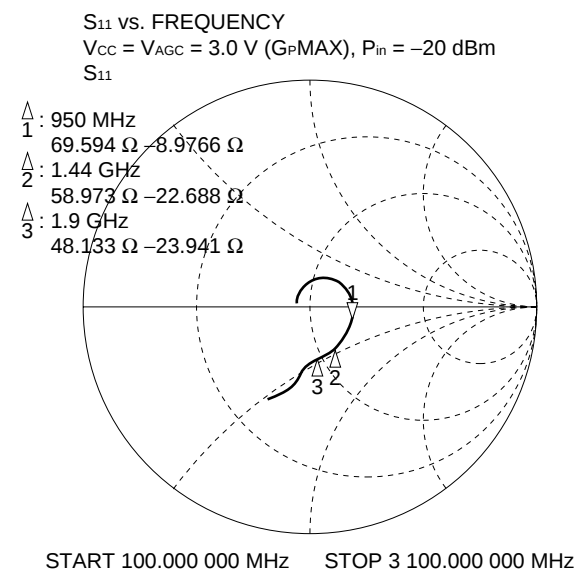
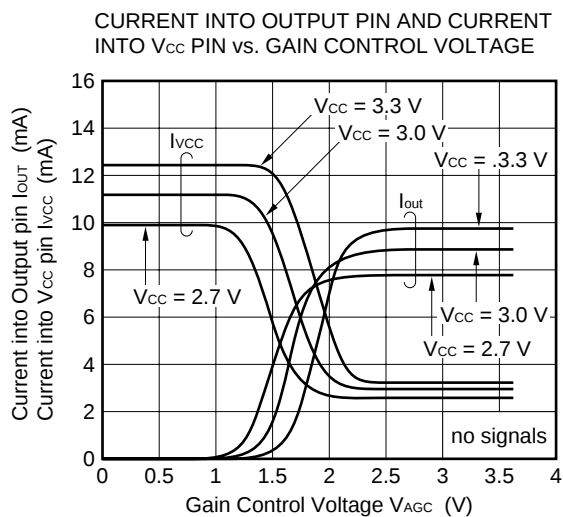
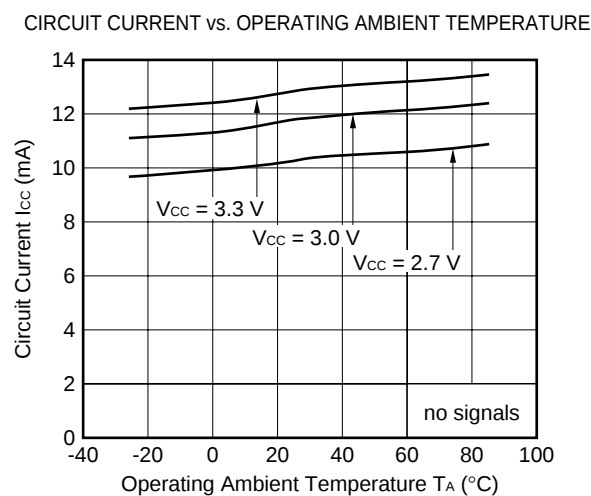
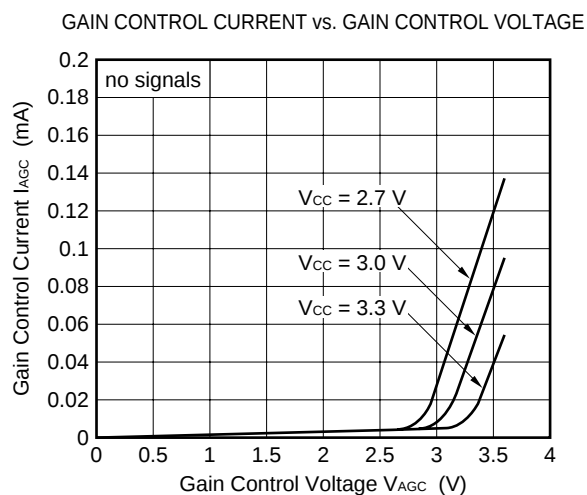
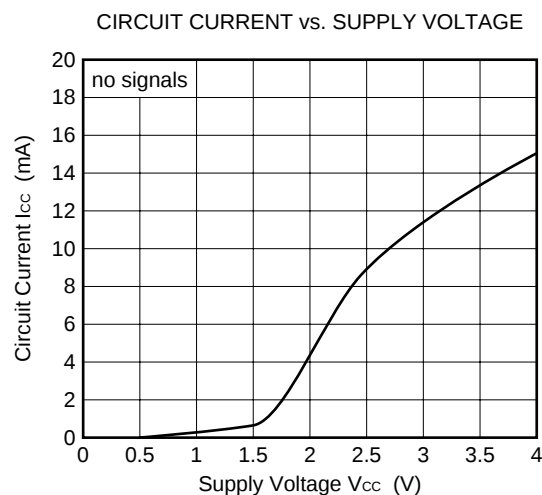
The μ PC8130TA and μ PC8131TA has difference in internal circuit in order to reduce the number of external component with μ PC8119T and μ PC8120T. For this reason, they have difference in mechanism for determining minimum gain and external suitable constant.

	Determining Minimum Gain	External Feedback Capacitor of V_{CC} to V_{AGC} Pin	Optimize Choke Inductance of π Type Circuit on V_{CC} Line
μ PC8119T μ PC8120T	High frequency negative feed back between OUT, V_{CC} and V_{AGC} pin optimized by external choke inductance.	Necessary	The impedance of inductance should be very low at high frequency region.
μ PC8130TA μ PC8131TA	Isolation of V_{CC} to OUT pin optimized by external choke inductance.	Unnecessary	The impedance of inductance should be very high at high frequency region.



TYPICAL CHARACTERISTICS

μ PC8130TA

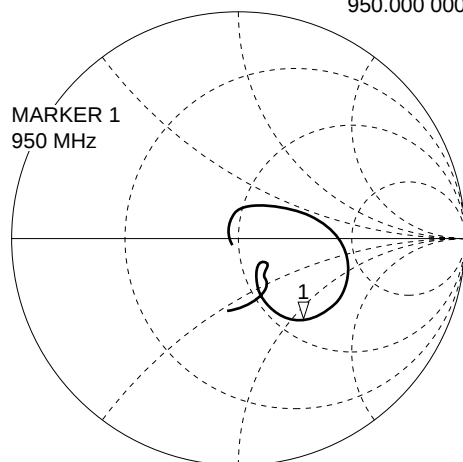


μ PC8130TA

Output port matching at $f = 950$ MHz

$V_{CC} = V_{AGC} = 3.0$ V(GP MAX), $P_{in} = -20$ dBm

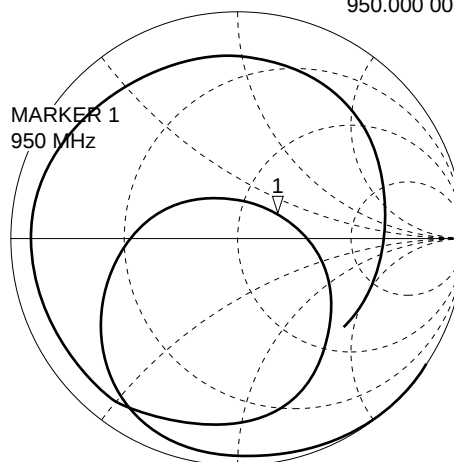
S_{11} vs. FREQUENCY 1: 65.098 Ω -56.266 Ω 2.9775 pF
950.000 000 MHz



START 100.000 000 MHz STOP 3 100.000 000 MHz

$V_{CC} = V_{AGC} = 3.0$ V(GP MAX), $P_{in} = -20$ dBm

S_{22} vs. FREQUENCY 1: 69.219 Ω 13.313 Ω 2.2303 nH
950.000 000 MHz

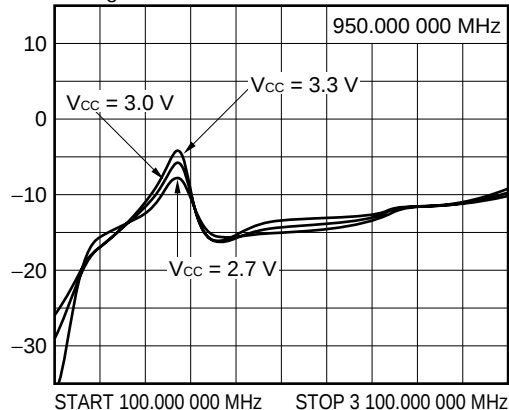


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY

$V_{AGC} = V_{CC}$ (GP MAX), $P_{in} = -20$ dBm

S_{11} log MAG 5 dB/REF 0 dB 1: -6.8118 dB

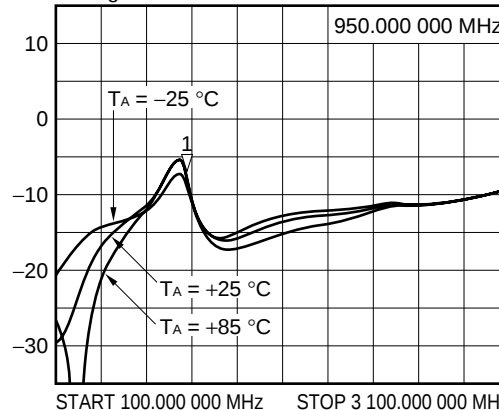


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY

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S_{11} log MAG 5 dB/REF 0 dB 1: -5.9537 dB

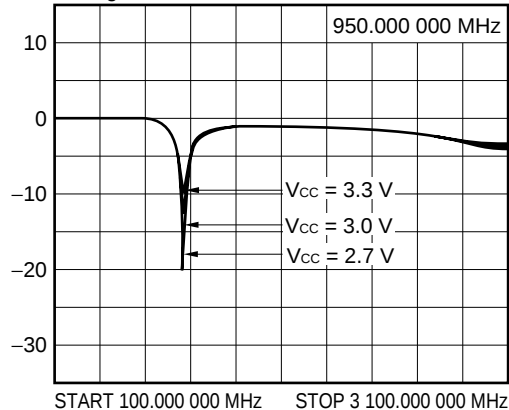


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY

$V_{AGC} = V_{CC}$ (GP MAX), $P_{in} = -20$ dBm

S_{22} log MAG 5 dB/REF 0 dB 1: -13.235 dB

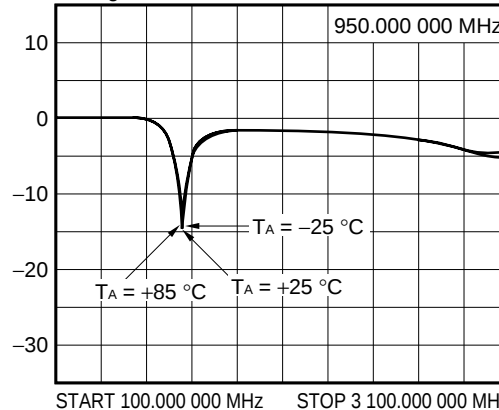


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY

$V_{CC} = V_{AGC} = 3.0$ V(GP MAX), $P_{in} = -20$ dBm

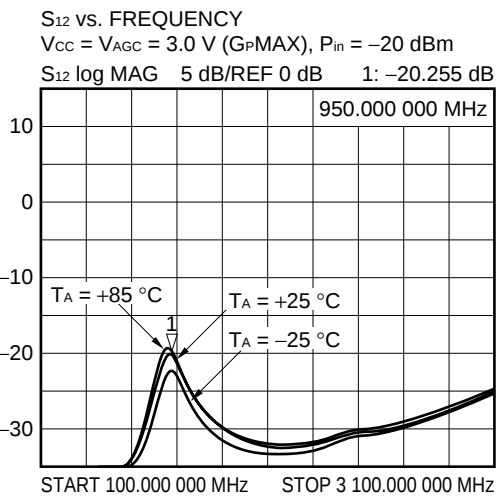
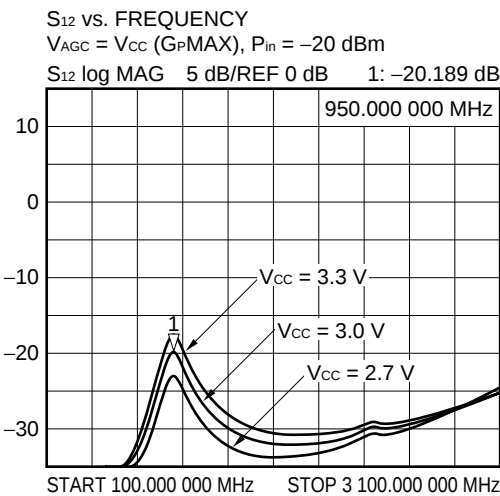
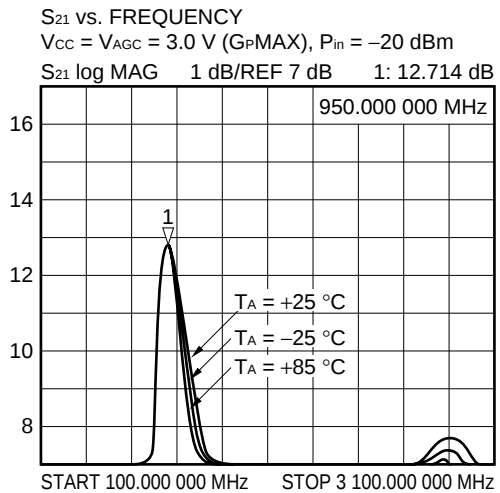
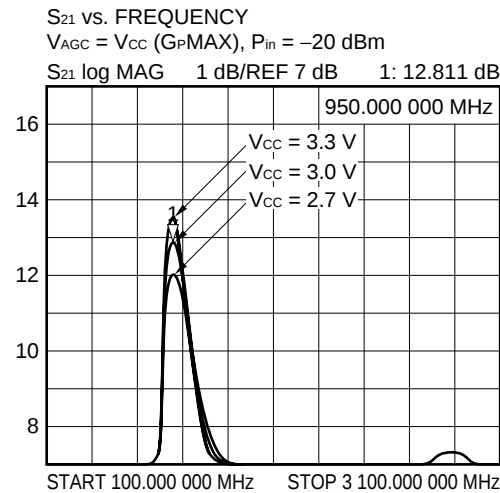
S_{22} log MAG 5 dB/REF 0 dB 1: -12.477 dB



START 100.000 000 MHz STOP 3 100.000 000 MHz

μ PC8130TA

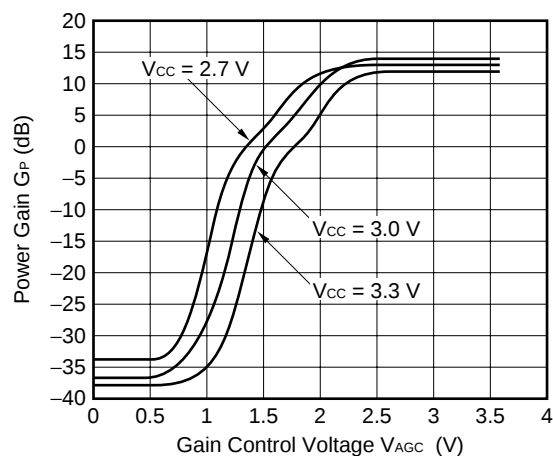
Output port matching at f = 950 MHz



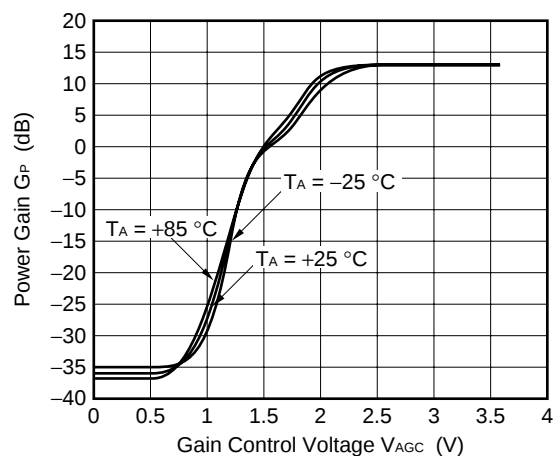
μ PC8130TA

Output port matching at $f = 950$ MHz

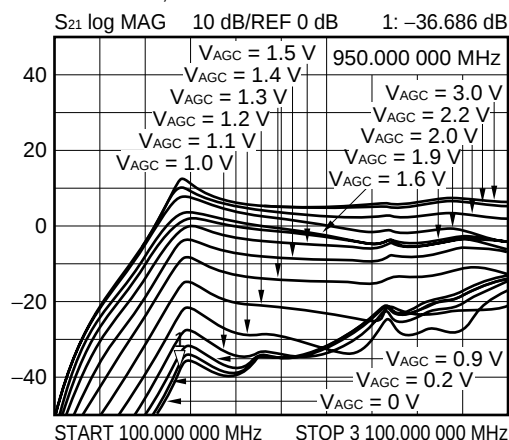
POWER GAIN vs. GAIN CONTROL VOLTAGE



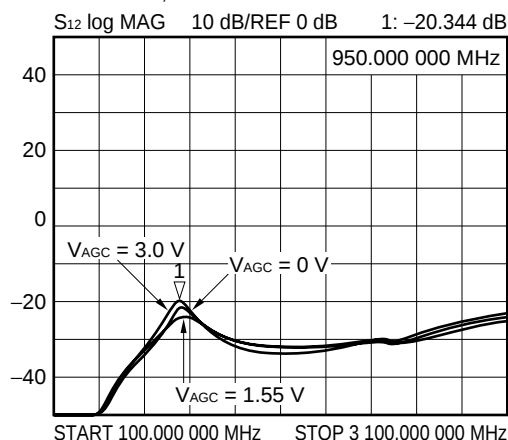
POWER GAIN vs. GAIN CONTROL VOLTAGE



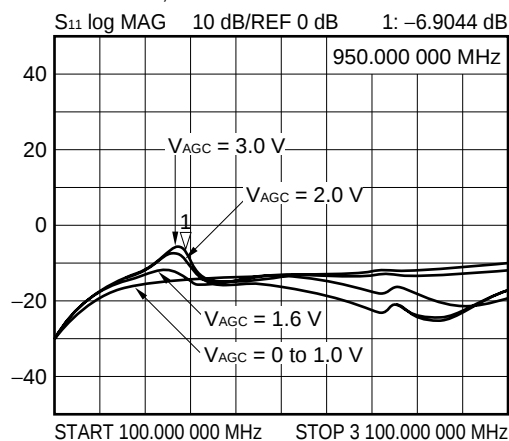
S_{21} vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE
 $V_{CC} = 3.0$ V, $P_{in} = -20$ dBm



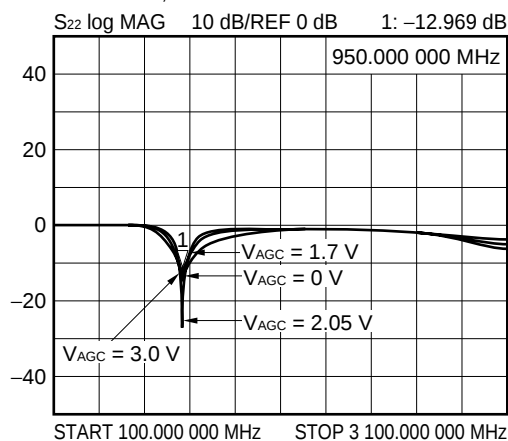
S_{12} vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE
 $V_{CC} = 3.0$ V, $P_{in} = -20$ dBm



S_{11} vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE
 $V_{CC} = 3.0$ V, $P_{in} = -20$ dBm

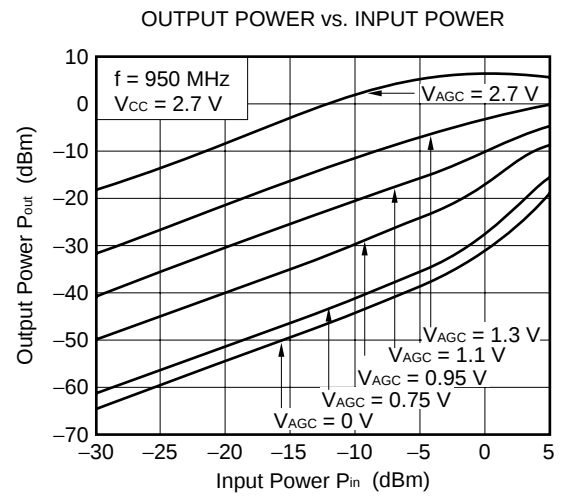
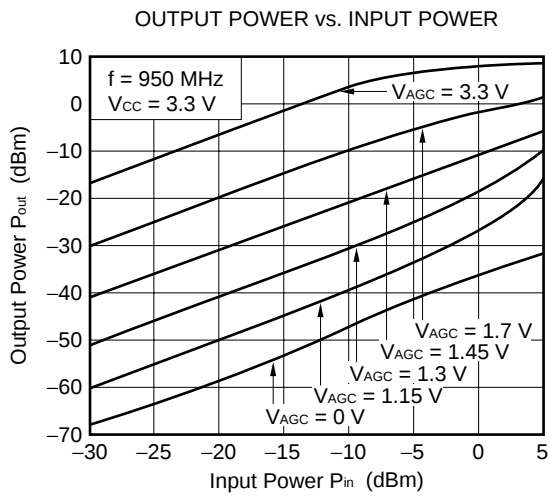
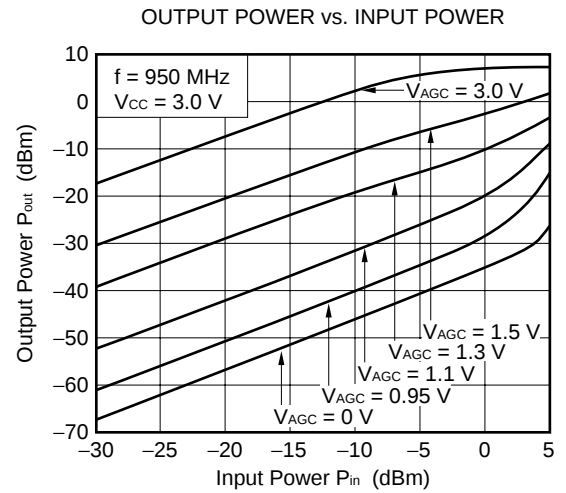
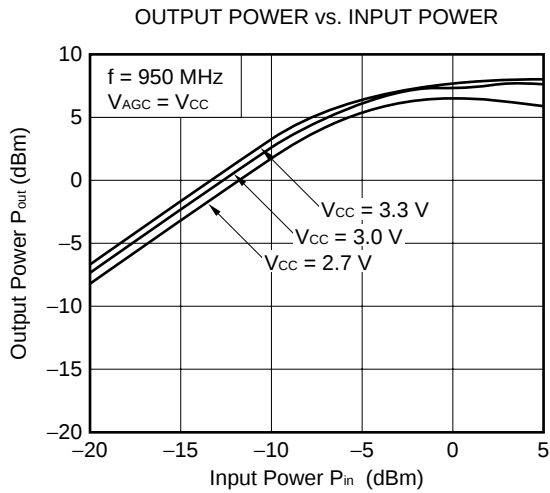


S_{22} vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE
 $V_{CC} = 3.0$ V, $P_{in} = -20$ dBm



μ PC8130TA

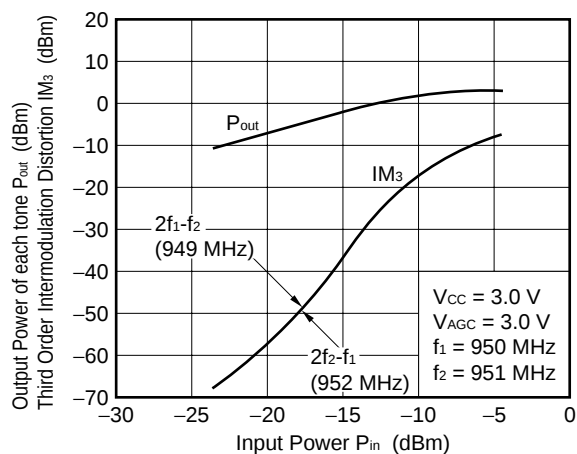
Output port matching at $f = 950$ MHz



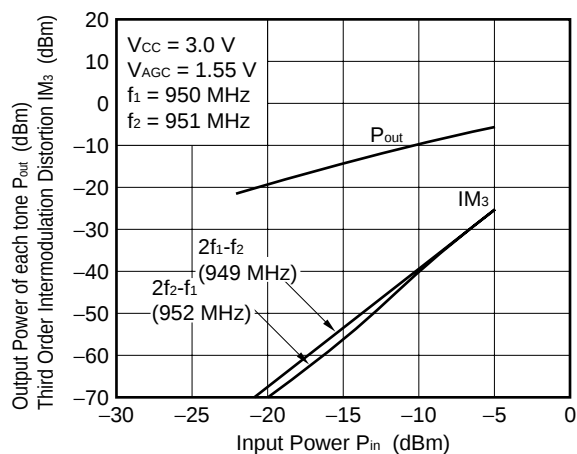
μ PC8130TA

Output port matching at $f = 950$ MHz

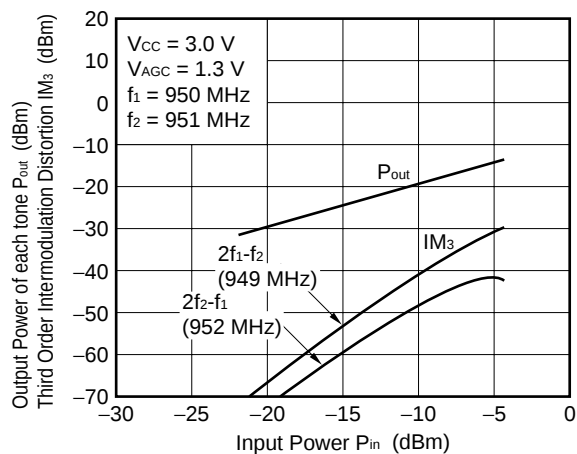
OUTPUT POWER AND IM_3 vs. INPUT POWER



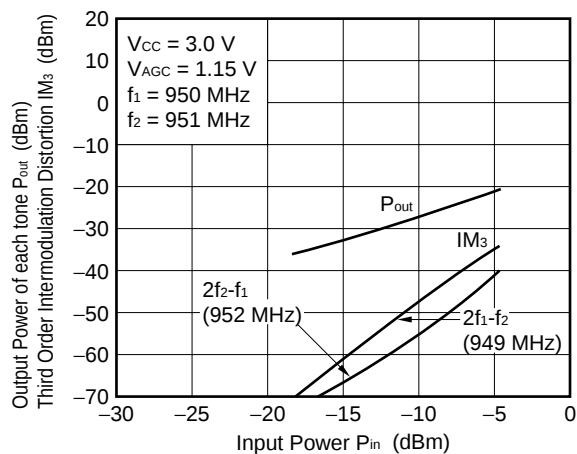
OUTPUT POWER AND IM_3 vs. INPUT POWER



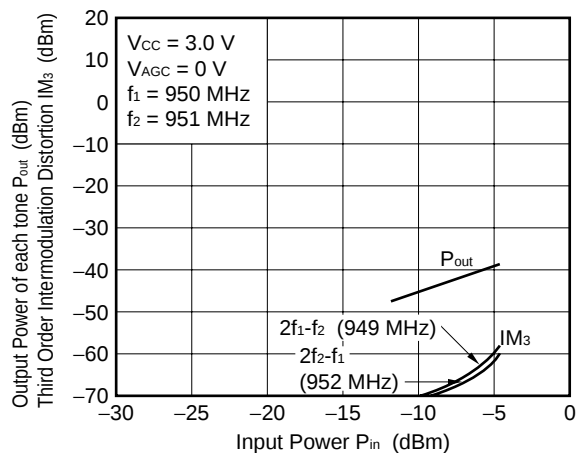
OUTPUT POWER AND IM_3 vs. INPUT POWER



OUTPUT POWER AND IM_3 vs. INPUT POWER



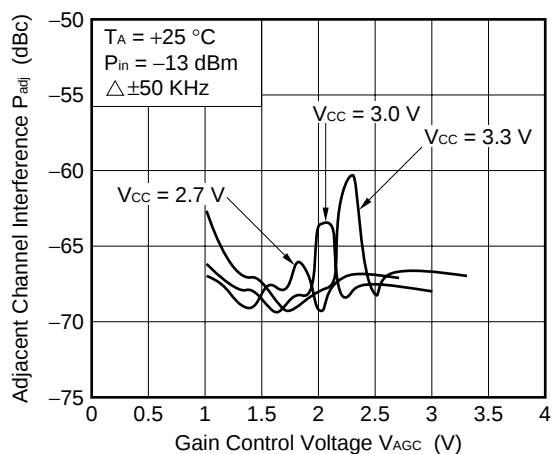
OUTPUT POWER AND IM_3 vs. INPUT POWER



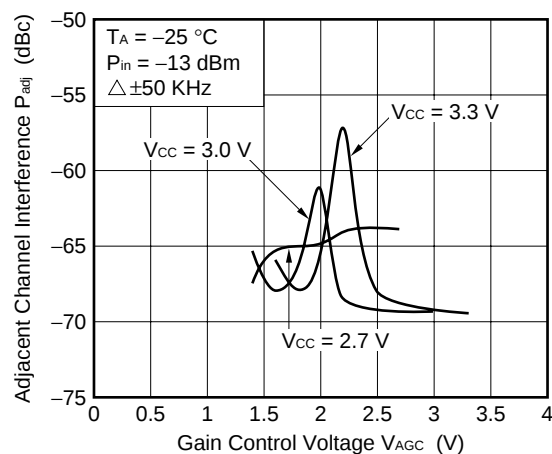
μ PC8130TA

Output port matching at $f = 950$ MHz

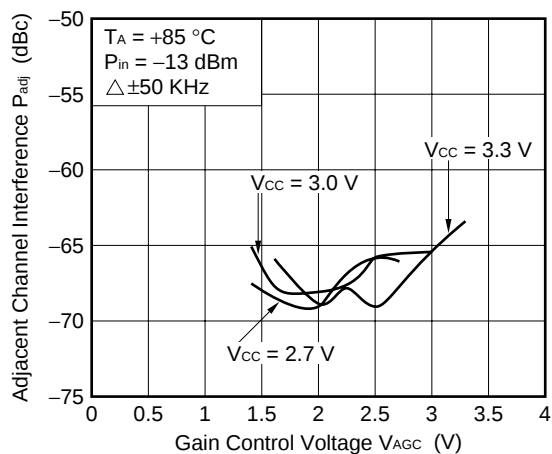
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



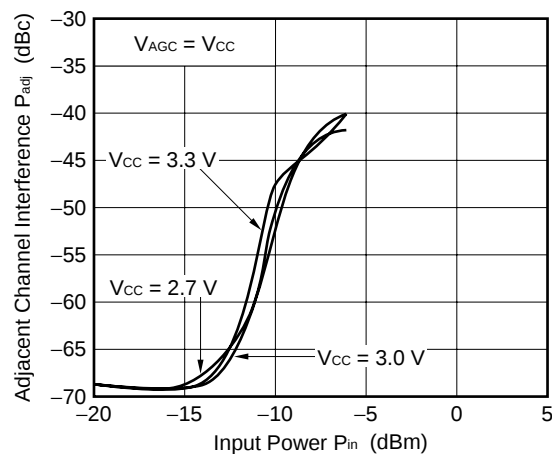
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



ADJACENT CHANNEL INTERFERENCE vs. INPUT POWER

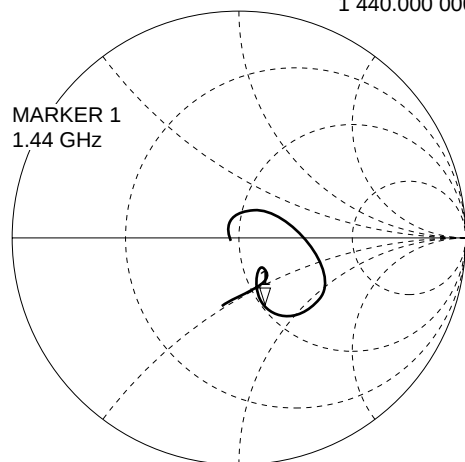


μ PC8130TA

Output port matching at f = 1440 MHz

$V_{CC} = V_{AGC} = 3.0$ V (G_PMAX), $P_{in} = -20$ dBm

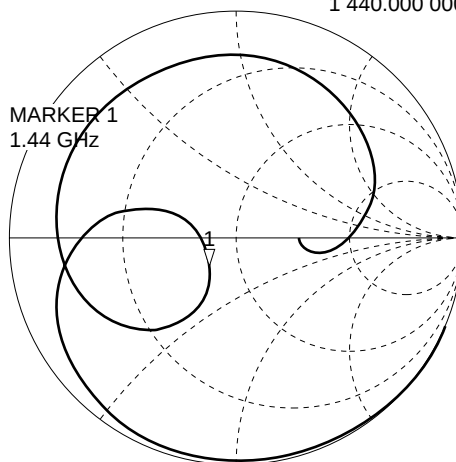
S_{11} vs. FREQUENCY 1: 51.363 Ω -34.424 Ω 3.2107 pF
1 440.000 000 MHz



START 100.000 000 MHz STOP 3 100.000 000 MHz

$V_{CC} = V_{AGC} = 3.0$ V (G_PMAX), $P_{in} = -20$ dBm

S_{22} vs. FREQUENCY 1: 37.857 Ω -11.791 Ω 9.3736 pF
1 440.000 000 MHz

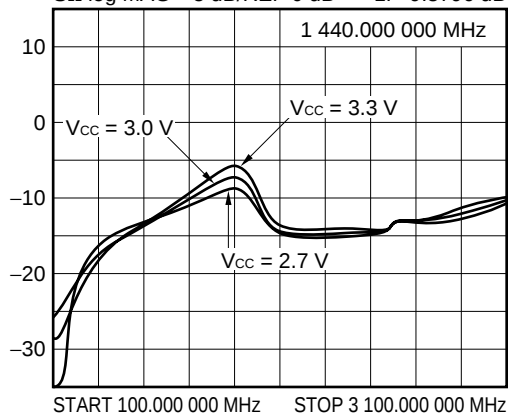


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY

$V_{AGC} = V_{CC}$ (G_PMAX), $P_{in} = -20$ dBm

S_{11} log MAG 5 dB/REF 0 dB 1: -9.8796 dB

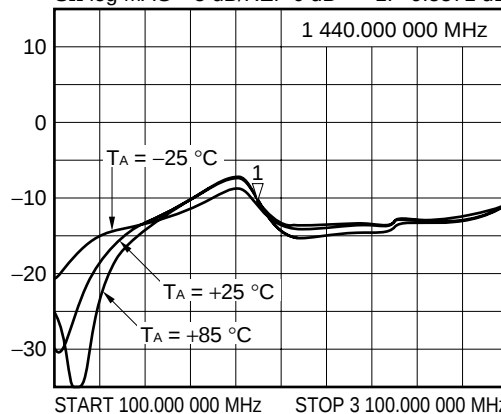


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY

$V_{CC} = V_{AGC} = 3.0$ V (G_PMAX), $P_{in} = -20$ dBm

S_{11} log MAG 5 dB/REF 0 dB 1: -9.5571 dB

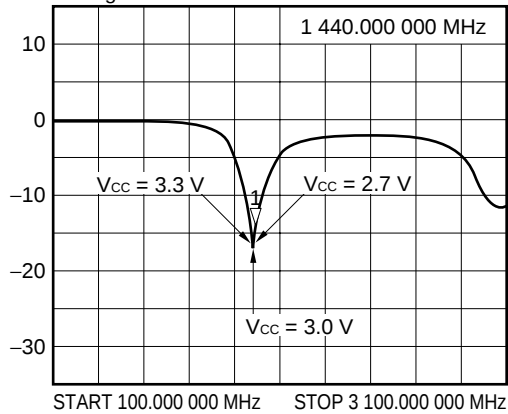


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY

$V_{AGC} = V_{CC}$ (G_PMAX), $P_{in} = -20$ dBm

S_{22} log MAG 5 dB/REF 0 dB 1: -14.444 dB

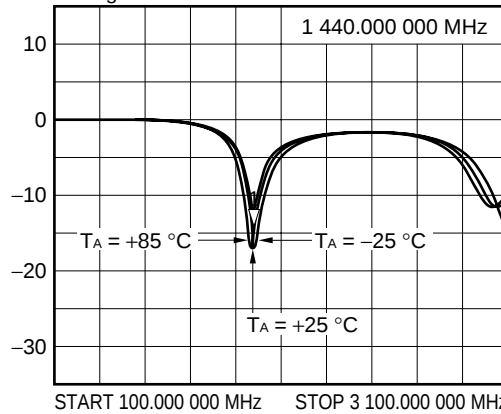


START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY

$V_{CC} = V_{AGC} = 3.0$ V (G_PMAX), $P_{in} = -20$ dBm

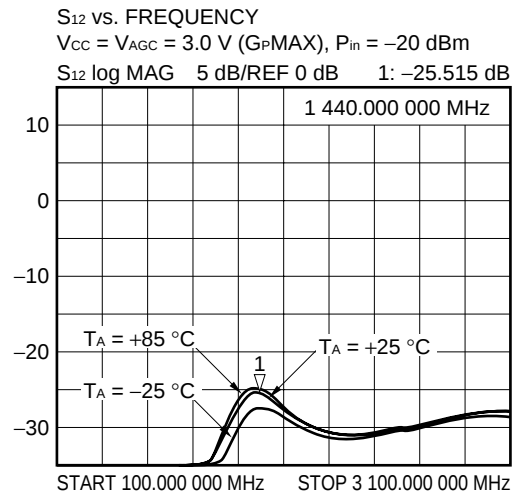
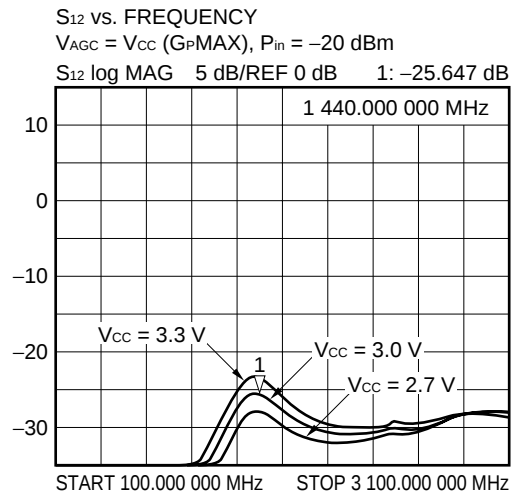
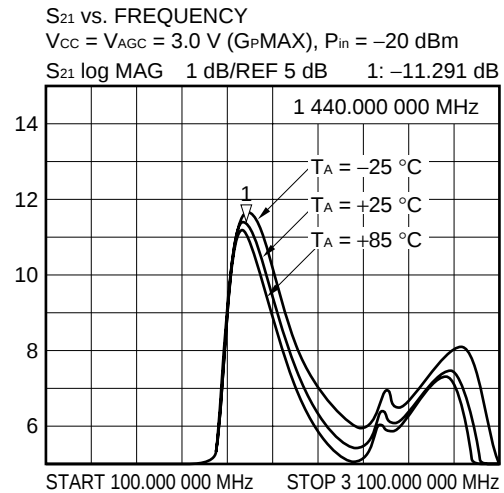
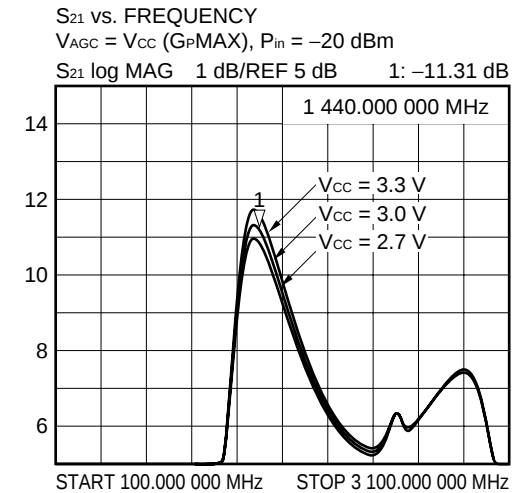
S_{22} log MAG 5 dB/REF 0 dB 1: -14.139 dB



START 100.000 000 MHz STOP 3 100.000 000 MHz

μ PC8130TA

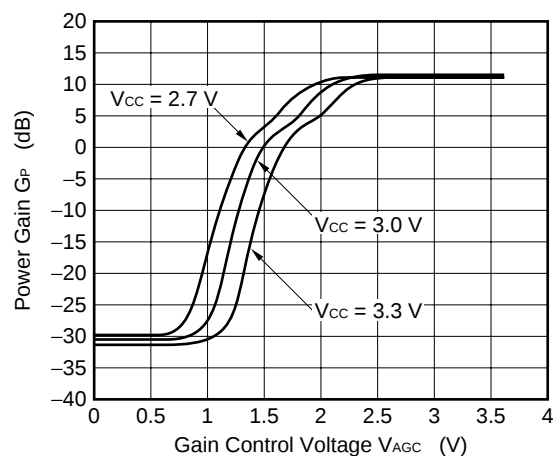
Output port matching at $f = 1440$ MHz



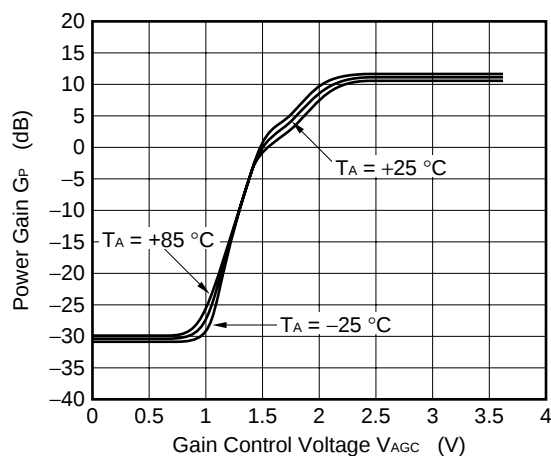
μ PC8130TA

Output port matching at $f = 1440$ MHz

POWER GAIN vs. GAIN CONTROL VOLTAGE



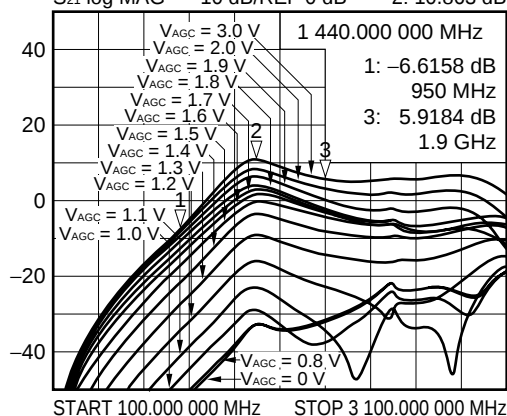
POWER GAIN vs. GAIN CONTROL VOLTAGE



S₂₁ vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE

$V_{CC} = 3.0$ V, $P_{in} = -20$ dBm

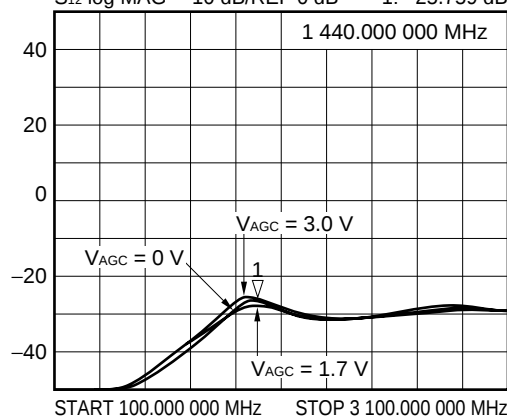
S₂₁ log MAG 10 dB/REF 0 dB 2: 10.863 dB



S₁₂ vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE

$V_{CC} = 3.0$ V, $P_{in} = -20$ dBm

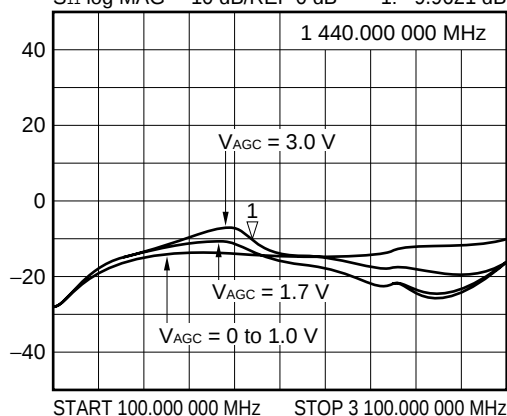
S₁₂ log MAG 10 dB/REF 0 dB 1: -25.759 dB



S₁₁ vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE

$V_{CC} = 3.0$ V, $P_{in} = -20$ dBm

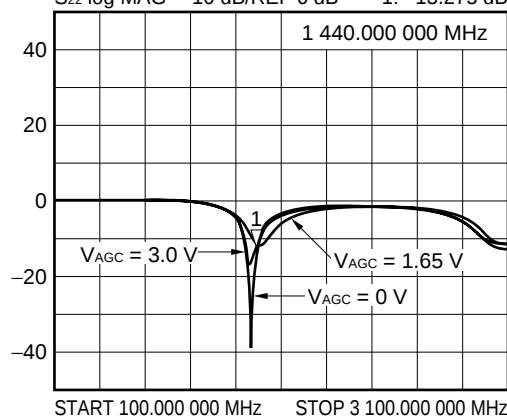
S₁₁ log MAG 10 dB/REF 0 dB 1: -9.9621 dB



S₂₂ vs. FREQUENCY DEPENDENCE OF GAIN CONTROL VOLTAGE

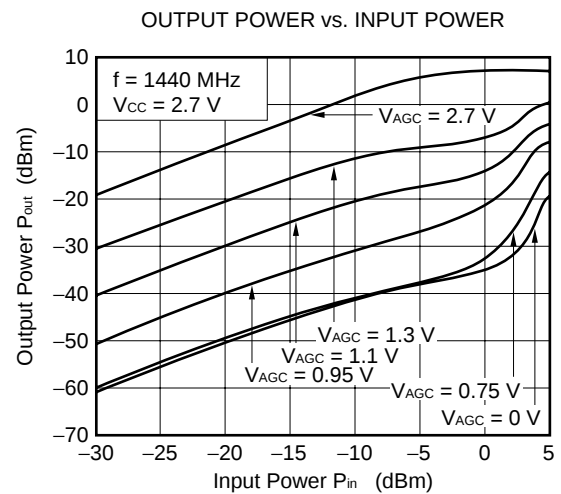
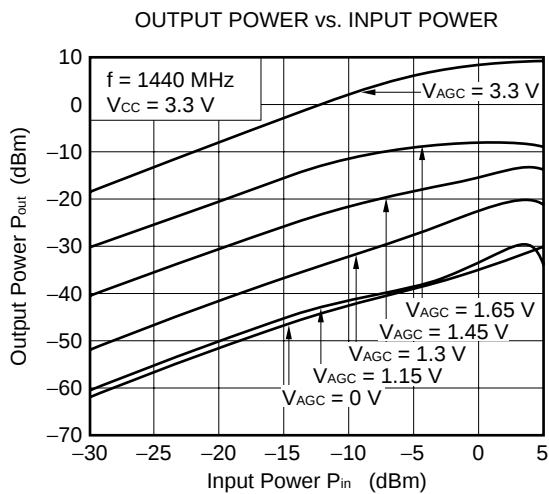
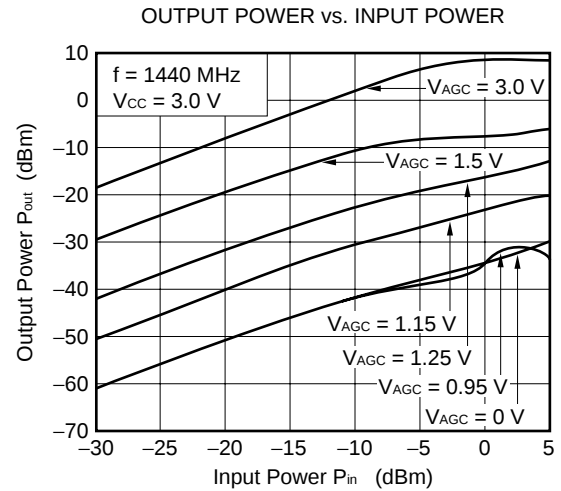
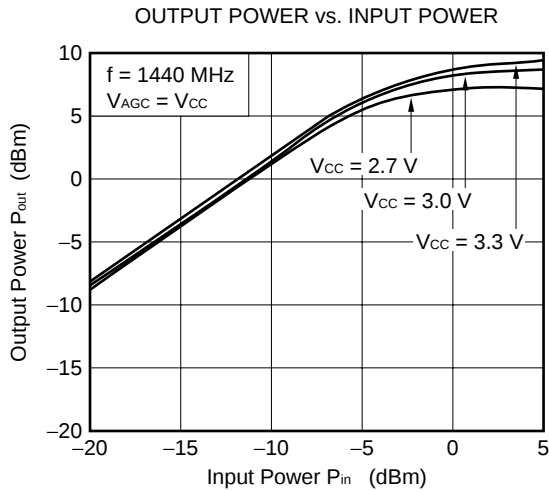
$V_{CC} = 3.0$ V, $P_{in} = -20$ dBm

S₂₂ log MAG 10 dB/REF 0 dB 1: -13.275 dB



μ PC8130TA

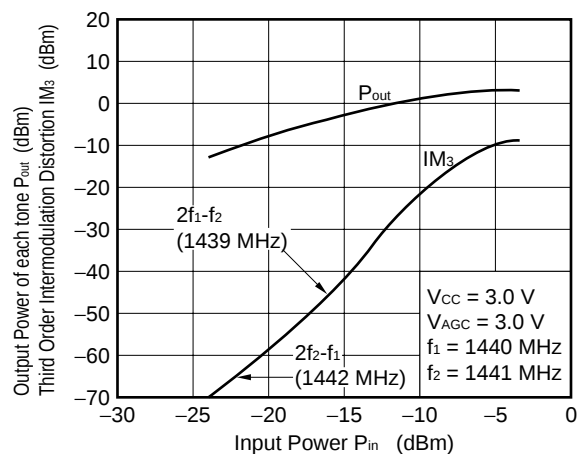
Output port matching at $f = 1440$ MHz



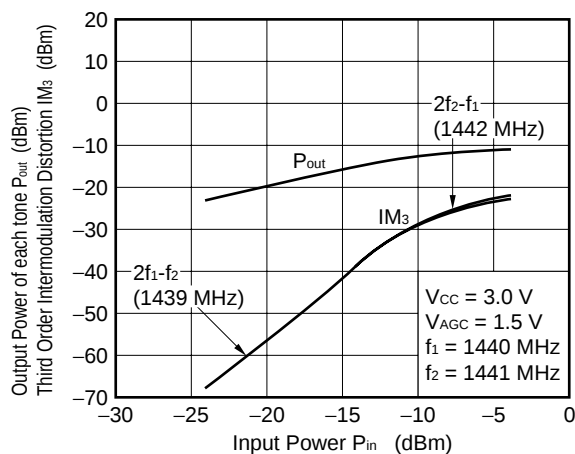
μ PC8130TA

Output port matching at $f = 1440$ MHz

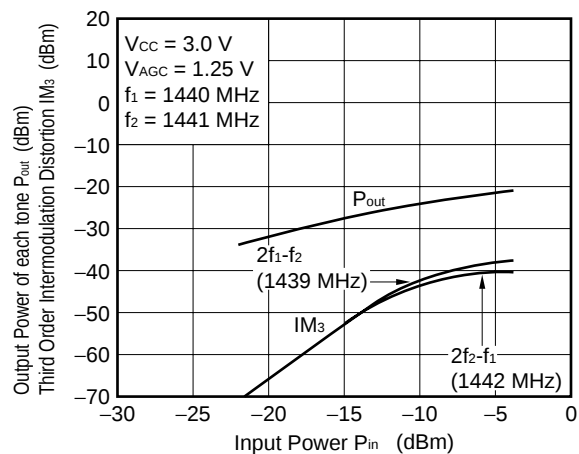
OUTPUT POWER AND IM_3 vs. INPUT POWER



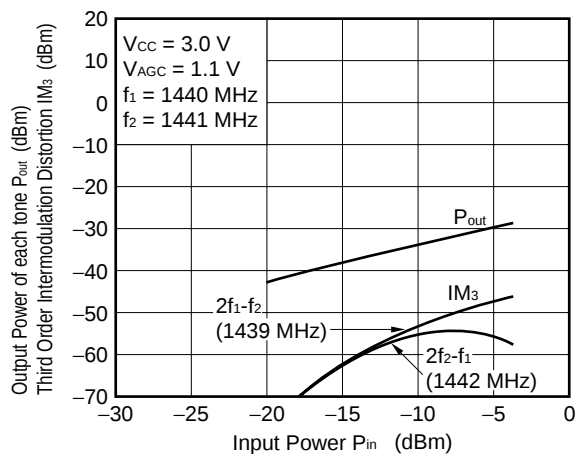
OUTPUT POWER AND IM_3 vs. INPUT POWER



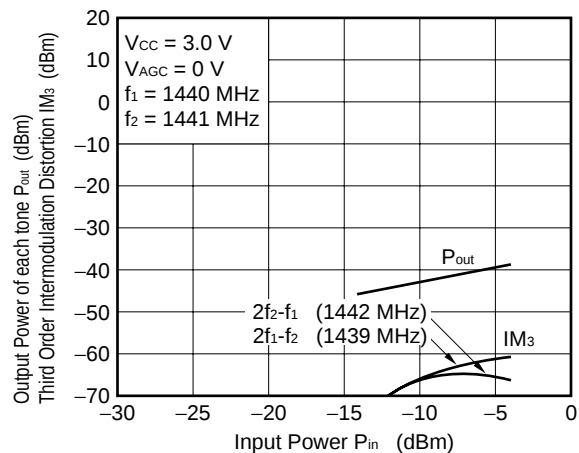
OUTPUT POWER AND IM_3 vs. INPUT POWER



OUTPUT POWER AND IM_3 vs. INPUT POWER



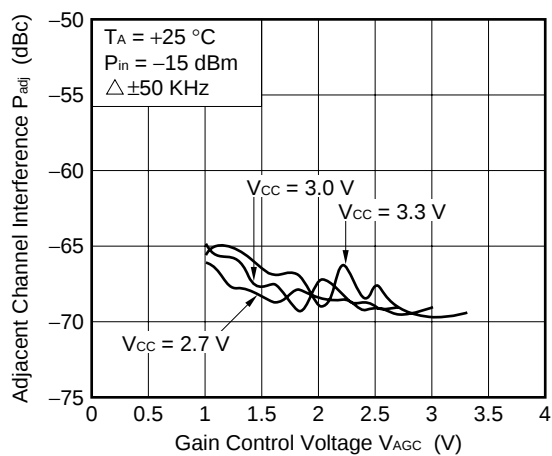
OUTPUT POWER AND IM_3 vs. INPUT POWER



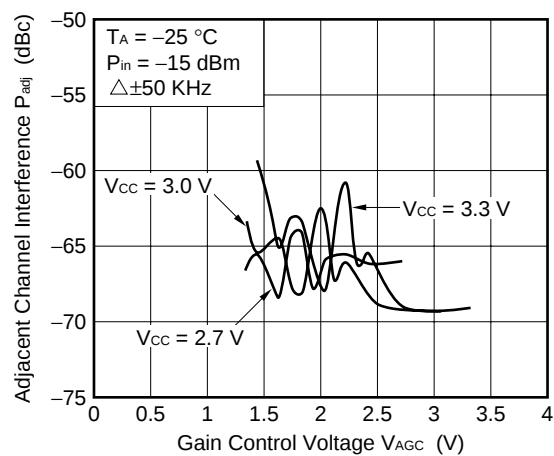
μ PC8130TA

Output port matching at $f = 1440$ MHz

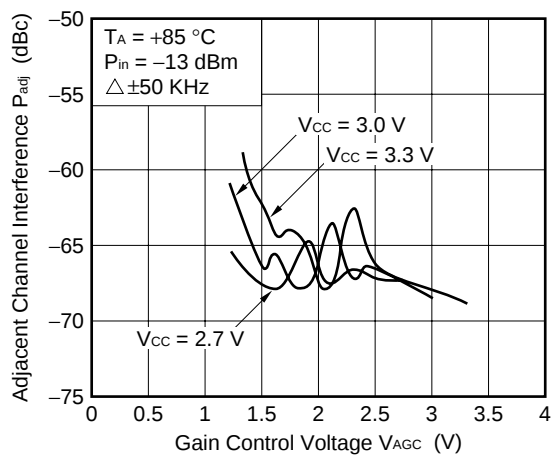
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



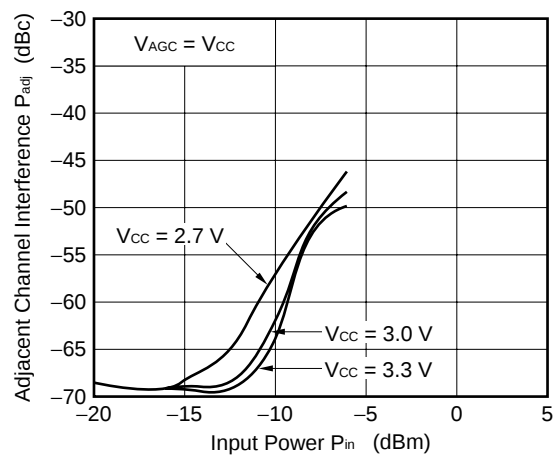
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



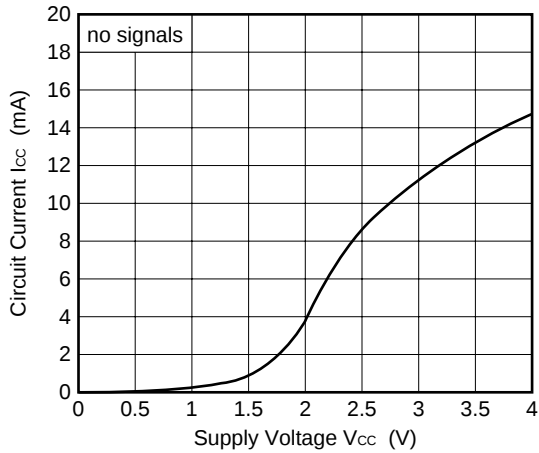
ADJACENT CHANNEL INTERFERENCE vs. INPUT POWER



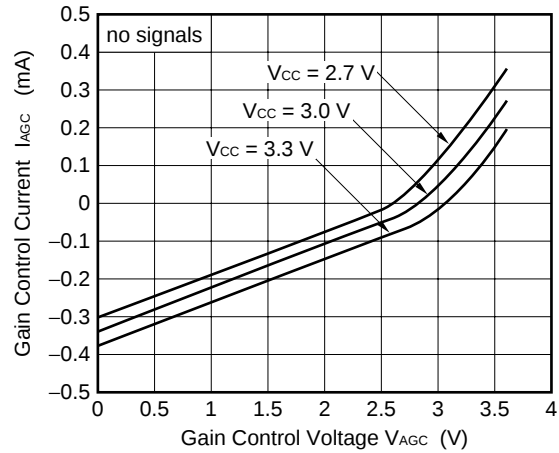
TYPICAL CHARACTERISTICS

μ PC8131TA

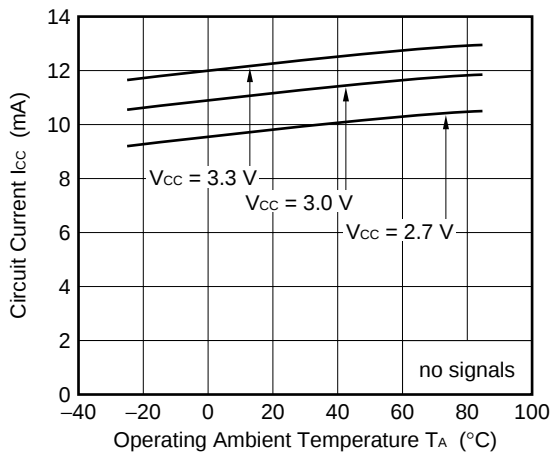
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



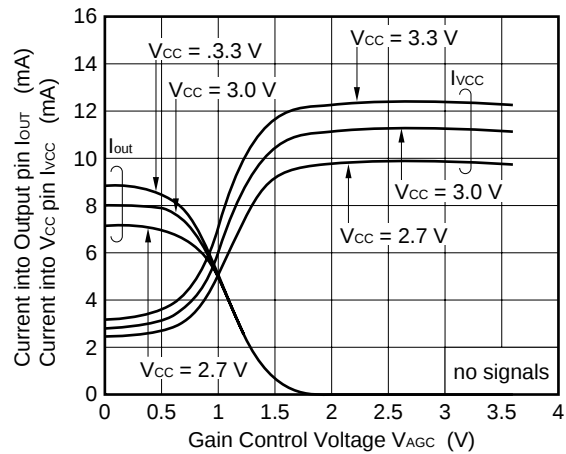
GAIN CONTROL CURRENT vs. GAIN CONTROL VOLTAGE



CIRCUIT CURRENT vs. OPERATING AMBIENT TEMPERATURE

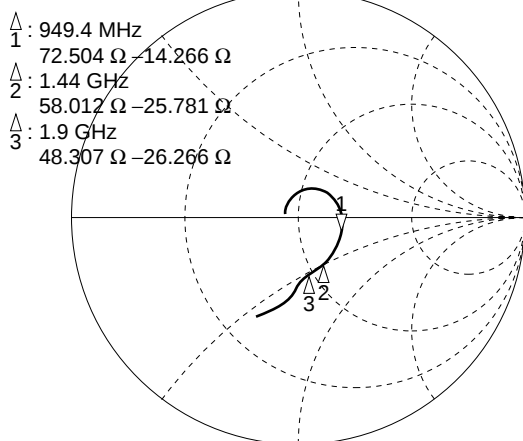


CURRENT INTO OUTPUT PIN AND CURRENT INTO V_{CC} PIN vs. GAIN CONTROL VOLTAGE



S_{11} vs. FREQUENCY

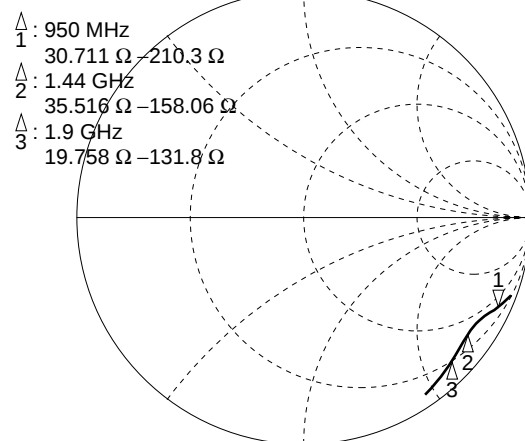
$V_{CC} = 3.0\text{ V}$, $V_{AGC} = 0\text{ V}$ (G_PMAX), $P_{in} = -20\text{ dBm}$
 S_{11}



START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY

$V_{CC} = 3.0\text{ V}$, $V_{AGC} = 0\text{ V}$ (G_PMAX), $P_{in} = -20\text{ dBm}$
 S_{22}

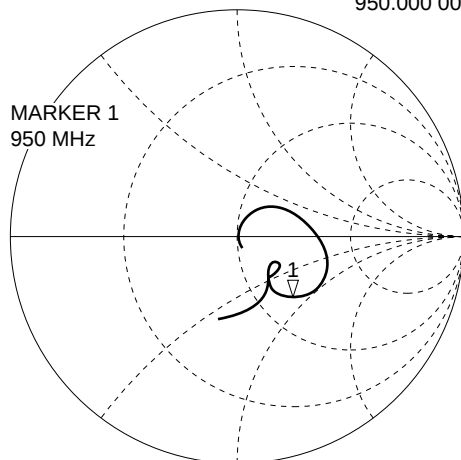


START 800.000 000 MHz STOP 2 700.000 000 MHz

μ PC8131TA

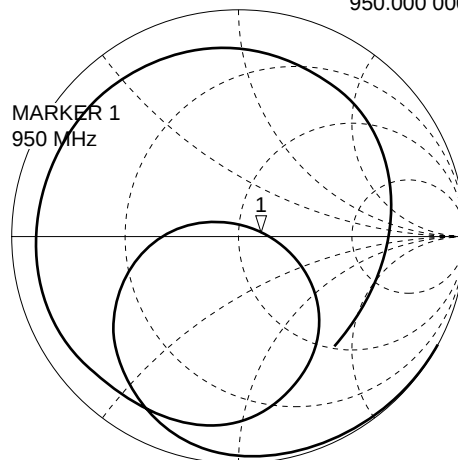
Output port matching at $f = 950$ MHz

$V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} vs. FREQUENCY 1: 66.246 Ω -41.039 Ω 4.0822 pF
 950.000 000 MHz



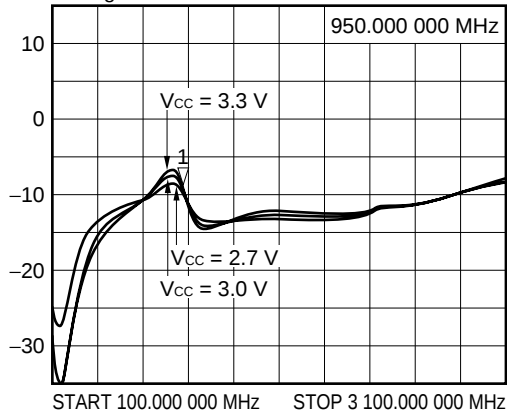
START 100.000 000 MHz STOP 3 100.000 000 MHz

$V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} vs. FREQUENCY 1: 57.439 Ω 3.3594 Ω 562.8 pF
 950.000 000 MHz



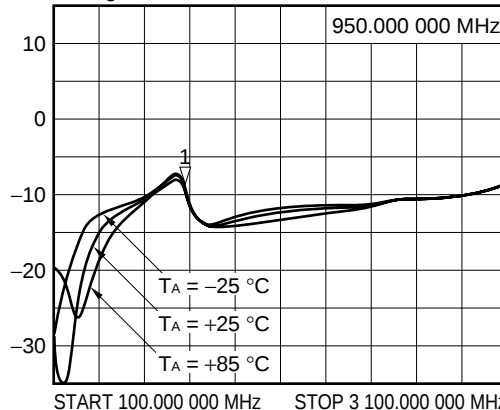
START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY
 $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} log MAG 5 dB/REF 0 dB 1: -8.9634 dB
 950.000 000 MHz



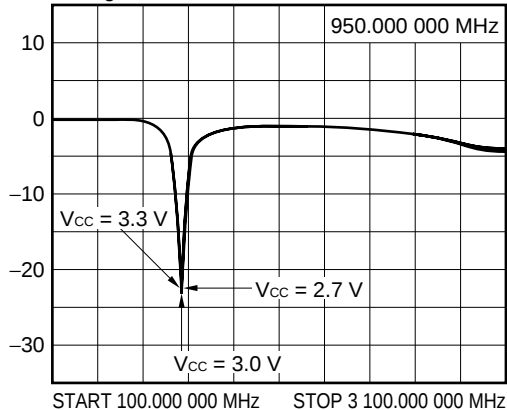
START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{11} vs. FREQUENCY
 $V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} log MAG 5 dB/REF 0 dB 1: -2.0122 dB
 950.000 000 MHz



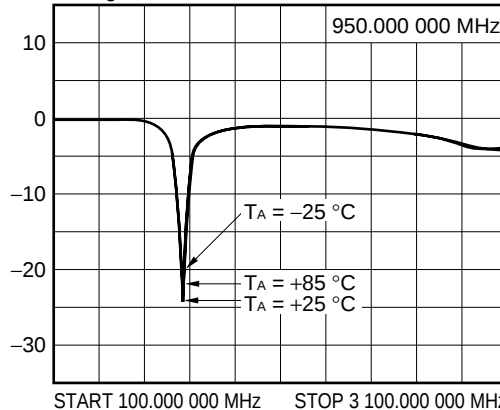
START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY
 $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} log MAG 5 dB/REF 0 dB 1: -19.264 dB
 950.000 000 MHz



START 100.000 000 MHz STOP 3 100.000 000 MHz

S_{22} vs. FREQUENCY
 $V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} log MAG 5 dB/REF 0 dB 1: -18.936 dB
 950.000 000 MHz



START 100.000 000 MHz STOP 3 100.000 000 MHz

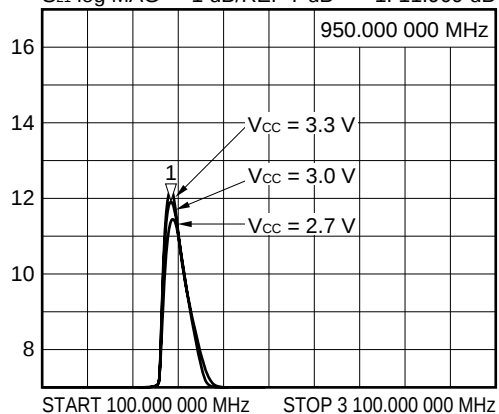
μ PC8131TA

Output port matching at $f = 950$ MHz

S₂₁ VS. FREQUENCY

V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

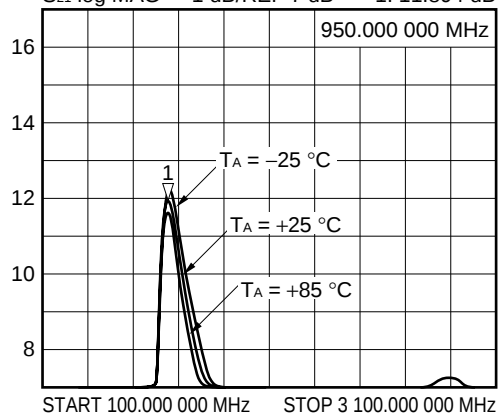
S₂₁ log MAG 1 dB/REF 7 dB 1: 11.909 dB



S₂₁ VS. FREQUENCY

V_{CC} = 3.0 V, V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

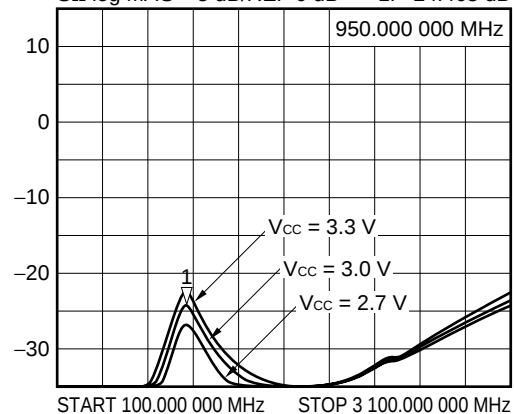
S₂₁ log MAG 1 dB/REF 7 dB 1: 11.894 dB



S₁₂ VS. FREQUENCY

V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

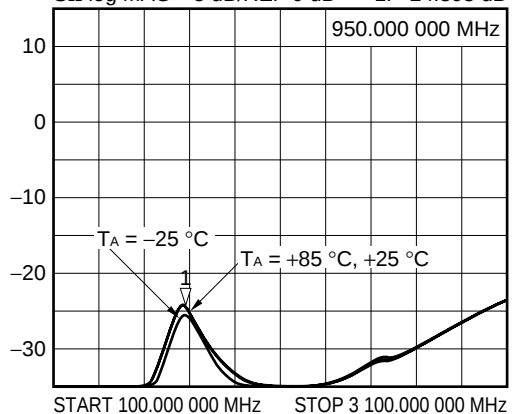
S₁₂ log MAG 5 dB/REF 0 dB 1: -24.468 dB



S₁₂ VS. FREQUENCY

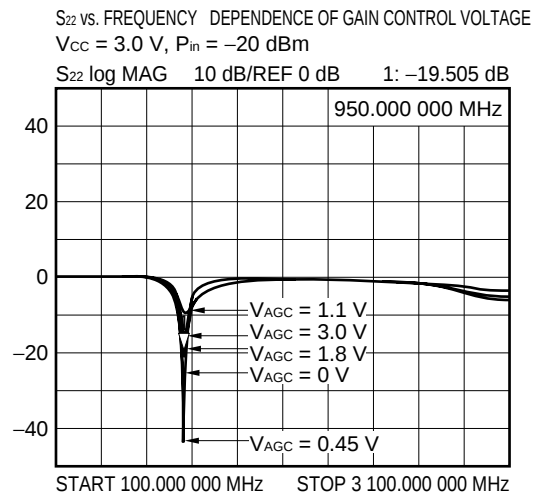
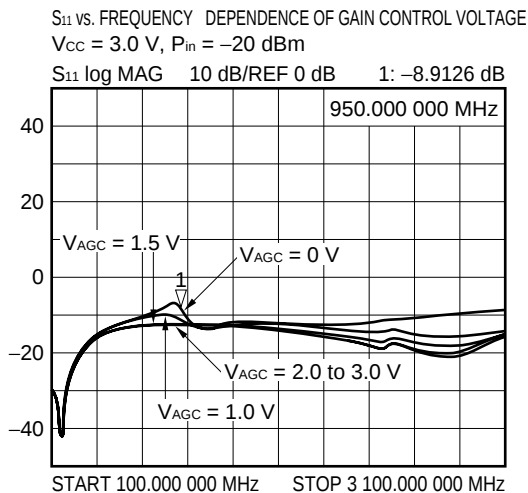
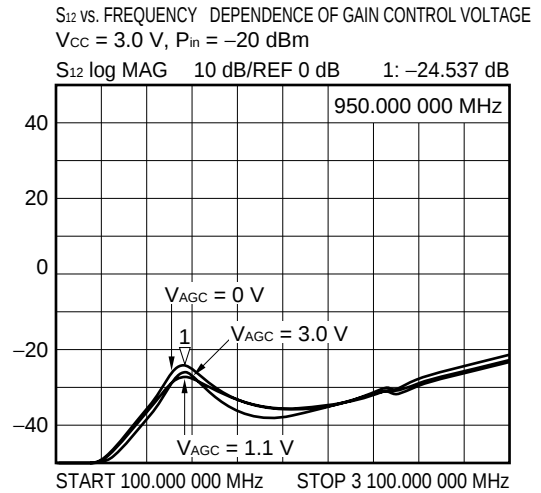
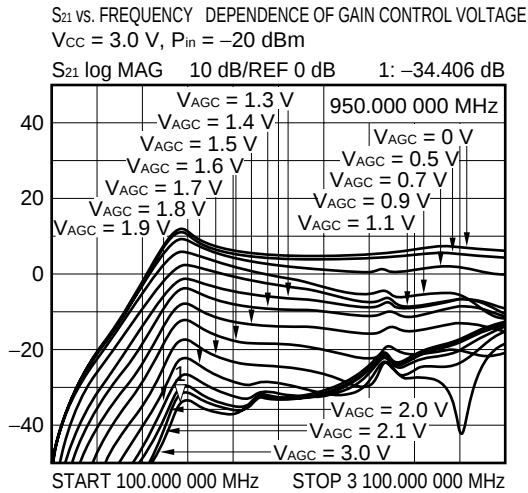
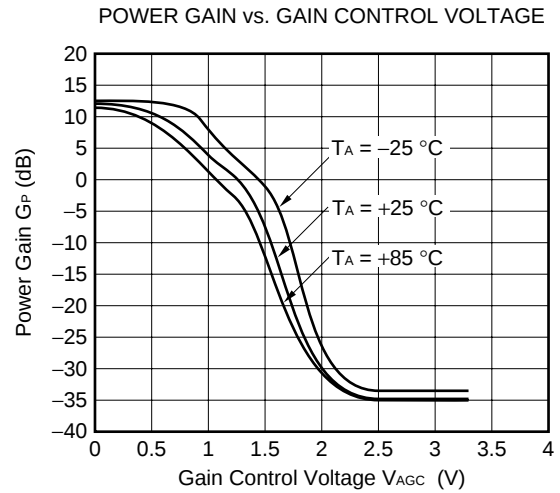
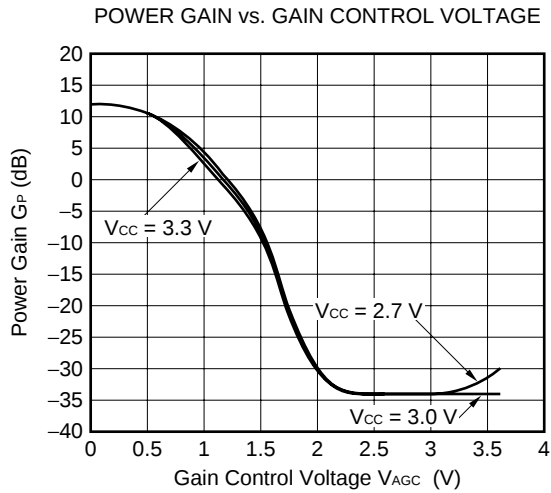
V_{CC} = 3.0 V, V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

S₁₂ log MAG 5 dB/REF 0 dB 1: -24.393 dB



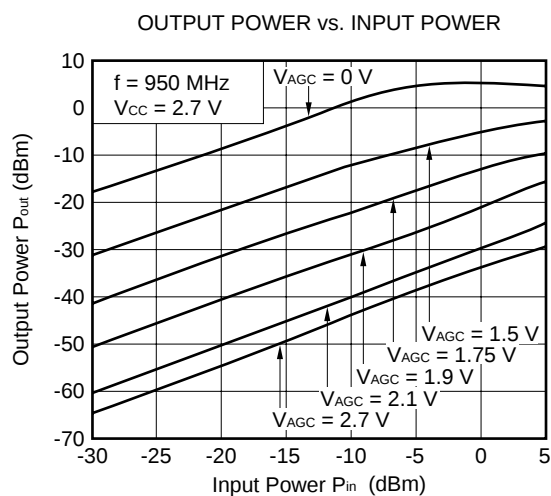
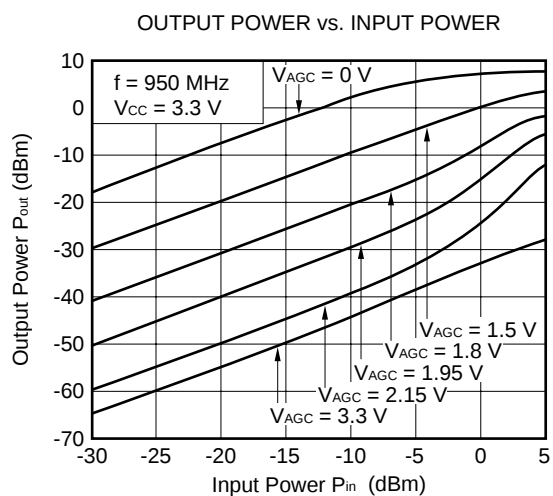
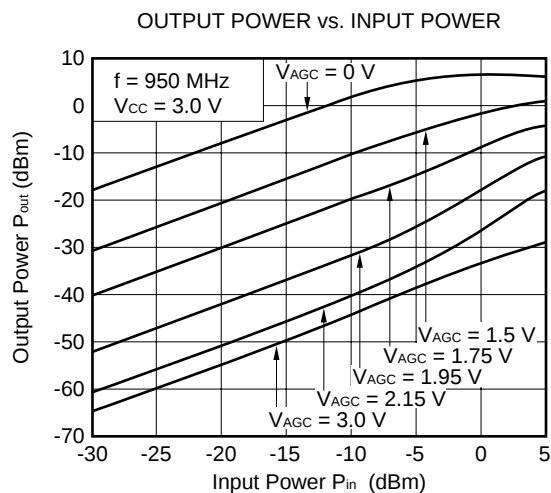
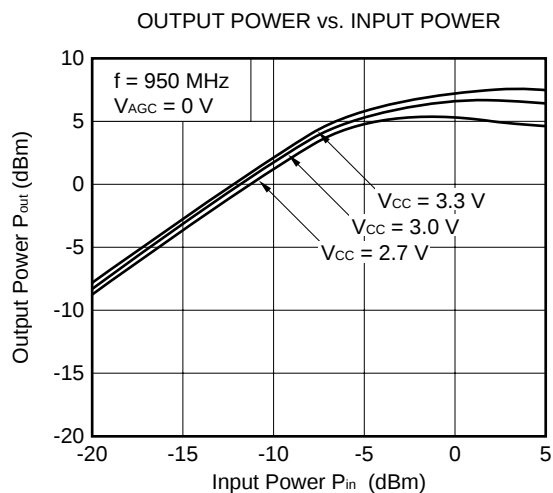
μ PC8131TA

Output port matching at $f = 950$ MHz



μ PC8131TA

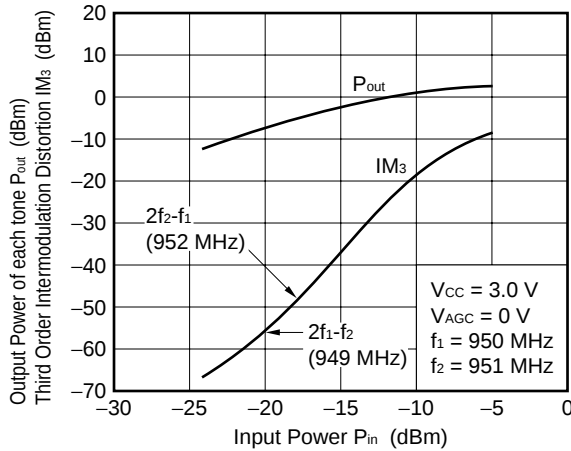
Output port matching at $f = 950$ MHz



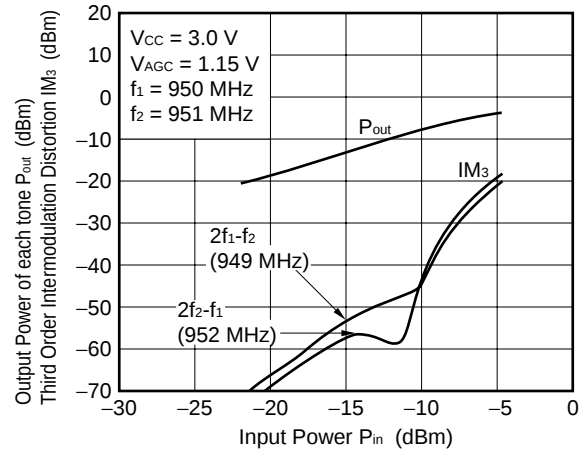
μ PC8131TA

Output port matching at $f = 950$ MHz

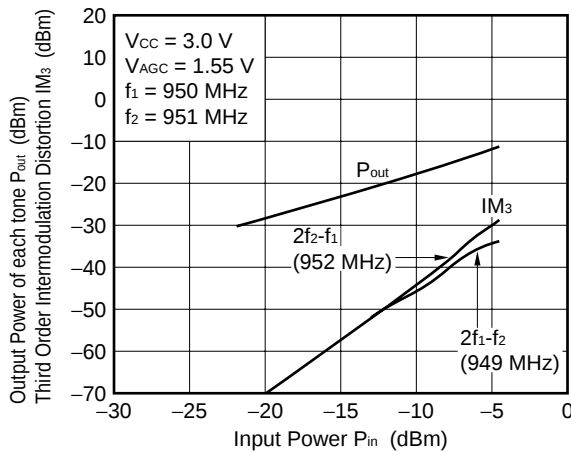
OUTPUT POWER AND IM_3 vs. INPUT POWER



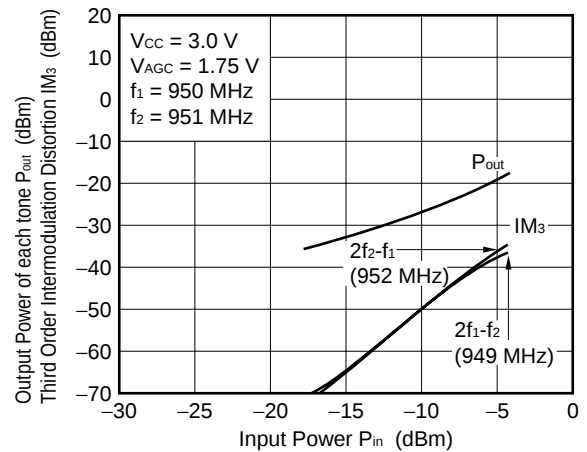
OUTPUT POWER AND IM_3 vs. INPUT POWER



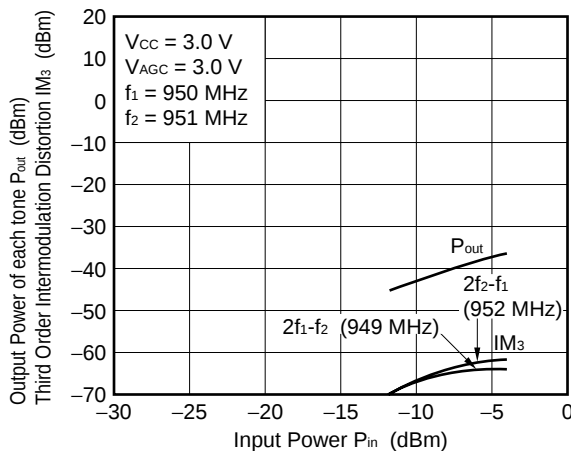
OUTPUT POWER AND IM_3 vs. INPUT POWER



OUTPUT POWER AND IM_3 vs. INPUT POWER



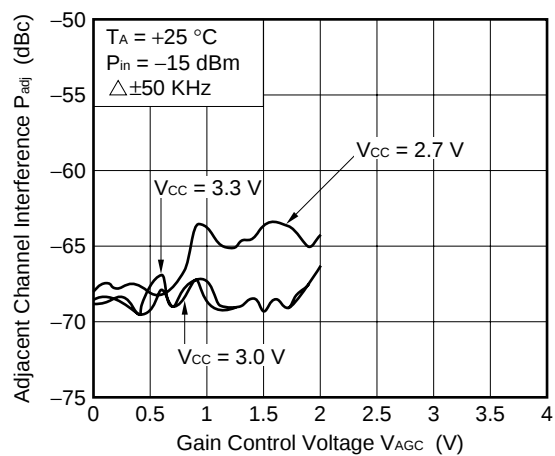
OUTPUT POWER AND IM_3 vs. INPUT POWER



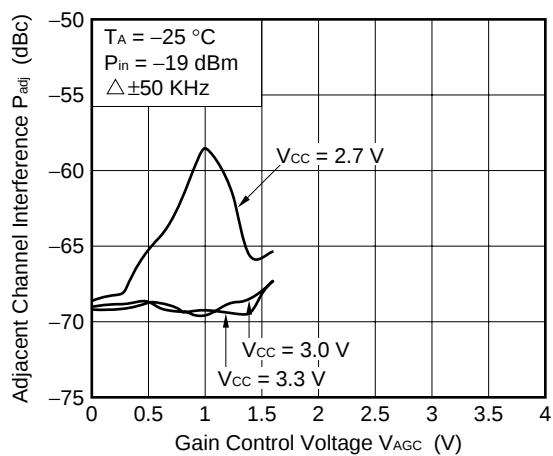
μ PC8131TA

Output port matching at $f = 950$ MHz

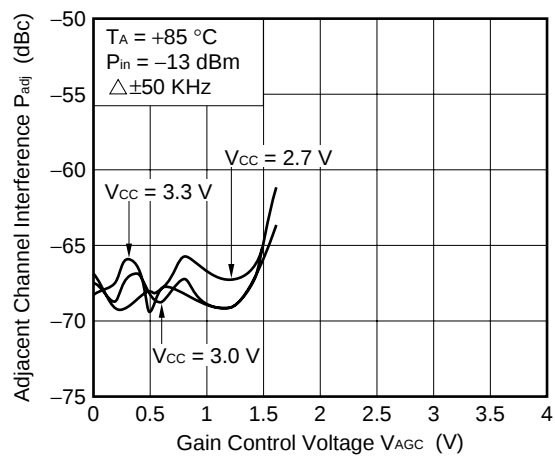
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



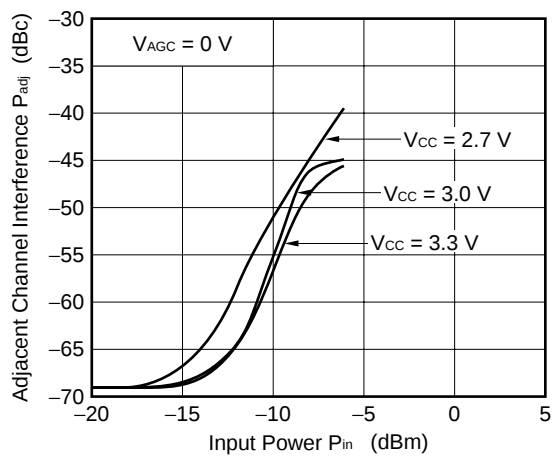
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



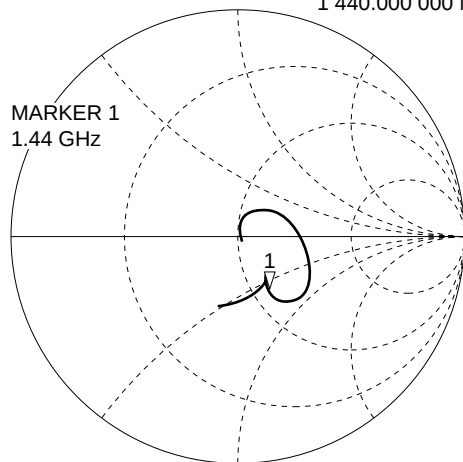
ADJACENT CHANNEL INTERFERENCE vs. INPUT POWER



μ PC8131TA

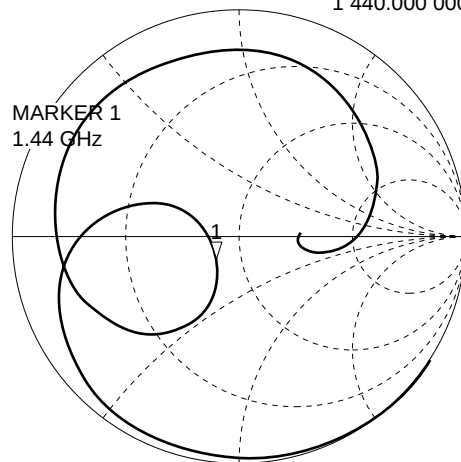
Output port matching at $f = 1440$ MHz

$V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} vs. FREQUENCY 1: 57.025Ω -32.578Ω 3.3926 pF
 $1\ 440.000\ 000$ MHz



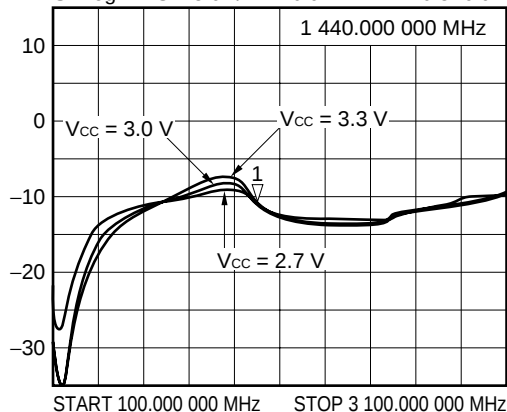
START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

$V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} vs. FREQUENCY 1: 40.016Ω -8.582Ω 12.879 pF
 $1\ 440.000\ 000$ MHz



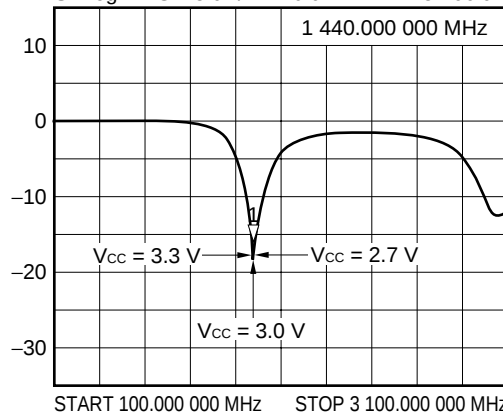
START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

S_{11} vs. FREQUENCY
 $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} log MAG 5 dB/REF 0 dB 1: -10.576 dB
 $1\ 440.000\ 000$ MHz



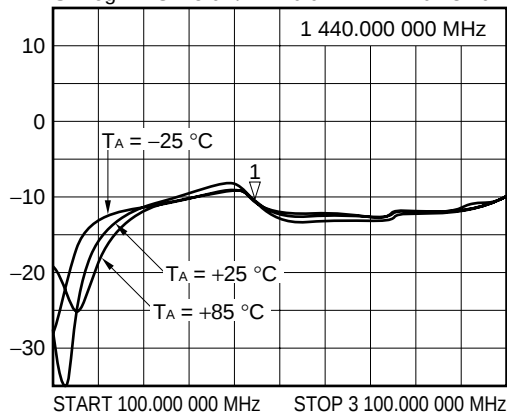
START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

S_{22} vs. FREQUENCY
 $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} log MAG 5 dB/REF 0 dB 1: -15.766 dB
 $1\ 440.000\ 000$ MHz



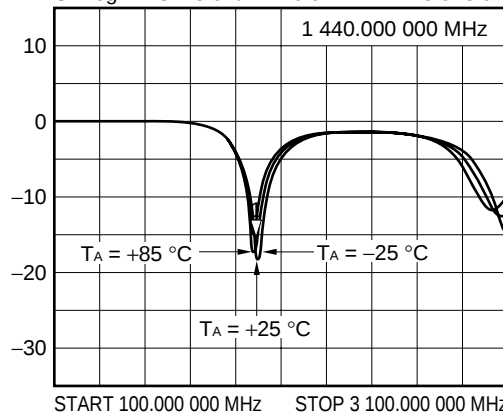
START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

S_{11} vs. FREQUENCY
 $V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{11} log MAG 5 dB/REF 0 dB 1: -10.784 dB
 $1\ 440.000\ 000$ MHz



START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

S_{22} vs. FREQUENCY
 $V_{CC} = 3.0$ V, $V_{AGC} = 0$ V (G_PMAX), $P_{in} = -20$ dBm
 S_{22} log MAG 5 dB/REF 0 dB 1: -15.915 dB
 $1\ 440.000\ 000$ MHz



START $100.000\ 000$ MHz STOP $3\ 100.000\ 000$ MHz

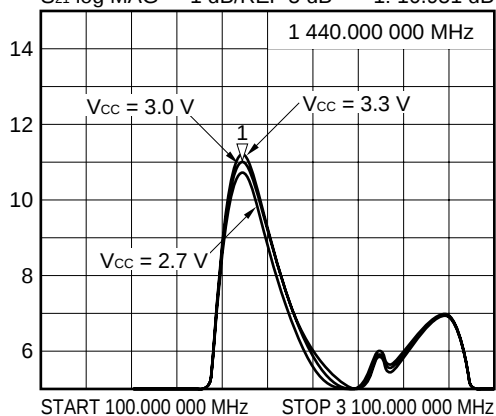
μ PC8131TA

Output port matching at $f = 1440$ MHz

S₂₁ VS. FREQUENCY

V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

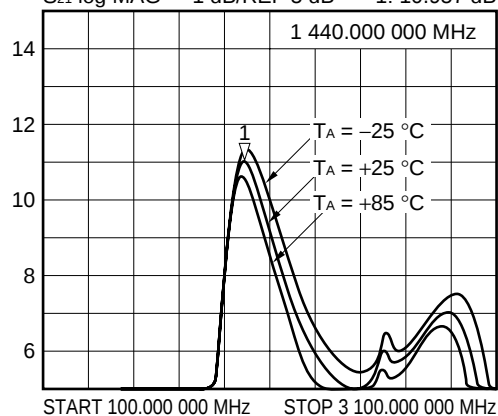
S₂₁ log MAG 1 dB/REF 5 dB 1: 10.951 dB



S₂₁ VS. FREQUENCY

V_{CC} = 3.0 V, V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

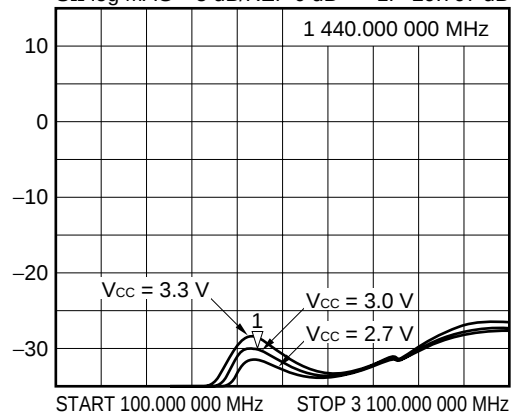
S₂₁ log MAG 1 dB/REF 5 dB 1: 10.957 dB



S₁₂ VS. FREQUENCY

V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

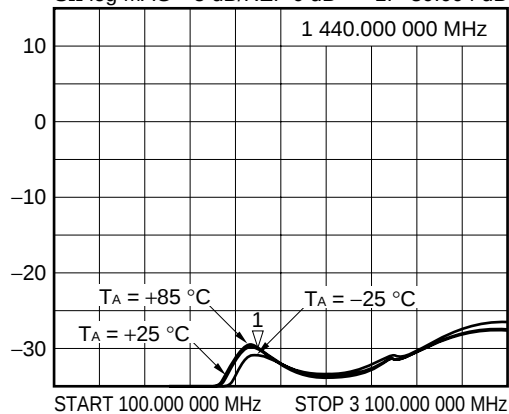
S₁₂ log MAG 5 dB/REF 0 dB 1: -29.767 dB



S₁₂ VS. FREQUENCY

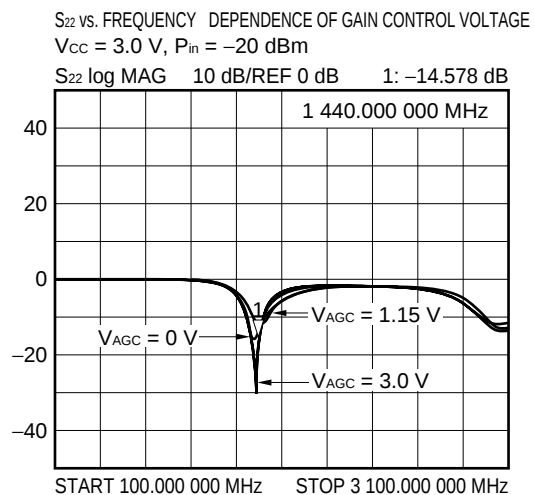
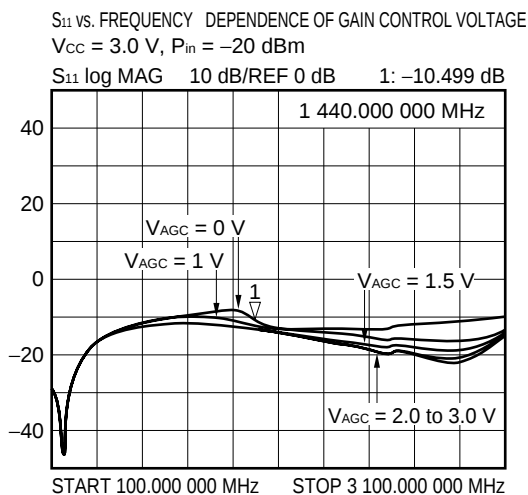
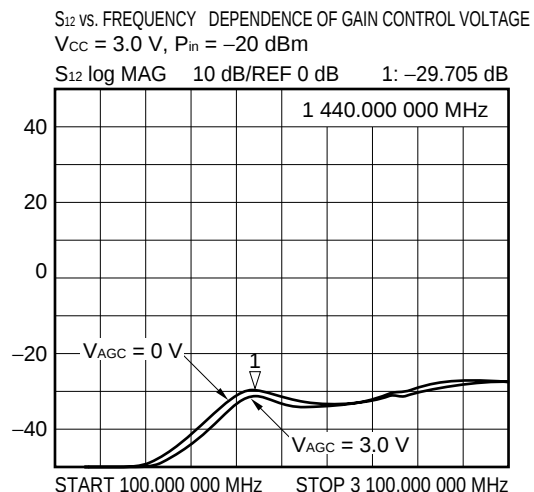
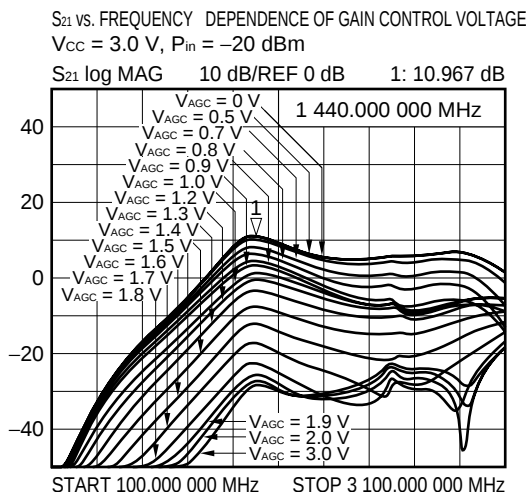
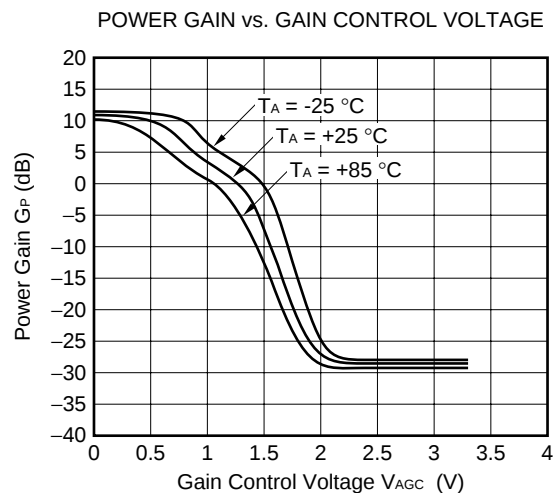
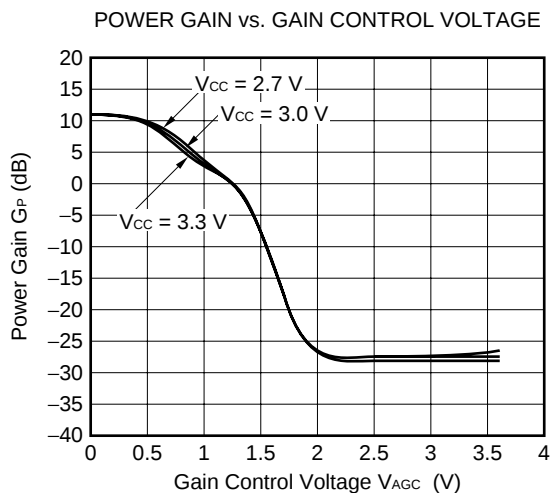
V_{CC} = 3.0 V, V_{AGC} = 0 V (G_PMAX), P_{in} = -20 dBm

S₁₂ log MAG 5 dB/REF 0 dB 1: -30.004 dB



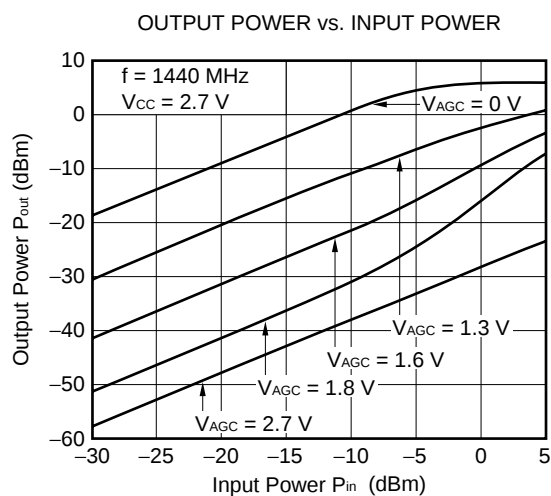
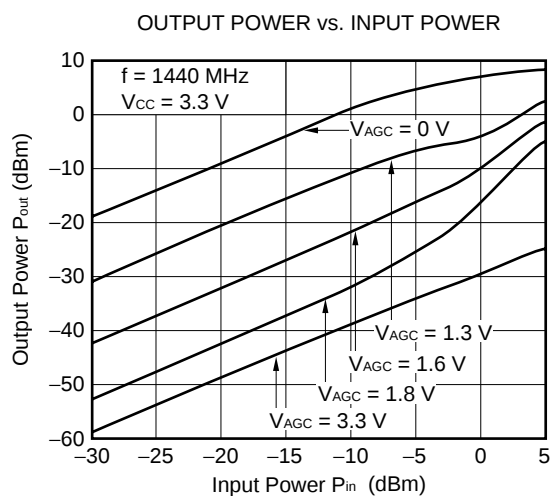
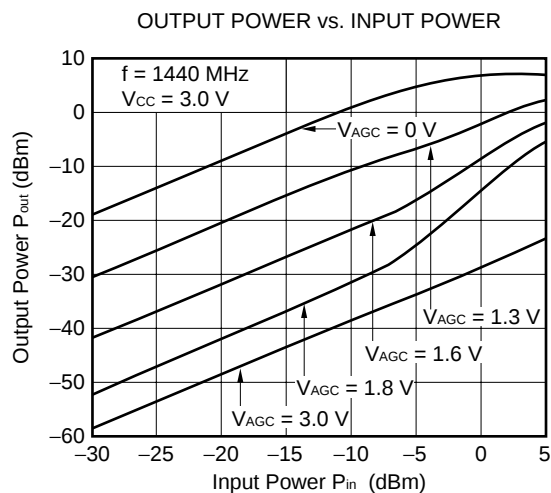
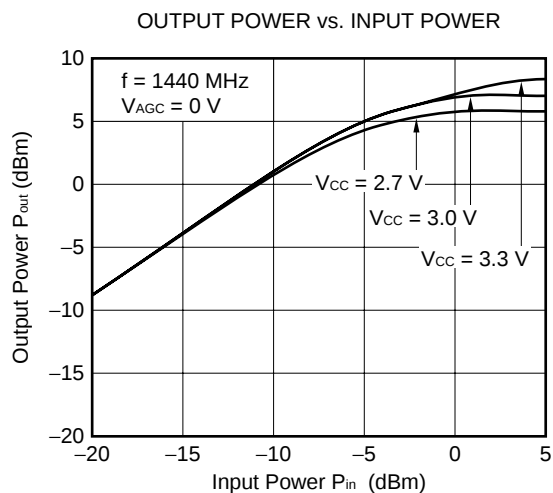
μ PC8131TA

Output port matching at $f = 1440$ MHz



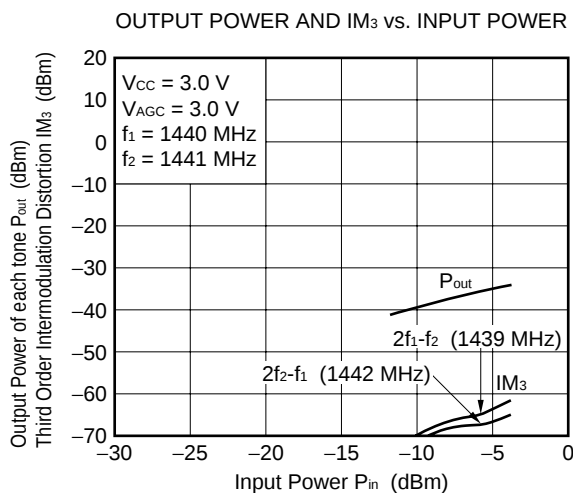
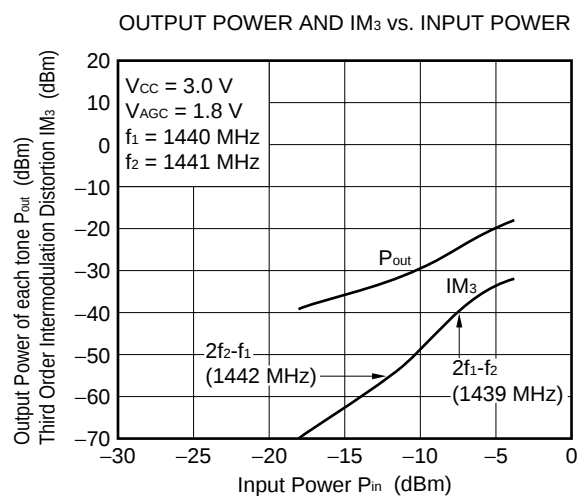
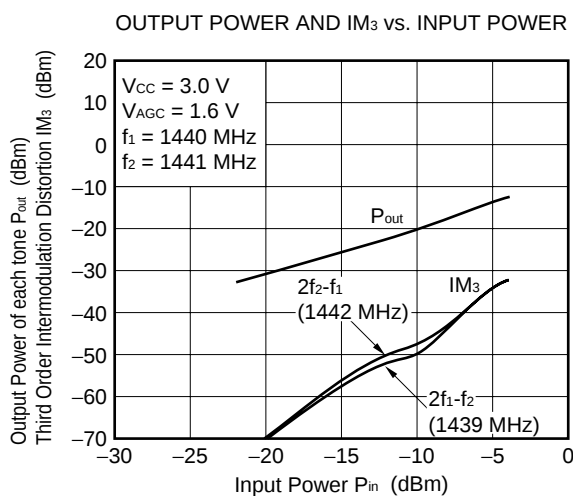
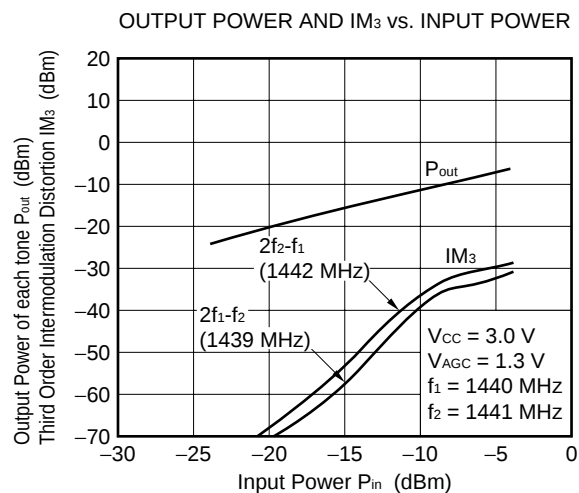
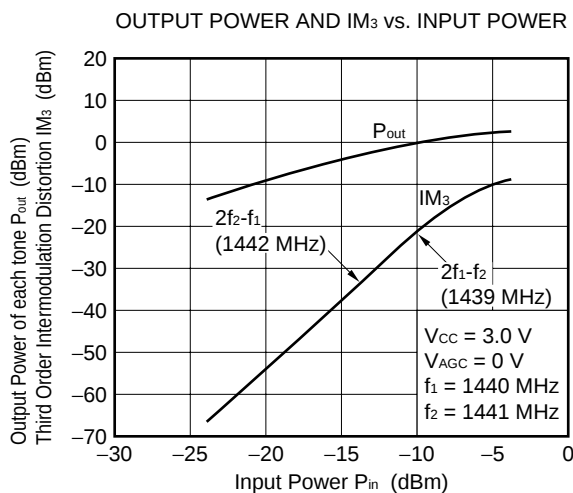
μ PC8131TA

Output port matching at $f = 1440$ MHz



μ PC8131TA

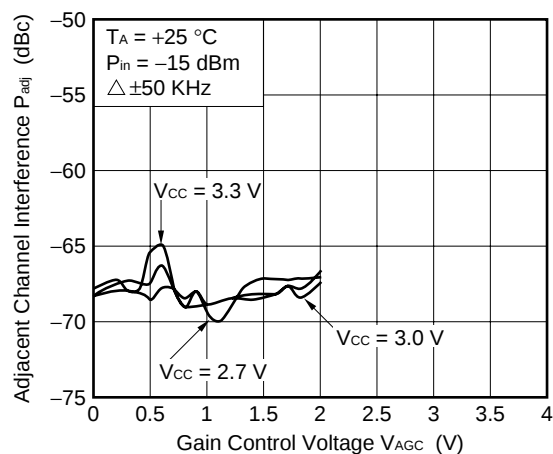
Output port matching at $f = 1440$ MHz



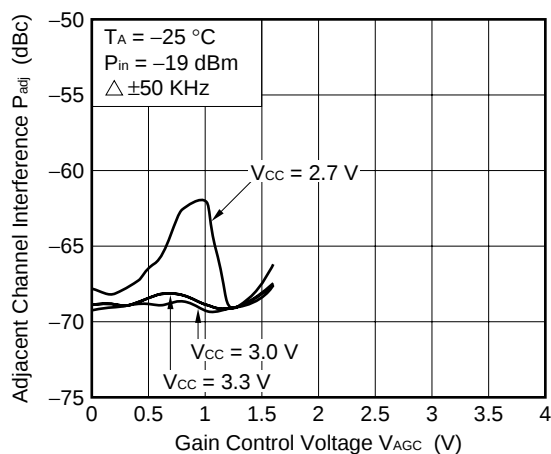
μ PC8131TA

Output port matching at $f = 1440$ MHz

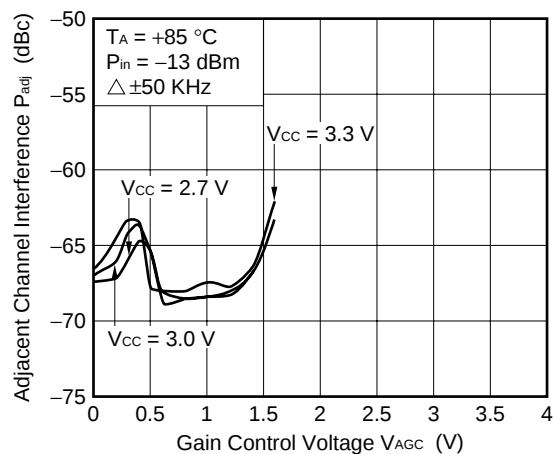
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



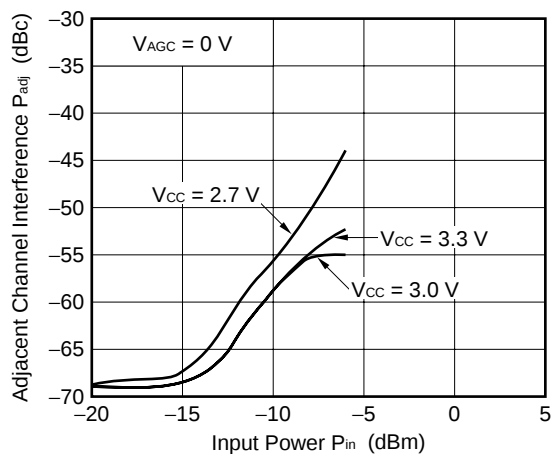
ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE



ADJACENT CHANNEL INTERFERENCE vs. GAIN CONTROL VOLTAGE

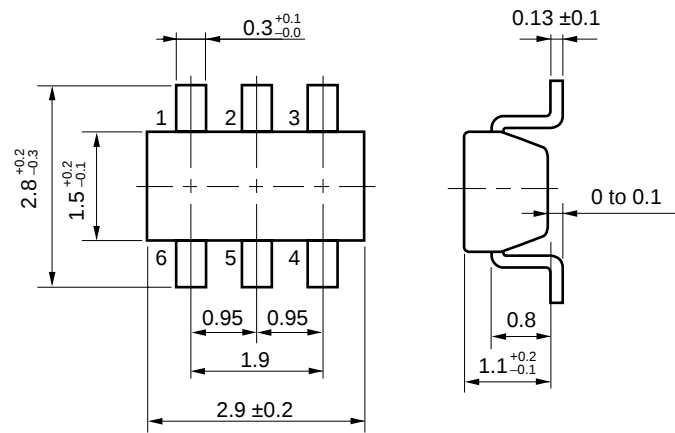


ADJACENT CHANNEL INTERFERENCE vs. INPUT POWER



PACKAGE DIMENSIONS

6 PIN MINI-MOLD PACKAGE (UNIT: mm)



NOTES ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
- (3) The bypass capacitor (eg. 1000 pF) should be attached to the V_{CC} pin.
- (4) Impedance matching circuit must be each externally attached to input and output ports.
- (5) The bias must be applied to output pin through the matching inductor. (The bias must not be applied to input pin.)

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit ^{Note} : None	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit ^{Note} : None	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit ^{Note} : None	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit ^{Note} : None	—

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

[MEMO]

NEC

μPC8130TA, μPC8131TA

[MEMO]

[MEMO]



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.