NEC

MOS INTEGRATED CIRCUIT

μPD161644

241 OUTPUT GATE DRIVER WITH POWER SUPPLY FOR TFT-LCD GATE DRIVER

DESCRIPTION

The μPD161644 is a TFT-LCD gate driver with power supply for TFT-LCD driver. Because this gate driver has a level shift circuit for logic input, it can output a high gate scanning voltage in response to a CMOS-level input. This ICs can generate the levels which TFT-LCD driver need, from 2.7 V.

FEATURES

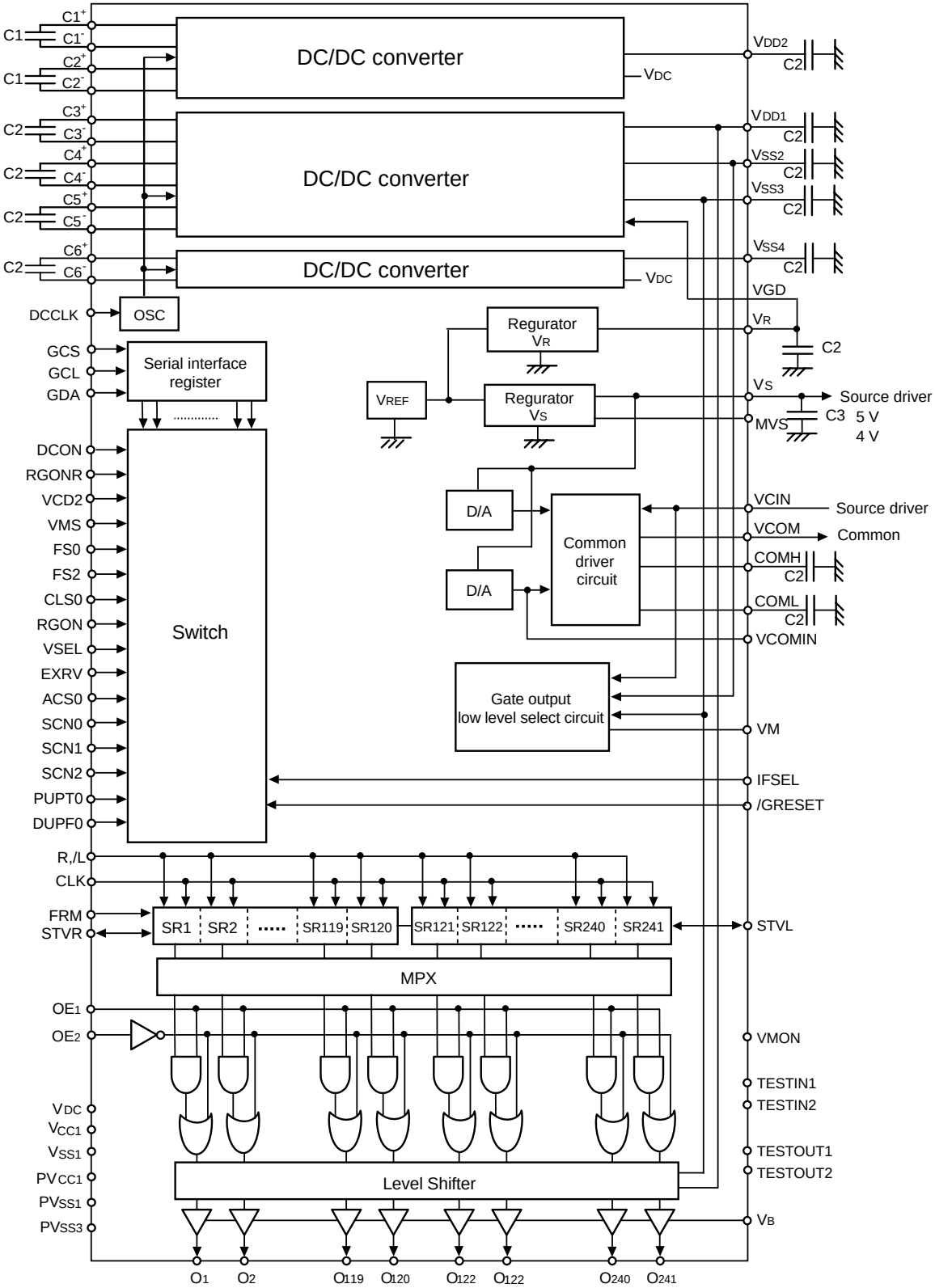
- High breakdown voltage output (V_{DD1}-V_{SS3} = 40 V MAX.)
- 2.7 V CMOS level input
- Number of output: 241 output selectable
- To generate 4 levels from single voltage input
- To integrate regulator circuit for source driver
- Mode setting from source driver: Serial I/F or pin control
- On-chip VCOM driver
- On-chip gate output low-level selector

ORDERING INFORMATION

Part number	Package
μPD161644P	Chip

Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representatives.

1. BLOCK DIAGRAM/SYSTEM DIAGRAM

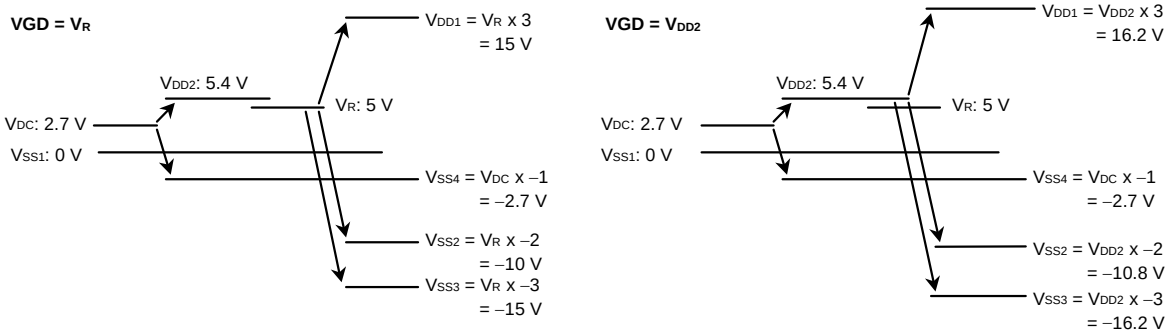


Remarks 1. /xxx indicates active low signal.

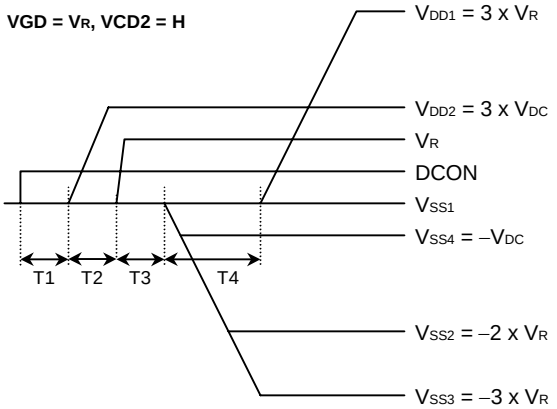
2. Level Shifter (LS): Interfaces between 2.7 V CMOS level and V_{DD1} to V_B level.

1.1 Boost Voltage Construction

The boost voltage generated in μPD161644 is shown below.



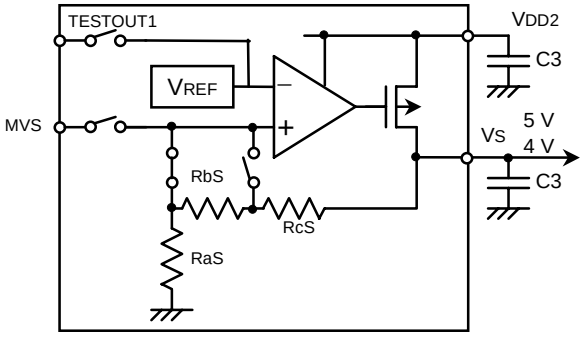
1.2 Boost Voltage Auto Start and Rising Order



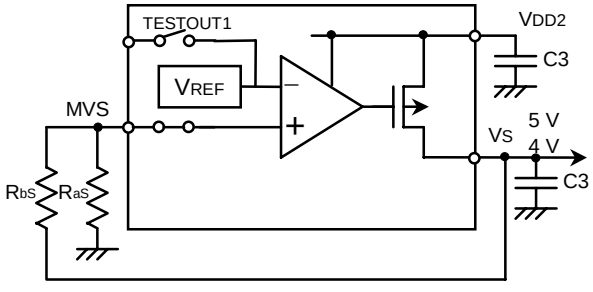
T1, T2, T3, T4: changeable by PUPT0, PUPT01, DUPF0, DUPF1

1.3 VS_AMP Circuit

VS_AMP circuits are shown below.



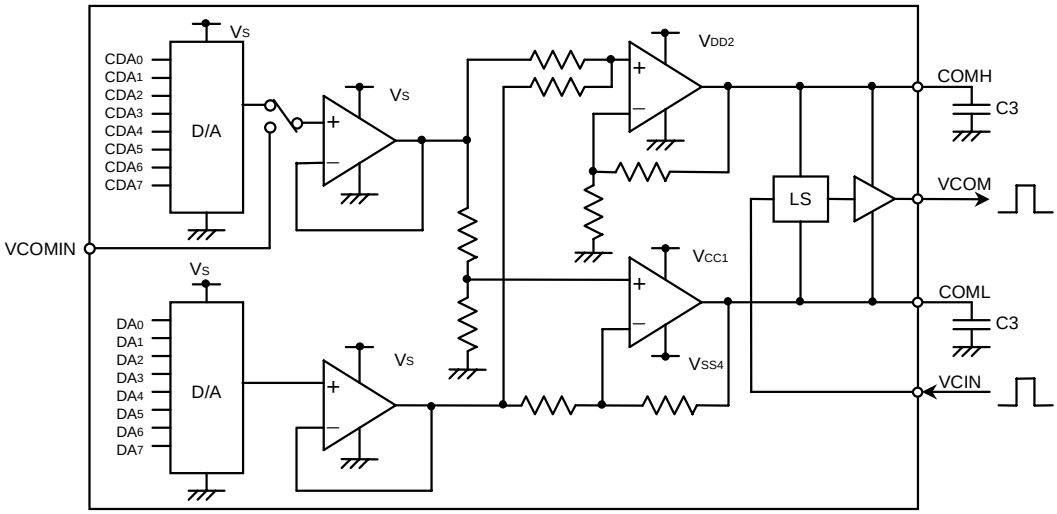
Internal Resistor Mode
EXRV = L



External Resistor Mode
EXRV = H
$V_S = (1+ \frac{R_{bS}}{R_{aS}})V_{REF}$

1.4 Common Drive Circuit

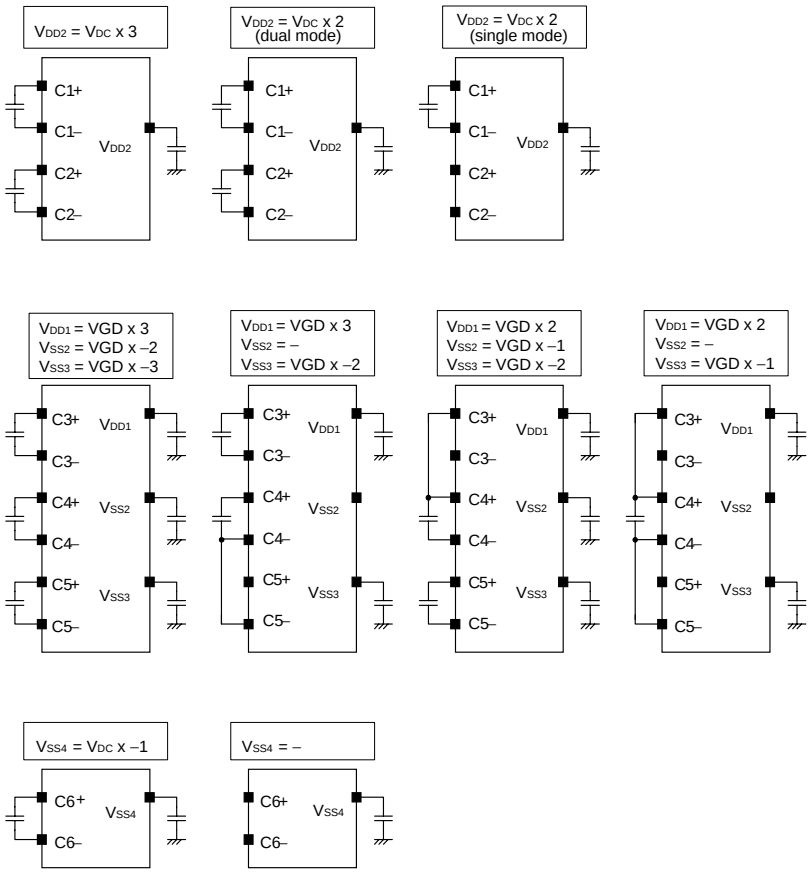
The common drive circuit is shown below.



1.5 Variable Boost Steps

The boost steps of V_{DD1}, V_{SS2}, V_{SS3} are selected according to how the external capacitor is connected.

The examples of connection are shown below. V_S is selected as a boost reference voltage in these examples (short between the V_S and VGD pins).



2. PIN CONFIGURATION (Pad Layout)

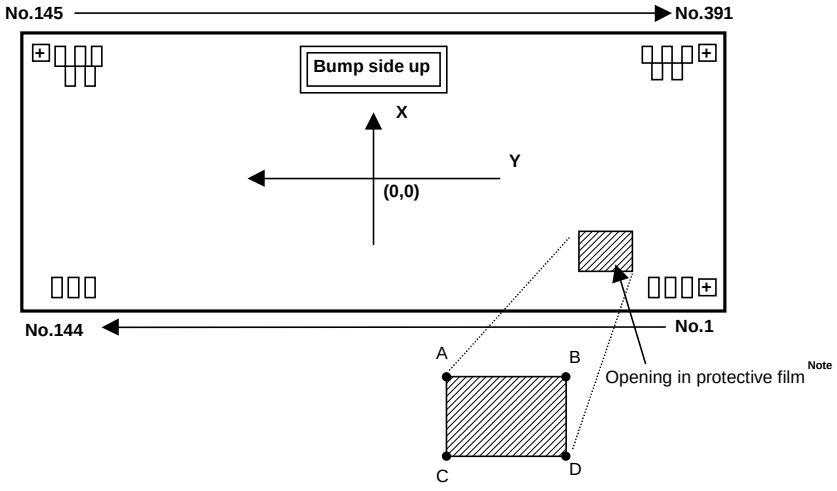
Chip size: 2.8 x 9.4 mm^2

Bump size

Input/Left/Right (includes DUMMY of input side) : 100 x 40 μm^2

Output (includes DUMMY output side) : 86 x 35 μm^2

Figure 2-1. Chip Schematic



Note A part of the protective film on the chip surface is absent to enable a transistor check at shipment. The position of this opening is indicated by the shaded section in the above chip schematic. The specific coordinates of this opening are as follows.

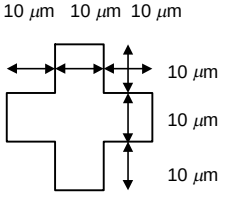
	X (μm)	Y (μm)
A	–847.74	–3143.37
B	–687.75	–3143.37
C	–687.75	–3438.78
D	–847.74	–3438.78

Alignment Mark Coordinate (mark center, unit: mm)

X	Y	Shape of Alignment Mark
–1.125	–4.5705	Type A
0.9705	4.5495	Type B
0.9705	–4.5495	Type B

Alignment Mark

Type A



Type B

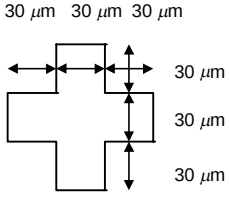


Table 2-1. Pad Layout (1/3)

PADTYPE : BUMP SIZE 100 μm x 40 μm			
GATE INPUTS			
PAD No.	PAD NAME	X [mm]	Y [mm]
1	DUMMY	-1.242	-4.5500
2	TESTOUT2	-1.242	-4.4900
3	TESTIN2	-1.242	-4.4300
4	TESTIN1	-1.242	-4.3700
5	TESTOUT1	-1.242	-4.3100
6	PVCC1	-1.242	-4.2500
7	DUPF0	-1.242	-4.1900
8	PUPT0	-1.242	-4.1300
9	SCN2	-1.242	-4.0700
10	SCN1	-1.242	-4.0100
11	SCN0	-1.242	-3.9500
12	ACS0	-1.242	-3.8900
13	EXRV	-1.242	-3.8300
14	VSEL	-1.242	-3.7700
15	CLS0	-1.242	-3.7100
16	FS2	-1.242	-3.6500
17	FS0	-1.242	-3.5900
18	VMS	-1.242	-3.5300
19	RGONR	-1.242	-3.4700
20	PVSS1	-1.242	-3.4100
21	PVSS3	-1.242	-3.3500
22	VMON	-1.242	-3.2900
23	DUMMY	-1.242	-3.2300
24	PVCC1	-1.242	-3.1700
25	R,/L	-1.242	-3.1100
26	IFSEL	-1.242	-3.0500
27	PVSS1	-1.242	-2.9900
28	VCOMIN	-1.242	-2.9200
29	VCOM	-1.242	-2.8500
30	VCOM	-1.242	-2.7900
31	VCOM	-1.242	-2.7300
32	COML	-1.242	-2.6600
33	COML	-1.242	-2.6000
34	COMH	-1.242	-2.5300
35	COMH	-1.242	-2.4700
36	VM	-1.242	-2.4000
37	VM	-1.242	-2.3400
38	VB	-1.242	-2.2700
39	VB	-1.242	-2.2100
40	VSS3	-1.242	-2.1400
41	VSS3	-1.242	-2.0800
42	VSS3	-1.242	-2.0200
43	VSS4	-1.242	-1.9500
44	VSS4	-1.242	-1.8900
45	VSS4	-1.242	-1.8300
46	VSS2	-1.242	-1.7600
47	VSS2	-1.242	-1.7000
48	VSS2	-1.242	-1.6400
49	C6-	-1.242	-1.5700
50	C6-	-1.242	-1.5100
51	C6+	-1.242	-1.4400
52	C6+	-1.242	-1.3800
53	C5-	-1.242	-1.3100
54	C5-	-1.242	-1.2500
55	C5+	-1.242	-1.1800
56	C5+	-1.242	-1.1200
57	C4-	-1.242	-1.0500
58	C4-	-1.242	-0.9900
59	C4+	-1.242	-0.9200
60	C4+	-1.242	-0.8600
61	C3-	-1.242	-0.7900
62	C3-	-1.242	-0.7300
63	C3+	-1.242	-0.6600
64	C3+	-1.242	-0.6000
65	VDD1	-1.242	-0.5300
66	VDD1	-1.242	-0.4700
67	VDD1	-1.242	-0.4100
68	C2-	-1.242	-0.3400
69	C2-	-1.242	-0.2800
70	C2-	-1.242	-0.2200
71	C2-	-1.242	-0.1600
72	C2+	-1.242	-0.0900

PADTYPE : BUMP SIZE 100 μm x 40 μm			
GATE INPUTS			
PAD No.	PAD NAME	X [mm]	Y [mm]
73	C2+	-1.242	-0.0300
74	C2+	-1.242	0.0300
75	C2+	-1.242	0.0900
76	C1-	-1.242	0.1600
77	C1-	-1.242	0.2200
78	C1-	-1.242	0.2800
79	C1-	-1.242	0.3400
80	C1+	-1.242	0.4100
81	C1+	-1.242	0.4700
82	C1+	-1.242	0.5300
83	C1+	-1.242	0.5900
84	VDD2	-1.242	0.6600
85	VDD2	-1.242	0.7200
86	VDD2	-1.242	0.7800
87	VDD2	-1.242	0.8400
88	VSS1	-1.242	0.9100
89	VSS1	-1.242	0.9700
90	VSS1	-1.242	1.0300
91	VSS1	-1.242	1.0900
92	DUMMY	-1.242	1.1600
93	VDC	-1.242	1.2300
94	VDC	-1.242	1.2900
95	VDC	-1.242	1.3500
96	VDC	-1.242	1.4100
97	VDC	-1.242	1.4700
98	VDC	-1.242	1.5300
99	VDC	-1.242	1.5900
100	VDC	-1.242	1.6500
101	VCC1	-1.242	1.7200
102	VCC1	-1.242	1.7800
103	VCC1	-1.242	1.8400
104	VCC1	-1.242	1.9000
105	VSS1	-1.242	1.9700
106	VSS1	-1.242	2.0300
107	VSS1	-1.242	2.0900
108	VSS1	-1.242	2.1500
109	VSS1	-1.242	2.2100
110	VSS1	-1.242	2.2700
111	VR	-1.242	2.3400
112	VR	-1.242	2.4000
113	VR	-1.242	2.4600
114	VGD	-1.242	2.5300
115	VGD	-1.242	2.5900
116	VGD	-1.242	2.6500
117	MVS	-1.242	2.7200
118	VS	-1.242	2.7900
119	VS	-1.242	2.8500
120	VS	-1.242	2.9100
121	VS	-1.242	2.9700
122	VS	-1.242	3.0300
123	VS	-1.242	3.0900
124	DUMMY	-1.242	3.1600
125	PVCC1	-1.242	3.2300
126	VCD2	-1.242	3.3000
127	RGON	-1.242	3.3700
128	DCON	-1.242	3.4400
129	FRM	-1.242	3.5100
130	VCIN	-1.242	3.5800
131	PVSS1	-1.242	3.6500
132	/GRESET	-1.242	3.7200
133	GCS	-1.242	3.7900
134	GCL	-1.242	3.8600
135	GDA	-1.242	3.9300
136	STVR	-1.242	4.0000
137	STVL	-1.242	4.0700
138	DCCLK	-1.242	4.1400
139	CLK	-1.242	4.2100
140	OE1	-1.242	4.2800
141	OE2	-1.242	4.3500
142	DUMMY	-1.242	4.4200
143	VSS3	-1.242	4.4900
144	DUMMY	-1.242	4.5600

Table 2-1. Pad Layout (2/3)

PADTYPE : BUMP SIZE 86 μm x 35 μm			
GATE OUTPUTS 35 μm pitch			
PAD No.	PAD NAME	X [mm]	Y [mm]
145	DUMMY	1.249	4.3050
146	DUMMY	1.127	4.2700
147	DUMMY	1.249	4.2350
148	O241	1.127	4.2000
149	O240	1.249	4.1650
150	O239	1.127	4.1300
151	O238	1.249	4.0950
152	O237	1.127	4.0600
153	O236	1.249	4.0250
154	O235	1.127	3.9900
155	O234	1.249	3.9550
156	O233	1.127	3.9200
157	O232	1.249	3.8850
158	O231	1.127	3.8500
159	O230	1.249	3.8150
160	O229	1.127	3.7800
161	O228	1.249	3.7450
162	O227	1.127	3.7100
163	O226	1.249	3.6750
164	O225	1.127	3.6400
165	O224	1.249	3.6050
166	O223	1.127	3.5700
167	O222	1.249	3.5350
168	O221	1.127	3.5000
169	O220	1.249	3.4650
170	O219	1.127	3.4300
171	O218	1.249	3.3950
172	O217	1.127	3.3600
173	O216	1.249	3.3250
174	O215	1.127	3.2900
175	O214	1.249	3.2550
176	O213	1.127	3.2200
177	O212	1.249	3.1850
178	O211	1.127	3.1500
179	O210	1.249	3.1150
180	O209	1.127	3.0800
181	O208	1.249	3.0450
182	O207	1.127	3.0100
183	O206	1.249	2.9750
184	O205	1.127	2.9400
185	O204	1.249	2.9050
186	O203	1.127	2.8700
187	O202	1.249	2.8350
188	O201	1.127	2.8000
189	O200	1.249	2.7650
190	O199	1.127	2.7300
191	O198	1.249	2.6950
192	O197	1.127	2.6600
193	O196	1.249	2.6250
194	O195	1.127	2.5900
195	O194	1.249	2.5550
196	O193	1.127	2.5200
197	O192	1.249	2.4850
198	O191	1.127	2.4500
199	O190	1.249	2.4150
200	O189	1.127	2.3800
201	O182	1.249	2.3450
202	O187	1.127	2.3100
203	O186	1.249	2.2750
204	O185	1.127	2.2400
205	O184	1.249	2.2050
206	O183	1.127	2.1700
207	O182	1.249	2.1350
208	O181	1.127	2.1000
209	O180	1.249	2.0650
210	O179	1.127	2.0300
211	O178	1.249	1.9950
212	O177	1.127	1.9600
213	O176	1.249	1.9250
214	O175	1.127	1.8900
215	O174	1.249	1.8550
216	O173	1.127	1.8200

PADTYPE : BUMP SIZE 86 μm x 35 μm			
GATE OUTPUTS 35 μm pitch			
PAD No.	PAD NAME	X [mm]	Y [mm]
217	O172	1.249	1.7850
218	O171	1.127	1.7500
219	O170	1.249	1.7150
220	O169	1.127	1.6800
221	O168	1.249	1.6450
222	O167	1.127	1.6100
223	O166	1.249	1.5750
224	O165	1.127	1.5400
225	O164	1.249	1.5050
226	O163	1.127	1.4700
227	O162	1.249	1.4350
228	O161	1.127	1.4000
229	O160	1.249	1.3650
230	O159	1.127	1.3300
231	O158	1.249	1.2950
232	O157	1.127	1.2600
233	O156	1.249	1.2250
234	O155	1.127	1.1900
235	O154	1.249	1.1550
236	O153	1.127	1.1200
237	O152	1.249	1.0850
238	O151	1.127	1.0500
239	O150	1.249	1.0150
240	O149	1.127	0.9800
241	O148	1.249	0.9450
242	O147	1.127	0.9100
243	O146	1.249	0.8750
244	O145	1.127	0.8400
245	O144	1.249	0.8050
246	O143	1.127	0.7700
247	O142	1.249	0.7350
248	O141	1.127	0.7000
249	O140	1.249	0.6650
250	O139	1.127	0.6300
251	O138	1.249	0.5950
252	O137	1.127	0.5600
253	O136	1.249	0.5250
254	O135	1.127	0.4900
255	O134	1.249	0.4550
256	O133	1.127	0.4200
257	O132	1.249	0.3850
258	O131	1.127	0.3500
259	O130	1.249	0.3150
260	O129	1.127	0.2800
261	O128	1.249	0.2450
262	O127	1.127	0.2100
263	O126	1.249	0.1750
264	O125	1.127	0.1400
265	O124	1.249	0.1050
266	O123	1.127	0.0700
267	O122	1.249	0.0350
268	O121	1.127	0.0000
269	O120	1.249	-0.0350
270	O119	1.127	-0.0700
271	O118	1.249	-0.1050
272	O117	1.127	-0.1400
273	O116	1.249	-0.1750
274	O115	1.127	-0.2100
275	O114	1.249	-0.2450
276	O113	1.127	-0.2800
277	O112	1.249	-0.3150
278	O111	1.127	-0.3500
279	O110	1.249	-0.3850
280	O109	1.127	-0.4200
281	O108	1.249	-0.4550
282	O107	1.127	-0.4900
283	O106	1.249	-0.5250
284	O105	1.127	-0.5600
285	O104	1.249	-0.5950
286	O103	1.127	-0.6300
287	O102	1.249	-0.6650
288	O101	1.127	-0.7000

Table 2-1. Pad Layout (3/3)

PADTYPE : BUMP SIZE 86 μm x 35 μm			
GATE OUTPUTS 35 μm pitch			
PAD No.	PAD NAME	X [mm]	Y [mm]
289	O100	1.249	-0.7350
290	O99	1.127	-0.7700
291	O98	1.249	-0.8050
292	O97	1.127	-0.8400
293	O96	1.249	-0.8750
294	O95	1.127	-0.9100
295	O94	1.249	-0.9450
296	O93	1.127	-0.9800
297	O92	1.249	-1.0150
298	O91	1.127	-1.0500
299	O90	1.249	-1.0850
300	O89	1.127	-1.1200
301	O88	1.249	-1.1550
302	O87	1.127	-1.1900
303	O86	1.249	-1.2250
304	O85	1.127	-1.2600
305	O84	1.249	-1.2950
306	O83	1.127	-1.3300
307	O82	1.249	-1.3650
308	O81	1.127	-1.4000
309	O80	1.249	-1.4350
310	O79	1.127	-1.4700
311	O78	1.249	-1.5050
312	O77	1.127	-1.5400
313	O76	1.249	-1.5750
314	O75	1.127	-1.6100
315	O74	1.249	-1.6450
316	O73	1.127	-1.6800
317	O72	1.249	-1.7150
318	O71	1.127	-1.7500
319	O70	1.249	-1.7850
320	O69	1.127	-1.8200
321	O68	1.249	-1.8550
322	O67	1.127	-1.8900
323	O66	1.249	-1.9250
324	O65	1.127	-1.9600
325	O64	1.249	-1.9950
326	O63	1.127	-2.0300
327	O62	1.249	-2.0650
328	O61	1.127	-2.1000
329	O60	1.249	-2.1350
330	O59	1.127	-2.1700
331	O58	1.249	-2.2050
332	O57	1.127	-2.2400
333	O56	1.249	-2.2750
334	O55	1.127	-2.3100
335	O54	1.249	-2.3450
336	O53	1.127	-2.3800
337	O52	1.249	-2.4150
338	O51	1.127	-2.4500
339	O50	1.249	-2.4850
340	O49	1.127	-2.5200
341	O48	1.249	-2.5550
342	O47	1.127	-2.5900
343	O46	1.249	-2.6250
344	O45	1.127	-2.6600
345	O44	1.249	-2.6950
346	O43	1.127	-2.7300
347	O42	1.249	-2.7650
348	O41	1.127	-2.8000
349	O40	1.249	-2.8350
350	O39	1.127	-2.8700
351	O38	1.249	-2.9050
352	O37	1.127	-2.9400
353	O36	1.249	-2.9750
354	O35	1.127	-3.0100
355	O34	1.249	-3.0450
356	O33	1.127	-3.0800
357	O32	1.249	-3.1150
358	O31	1.127	-3.1500
359	O30	1.249	-3.1850
360	O29	1.127	-3.2200

PADTYPE : BUMP SIZE 86 μm x 35 μm			
GATE OUTPUTS 35 μm pitch			
PAD No.	PAD NAME	X [mm]	Y [mm]
361	O28	1.249	-3.2550
362	O27	1.127	-3.2900
363	O26	1.249	-3.3250
364	O25	1.127	-3.3600
365	O24	1.249	-3.3950
366	O23	1.127	-3.4300
367	O22	1.249	-3.4650
368	O21	1.127	-3.5000
369	O20	1.249	-3.5350
370	O19	1.127	-3.5700
371	O18	1.249	-3.6050
372	O17	1.127	-3.6400
373	O16	1.249	-3.6750
374	O15	1.127	-3.7100
375	O14	1.249	-3.7450
376	O13	1.127	-3.7800
377	O12	1.249	-3.8150
378	O11	1.127	-3.8500
379	O10	1.249	-3.8850
380	O9	1.127	-3.9200
381	O8	1.249	-3.9550
382	O7	1.127	-3.9900
383	O6	1.249	-4.0250
384	O5	1.127	-4.0600
385	O4	1.249	-4.0950
386	O3	1.127	-4.1300
387	O2	1.249	-4.1650
388	O1	1.127	-4.2000
389	DUMMY	1.249	-4.2350
390	DUMMY	1.127	-4.2700
391	DUMMY	1.249	-4.3050

3. PIN FUNCTIONS

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Symbol	Pin Name	Pad No.	I/O	Function
V_{DC}	DC/DC converter reference voltage	93 to 100	–	Reference voltage input pin for DC/DC converter.
V_{CC1}	Logic reference voltage	101 to 104	–	2.5 to 3.3 V LS (level shifter) reference voltage input pin.
V_{SS1}	Ground	88 to 91, 105 to 110	–	Connect to the system ground.
VGD	Power supply input for DC/DC converter	114 to 116	Input	Reference voltage input pin for V_{DD1}, V_{SS1} to V_{SS4} boost. Connect to any of V_{DD2}, V_R or V_S.
V_{DD1}	DC/DC converter output	65 to 67	Output	Boost output voltage of DC/DC converter (VGD x 2 or x 3). The boost step number of V_{DD1} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to the function of VGD pin.
V_{DD2}	DC/DC converter output	84 to 87	Output	Boost output voltage of DC/DC converter (V_{DC} x 2 or x 3). The boost step number of V_{DD2} can be set using VCD2.
V_{SS2}	DC/DC converter output	46 to 48	Output	Boost output voltage of DC/DC converter (VGD x –1 or x –2). The boost step number of V_{SS2} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to the function of VGD pin.
V_{SS3}	DC/DC converter output	40 to 42, 143	Output	Boost output voltage of DC/DC converter (VGD x –2 or x –3). The boost step number of V_{SS3} is selected according to how the external capacitor is connected. The boost reference voltage can be set using VGD. Refer to VGD pin function.
V_{SS4}	DC/DC converter output	43 to 45	Output	Boost output voltage of DC/DC converter (V_{DC} x –1).
VM	Gate output low level select voltage	36, 37	Output	The voltage level of V_{SS2} or V_{SS3} is output synchronized with the VCIN input. VCIN = 0: Output the voltage level of V_{SS3} VCIN = 1: Output the voltage level of V_{SS2} The timing chart is shown in **Figure 3-1**.
V_B	Driver negative voltage	38, 39	Input	Negative voltage of output buffer. This is the input pin of the liquid crystal driver negative voltage. Input the negative power supply of the gate output. V_B pin connection examples are shown in **Figure 3-2**.
C_1^+, C_1^- C_2^+, C_2^- C_3^+, C_3^- C_4^+, C_4^- C_5^+, C_5^- C_6^+, C_6^-	Capacitor connect pin for boost	80 to 83, 76 to 79, 72 to 75, 68 to 71, 63, 64, 61, 62, 59, 60, 57, 58, 55, 56, 53, 54, 51, 52, 49, 50	Output	To connect booster for DC/DC converter. For the recommended values of the capacitance and withstanding voltage of each capacitor, refer to **9. RECOMMENDED CAPACITANCE VALUES OF EXTERNAL CAPACITOR.**
V_R	Power supply output for DC/DC converter	111 to 113	Output	Positive power supply voltage output for the DC/DC converter. The V_R output voltage can be changed by setting VRSEL0 to VRSEL2.

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Symbol	Pin Name	Pad No.	I/O	Function
V_S	Positive power output supply for driver	118 to 123	Output	Positive power supply voltage output for source driver. The V_S output voltage can be changed by setting VSEL0 to VSEL2.
MVS	External resistor input	117	Input	Any output voltage can be set by connecting an external resistor. <EXRV = 0> Leave open. <EXRV = 1> Connect to external resistor.
PV_{CC1}	Pull-up voltage	6, 24, 125	–	Pull-up voltage for mode setting pin.
PV_{SS1}	Pull-down voltage	20, 27, 131	–	Pull-down voltage for mode setting pin.
PV_{SS3}	Pull-down voltage	21	–	Pull-down voltage for mode setting pin.
CLK	Shift clock input	139	Input	Shift clock input pin of the internal shift resistor. The contents of internal shift resistor are shifted at the rising edge of CLK. Connect to GCLK pin of source driver.
STVR, STVL	Start pulse input/output pin	136, 137	I/O	Input/output pin of the internal shift resistor. Start pulse signal is read at the rising edge of shift clock CLK and a scan signal is output from the driver output pin. The valid level of the STVR/STVL pin is determined by the setting of STVSEL. When STVSEL = L, the pulse becomes low level at the falling edge of the 240th shift clock CLK and high level at falling edge of the 241st clock.
OE_1	Enable input	140	Input	If the level selected by OE1SEL is input, the driver output is fixed to low level (When OE1SEL = L the driver output is fixed to low level if a low level is input). However, the shift resistor is not cleared. And, output enable actuation is asynchronous in the clock. Connect to GOE_1 pin of source driver.
OE_2	Enable input	141	Input	If the level selected by OE2SEL is input, the driver output is fixed to high level (When OE2SEL = L the driver output is fixed to low level if a high level is input). However, the shift resistor is not cleared. And, output enable actuation is asynchronous in the clock. Connect to GOE_2 pin of source driver.
R,/L	Shift direction control	25	Input	The shift direction control pin of shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STVR input, $O_1 \rightarrow O_{241}$, STVL output R,/L = L (left shift) : STVL input, $O_{241} \rightarrow O_1$, STVR output
FRM	Frame signal input	129	Input	Input frame reverse signals. Connect to GFRAME pin of source driver.
DCCLK	Clock input for DC/DC converter	138	Input	To input the external clock for the DC/DC converter. This pin is valid only when CLS0 = 1 and CLS1 = 1. In other settings, leave open.

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Symbol	Pin Name	Pad No.	I/O	Function
O_1 to O_{241}	Driver output pins	388 to 148	Output	Scan signal output pins that drive the gate electrode of a TFT-LCD. The status of each output pin changes in synchronization with the rising edge of shift clock CLK. The output voltage of the driver is V_{DD1} to V_B.
COMH	Common high level output	34, 35	Output	<COMON = 1> High level of common voltage is output. The voltage level changes accordance with DA_0 to DA_7 and CDA_0 to CDA_7. <COMON = 0> Leave open when not using it.
COML	Common low level output	32, 33	Output	<COMON = 1> Low level of common voltage is output. The voltage level changes accordance with DA_0 to DA_7 and CDA_0 to CDA_7. <COMON = 0> Leave open when not using it.
VCOM	Common output	29 to 31	Output	<COMON = 1> The common voltage synchronized with the VCIN input is output. Connect to common pin of panel. <COMON = 0> Leave open when not using it.
VCOMIN	VCOM center voltage input	28	Input	VCOM center voltage input pin. Leave open when COMSEL = 0. <COMSEL = 0> Internal D/A is valid. <COMSEL = 1> VCOMIN input voltage is valid.
VCIN	Common pulse input	130	Input	To input common pulse. Connect to VCOUT3 pin of source driver. Fix this pin to low when not using it.
/GRESET	Reset input	132	Input	Reset input pin. Connect to /GRESET pin of source driver. If /GRESET is made low, the serial interface is initialized (the register values are not initialized). A reset operation is executed according to the level of the /GRESET signal. Be sure to execute a reset using this pin at power application.
IFSEL	Interface selection	26	Input	The serial interface input switching pin. <IFSEL = 0> Serial interface input. The DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0 to SCN2, PUPT0, DUPF0 pins should be left open. <IFSEL = 1> Control pin input. The GCS, GCL, GDA pins should be left open.
GCS	Chip select input	133	Input	<IFSEL = 0> To input chip select signals. Connect to GCS pin of source driver. <IFSEL = 1> Leave open.
GCL	Serial clock input	134	Input	<IFSEL = 0> To input serial clock signals. Connect to GCL pin of source driver. <IFSEL = 1> Leave open.
GDA	Serial data input	135	Input	<IFSEL = 0> To input serial data signals. Connect to GDA pin of source driver. <IFSEL = 1> Leave open.

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Symbol	Pin Name	Pad No.	I/O	Function
DCON	DC/DC converter control	128	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> The DC/DC converter ON/OFF control signal is input. Connect to the DCON pin of the source driver. <DCON = 0> DC/DC converter OFF <DCON = 1> DC/DC converter ON
RGONR	V_R regulator control	19	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> The V_R regulator ON/OFF control signal is input. <RGONR = 0> V_R regulator OFF <RGONR = 1> V_R regulator ON
VCD2	V_{DD2} boost selection	126	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> The V_{DD2} boost step number select pin. <VCD2 = 0> $V_{DD2} = V_{DC}$ x 2 <VCD2 = 1> $V_{DD2} = V_{DC}$ x 3
VMS	V_{DD2} boost selection	18	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> V_{DD2} boost mode select pin. <VMS = 0> V_{DD2}: single boost mode <VMS = 1> V_{DD2}: dual boost mode
FS0	V_{DD2}, V_{SS4} boost frequency selection in scan mode	17	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> V_{DD2}, V_{SS4} boost frequency select pin in scan mode. <FS0 = 0 > f_{OSC}/2 <FS0 = 1 > f_{OSC}/4
FS2	V_{DD1}, V_{SS2}, V_{SS3} boost frequency selection in scan mode	16	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> V_{DD1}, V_{SS2}, V_{SS3} boost frequency select pin in scan mode. <FS2 = 0 > f_{OSC}/2 <FS2 = 1, > f_{OSC}/4
CLS0	DC/DC OSC frequency selection	15	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> Select pin of the OSC oscillation frequency for DC/DC converter. <CLS0 = 0> f_{OSC} = 25 kHz, DCCLK: Open <CLS0 = 1> External CK input mode
RGON	V_S regulator control	127	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> The V_S regulator ON/OFF control signal is input. Connect this pin to the RGON pin of the source driver. <RGON = 0> V_S regulator OFF <RGON = 1> V_S regulator ON
VSEL	V_S regulator voltage selection	14	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> Select pin of output voltage for V_S regulator. <VSEL = 1> V_S = 4 V <VSEL = 0> V_S = 5 V
EXRV	V_S regulating resistor selection	13	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> Select pin of external resistor for V_S regulator. <EXRV = 0> Internal resistor setting mode. <EXRV = 1> Any output voltage can be set by connecting MVS to an external resistor.

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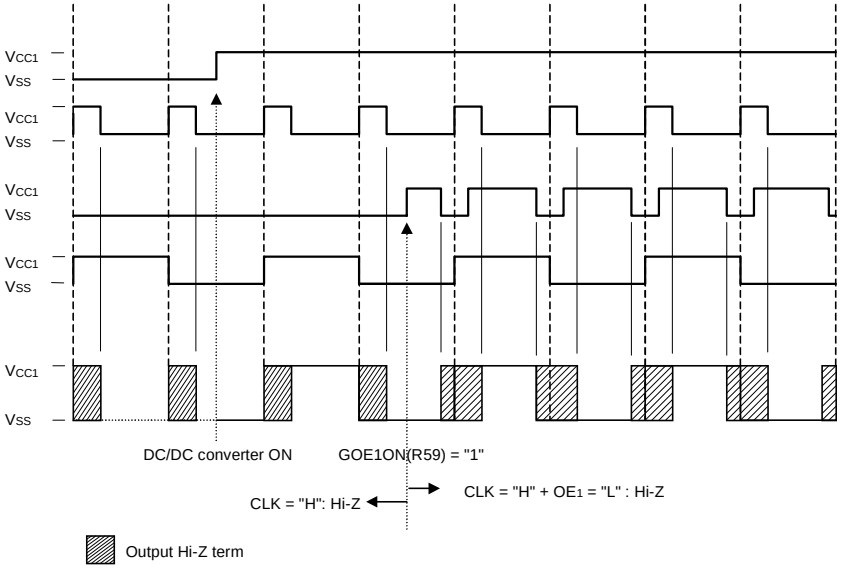
Symbol	Pin Name	Pad No.	I/O	Function
ACS0	Amp. current selection in scan mode	12	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> Amp. current select pin in scan mode. <ACS0 = 0> Amp. current = 5 μA <ACS0 = 1> Amp. current = 15 μA
SCN0, SCN1, SCN2	Gate scan selection	11, 10, 9	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> Select pin of gate scan order. <SCN0 = 1, SCN1 = 1, SCN2 = 1> MODE1 <SCN0 = 1, SCN1 = 1, SCN2 = 0> MODE2 <SCN0 = 1, SCN1 = 0, SCN2 = 1> MODE3 <SCN0 = 1, SCN1 = 0, SCN2 = 0> MODE4 <SCN0 = 0, SCN1, SCN2 = x> MODE5
PUPT0	Setting pin of DC/DC converter power on time	8	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> This pin sets the rising time of V_{DD1}, V_{DD2}, V_{SS2} to V_{SS4} at DC/DC converter power on time.
DUPF0	Operating frequency setting pin at DC/DC converter power on	7	Input	<IFSEL = 0> Leave open (Internal resistors are valid). <IFSEL = 1> This pin sets the operating frequency at DC/DC converter power on time. <DUPT0 = 0> f_{OSC}/8 <DUPT0 = 1> f_{OSC}/16
VMON	Stand-by current reduction control pin	22	Input	The standby current reduction control pin. <VMON = PV_{SS3}> Normal mode. A quiescent current of about 0.5 μA is consumed in standby mode. When the V_{CC1} voltage drops, the driver output pins are fixed to ALL-High. <VMON = PV_{CC1}> Standby current reduction mode. Makes the quiescent current consumed in standby mode 0. When the V_{CC1} voltage drops, the driver output pins are undefined.
TESTOUT1	V_{REF} reference voltage output	5	Output	The V_{REF} voltage measurement pin. Leave open.
TESTIN1, TESTIN2	TEST input pin	4, 3	Input	Test input pins. Leave open.
TESTOUT2	TEST output pin	2	Output	Test output pin. Leave open.
DUMMY	Dummy	1, 23, 92, 124, 142, 144 to 147, 389 to 391	–	Dummy data

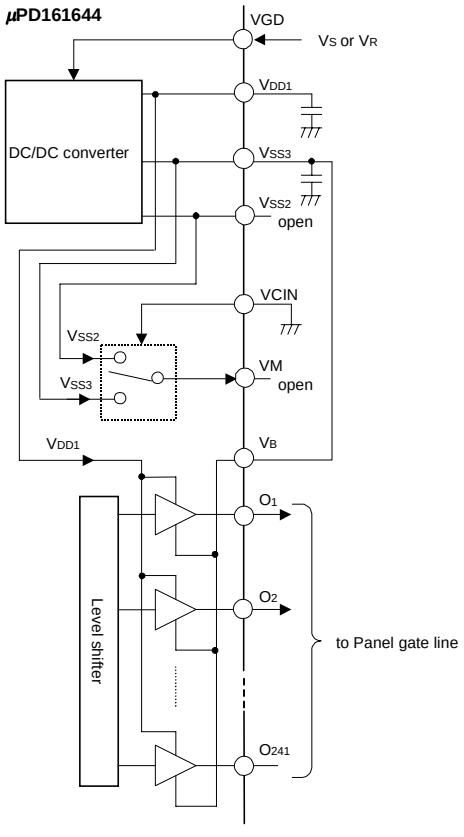
Figure 3-1. VM signal Timing Chart



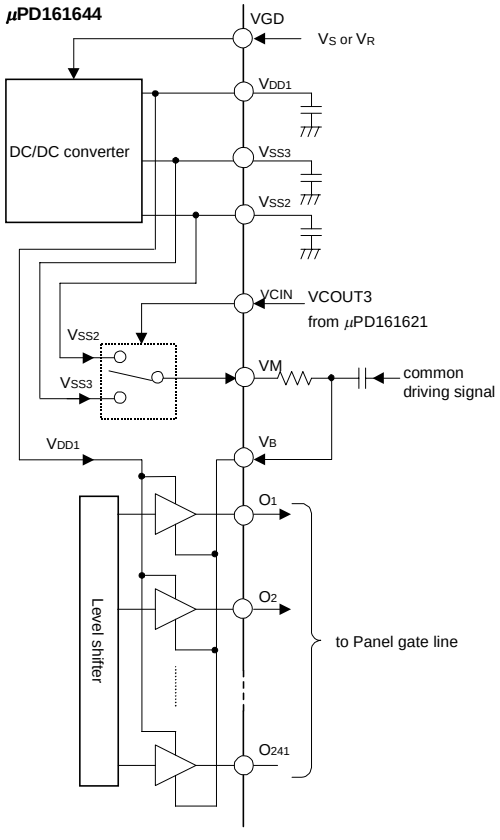
Remark Hi-Z (High impedance)

Figure 3-2. Examples of V_B pin connection

(a) When the negative voltage level of the gate output is set to V_{SS3}



(b) When the negative voltage level of the gate output is switched between V_{SS2} and V_{SS3}



4. COMMAND

4.1 Command List

										Data bit							
7	6	5	4	3	2	1	0	Rn	Register	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	1	0	0	0	R24	DC/DC operation setting		RGONR	VS4ON	VS3ON	VS2ON	VD2ON	VD1ON	DCON
0	0	0	1	1	0	0	1	R25	DC/DC step setting				VRSEL2	VRSEL1	VRSEL0	VMS	VCD2
0	0	0	1	1	0	1	0	R26	DC/DC oscillation setting		FUP	CLS1	CLS0	FS3	FS2	FS1	FS0
0	0	0	1	1	0	1	1	R27	Regulator output setting		ACS1	ACS0	EXRV	VSEL2	VSEL1	VSEL0	RGON
0	0	0	1	1	1	0	0	R28	LPM setting		LACS1	LACS0	LFS3	LFS2	LFS1	LFS0	LPM
0	0	0	1	1	1	0	1	R29	Gate scan setting			OE2SEL	OE1SEL	STVSEL	SCN2	SCN1	SCN0
0	0	0	1	1	1	1	0	R30	Gate mode setting				COMHI	COMSEL	COMON	NLINE2	NLINE1
0	0	0	1	1	1	1	1	R31	Common amplitude setting	DA_7	DA_6	DA_5	DA_4	DA_3	DA_2	DA_1	DA_0
0	0	1	0	0	0	0	0	R32	Common center setting	CDA_7	CDA_6	CDA_5	CDA_4	CDA_3	CDA_2	CDA_1	CDA_0
0	0	1	0	0	0	0	1	R33	DC/DC power on setting			PONM	PON	DUPF1	DUPF0	PUPT1	PUPT0
0	0	1	0	0	0	1	0	R34	Reset								RES

4.2 Command Description

Reset the internal data at power application by inputting a low level to the /GRESET pin.

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Resistor	Bit	Symbol	Reset	Function	Description
R24	D_0	DCON	0	DC/DC converter control	Control ON/OFF of DC/DC converter. <DCON = 0> DC/DC converter OFF <DCON = 1> DC/DC converter ON
	D_1	VD1ON	0	V_{DD1} boost control	Control ON/OFF of V_{DD1} boost. <VD1ON = 0> V_{DD1} boost OFF <VD1ON = 1> V_{DD1} boost ON
	D_2	VD2ON	0	V_{DD2} boost control	Control V_{DD2} boost ON/OFF. <VD2ON = 0> V_{DD2} boost OFF <VD2ON = 1> V_{DD2} boost ON
	D_3	VS2ON	0	V_{SS2} boost control	Control V_{SS2} boost ON/OFF. <VS2ON = 0> V_{SS2} boost OFF <VS2ON = 1> V_{SS2} boost ON
	D_4	VS3ON	0	V_{SS3} boost control	Control V_{SS3} boost ON/OFF. <VS3ON = 0> V_{SS3} boost OFF <VS3ON = 1> V_{SS3} boost ON
	D_5	VS4ON	0	V_{SS4} boost control	Control V_{SS4} boost ON/OFF. <VS4ON = 0> V_{SS4} boost OFF <VS4ON = 1> V_{SS4} boost ON
	D_6	RGONR	0	V_R regulator control	Control ON/OFF of V_R regulator. <RGONR = 0> V_R regulator OFF <RGONR = 1> V_R regulator ON

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Resistor	Bit	Symbol	Reset	Function	Description
R25	D_0	VCD2	0	V_{DD2} boost selection	Select the number of V_{DD2} boost step (x2/x3). <VCD2 = 0> $V_{DD2} = V_{DC}$ x 2 <VCD2 = 1> $V_{DD2} = V_{DC}$ x 3
	D_1	VMS	1	V_{DD2} boost mode selection	Select V_{DD2} boost mode. <VMS = 0> V_{DD2} = Single boost mode <VMS = 1> V_{DD2} = Dual boost mode
	D_2	VRSEL0	1	V_R regulator output voltage selection	Select output voltage of V_R regulator. When IFSEL = 1, V_R is fixed to 5 V. <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 0> V_R = 3 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 0> V_R = 3.5 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 0> V_R = 4 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 0> V_R = 4.5 V <VRSEL0 = 0, VRSEL1 = 0, VRSEL2 = 1> V_R = 4.75 V <VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 1> V_R = 5 V <VRSEL0 = 0, VRSEL1 = 1, VRSEL2 = 1> V_R = 5.25 V <VRSEL0 = 1, VRSEL1 = 1, VRSEL2 = 1> V_R = 5.5 V
	D_3	VRSEL1	0		
	D_4	VRSEL2	1		
R26	D_0	FS0	1	V_{DD2}, V_{SS4} boost frequency selection in scan mode	Select V_{DD2}, V_{SS4} boost frequency in scan mode. When IFSEL = 1, FS1 is fixed to 0. <FS0 = 0, FS1 = 0> f_{OSC}/2 <FS0 = 1, FS1 = 0> f_{OSC}/4 <FS0 = 0, FS1 = 1> f_{OSC}/8 <FS0 = 1, FS1 = 1> f_{OSC}/16
	D_1	FS1	0		
	D_2	FS2	1	V_{DD1}, V_{SS2}, V_{SS3} boost frequency selection in scan mode	Select V_{DD1}, V_{SS2}, V_{SS3} boost frequency in scan mode. When IFSEL = 1, FS3 is fixed to 0. <FS2 = 0, FS3 = 0> f_{OSC}/2 <FS2 = 1, FS3 = 0> f_{OSC}/4 <FS2 = 0, FS3 = 1> f_{OSC}/8 <FS2 = 1, FS3 = 1> f_{OSC}/16
	D_3	FS3	0		
	D_4	CLS0	1	DC/DC OSC frequency selection	Select oscillation frequency of OSC for DC/DC converter. When IFSEL = 1, CLS1 is fixed to 1. <CLS0 = 0, CLS1 = 0> f_{OSC} = 18 kHz, DCCLK: Open <CLS0 = 1, CLS1 = 0> f_{OSC} = 25 kHz, DCCLK: Open <CLS0 = 0, CLS1 = 1> f_{OSC} = 37 kHz, DCCLK: Open <CLS0 = 1, CLS1 = 1> External CK input mode
	D_5	CLS1	0		
	D_6	FUP	0	Switching of DC/DC OSC frequency	Select oscillation frequency of OSC for DC/DC converter. When IFSEL = 1, the frequency is fixed to f_{OSC}. <FUP = 0> f_{OSC} <FUP = 1> f_{OSC} x 2

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Resistor	Bit	Symbol	Reset	Function	Description
R27	D_0	RGON	0	V_S regulator control	Control ON/OFF of V_S regulator. <RGON = 0> V_S regulator OFF <RGON = 1> V_S regulator ON
	D_1	VSEL0	1	V_S regulator output voltage selection	Select the output voltage of V_S regulator. VSEL0 = 0: V_S = 5 V, VSEL = 1: V_S = 4 V when IFSEL = 1. <VSEL0 = 0, VSEL1 = 0, VSEL2 = 0> V_S = 3 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 0> V_S = 3.5 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 0> V_S = 4 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 0> V_S = 4.5 V <VSEL0 = 0, VSEL1 = 0, VSEL2 = 1> V_S = 4.75 V <VSEL0 = 1, VSEL1 = 0, VSEL2 = 1> V_S = 5 V <VSEL0 = 0, VSEL1 = 1, VSEL2 = 1> V_S = 5.25 V <VSEL0 = 1, VSEL1 = 1, VSEL2 = 1> V_S = 5.5 V
	D_2	VSEL1	0		
	D_3	VSEL2	1		
	D_4	EXRV	0	V_S regulator resistor selection	Select external resistor of V_S regulator. <EXRV = 0> Internal resistor mode <EXRV = 1> Connect external resistor to MVS and set any level of voltage
	D_5	ACS0	0	Amp. current selection in scan mode	Select Amp. current of V_R and V_S regulators in scan mode. When IFSEL = 1, ACS1 is fixed to 0. <ACS0 = 0, ACS1 = 0> Amp. current = 5 μA <ACS0 = 0, ACS1 = 1> Amp. current = 10 μA <ACS0 = 1, ACS1 = 0> Amp. current = 15 μA <ACS0 = 1, ACS1 = 1> Amp. current = 30 μA
	D_6	ACS1	0		
R28	D_0	LPM	0	Low power mode control	Control in low power mode. When IFSEL = 1, LPM is fixed to 0. <LPM = 0> Scan mode <LPM = 1> Low power mode
	D_1	LFS0	0	V_{DD2}, V_{SS4} boost frequency selection in low power mode	Select boost frequency of V_{DD2}, V_{SS4} in low power mode. <LFS0 = 0, LFS1 = 0> f_{OSC}/8 <LFS0 = 1, LFS1 = 0> f_{OSC}/16 <LFS0 = 0, LFS1 = 1> f_{OSC}/32 <LFS0 = 1, LFS1 = 1> f_{OSC}/64
	D_2	LFS1	0		
	D_3	LFS2	0	V_{DD1}, V_{SS2}, V_{SS3} boost frequency selection in low power mode	Select boost frequency of V_{DD1}, V_{SS2}, V_{SS3} in low power mode. <LFS2 = 0, LFS3 = 0> f_{OSC}/8 <LFS2 = 1, LFS3 = 0> f_{OSC}/16 <LFS2 = 0, LFS3 = 1> f_{OSC}/32 <LFS2 = 1, LFS3 = 1> f_{OSC}/64
	D_4	LFS3	0		
	D_5	LACS0	0	Amp. current selection in low power mode	Select Amp. current in low power mode. <LACS0 = 0, LACS1 = 0> Amp. current = 1.25 μA <LACS0 = 0, LACS1 = 1> Amp. current = 2.5 μA <LACS0 = 1, LACS1 = 0> Amp. current = 5 μA <LACS0 = 1, LACS1 = 1> Amp. current = 7.5 μA
	D_6	LACS1	0		

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Resistor	Bit	Symbol	Reset	Function	Description
R29	D_0	SCN0	1	Gate scan selection	Select scan order of gate scan. <SCN0 = 1, SCN1 = 1, SCN2 = 1> MODE1 <SCN0 = 1, SCN1 = 1, SCN2 = 0> MODE2 <SCN0 = 1, SCN1 = 0, SCN2 = 1> MODE3 <SCN0 = 1, SCN1 = 0, SCN2 = 0> MODE4 <SCN0 = 0, SCN1, SCN2 = X> MODE5
	D_1	SCN1	1		
	D_2	SCN2	1		
	D_3	STVSEL	0	Start pulse input/output valid level selection	Select start pulse input/output valid level to STVR/STVL. But there is no pin to select start pulse input/output valid level. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <STVSEL= 0> Low level is valid. <STVSEL= 1> High level is valid.
	D_4	OE1SEL	0	OE_1 valid level selection	Select valid level of OE_1. But there is no pin to select valid level of OE_1. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <OE1SEL = 0> OE_1 = Low, gate output OFF <OE1SEL = 1> OE_1 = High, gate output OFF
	D_5	OE2SEL	0	OE_2 valid level selection	Select valid level of OE_2. There is no pin to select valid level of OE_2. When IFSEL = H (When using control pins), low-fixed is valid. Refer to **4.3 Command Setting Values When IFSEL = H (When Using Control Pins).** <OE2SEL = 0> OE_2 = Low, gate output ON <OE2SEL = 1> OE_2 = High, gate output ON
R30	D_0	NLINE1	1	Gate mode selection	Select 1-line skip, 2-line skip or N frame inversion of a gate scan. When IFSEL = 1, this is fixed to normal mode. <NLINE1 = 1, NLINE2 = 1> Normal mode <NLINE1 = 1, NLINE2 = 0> 1-line skip mode <NLINE1 = 0, NLINE2 = 1> 2-line skip mode <NLINE1 = 0, NLINE2 = 0> N frame inversion
	D_1	NLINE2	1		
	D_2	COMON	0	COM output control	Control ON/OFF of COM output. When IFSEL = 1, COMON is fixed to 0. <COMON = 0> COM_AMP, COM output OFF <COMON = 1> COM_AMP, COM output ON
	D_3	COMSEL	0	VCOM center input selection	Select VCOM center voltage input. <COMSEL = 0> Internal D/A is valid. <COMSEL = 1> VCOMIN input voltage is valid.
	D_4	COMHI	0	VCOM output selection	Select VCOM output. <COMHI = 0> VCOM = Hi-Z <COMHI = 1> VCOM = Output

(5/5)

Resistor	Bit	Symbol	Reset	Function	Description
R31	D_0 to D_7	DA_0 to DA_7	0	COM amplitude control	Control COM output amplitude using 8-bit D/A.
R32	D_0 to D_7	CDA_0 to CDA_7	0	COM center level control	Control COM output center level using 8-bit D/A.
R33	D_0	PUPT0	0	Setting of DC/DC converter power on time	This pin sets the ON time of V_{DD1} and V_{DD2}, V_{SS2} to V_{SS4}, and RGON when the DC/DC converter is started up. This setting is valid only when PONM = 1. When IFSEL = 1, PUPT1 is fixed to 0.
	D_1	PUPT1	1		
	D_2	DUPF0	1	Setting of DC/DC converter power on operating frequency	This pin sets the DC/DC operating frequency when the DC/DC converter is started up. When IFSEL = 1, DUPF1 is fixed to 0. <DUPF0 = 0, DUPF1 = 0> $f_{OSC}/8$ <DUPF0 = 1, DUPF1 = 0> $f_{OSC}/16$ <DUPF0 = 0, DUPF1 = 1> $f_{OSC}/2$ <DUPF0 = 1, DUPF1 = 1> $f_{OSC}/4$
	D_3	DUPF1	0		
	D_4	PON	0	Switching DC/DC converter startup operating frequency	This pin selects the V_{DD1}, V_{DD2}, V_{SS2} to V_{SS4} rising operating frequency when the DC/DC converter is started up. This setting is valid only when PONM = 1. <PON = 0> Normal operation <PON = 1> Power on operation startup operation
	D_5	PONM	1	DC/DC operation startup operating selection	Select internal/external sequence of DC/DC converter power on operation. <PONM = 0> External sequence <PONM = 1> Internal sequence
R34	D_0	RES	–	Command reset	This is the command reset function. A command reset must always be executed after power application. All contents of registers are initialized. This bit is automatically cleared after command reset execution (RES = 1). It is therefore not necessary to set this bit to 0 again by software (to select normal operation). Also, because this bit changes from 1 to 0 very quickly following a command reset, it is not necessary to leave any time before setting the next command after setting a command reset. <RES = 0> Normal operation <RES = 1> Command reset

4.3 Command Setting Values When IFSEL = H (When Using Control Pins)

(1/2)

Register	Bit	Symbol	Setting value	Conditions
R24	D_0	DCON	–	DCON control pin is valid.
	D_1	VD1ON	1	<VD1ON = 1> V_{DD1} boost ON
	D_2	VD2ON	1	<VD2ON = 1> V_{DD2} boost ON
	D_3	VS2ON	1	<VS2ON = 1> V_{SS2} boost ON
	D_4	VS3ON	1	<VS3ON = 1> V_{SS3} boost ON
	D_5	VS4ON	0	<VS4ON = 0> V_{SS4} boost OFF
	D_6	RGONR	–	RGONR control pin is valid.
R25	D_0	VCD2	–	VCD2 control pin is valid.
	D_1	VMS	–	VMS control pin is valid.
	D_2	VRSEL0	1	<VRSEL0 = 1, VRSEL1 = 0, VRSEL2 = 1 > V_R = 5 V
	D_3	VRSEL1	0	
	D_4	VRSEL2	1	
R26	D_0	FS0	–	FS0 control pin is valid.
	D_1	FS1	0	<FS0 = 0> f_{OSC}/2, <FS0 = 1> f_{OSC}/4
	D_2	FS2	–	FS2 control pin is valid.
	D_3	FS3	0	<FS2 = 0> f_{OSC}/2, <FS2 = 1> f_{OSC}/4
	D_4	CLS0	–	CLS1 control pin is valid.
	D_5	CLS1	1	<CLS0 = 0> f_{OSC} = 37 kHz, <CLS0 = 1> External
	D_6	FUP	0	<FUP = 0> f_{OSC}
R27	D_0	RGON	–	RGON control pin is valid.
	D_1	VSEL0	–	VSEL control pin is valid.
	D_2	VSEL1	–	<VSEL = 0> V_S = 5 V
	D_3	VSEL2	–	<VSEL = 1> V_S = 4 V
	D_4	EXRV	–	EXRV control pin is valid.
	D_5	ACS0	–	ACS0 control pin is valid.
	D_6	ACS1	0	<ACS0 = 0> Current = 5 μA, <ACS0 = 1> Current = 15 μA
R28	D_0	LPM	0	<LPM = 0> Scan mode
	D_1, D_2	LFS0, LFS1	0,1	<LFS0 = 0, LFS1 = 1> f_{OSC}/32
	D_3, D_4	LFS2, LFS3	0,1	<LFS2 = 0, LFS3 = 1> f_{OSC}/32
	D_5, D_6	LACS0, LACS1	0,1	<LACS0 = 0, LACS1 = 1> Amp. current = 2.5 μA
R29	D_0	SCN0	–	SCN0 control pin is valid
	D_1	SCN1	–	SCN1 control pin is valid
	D_2	SCN2	–	SCN2 control pin is valid
	D_3	STVSEL	0	<STVSEL = 0> low-level is valid
	D_4	OE1SEL	0	<OE1SEL = 0> OE_1 = low-level, gate output OFF
	D_5	OE2SEL	0	<OE2SEL = 0> OE_2 = low-level, gate output ON

Remark When IFSEL = H (when using the control pins), the GCS, GCL, and GDA pins are pulled down to low level, so be sure to leave these pins open.

When IFSEL = L (when using the serial interface), DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0, SCN1, SCN2, PUPT0, DUPF0 pins should be left open.

(2/2)

Register	Bit	Symbol	Setting value	Conditions
R30	D_0	NLINE1	1	<NLINE = 1, NLINE2 = 1> normal mode
	D_1	NLINE2	1	
	D_2	COMON	0	<COMON = 0> COM_AMP, COM output OFF
R31	D_0 to D_7	DA_0 to DA_7	0	<DA_0 to DA_7> 0
R32	D_0 to D_7	CDA_0 to CDA_7	0	<CDA_0 to CDA_7> 0
R33	D_0	PUPT0	–	PUPT0 control pin is valid
	D_1	PUPT1	0	<PUPT0 = 0> RGONR = 2048/fosc <PUPT0 = 1> RGONR = 256/fosc
	D_2	DUPF0	–	DUPF0 control pin is valid
	D_3	DUPF1	0	<DUPF0 = 0> fosc/8 <DUPF0 = 1> fosc/16
	D_4	PON	1	<PON = 1> Internal sequence
	D_5	PONM	1	<PONM = 1> Internal sequence
R34	D_0	RES	0	<RES = 0> Normal operation

Remark When IFSEL = H (when using the control pins), the GCS, GCL, and GDA pins are pulled down to low level, so be sure to leave these pins open.

When IFSEL = L (when using the serial interface), DCON, RGONR, VCD2, VMS, FS0, FS2, CLS0, RGON, VSEL, EXRV, ACS0, SCN0, SCN1, SCN2, PUPT0, DUPF0 pins should be left open.

5. MODE DESCRIPTION

5.1 Output Mode and Gate Scan Selection

Normal mode: NLINE1 =1, NLINE2 = 1

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1→240, 241	241	240
	L	241→2,1	1	2
MODE2	H	1→121 • 241→123, 122	122	123
	L	122→241 • 121→2, 1	1	2
MODE3	H	1→161 • 241→163, 162	162	163
	L	162→241 • 161→2, 1	1	2
MODE4	H	1→201, 241→203, 202	202	203
	L	202→241 • 201→2, 1	1	2
MODE5	H	1, 241, 2, 240, 3, 239…..118, 124, 119, 123, 120, 122, 121	121	122
	L	121, 122, 120, 123, 119, 124…..4, 239, 3, 240, 2, 241, 1	1	241

1-line step mode: NLINE1 =1, NLINE2 = 0

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1, 3, 5…235, 237, 239, 241 • 2, 4, 6…236, 238, 240	241	240
	L	241, 239, 237…7, 5, 3, 1 • 240, 238, 236…6, 4, 2	1	2
MODE2	H	1, 3, 5…117, 119, 121 • 240, 238, 236…128, 126, 124, 122, • 2, 4, 6…116, 118, 120 • 241, 239, 237…127, 125, 123	122	123
	L	122, 124, 126…236, 238, 240 • 121, 119, 117…7, 5, 3, 1, • 123, 125, 127…237, 239, 241 • 120, 118, 116…6, 4, 2	1	2
MODE3	H	1, 3, 5…157, 159, 161 • 240, 238, 236…168, 166, 164, 162 • 2, 4, 6…156, 158, 160 • 241, 239, 237…167, 165, 163	162	163
	L	162, 164, 166…236, 238, 240 • 161, 159, 157…7, 5, 3, 1, • 163, 165, 167…237, 239, 241 • 160, 158, 156…6, 4, 2	1	2
MODE4	H	1, 3, 5…197, 199, 201 • 240, 238, 236…208, 206, 204, 202, • 2, 4, 6…196, 198, 200 • 241, 239, 237…207, 205, 203	202	203
	L	202, 204, 206…236, 238, 240 • 201, 199, 197…7, 5, 3, 1, • 203, 205, 207…237, 239, 241 • 200, 198, 196…6, 4, 2	1	2

2-line step mode: NLINE1 = 0, NLINE2 = 1

Scan MODE	R,/L	Scan direction	Dummy output	Cascade output
MODE1	H	1, 4, 7…232, 235, 238, 241 • 2, 5, 8…233, 236, 239 • 3, 6, 9…234, 237, 240	241	240
	L	241, 238, 235…10, 7, 4, 1 • 240, 237, 234…9, 6, 3 • 239, 236, 233…8, 5, 2	1	2
MODE2	H	1, 4, 7…115, 118, 121 • 239, 236, 233…131, 128, 125, 122, • 2, 5, 8…113, 116, 119 • 241, 238, 235…130, 127, 124 • 3, 6, 9…114, 117, 120 • 240, 237, 234,…129, 126, 123	122	123
	L	122, 125, 128…233, 236, 239 • 121, 118, 115…10, 7, 4, 1, • 123, 126, 129…234, 237, 240 • 120, 117, 114…9, 6, 3 • 124, 127, 130…235, 238, 241 • 119, 116, 113…8, 5, 2	1	2
MODE3	H	1, 4, 7…154, 157, 160 • 240, 237, 234…171, 168, 165, 162, • 2, 5, 8…155, 158, 161 • 239, 236, 233…170, 167, 164 • 3, 6, 9…153, 156, 159 • 241, 238, 235…169, 166, 163	162	163
	L	162, 165, 168…234, 237, 240 • 160, 157, 154…10, 7, 4, 1, • 163, 166, 169…235, 238, 241 • 159, 156, 153…9, 6, 3 • 164, 167, 170…233, 236, 239 • 161, 158, 155..8, 5, 2	1	2
MODE4	H	1, 4, 7…193, 196, 199 • 241, 238, 235…211, 208, 205, 202, • 2, 5, 8…194, 197, 200 • 240, 237, 234…210, 207, 204 • 3, 6, 9…195, 198, 201 • 239, 236, 233…209, 206, 203	202	203
	L	202, 205, 208…235, 238, 241 • 199, 196, 193…10, 7, 4, 1, • 203, 206, 209…2337, 236, 239 • 201, 198, 195…9, 6, 3 • 204, 207, 210…234, 240, 200 • 197, 194…8, 5, 2	1	2

N-frame reverse: NLINE1 = 0, NLINE2 = 0

Scan MODE	R,/L	FMR	Scan direction	Dummy output	Cascade output
MODE1	H	1	1→240, 241	241	240
		0	241→2, 1 (reverse operation)	241	2
	L	1	241→2, 1	1	2
		0	1→240, 241 (reverse operation)	1	240

5.2 DC/DC OSC Frequency Selection

CLS0	CLS1	OSC oscillation frequency for DC/DC converter	DCCLK
0	0	fosc = 18 kHz	Open
1	0	fosc = 25 kHz	Open
0	1	fosc = 37 kHz	Open
1	1	fosc = External CK	External CK input

5.3 DC/DC Converter Control

DCON	VD1ON	VD2ON	VS2ON	VS3ON	VS4ON	State of V_{DD1}, V_{DD2}, V_{SS2}, V_{SS3}, V_{SS4}
0	x	x	x	x	x	V_{DD1}, V_{DD2}, V_{SS2}, V_{SS3}, V_{SS4}: OFF
1	0	–	–	–	–	V_{DD1}: OFF
1	1	–	–	–	–	V_{DD1}: ON
1	–	0	–	–	–	V_{DD2}: OFF
1	–	1	–	–	–	V_{DD2}: ON
1	–	–	0	–	–	V_{SS2}: OFF
1	–	–	1	–	–	V_{SS2}: ON
1	–	–	–	0	–	V_{SS3}: OFF
1	–	–	–	1	–	V_{SS3}: ON
1	–	–	–	–	0	V_{SS4}: OFF
1	–	–	–	–	1	V_{SS4}: ON

Remark x: 0 or 1

5.4 V_{DD2} Boost Selection

VCD2	V_{DD2}
0	V_{DC} x 2 boost
1	V_{DC} x 3 boost

5.5 Division Ratio Selection of the DC/DC Converter at Power on

PONM	PON	DUPF0	DUPF1	Division ratio of the DC/DC converter OSC frequency
1	x	0	0	Internal sequence: OSC = f_{OSC}/8
1	x	1	0	Internal sequence: OSC = f_{OSC}/16
1	x	0	1	Internal sequence: OSC = f_{OSC}/2
1	x	1	1	Internal sequence: OSC = f_{OSC}/4
0	1	0	0	External sequence: OSC = f_{OSC}/8
0	1	1	0	External sequence: OSC = f_{OSC}/16
0	1	0	1	External sequence: OSC = f_{OSC}/2
0	1	1	1	External sequence: OSC = f_{OSC}/4
0	0	x	x	Normal mode

Remark x: 0 or 1

5.6 DC/DC Converter Power on Time Selection

PONM	PON	PUPT0	PUPT1	VD2ON	RGONR	VS2ON to VS4ON	VD1ON	
1	x	0	0	16/f_{OSC}	2048/f_{OSC}	1.5 x 2048/f_{OSC}	2.5 x 2048/f_{OSC}	Internal sequence
1	x	1	0	16/f_{OSC}	256/f_{OSC}	1.5 x 256/f_{OSC}	2.5 x 256/f_{OSC}	Internal sequence
1	x	0	1	16/f_{OSC}	512/f_{OSC}	1.5 x 512/f_{OSC}	2.5 x 512/f_{OSC}	Internal sequence
1	x	1	1	16/f_{OSC}	1024/f_{OSC}	1.5 x 1024/f_{OSC}	2.5 x 1024/f_{OSC}	Internal sequence
0	1	x	x	External input	External input	External input	External input	External sequence
0	0	x	x					Normal mode

Remark x: 0 or 1

5.7 Division Ratio Selection of the DC/DC Converter OSC Frequency

LPM	FS0	FS1	FS2	FS3	LFS0	LFS1	LFS2	LFS3	Division ratio of the DC/DC converter OSC frequency
0	0	0	x	x	x	x	x	x	V_{DD2}, V_{SS4}: fosc/2
0	1	0	x	x	x	x	x	x	V_{DD2}, V_{SS4}: fosc/4
0	0	1	x	x	x	x	x	x	V_{DD2}, V_{SS4}: fosc/8
0	1	1	x	x	x	x	x	x	V_{DD2}, V_{SS4}: fosc/16
0	x	x	0	0	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}: fosc/2
0	x	x	1	0	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}: fosc/4
0	x	x	0	1	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}: fosc/8
0	x	x	1	1	x	x	x	x	V_{DD1}, V_{SS2}, V_{SS3}: fosc/16
1	x	x	x	x	0	0	x	x	V_{DD2}, V_{SS4}: fosc/8
1	x	x	x	x	1	0	x	x	V_{DD2}, V_{SS4}: fosc/16
1	x	x	x	x	0	1	x	x	V_{DD2}, V_{SS4}: fosc/32
1	x	x	x	x	1	1	x	x	V_{DD2}, V_{SS4}: fosc/64
1	x	x	x	x	x	x	0	0	V_{DD1}, V_{SS2}, V_{SS3}: fosc/8
1	x	x	x	x	x	x	0	0	V_{DD1}, V_{SS2}, V_{SS3}: fosc/16
1	x	x	x	x	x	x	1	1	V_{DD1}, V_{SS2}, V_{SS3}: fosc/32
1	x	x	x	x	x	x	1	1	V_{DD1}, V_{SS2}, V_{SS3}: fosc/64

Remark x: 0 or 1

5.8 Amp. Current Selection

RGON, RGONR	LPM	ACS0	ACS1	LACS0	LACS1	V_R condition	V_S condition	State of Circuit Current
0	x	x	x	x	x	V_{SS1}	V_{SS1}	Amp, CS Power OFF
1	0	0	0	x	x	Output	Output	Amp. current = 5 μA
1	0	0	1	x	x	Output	Output	Amp. current = 10 μA
1	0	1	0	x	x	Output	Output	Amp. current = 15 μA
1	0	1	1	x	x	Output	Output	Amp. current = 30 μA
1	1	x	x	0	0	Output	Output	Amp. current = 1.25 μA
1	1	x	x	0	1	Output	Output	Amp. current = 2.5 μA
1	1	x	x	1	0	Output	Output	Amp. current = 5 μA
1	1	x	x	1	1	Output	Output	Amp. current = 7.5 μA

Remark x: 0 or 1

5.9 V_R Regulator Selection Output

Register control

RGONR	VRSEL0	VRSEL1	VRSEL2	V_R
0	x	x	x	V_R regulator OFF (V_R = V_{SS1})
1	0	0	0	3 V : Internal resistor connection
1	1	0	0	3.5 V : Internal resistor connection
1	0	1	0	4 V : Internal resistor connection
1	1	1	0	4.5 V : Internal resistor connection
1	0	0	1	4.75 V: Internal resistor connection
1	1	0	1	5 V : Internal resistor connection
1	0	1	1	5.25 V: Internal resistor connection
1	1	1	1	5.5 V : Internal resistor connection

Remark x: 0 or 1

Pin control

RGONR	V_R
0	V_R regulator OFF ($V_R = V_{SS1}$)
1	5 V: Internal resistor connection

5.10 V_S Regulator Selection Output

Register control

RGON	EXRV	VSEL0	VSEL1	VSEL2	MVS condition	V_S
0	x	x	x	x	Hi-Z	V_S regulator OFF ($V_S = V_{SS1}$)
1	1	x	x	x	Amp.-input	External resistor connection
1	0	0	0	0	Hi-Z	3 V : Internal resistor connection
1	0	1	0	0	Hi-Z	3.5 V : Internal resistor connection
1	0	0	1	0	Hi-Z	4 V : Internal resistor connection
1	0	1	1	0	Hi-Z	4.5 V : Internal resistor connection
1	0	0	0	1	Hi-Z	4.75 V : Internal resistor connection
1	0	1	0	1	Hi-Z	5 V : Internal resistor connection
1	0	0	1	1	Hi-Z	5.25 V : Internal resistor connection
1	0	1	1	1	Hi-Z	5.5 V : Internal resistor connection

Remark x: 0 or 1

Pin control

RGON	VSEL	V_R
0	x	V_S regulator OFF ($V_S = V_{SS1}$)
1	0	5 V : Internal resistor connection
1	1	4 V : Internal resistor connection

Remark x: 0 or 1

5.11 Control of VM Output Control, VCOM Output

COMON	COMHI	DAC, COM_AMP	VCOM
0	x	OFF	Hi-Z
1	0	ON	Hi-Z
1	1	ON	Output

Remark x: 0 or 1

★ **5.12 VCOM Output Frequency Adjustment**

This is used to adjust the output amplitude of VCOM output. The VCOM output amplitude voltage (V_{COMpp}) can be adjusted as shown by the expression below using power supply control register 9 (R31), which is the output voltage of a D/A converter circuit for which V_S is the reference potential.

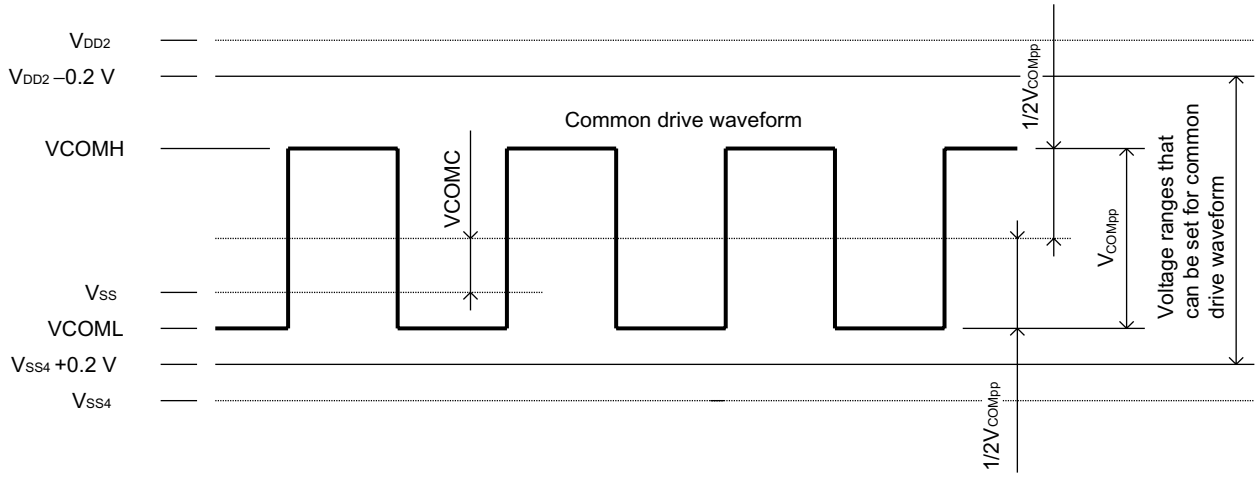
$V_{COMpp} = V_S \times 2 \times \{4/5 \times (DA_{R31}/255)\}$

Remark DA_{R31}: R31 setting values

The values of R31 that can be set are determined by the relationship of booster voltages V_{DD2} and V_{SS4} to the potential level of the actual common drive waveform after VCOM center adjustment.

Set the VCOM output amplitude voltage according to R31, the VCOM output center potential voltage setting level according to power supply control register 10 (R32), or the VCOM output center potential input from VCOMIN in the relationships shown in the figure below.

Figure 5-1. Voltage Ranges that can be set for Common Drive Waveform



<Conditions on common drive waveform voltage settings>

$V_{COMpp} \geq 2$ V

VCOMH $\leq V_{DD2} - 0.2$ V

VCOML $\geq V_{SS4} + 0.2$ V

Remark VCOMH = 1/2 V_{COMpp} + VCOMC

VCOML = 1/2 V_{COMpp} − VCOMC

VCOMC: R32 setting values [COMSEL(R30) = 0] or VCOMIN input voltage level [COMSEL (R30) = 1]

VCOM output amplitude voltage (V_{COMpp}) adjustment and D/A converter setting values

DA_7	DA_6	DA_5	DA_4	DA_3	DA_2	DA_1	DA_0	DA_{R31}	V_{COMpp} (V_S = 5 V)
0	0	0	0	0	0	0	0	0	0.0000 V (Setting prohibited)
0	0	0	0	0	0	0	1	1	0.0314 V (Setting prohibited)
0	0	0	0	0	0	1	0	2	0.0627 V (Setting prohibited)
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	0	1	1	1	1	1	0	62	1.9451 V (Setting prohibited)
0	0	1	1	1	1	1	1	63	1.9765 V (Setting prohibited)
0	1	0	0	0	0	0	0	64	2.0078 V
0	1	0	0	0	0	0	1	65	2.0392 V
0	1	0	0	0	0	1	0	66	2.0706 V
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253	7.9373 V
1	1	1	1	1	1	1	0	254	7.9686 V
1	1	1	1	1	1	1	1	255	8.0000 V

Remark The range in which the VCOM output amplitude can be varied is restricted by the output voltage of V_{DD2} and V_{SS4}.

★ **5.13 VCOM Output Center Adjustment**

This is used to adjust the center potential level of VCOM output. The VCOM output center potential voltage (V_{COMC}) can be adjusted as shown by the expression below using power supply control register 9 (R32), which is the output voltage of a D/A converter circuit for which V_S is the reference potential.

$V_{COMpp} = V_S \times \{4/5 \times (DA_{R32}/255)\}$

Remark DA_{R32}: R32 setting values

VCOM output center potential voltage (V_{COMC}) and D/A converter setting values

DA_7	DA_6	DA_5	DA_4	DA_3	DA_2	DA_1	DA_0	DA_{R31}	V_{COMC} (V_S = 5 V)
0	0	0	0	0	0	0	0	0	0.0000 V
0	0	0	0	0	0	0	1	1	0.0157 V
0	0	0	0	0	0	1	0	2	0.0314 V
0	0	0	0	0	0	1	1	3	0.0471 V
0	0	0	0	0	1	0	0	4	0.0627 V
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253	3.9686 V
1	1	1	1	1	1	1	0	254	3.9843 V
1	1	1	1	1	1	1	1	255	4.0000 V

Remark The range in which the VCOM output center can be varied is restricted by the output voltage of V_{DD2} and V_{SS4}.

The values of R32 that can be set are determined by the relationship of booster voltages V_{DD2} and V_{SS4} to the potential level of the actual common drive waveform due to VCOM output amplitude voltage (V_{COMpp}) adjustment.

Refer to **5.12 VCOM Output Frequency Adjustment** for the relationship between the VCOM output center potential voltage according to R32 and the VCOM output amplitude voltage (V_{COMpp}) according to power supply control register 9 (R31).

5.14 VCOM Center Adjustment Selection

The method of setting the center voltage of common drive waveform VCOM is selected according to the setting of COMSEL (R30).

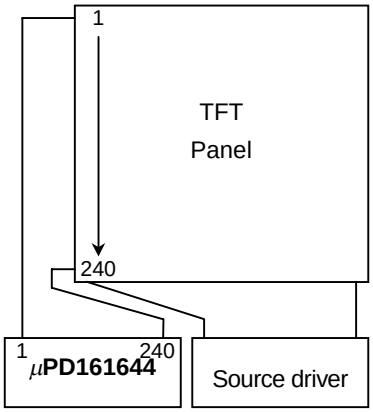
When COMSEL is set to 1, directly input the VCOM center voltage to the VOMIN pin from outside the IC.

COMSEL	VCOM center adjustment
0	Internal D/A is valid (R31 setting is valid).
1	VCOMIN input voltage is valid.

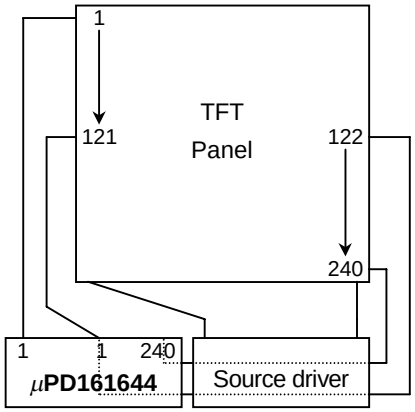
6. PANNEL CONNECTION EXAMPLES

[MODE1]

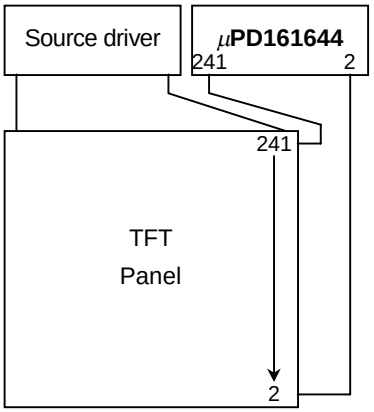
MODE1R (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 1)



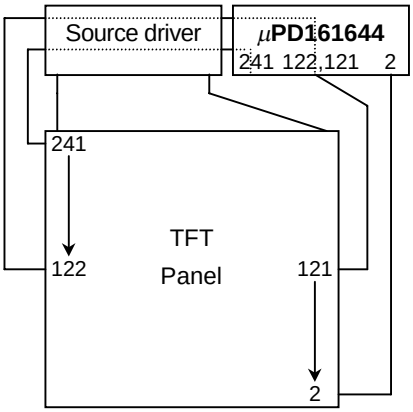
MODE1R (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 1)



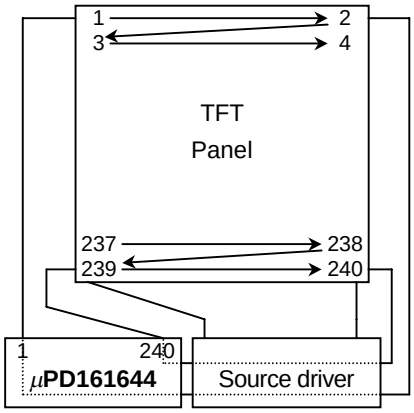
MODE1L (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 0)



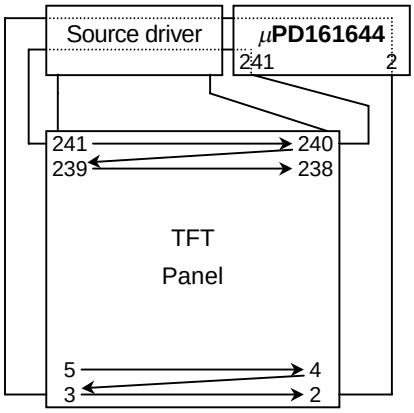
MODE1L (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 0)



MODE1R (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 1)

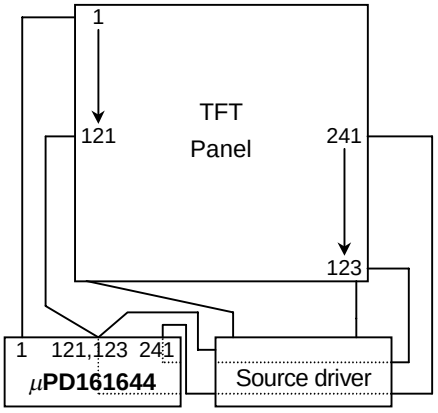


MODE1L (SCN0 = 1, SCN1 = 1, SCN2 = 1, R,/L = 0)

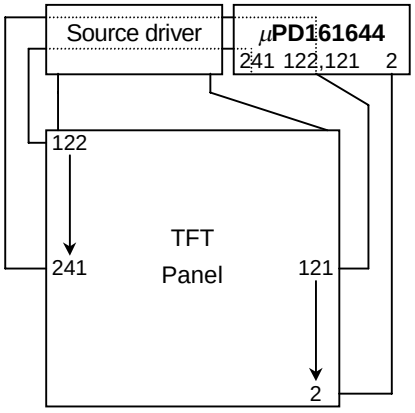


[MODE2]

MODE2R (SCN0 = 1, SCN1 = 1, SCN2 = 0, R,/L = 1)

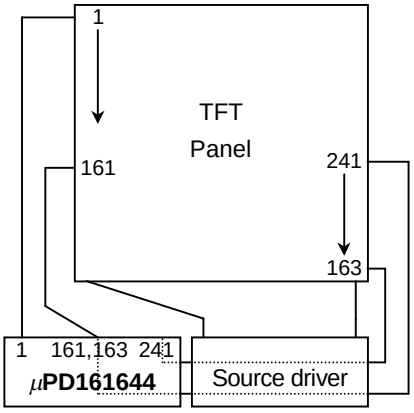


MODE2L (SCN0 = 1, SCN1 = 1, SCN2 = 0, R,/L = 0)

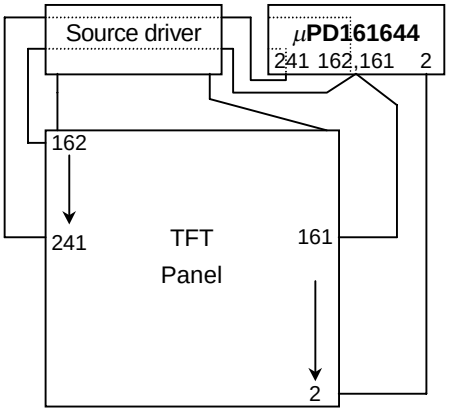


[MODE3]

MODE3R (SCN0 = 1, SCN1 = 0, SCN2 = 1, R,/L = 1)

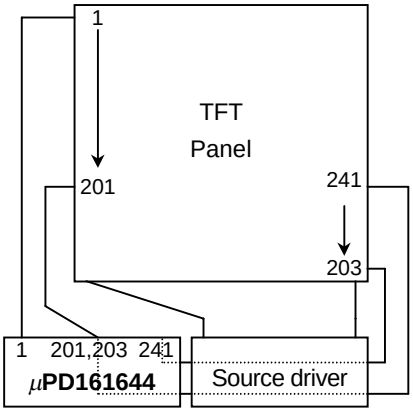


MODE3L (SCN0 = 1, SCN1 = 0, SCN2 = 1, R,/L = 0)

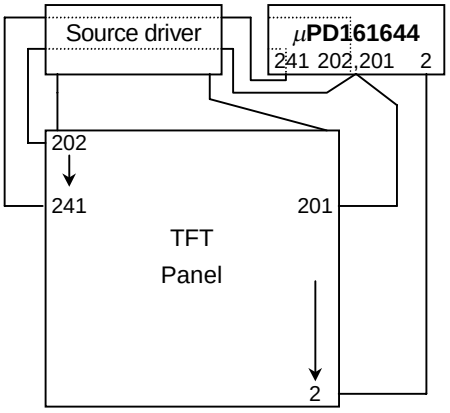


[MODE4]

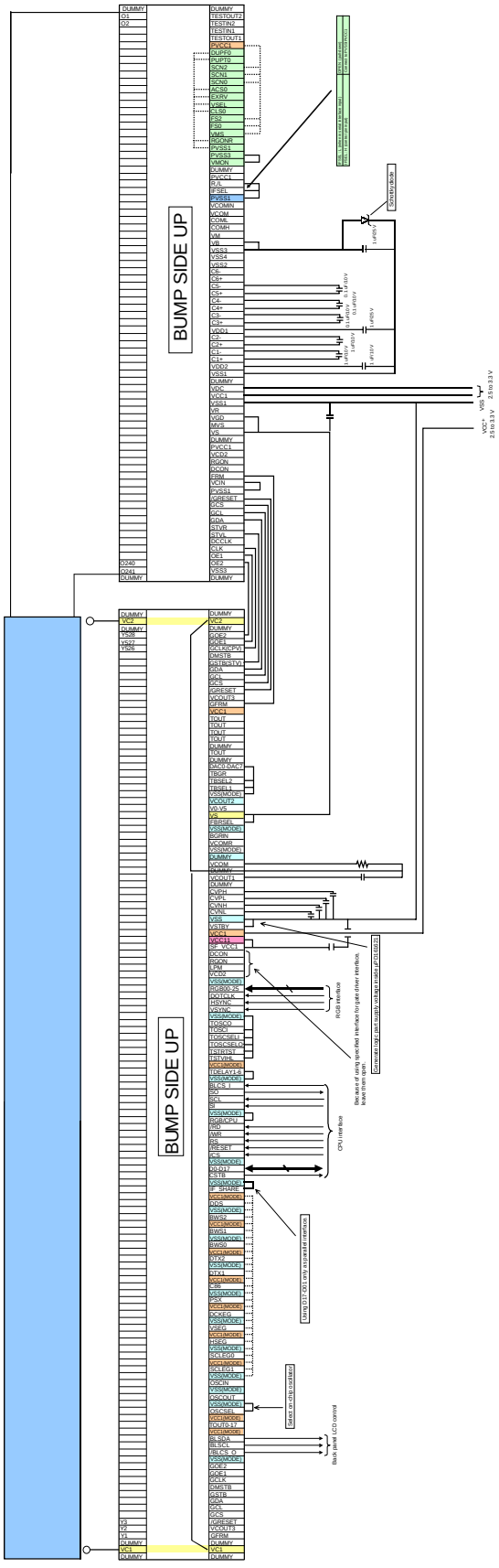
MODE4R (SCN0 = 1, SCN1 = 0, SCN2 = 0, R,/L = 1)



MODE4L (SCN0 = 1, SCN1 = 0, SCN2 = 0, R,/L = 0)



7. CONNECTION EXAMPLE WITH SOURCE DRIVER



8. VALUE OF WIRING RESISTANCE TO EACH PIN

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

Table 8-1. Recommended Wiring Resistor Values

Pin name	Wiring Resistor Values (Ω)
V_{SS1}	< 10
V_{CC1}	< 10
V_{DC}	< 10
V_S	< 10
V_{DD2}	< 10
C_1^+	< 10
C_1^-	< 10
C_2^+	< 10
C_2^-	< 10
V_{DD1}	< 50
V_{SS2}	< 50
V_{SS3}	< 50
V_{SS4}	< 50
C_3^+	< 50
C_3^-	< 50
C_4^+	< 50
C_4^-	< 50
C_5^+	< 50
C_5^-	< 50
C_6^+	< 50
C_6^-	< 50

9. RECOMMENDED CAPACITANCE VALUES OF EXTERNAL CAPACITOR

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Table 9-1. Recommended Values of External Capacitor

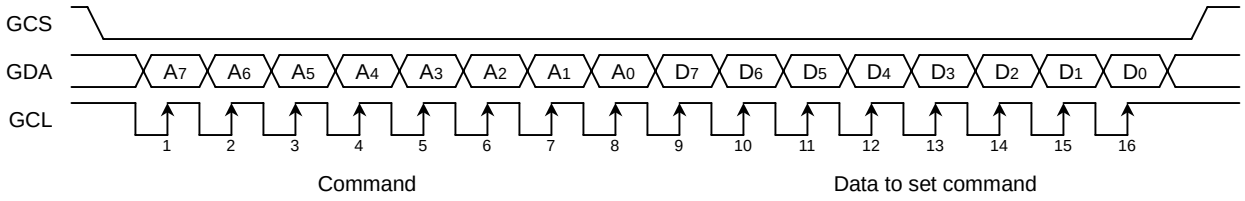
Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
V_S	1 to 4.7	6.3 or more
V_R	1 to 4.7	6.3 or more
V_{DD1}	0.47 to 1	25 or more
V_{DD2}	1 to 4.7	15 or more
V_{SS2}	0.47 to 1	25 or more
V_{SS3}	0.47 to 1	25 or more
V_{SS4}	1 to 4.7	10 or more
COMH	1 to 4.7	6.3 or more
COML	1 to 4.7	6.3 or more
C_1^+, C_1^-	1 to 4.7	10 or more
C_2^+, C_1^-	1 to 4.7	10 or more
C_3^+, C_1^-	0.47 to 1	10 or more
C_4^+, C_1^-	0.47 to 1	10 or more
C_5^+, C_1^-	0.47 to 1	10 or more
C_6^+, C_1^-	1 to 4.7	10 or more

10. SERIAL INTERFACE

When the serial interface has been selected, if the chip is active (GCS = L), serial data input (GDA) and serial clock input (GCL) can be received. Serial data is read from D_7 and then from D_6 to D_0 on the rising edge of the serial clock, via the serial input pin. This data is synchronized on the eighth serial clock's rising edge and is then converted to parallel data for processing.

The serial interface signal chart is shown below.

Figure 10-1. Serial Interface Signal Chart



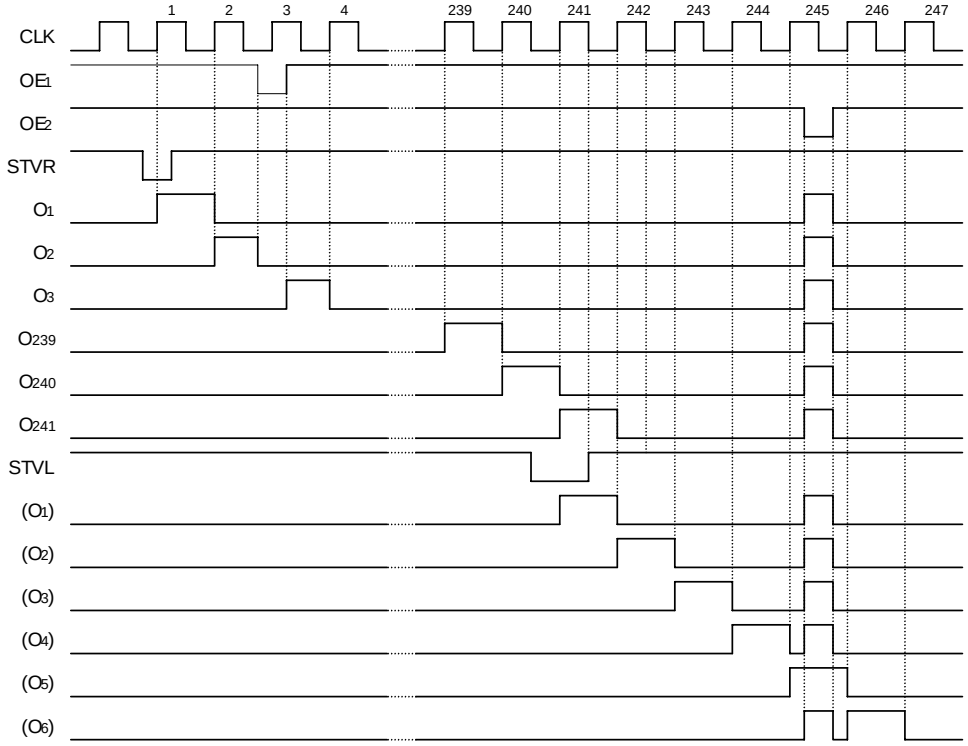
Note that odd bytes of data received after the reset command is input are recognized as commands, and even bytes of data are recognized as data values to be set to commands.

Remarks 1. The shift register and counter are reset to their initial values when the chip select signal is inactive. Do not set the chip select signal to inactive between transmission of an 8-bit command and transmission of the 8-bit data set for the command.

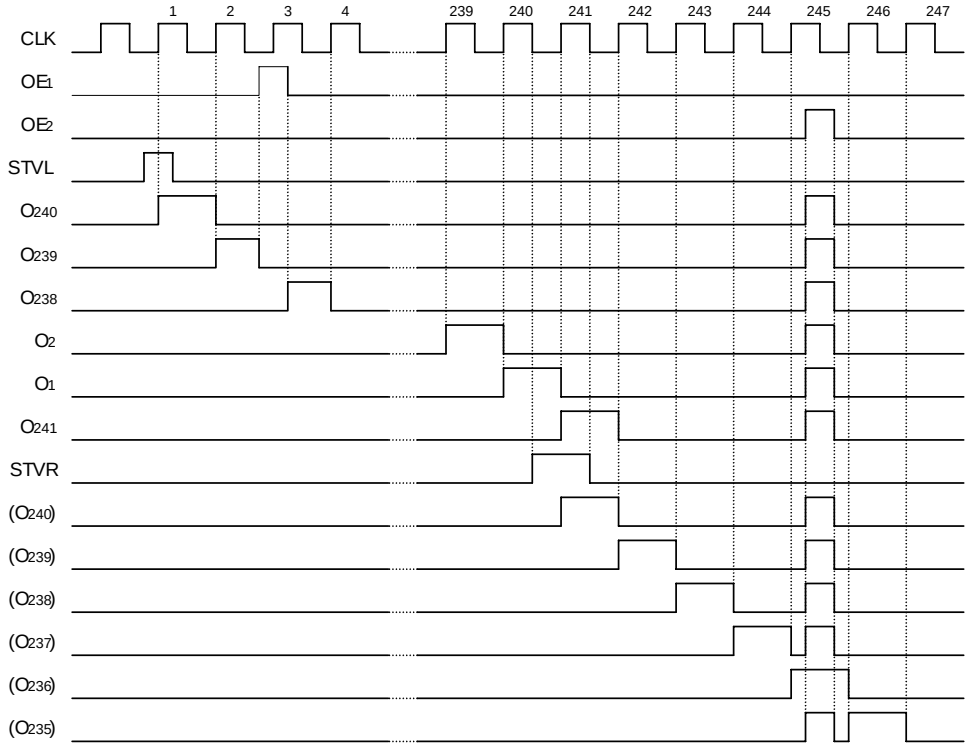
2. When using GCL wiring, take care concerning the possible effects of terminating reflection and noise from external sources. We recommend checking operation with the actual device.

11. TIMING CHARTS (MODE1: SCN0 = 1, SCN1 = 1, SCN2 = 1)

R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0



R,/L = L, STVSEL = 1, OE1SEL = 1, OE2SEL = 1



12. POWER ON/OFF SEQUENCE

There are three ways to turn on the power of the μPD161644:

<When power supply is controlled by serial interface>

- Simple sequence
- Command control sequence

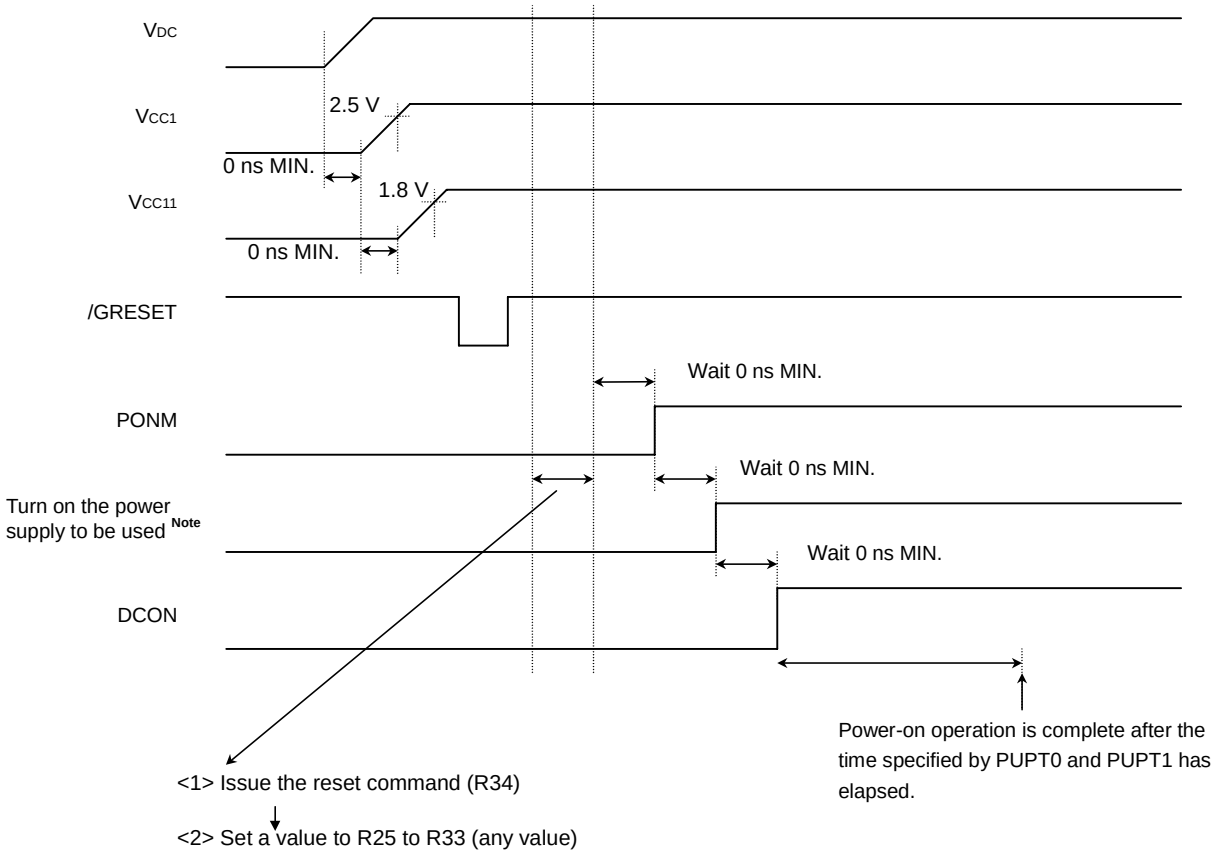
<When power supply is controlled by pin>

- Simple sequence

12.1 Power ON sequence

(1) Power supply control via serial interface (simple sequence)

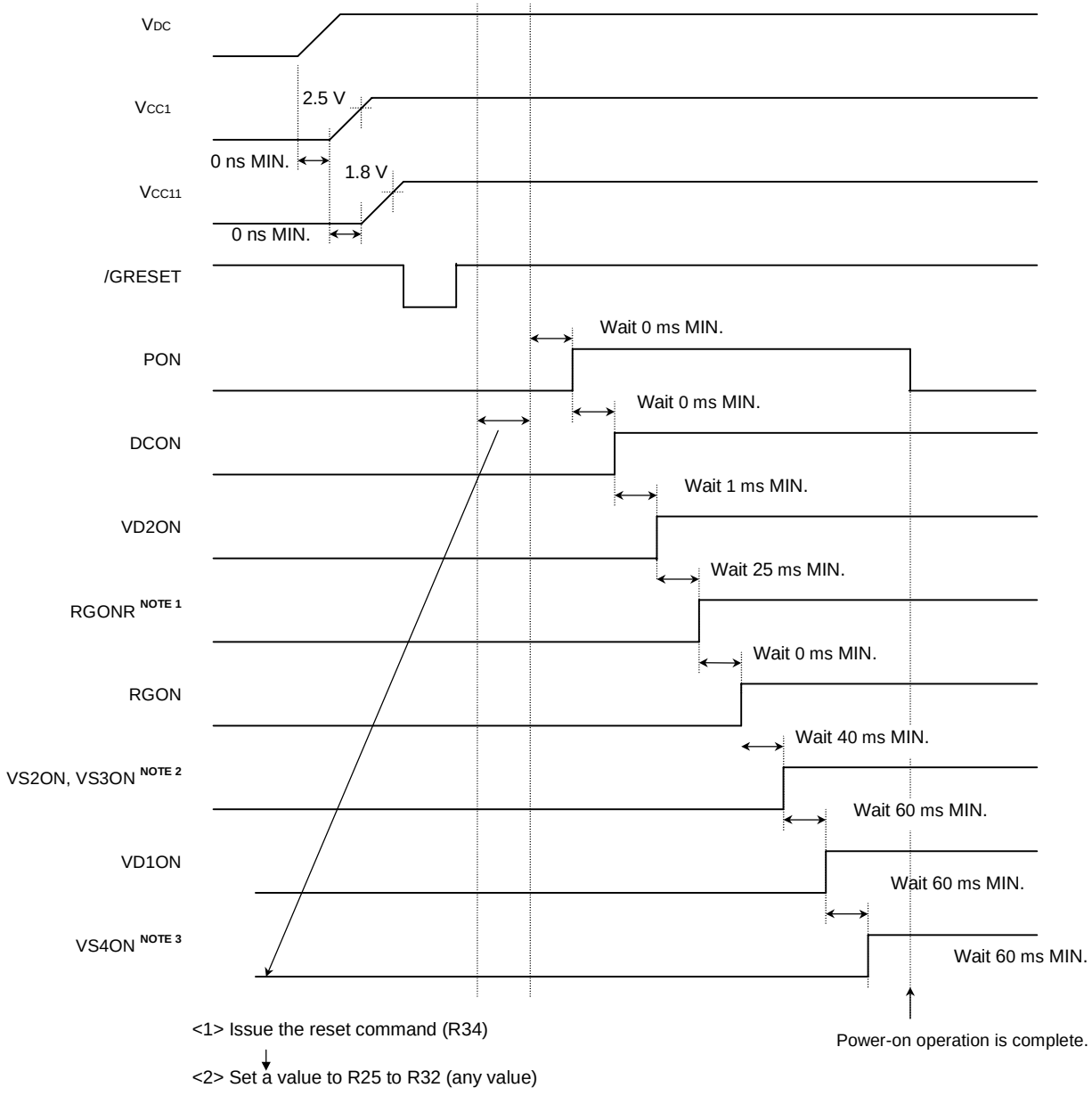
Control /GRESET pin and each command of PONM, VD2ON, RGONR, RGON, VS2ON, VS3ON, VD1ON, and DCON using the following sequence, after applying power to V_{DC}, V_{CC1}, and V_{CC11}.



Note Turn on the power supply to be used among VD2ON, RGONR, RGON, VS2ON, VS3ON, and VD1ON.

(2) Power control by serial interface (command control sequence)

Control /GRESET pin and each command of PON, DCON, VD2ON, RGONR, RGON, VS2ON, VS3ON, VD1ON, and VS4ON after power on of V_{DC}, V_{CC1}, V_{CC11} as shown below.



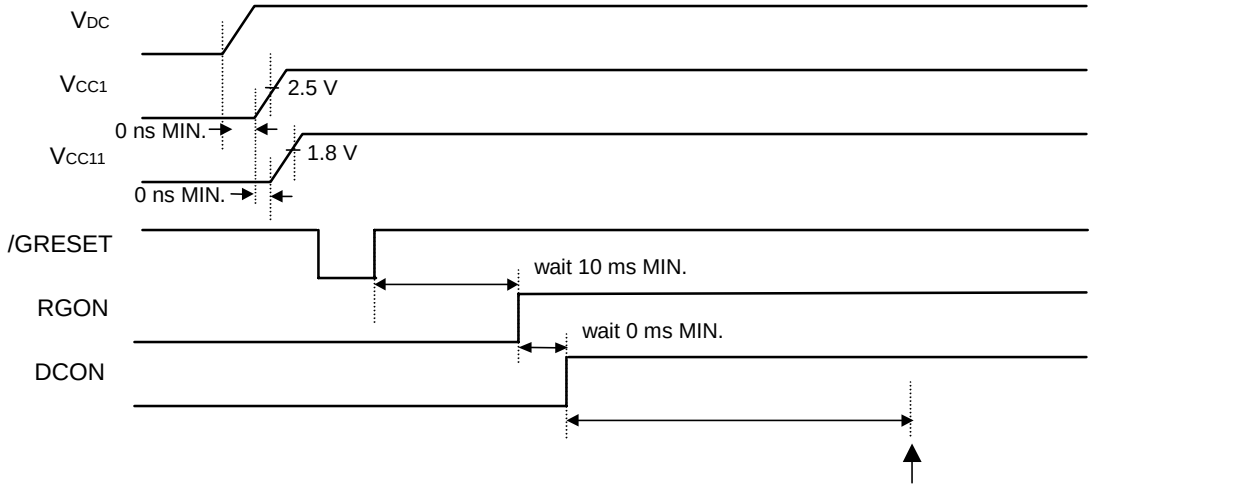
Notes 1. This pin only needs to be controlled when the V_R amplifier is used.

2. VS2ON only needs to be controlled when V_{SS2} is used.

3. This pin only needs to be controlled when VCOM is used.

(3) Power control by pins (simple sequence)

Control each pin of /GRESET, RGON, and DCON after power on of V_{DC}, V_{CC1}, V_{CC11} as shown below.



Remarks 1. When using RGON, pull it up to the high level by wiring the RGONR pin.

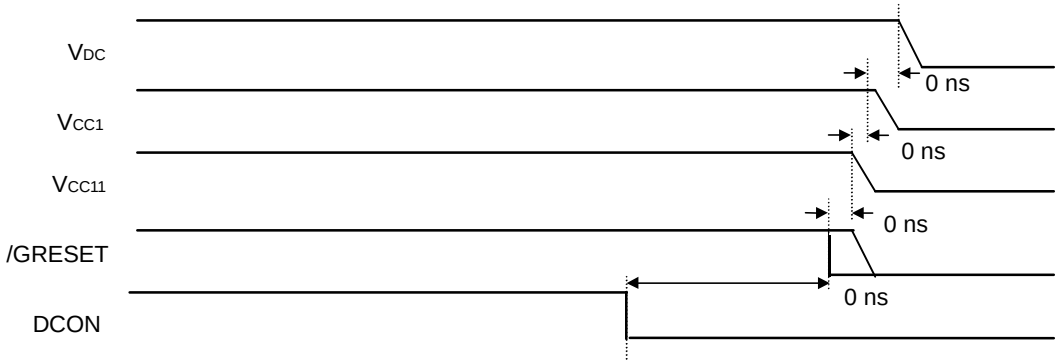
2. When using V_{SS4}, pull it up to the high level by wiring the COMON pin.

12.2 Power OFF sequence

When turning the power off, turn off the pins and commands used for control simultaneously, both when performing control via the serial interface and via the pins.

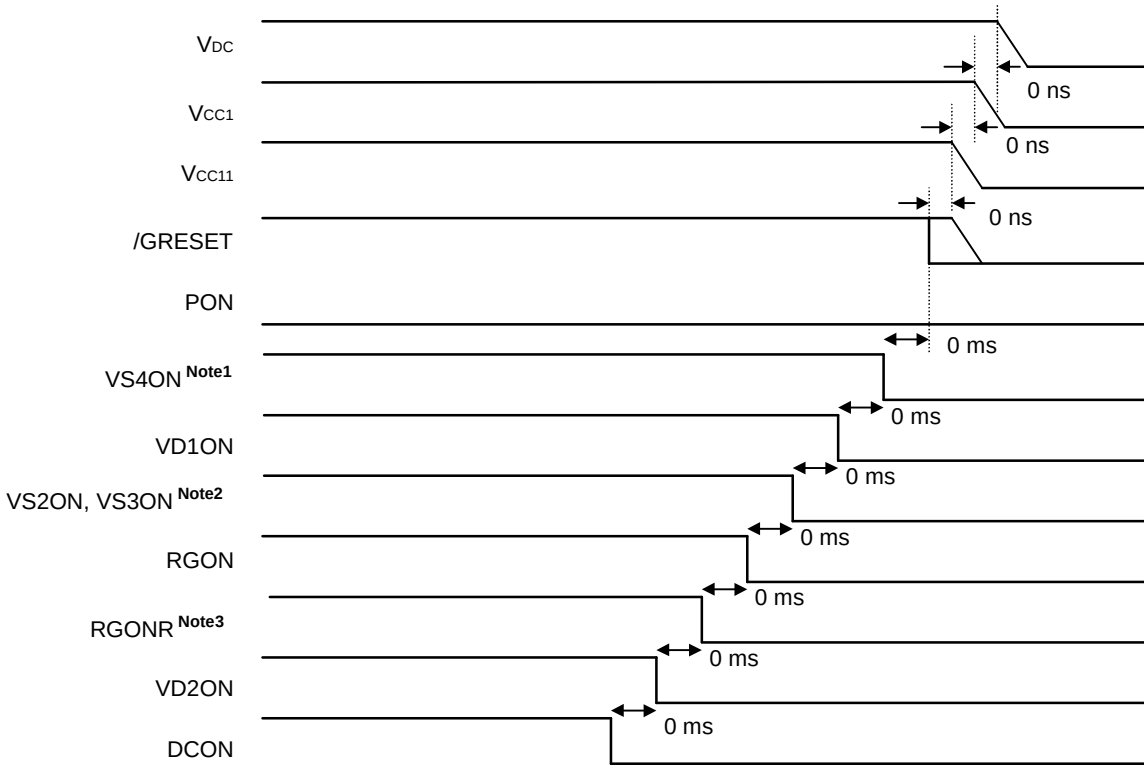
(1) Power control by serial interface (Simplified sequence)

Control DCON pin as shown below.



(2) Power control by serial interface (Command control sequence)

Control each pin of /GRESET, RGON, and DCON as shown below.



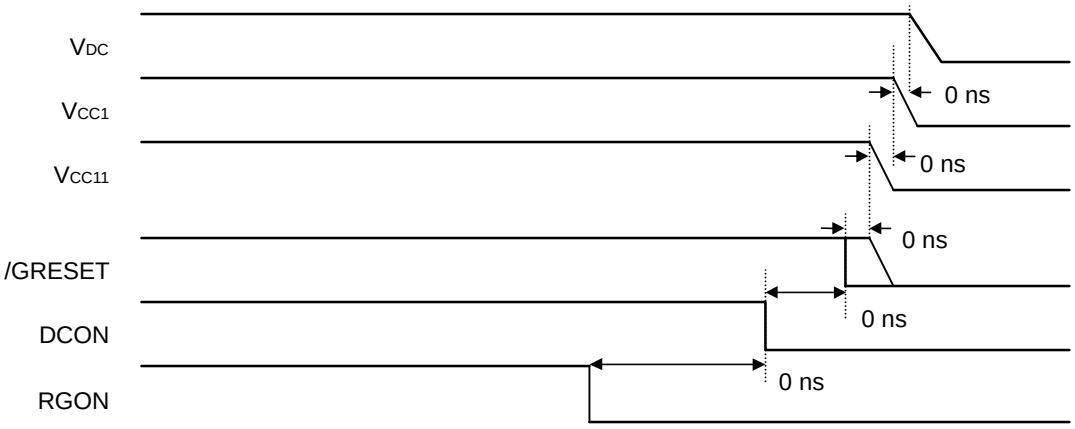
Notes 1. This pin only needs to be controlled when the VCOM is used.

2. VS2ON only needs to be controlled when V_{SS2} is used.

3. This pin only needs to be controlled when V_R amplifier is used.

(3) Power control by pins (Simplified sequence)

Control each pin of /GRESET, RGON, and DCON as shown below.



Remarks 1. When using RGON, pull it up to the high level by wiring the RGONR pin.

2. When using V_{SS4}, pull it up to the high level by wiring the COMON pin.

13. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC1}	−0.5 to +4.0	V
Supply Voltage	V_{DC}	−0.5 to +4.0	V
Supply Voltage	V_{SS3}	V_{DD1} −42 V to +0.5	V
Supply Voltage	V_{DD1}-V_{SS3}	−0.5 to +42	V
Input Voltage Note 1	V_I	−0.5 to V_{CC1}+0.5	V
Input Current Note 1	I_I	±1	mA
Output Current Note 2	I_{O1}	±10	mA
Output Current Note 3	I_{O2}	+10	mA
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Notes 1. CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, DCCLK, VCIN, DCON, RGON, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1

2. STVR, STVL, VM, VCOM

3. V_S

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC1}		2.5	2.7	3.3	V
Supply Voltage	V_{DC}		2.5	2.7	3.3	V
Supply Voltage	V_{DD1}		10	15	20	V
Supply Voltage	V_{SS3}		−20	−15	−10	V
Supply Voltage	V_{DD1}-V_{SS3}		20	30	40	V
Supply Voltage	V_{GD}				6.0	V
Input Voltage Note	V_I		0		V_{CC1}	V

Note CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, DCCLK, VCIN, DCON, RGON, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1

Electrical Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS1} = 0 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	**Note 1**	0.8 V_{CC1}			V
Low-level input voltage	V_{IL1}				0.2 V_{CC1}	V
High-level output voltage	V_{OH}	STVR, STVL, I_{OH} = –40 μA	V_{CC1} –0.4		V_{CC1}	V
Low-level output voltage	V_{OL}	STVR, STVL, I_{OH} = +40 μA	0		0.4	V
V_{DD1} boost voltage	V_{DD1}	I_{DD1} = 300 μA, 3 x boost, **Note 2**	2.7 V_{GD}	–	3 V_{GD}	V
V_{DD2} boost voltage1	V_{DD21}	I_{DD2} = 1 mA , V_{CD2} = L, V_{MS} = H (2 x boost, dual), **Note 2**	1.9 V_{DC}	–	2 V_{DC}	V
V_{DD2} boost voltage2	V_{DD22}	I_{DD2} = 1 mA , V_{CD2} = L, V_{MS} = L (2 x boost, single), **Note 2**	1.8 V_{DC}	–	2 V_{DC}	V
V_{DD2} boost voltage3	V_{DD23}	I_{DD2} = 1 mA , V_{CD2} = H (3 x boost), **Note 2**	2.7 V_{DC}	–	3 V_{DC}	V
V_{SS2} boost voltage	V_{SS2}	I_{SS2} = –300 μA, –2 x boost, **Note 2**	–2 V_S	–	–1.8 V_S	V
V_{SS3} boost voltage	V_{SS3}	I_{SS3} = –300 μA, –3 x boost, **Note 2**	–3 V_S	–	–2.7 V_S	V
V_{SS4} boost voltage	V_{SS4}	I_{SS4} = –300 μA, –1 x boost, **Note 2**	–V_{DC}	–	–0.9 V_{DC}	V
V_{DD1} output resister	R_{VDD1}	I_{DD1} = 300 μA, 3 x boost, **Note 2**	–	3	5	kΩ
V_{DD2} output resistor1	R_{VDD21}	I_{DD2} = 1 mA , V_{CD2} = L, V_{MS} = H (2x boost, dual), **Note 2**	–	100	200	Ω
V_{DD2} output resistor2	R_{VDD22}	I_{DD2} = 1 mA , V_{CD2} = L, V_{MS} = L (2x boost, single), **Note 2**	–	250	400	Ω
V_{DD2} output resistor3	R_{VDD23}	I_{DD2} = 1 mA , V_{CD2} = H (3 x boost), **Note 2**	–	450	700	Ω
V_{SS2} output resistor	R_{VSS2}	I_{SS2} = –300 μA , –2 x boost, **Note 2**	–	3	5	kΩ
V_{SS3} output resistor	R_{VSS3}	I_{SS2} = –300 μA , –3 x boost, **Note 2**	–	3	5	kΩ
V_{SS4} output resistor	R_{VSS4}	I_{SS2} = –300 μA , –1 x boost, **Note 2**	–	300	500	Ω
V_S output voltage	V_S	No load	4.5	5	5.5	V
V_R output voltage	V_R	No load	4.5	5	5.5	V
V_S output resistor	R_{VS}	V_{DD2} = 6 V, I_S = 1 mA, V_S = 5 V	–	15	30	Ω
V_R output resistor	R_{VR}	V_{DD2} = 6 V, I_R = 1 mA, V_R = 5 V	–	15	30	Ω
COMH output voltage	V_{comH}	No load, DA (7:0) = CDA (7:0) = A0H	4.5	5	5.5	V
COML output voltage	V_{comL}	No load, DA (7:0) = CDA (7:0) = A0H	–0.5	0	0.5	V
VCOM output high-level voltage	V_{VcomH}	I_{VCOM} = 1 mA, DA (7:0) = CDA (7:0) = A0H, VCIN = H	4.5	5	5.5	V
VCOM output low-level voltage	V_{VcomL}	I_{VCOM} = –1 mA, DA (7:0) = CDA (7:0) = A0H, VCIN = L	–0.5	0	0.5	V
COM output resistor1	R_{COM1}	COM output = High, I_{COM} = 1 mA	–	100	200	Ω
COM output resistor2	R_{COM2}	COM output = Low, I_{COM} = –1 mA	–	100	200	Ω
VM output high-level voltage	V_{M1H}	No load	0.9 V_{SS2}	V_{SS2}	1.1 V_{SS2}	V
VM output low-level voltage	V_{M1L}	No load	0.9 V_{SS3}	V_{SS3}	1.1 V_{SS3}	V
VM output resistance	R_{M1}	When I_{VM} = 100 μA, V_{SS2} is selected.	–	300	400	Ω
Output ON resistance	R_{ON1}	O_1 to O_{241}	1	2	4	kΩ

Notes 1. CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, VCOM, DCON, RGON, LPM, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1, VCIN

2. External capacitor: 1 μF, CLS0 = H, CLS1 = L, FS0 = H, FS1 = L, FS2 = H, FS3 = L, FUP = L

3. ACS0 = H, ACS1 = H, V_{DD2} = V_{DC} x 2, dual mode, V_{DD1} = VGD x 3, V_{SS2} = VGD x (–2), V_{SS3} = VGD x (–3), V_{SS4} = V_{DC} x (–1), VGD = V_S, CLS0 = H, CLS1 = L, FS0 = H, FS1 = L, FS2 = H, FS3 = L, FUP = L

(2/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input current	I_{I1}	**Note 1**	– 1	0	1	μA
Input leak current	I_{IL}	STVR, STVL	– 1	0	1	μA
Dynamic current	I_{CC1}	V_{CC1}, f_{CLK} = 12.5 kHz, no load, **Note 3**	–	–	200	μA
Dynamic current	I_{DC}	V_{DC}, f_{CLK} = 12.5 kHz, no load, **Note 3**	–	–	1.8	mA
Static current	I_{CC1}	V_{CC1}, stand-by	–	–	5	μA
Static current	I_{DC}	V_{DC}, stand-by	–	–	5	μA
V_{REF} voltage	V_{REF}		1.08	1.20	1.32	V

Notes 1. CLK, STVR, STVL, R,/L, OE_1, OE_2, GCS, GCL, GDA, VCOM, DCON, RGON, LPM, VCD2, /GRESET, IFSEL, EXRV, SCN0, SCN1, VCIN

2. External capacitor: 1 μF, CLS0 = H, CLS1 = L, FS0 = H, FS1 = L, FS2 = H, FS3 = L, FUP = L

3. ACS0 = H, ACS1 = H, $V_{DD2} = V_{DC}$ x 2, dual mode, V_{DD1} = VGD x 3, V_{SS2} = VGD x (–2), V_{SS3} = VGD x (–3), $V_{SS4} = V_{DC}$ x (–1), VGD = V_S, CLS0 = H, CLS1 = L, FS0 = H, FS1 = L, FS2 = H, FS3 = L, FUP = L

Switching Characteristics (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS1} = 0 V)

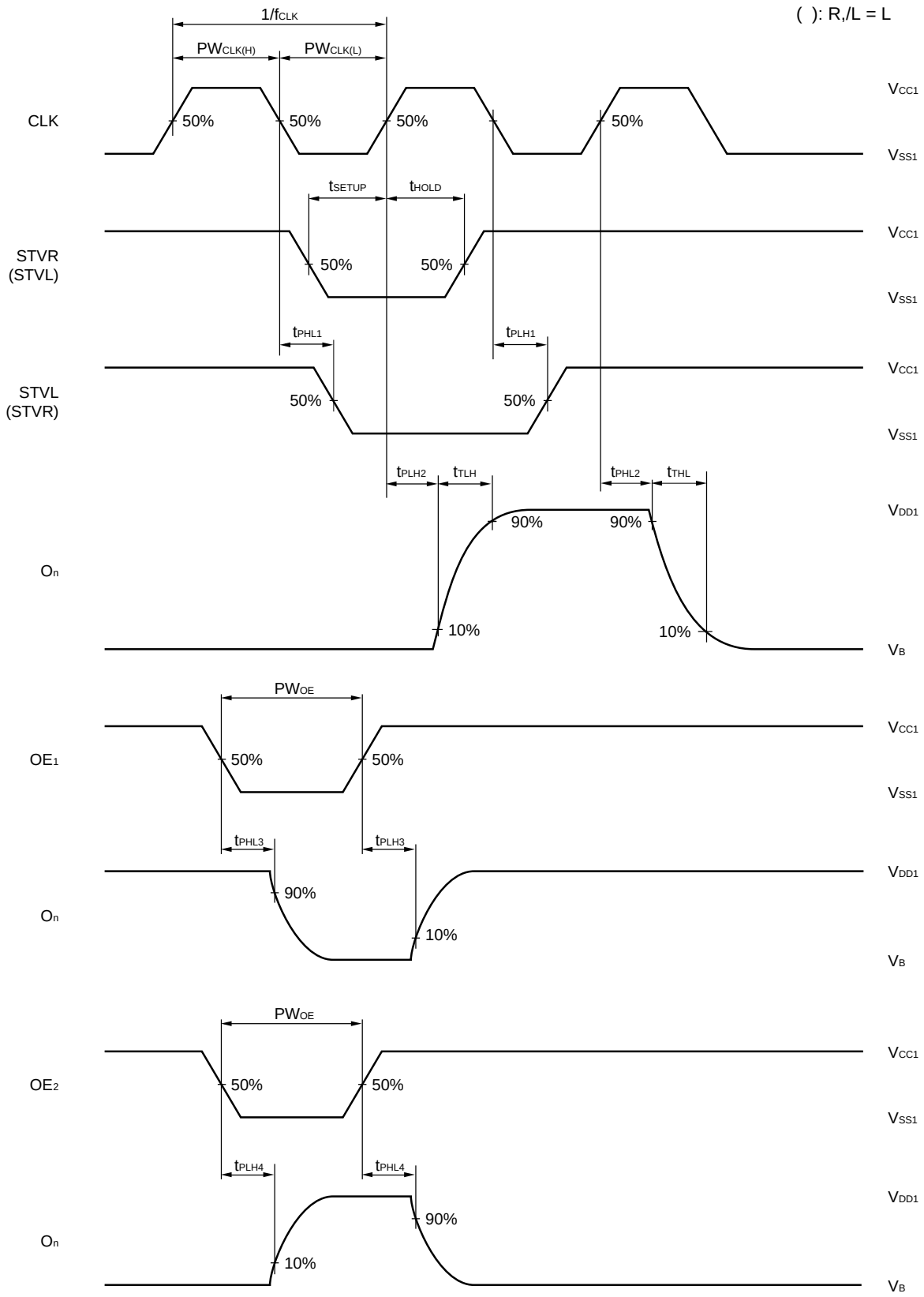
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t_{PHL1}	C_L = 20 pF			800	ns
	t_{PLH1}	CLK → STVL (STVR)			800	ns
Driver Output Delay Time 1	t_{PHL2}	C_L = 50 pF			1	μs
	t_{PLH2}	CLK → O_n			1	μs
Driver Output Delay Time2	t_{PHL3}	C_L = 50 pF			1	μs
	t_{PLH3}	OE_1 → O_n			1	μs
Driver Output Delay Time 3	t_{PHL4}	C_L = 50 pF			1	μs
	t_{PLH4}	OE_2 → O_n			1	μs
Output Rise Time	t_{TLH}	C_L = 50 pF			1	μs
Output Fall Time	t_{THL}				1	μs
Input Capacitance	C_I	T_A = 25°C			15	pF
DC/DC Oscillation Frequency	f_{DCDC}	CLS1 = L, CLS0 = H, FUP = L	12.5	25	37.5	kHz
DCCLK Input Frequency	f_{DCCLK}				50	kHz
VCIN Input Frequency	f_{VCIN}				50	kHz
Clock Input Frequency	f_{CLK}	When connected in cascade			400	kHz

Timing Requirement (T_A = –40 to +85°C, V_{CC1} = 2.5 to 3.3 V, V_{DC} = 2.5 to 3.3 V, V_{DD1} = 15 V, V_{SS3} = –15 V, V_S = 5 V, V_{SS1} = 0 V)

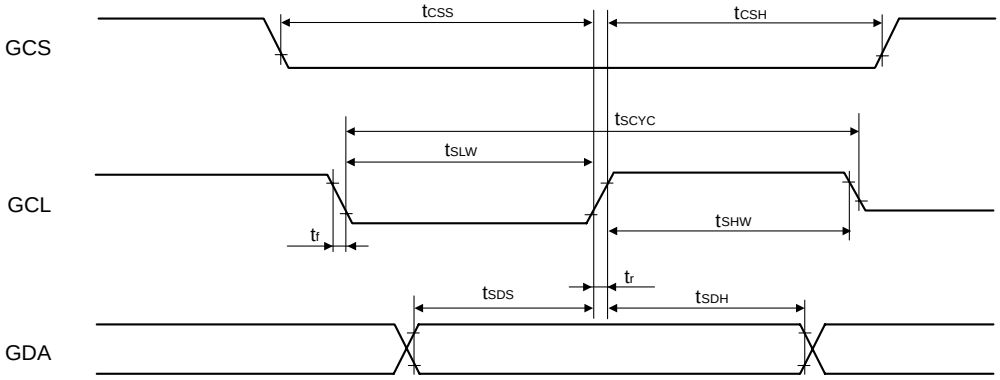
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse High Period	$PW_{CLK(H)}$	CLK	500			ns
Clock Pulse Low Period	$PW_{CLK(L)}$	CLK	500			ns
Enable Pulse High Period	PW_{OE}	OE_1, OE_2	1.0			μs
Data Setup Time	t_{SETUP}	STVR (STVL) ↓ →CLK↑	200			ns
Data Hold Time	t_{HOLD}	CLK↑→STVR (STVL) ↑	200			ns
Serial Clock Cycle	t_{SCYC}	GCL	250			ns
GCL High-level Pulse Width	t_{SHW}	GCL	100			ns
GCL Low-level Pulse Width	t_{SLW}	GCL	100			ns
GDA Data Setup Time	t_{SDS}	GDA	100			ns
GDA Data Hold Time	t_{SDH}	GDA	100			ns
GCS-GCL Time	t_{CSS}	GCS	150			ns
GCL-GCS Time	t_{CSH}	GCS	150			ns

Switching Characteristics Waveform (R,/L = H, STVSEL = 0, OE1SEL = 0, OE2SEL = 0)

(a) Gate interface



(b) Serial interface



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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.