

NEC

MOS INTEGRATED CIRCUIT  
 $\mu$ PD3734A

## 2660 PIXELS CCD LINEAR IMAGE SENSOR

The  $\mu$ PD3734A is a high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The  $\mu$ PD3734A has 2660 pixels and an output amplifier which has high gain and wide output range, but low noise.

Built-in sample and hold circuit converts and outputs independent signal from CCD register in every pixel to continuous video signal. So it is easy to interface to A/D converter or Bi-level converter.

## FEATURES

- Valid photocell : 2660 pixels
- Photocell's pitch : 11  $\mu$ m
- High sensitivity : 70 V/lx-s TYP.
- Peak response wavelength : 550 nm (green)
- Resolution : 12 dot/mm A4 (210  $\times$  297 mm) size (shorter side)  
300 dpi US letter (8.5"  $\times$  11") size (shorter side)
- Power supply : +12 V
- Drive clock level : CMOS output under 5 V operation
- High speed scan : 0.54 ms/line (S/H in used)
- Built-in circuit : Sample and hold circuit  
Reset feed-through level clamp circuit  
Clamp pulse generation circuit  
Voltage amplifier
- Low noise : A quarter of the  $\mu$ PD3734
- Low image lag : 1 % MAX.
- Pin assign : Compatible with the  $\mu$ PD3734

## ORDERING INFORMATION

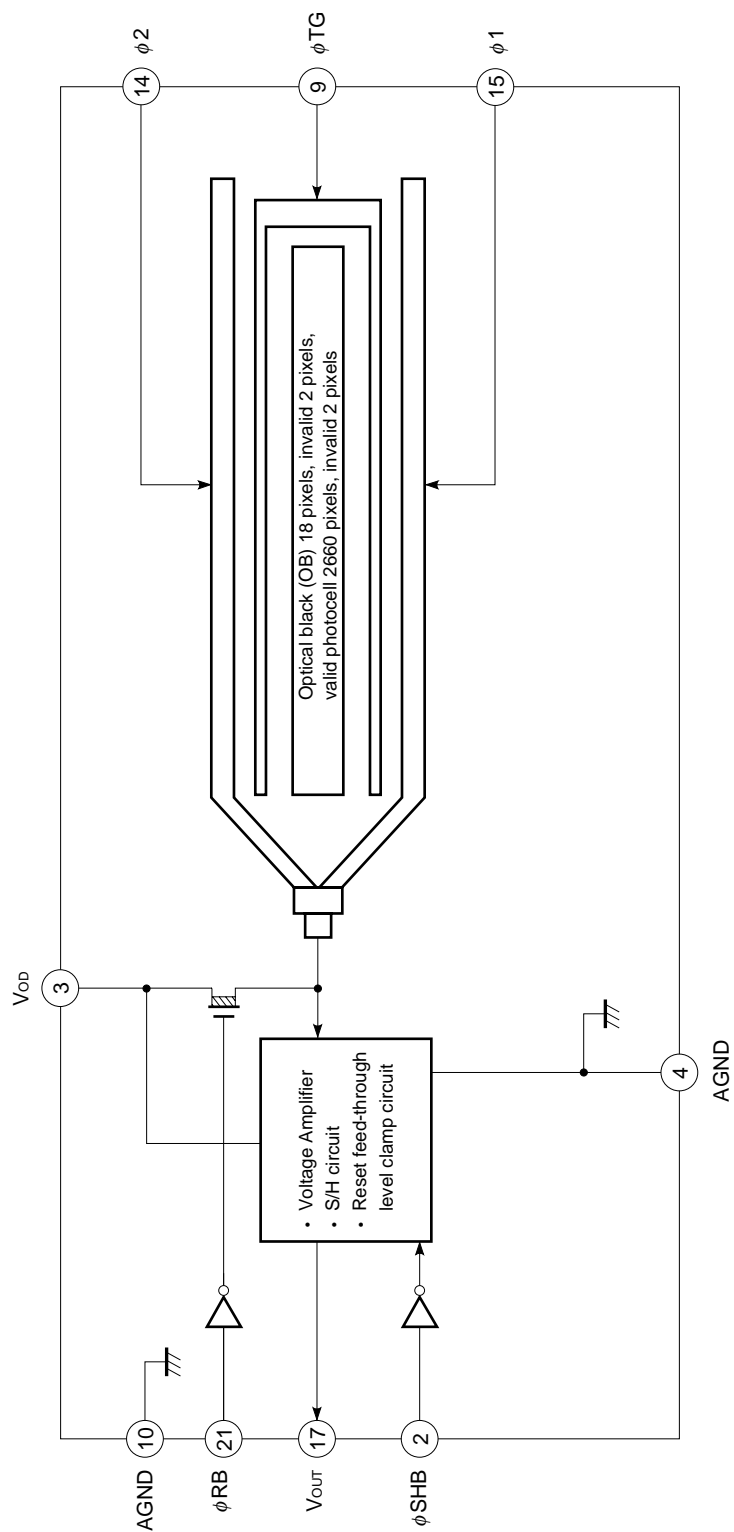
Part Number	Package
$\mu$ PD3734ACY	CCD linear image sensor 22-pin plastic DIP (400 mil)



COMPARISON CHART

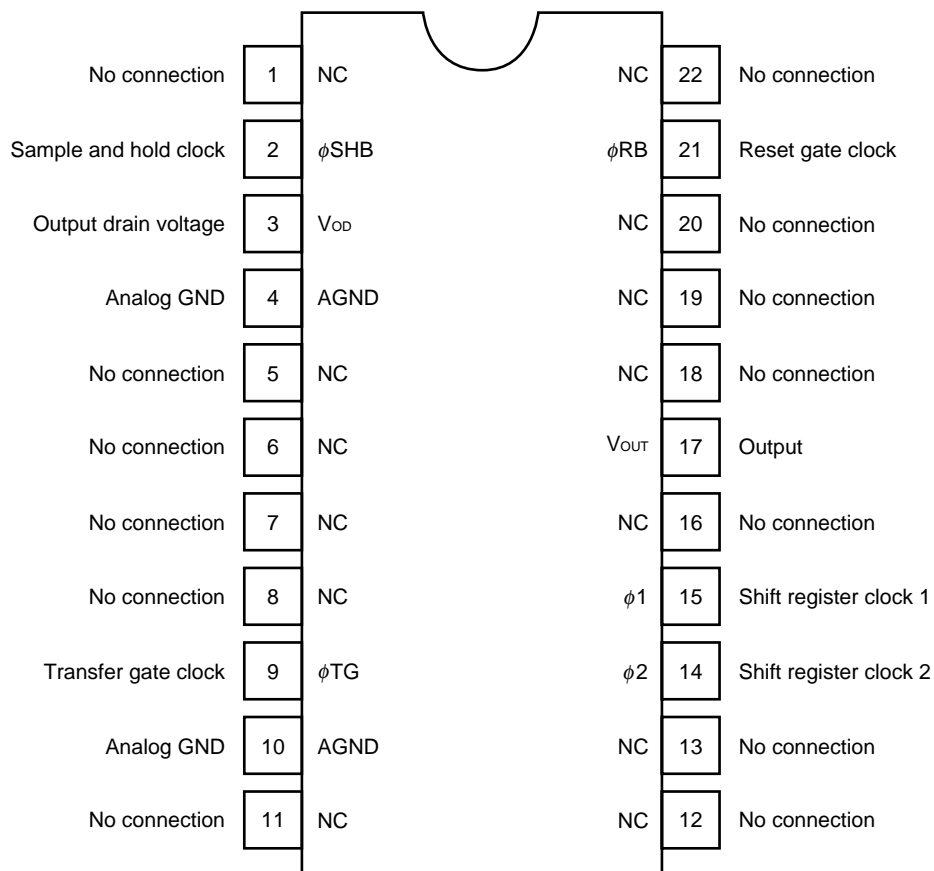
Item			μPD3734ACY	μPD3734CY-1
PIN CONFIGURATION	Pin 13		No connection	Digital GND
RECOMMENDED OPERATING CONDITIONS	Data rate MAX. (MHz)		5 (S/H in used)	3 (No conditions)
			4 (S/H not in used)	
ELECTRICAL CHARACTERISTICS	Average dark signal MAX. (mV)		3.0	8.0
	Dark signal non-uniformity (mV)	MIN.		−8
		TYP.	4	±4
		MAX.	6	+8
	Power consumption (mW)	TYP.	190	170
		MAX.	250	220
	Image lag (%)	TYP.	0.3	7
		MAX.	1.0	14
	Total transfer efficiency (test conditions)		Data rate = 4 MHz	Data rate = 3 MHz
	Reset feed-through noise (mV)	MIN.	−900	0
TYP.		−200	1000	
MAX.		+500	1800	
Bit noise TYP. (mV <sub>p-p</sub> )		4.5	16	
Random noise (mV)		0.9 (S/H in used)	No definition	
		0.9 (S/H not in used)		
TIMING CHART	t <sub>4</sub> MIN. (ns)		90	150
	t <sub>5</sub> MIN. (ns)		70	150
	t <sub>8</sub> MIN. (ns)		20	80
DEFINITIONS OF CHARACTERISTICS ITEMS	Dark signal non-uniformity		Absolute value	Minus and plus value
	Random noise		Refer to <b>DEFINITIONS OF CHARACTERISTICS ITEMS</b> 11. Random noise	No definition

BLOCK DIAGRAM

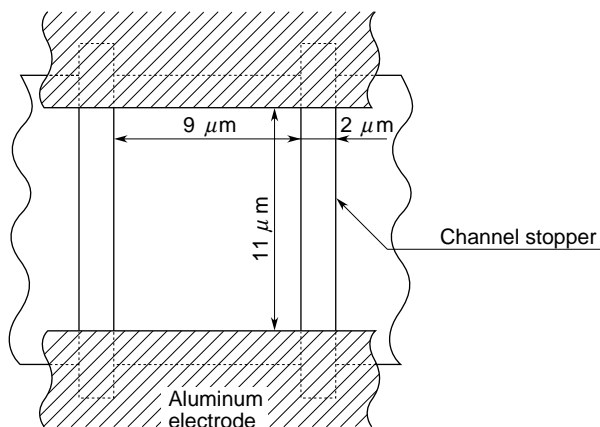


# PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (400 mil)



# PHOTOCELL STRUCTURE DIAGRAM



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	Ratings	Unit
Output drain voltage	V <sub>OD</sub>	−0.3 to +15	V
Shift register clock voltage	V <sub>φ1</sub> , V <sub>φ2</sub>	−0.3 to +15	V
Reset gate clock voltage	V <sub>φRB</sub>	−0.3 to +15	V
Transfer gate clock voltage	V <sub>φTG</sub>	−0.3 to +15	V
Sample and hold clock voltage	V <sub>φSHB</sub>	−0.3 to +15	V
Operating ambient temperature	T <sub>A</sub>	−25 to +60	°C
Storage temperature	T <sub>stg</sub>	−40 to +70	°C

**Caution** Exposure to ABSOLUTE MAXIMUM RATING for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = −25 to +60 °C)**

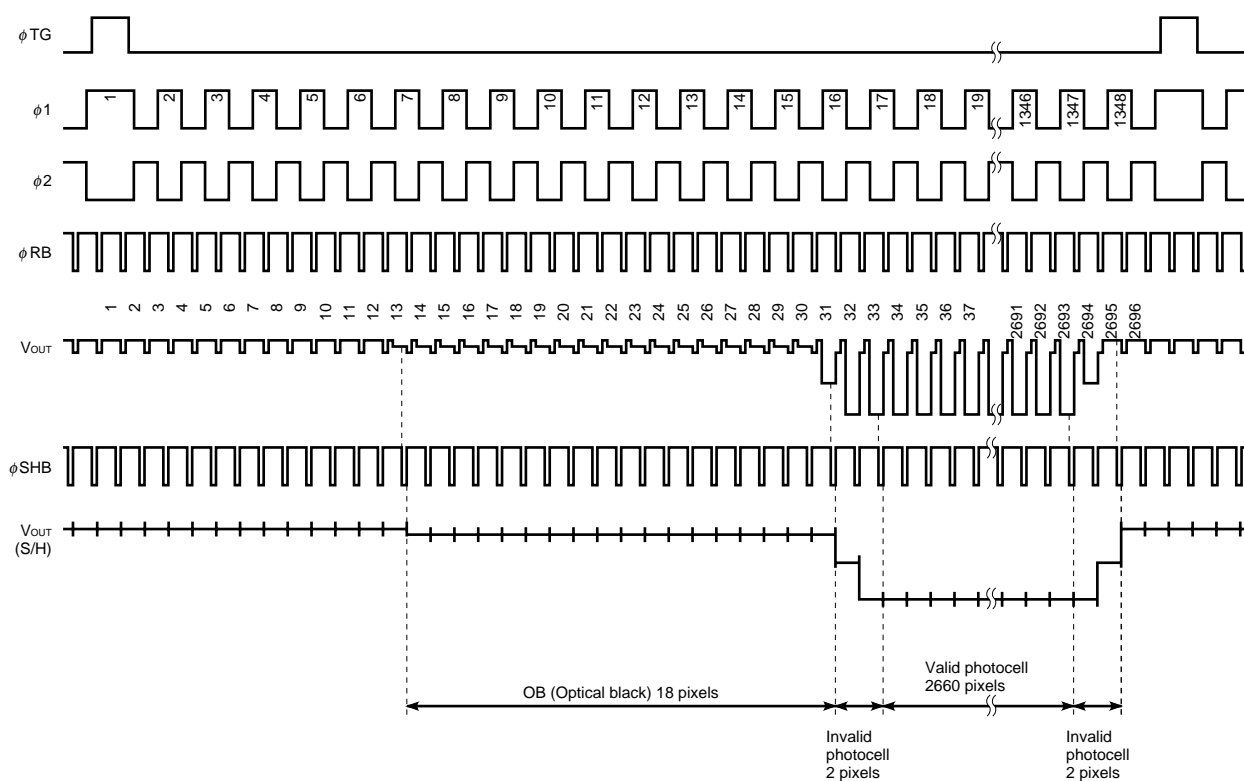
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V <sub>OD</sub>		11.4	12.0	12.6	V
Shift register clock high level	V <sub>φ1H</sub> , V <sub>φ2H</sub>		4.5	5.0	5.5	V
Shift register clock low level	V <sub>φ1L</sub> , V <sub>φ2L</sub>		−0.3	0	+0.5	V
Reset gate clock high level	V <sub>φRBH</sub>		4.5	5.0	5.5	V
Reset gate clock low level	V <sub>φRBL</sub>		−0.3	0	+0.5	V
Transfer gate clock high level	V <sub>φTGH</sub>		4.5	5.0	5.5	V
Transfer gate clock low level	V <sub>φTGL</sub>		−0.3	0	+0.5	V
Sample and hold clock high level	V <sub>φSHBH</sub>		4.5	5.0	5.5	V
Sample and hold clock low level	V <sub>φSHBL</sub>		−0.3	0	+0.5	V
Data rate	f <sub>φRB</sub>	S/H in used	0.2	1	5	MHz
		S/H not in used	0.2	1	4	MHz

# ELECTRICAL CHARACTERISTICS

(  $T_A = +25\text{ }^{\circ}\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi 1} = 0.5\text{ MHz}$ , data rate = 1 MHz, storage time = 10 ms  
light source: 3200 K halogen lamp + C-500S (infrared cut filter,  $t = 1\text{ mm}$ ), input signal clock = 5  $V_{p-p}$  )

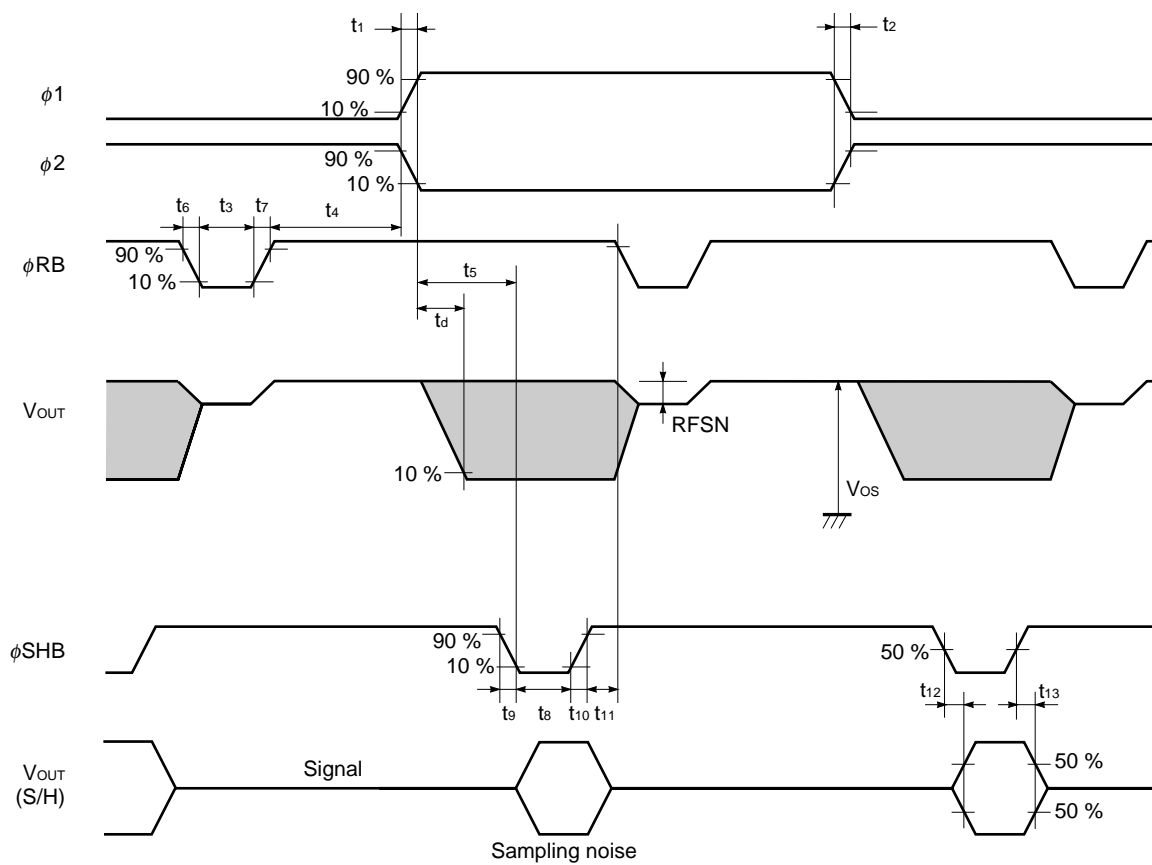
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Saturation voltage	$V_{sat}$		1.5	2.0		V
Saturation exposure	SE	Daylight color fluorescent lamp		0.029		lx•s
Photo response non-uniformity	PRNU	$V_{OUT} = 500\text{ mV}$		$\pm 2$	$\pm 8$	%
Average dark signal	ADS	Light shielding		1.0	3.0	mV
Dark signal non-uniformity	DSNU	Light shielding		4	6	mV
Power consumption	$P_W$			190	250	mW
Output impedance	$Z_O$			0.5	1	kΩ
Response	$R_F$	Daylight color fluorescent lamp	49	70	91	V/lx•s
Response peak wavelength				550		nm
Image lag	IL	$V_{OUT} = 1\text{ V}$		0.3	1.0	%
Offset level	$V_{OS}$		3.5	4.5	5.5	V
Input capacitance of shift register clock pin	$C_{\phi 1}$ , $C_{\phi 2}$			400		pF
Input capacitance of reset gate clock pin	$C_{\phi RB}$			5		pF
Input capacitance of sample and hold clock pin	$C_{\phi SHB}$			5		pF
Input capacitance of transfer gate clock pin	$C_{\phi TG}$			100		pF
Output fall delay time	$t_d$			80		ns
Register imbalance	RI	$V_{OUT} = 500\text{ mV}$			3	%
Total transfer efficiency	TTE	$V_{OUT} = 1\text{ V}$ , data rate = 4 MHz	92			%
Dynamic range	DR	$V_{sat}/DSNU$		500		times
Reset feed-through noise	RFSN	Light shielding	-900	-200	+500	mV
Sample and hold noise	SHSN	Light shielding, $\phi SHB$ series resistor 47 Ω	-50	0	+50	mV
Bit noise	BN			4.5		mV <sub>p-p</sub>
Random noise	$\sigma$	S/H in used		0.9		mV
		S/H not in used		0.9		mV
Resolution	MTF	Modulation transfer function at nyquist frequency		65		%

TIMING CHART 1



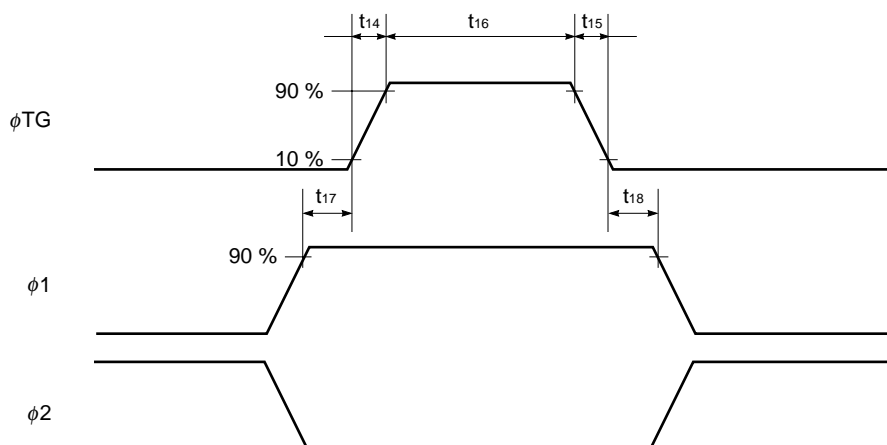
**Remark**  $V_{OUT}$  = Output when  $\phi_{SHB}$  is not in used (When  $\phi_{SHB}$  is not in used, connect  $\phi_{SHB}$  pin to GND).  
 $V_{OUT} (S/H)$  = Output when  $\phi_{SHB}$  is in used.

TIMING CHART 2

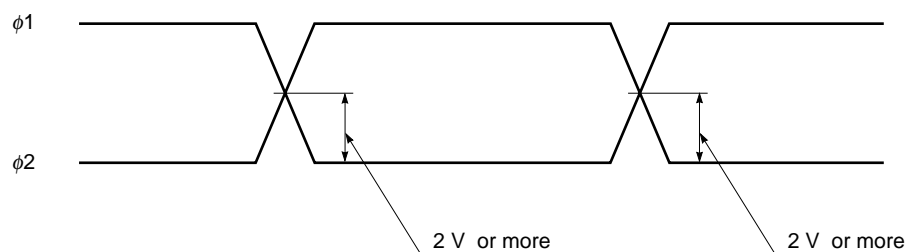


**Remark**  $V_{out}(S/H)$  = Output when  $\phi SHB$  is in used.

**TIMING CHART for  $\phi$ TG,  $\phi$ 1,  $\phi$ 2**



**CROSS POINTS for  $\phi$ 1,  $\phi$ 2**



**Remark** Adjust cross point of  $\phi$ 1,  $\phi$ 2 by  $\phi$ 1,  $\phi$ 2 pin external input resistors.

Parameter	MIN.	TYP.	MAX.	Unit
$t_1, t_2$	0	50	(100)	ns
$t_3$	20	100		ns
$t_4$	90	300		ns
$t_5$	70	300		ns
$t_6, t_7$	0	50		ns
$t_8$	20	200		ns
$t_9, t_{10}, t_{11}$	0	50		ns
$t_{12}$	0			ns
$t_{13}$		5	10	ns
$t_{14}, t_{15}$	0	50		ns
$t_{16}$	650	1000	(2000)	ns
$t_{17}, t_{18}$	0	100		ns

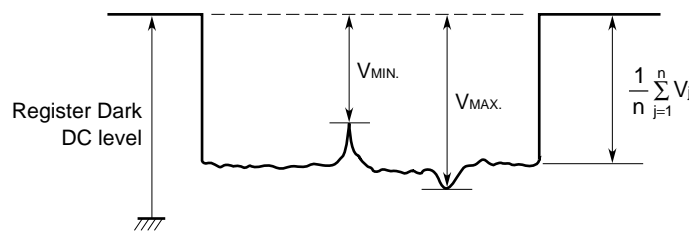
## DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage:  $V_{\text{sat}}$   
Output signal voltage at which the response linearity is lost.
2. Saturation exposure: SE  
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity: PRNU  
The peak/bottom ratio to the average output voltage of all the valid pixels calculated by the following formula.

$$\text{PRNU (\%)} = \left( \frac{V_{\text{MAX. or } V_{\text{MIN.}}}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

$n$  : Number of valid pixels

$V_j$  : Output voltage of each pixel



4. Average dark signal: ADS  
Output average voltage in light shielding.

$$\text{ADS (mV)} = \frac{1}{n} \sum_{j=1}^n V_j$$

$n$  : Number of valid pixels

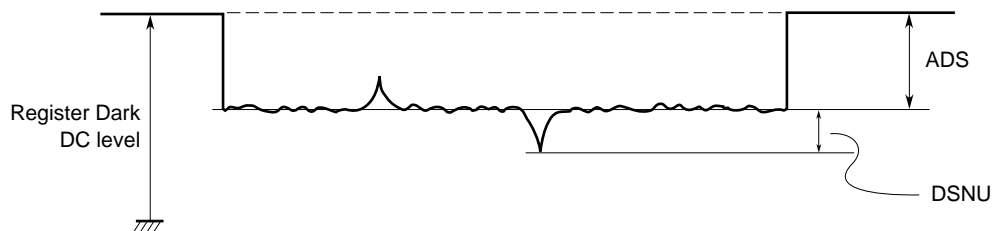
$V_j$  : Output voltage of each pixel

5. Dark signal non-uniformity: DSNU  
The difference between peak or bottom output voltage in light shielding and ADS.

$$\text{DSNU (mV): maximum of } |V_j - \text{ADS}| \quad j = 1 \text{ to } n$$

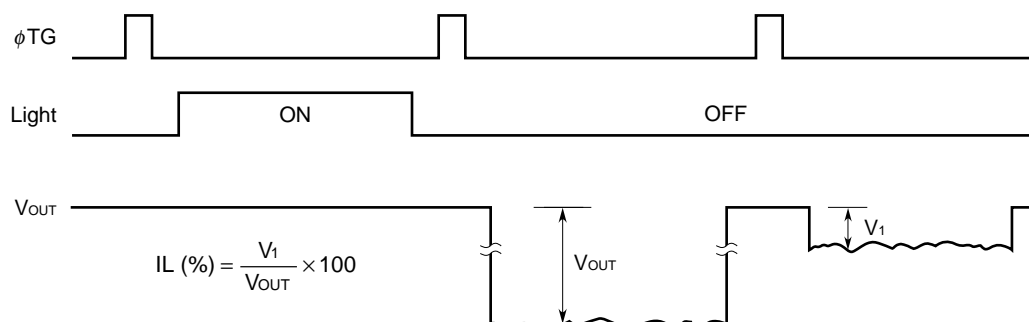
$n$  : Number of valid pixels

$V_j$  : Output voltage of each pixel



6. Output impedance:  $Z_o$   
Output pin impedance viewed from outside.
7. Response: R  
Output voltage divided by exposure (lx·s).  
Note that the response varies with a light source.

8. Image Lag: IL  
The rate between the last output voltage and the next one after read out the data of a line.



9. Register Imbalance: RI  
The rate of the difference between the average of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

$n$  : Number of valid pixels

$V_j$  : Output voltage of each pixel

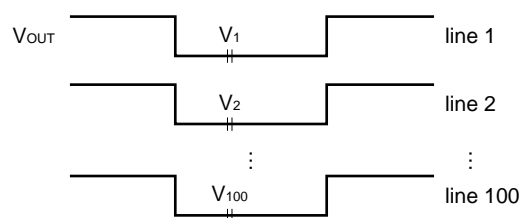
10. Bit Noise: BN  
Output signal distribution of a photocell by scan.

11. Random noise:  $\sigma$

Random noise  $\sigma$  is defined as the standard deviation of a valid photocell output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

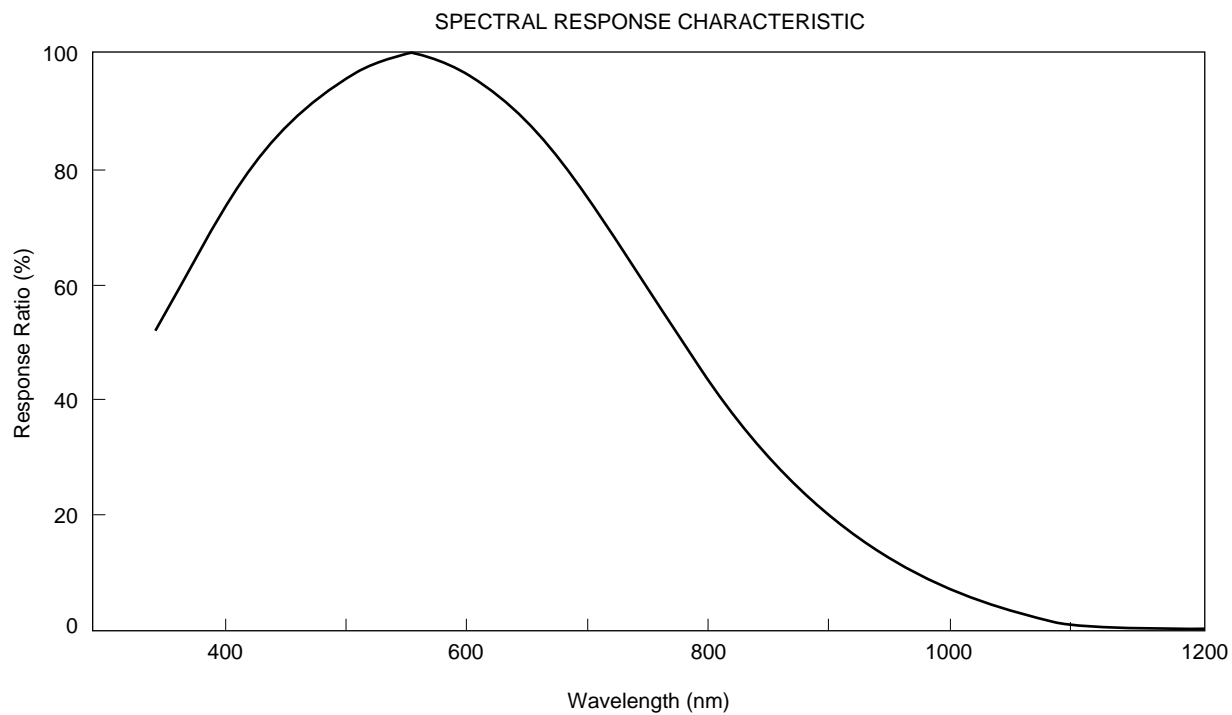
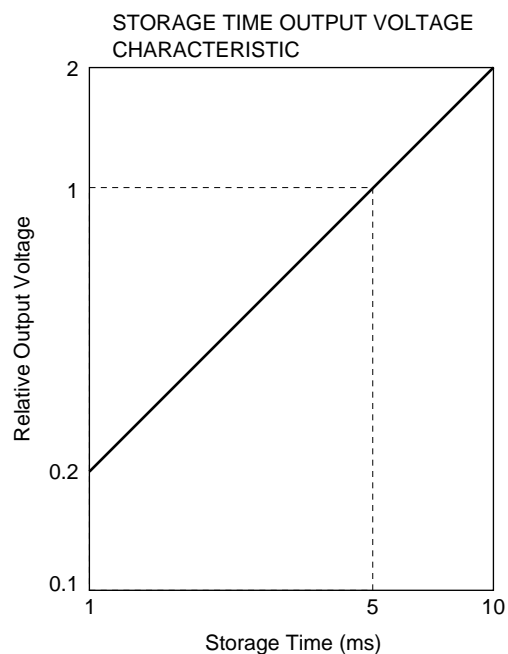
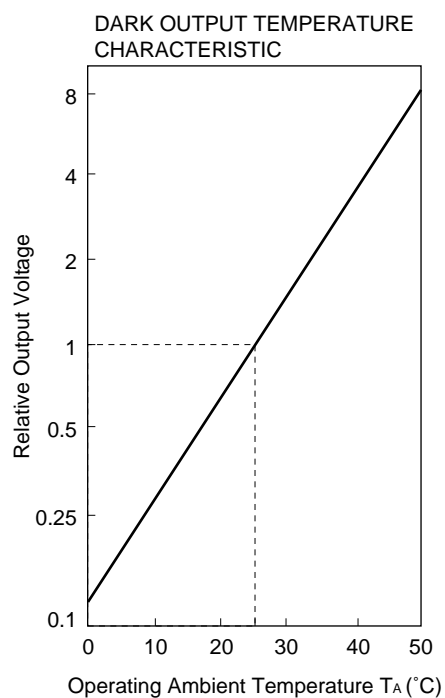
$$\sigma \text{ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

$V_i$ : A valid photocell output signal among all of the valid photocells

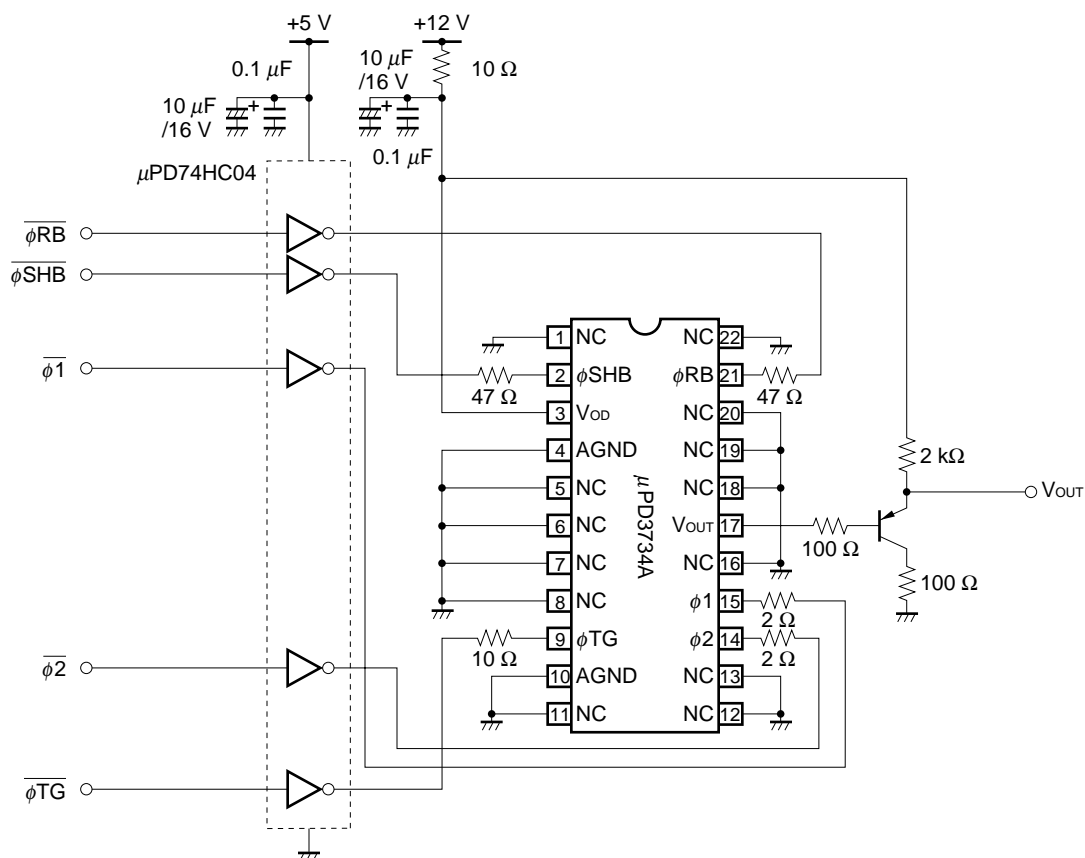


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

STANDARD CHARACTERISTIC CURVES ( $T_A = +25^\circ\text{C}$ )



# APPLICATION CIRCUIT EXAMPLE

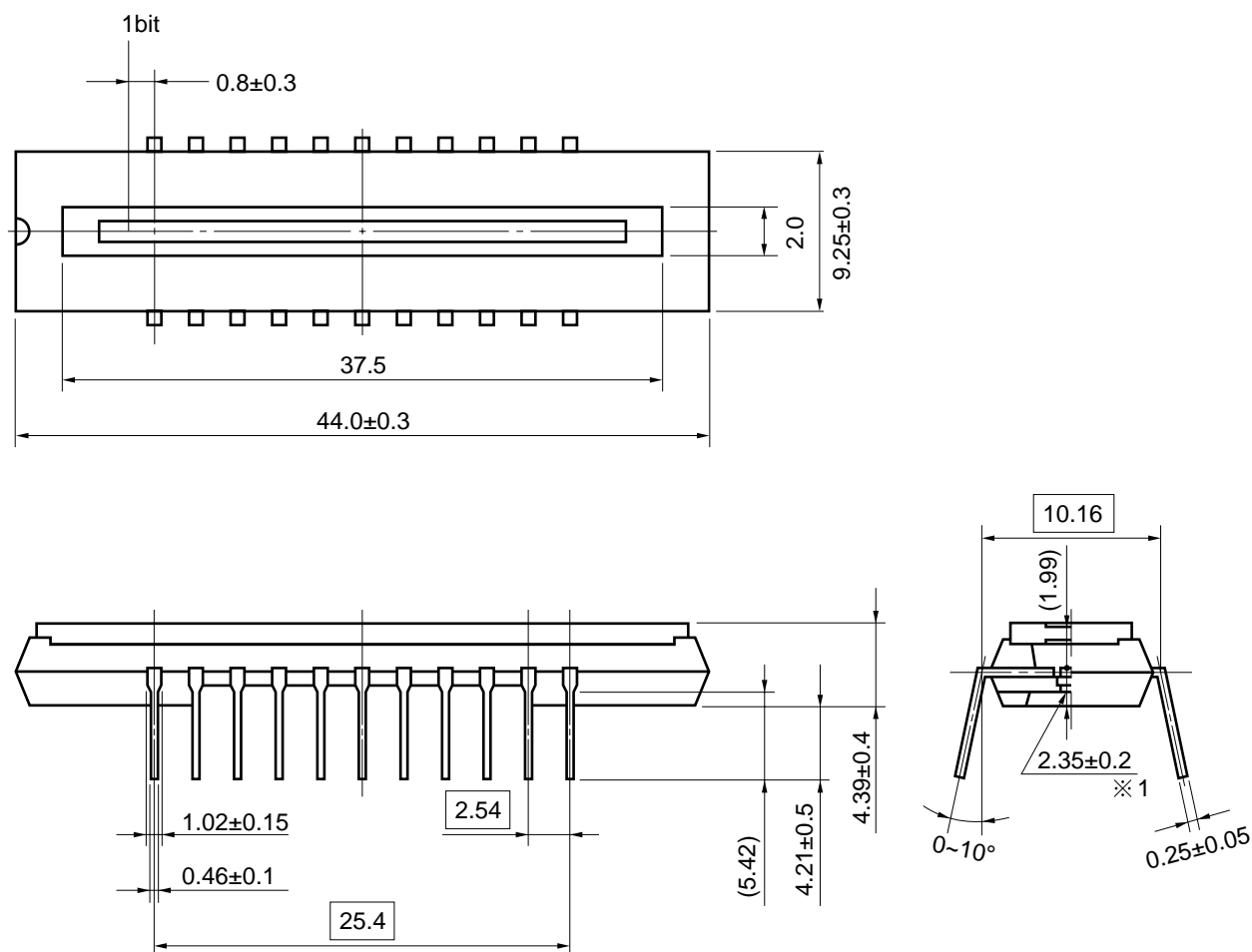


**Remark** When internal sample and hold circuit of the  $\mu$ PD3734A is not necessary, connect pin 2 ( $\phi$ SHB) to GND.

## PACKAGE DIMENSIONS

## CCD LINEAR IMAGE SENSOR 22PIN PLASTIC DIP (400 mil)

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	$42.9 \times 8.35 \times 0.7$ ※2	1.5

※1 The bottom of the package ↔ The surface of the chip

※2 The thickness of the cap over the chip

## RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document “**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**” (C10535E).

### Type of Through-hole Device

$\mu$ PD3734ACY: CCD linear image sensor 22-pin plastic DIP (400 mil)

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or less.
Partial heating method	Pin temperature: 260 °C or below, Heat time: 10 seconds or less (per each lead).

**Caution** For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

During assembly care should be taken to prevent solder or flux from contacting the plastic cap.  
The optical characteristics could be degraded by such contact.

## NOTES ON CLEANING THE PLASTIC CAP

### ① CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

### ② RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customer must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices in "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact NEC Sales Representative in advance.

Anti-radioactive design is not implemented in this product.