DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

# μPD3737

## 5150-BIT CCD LINEAR IMAGE SENSOR

The μPD3737 is a 5150-bit high sensitivity CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD3737 has high speed CCD register, so it is suitable for high resolution scanners and facsimiles which scan high definition document at high speed.

### FEATURES

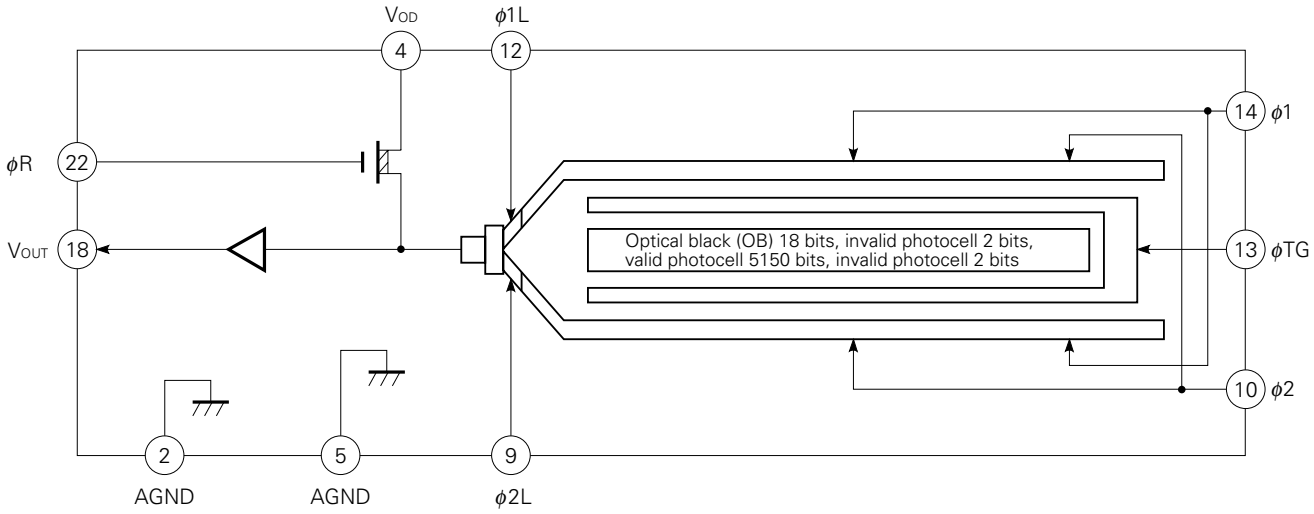
- Valid photocell: 5150-bit
- Photocell's pitch: 7 μm
- High response sensitivity: Providing a response 4.3 times better than the existing equivalent NEC product (μPD3571) to the light from a daylight fluorescent lamp
- Peak response wavelength: 550 nm (green)
- Resolution: 16 dot/mm across the shorter side of an A3-size (297 × 420 mm) sheet, 24 dot/mm across the shorter side of an A4-size (210 × 297 mm) sheet
- Power supply: +12 V
- Drive clock level: CMOS output under 5V operation
- High speed scan: 252 μs/line
- Data rate: 20 MHz

### ORDERING INFORMATION

| Part Number | Package | Quality Grade |
|---|---|---|
| μPD3737D | CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil) | Standard |

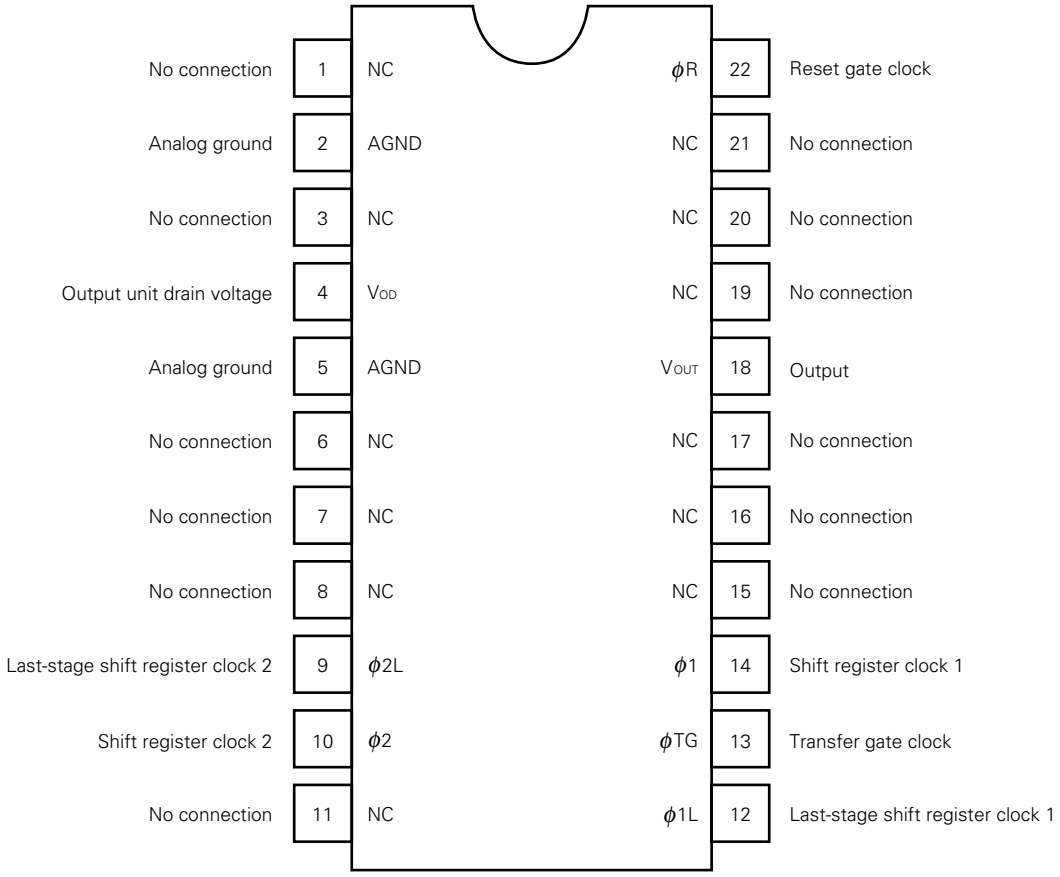
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

## BLOCK DIAGRAM

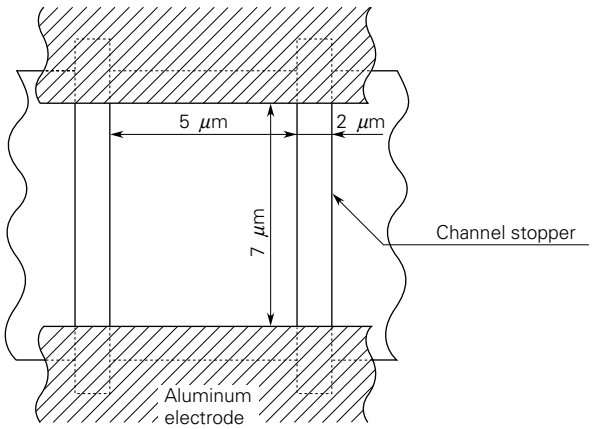


## PIN CONFIGURATION (Top View)

## CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)




## PHOTOELEMENT STRUCTURE DIAGRAM



## ABSOLUTE MAXIMUM RATINGS ($T_a$ = +25 °C)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Output unit drain voltage | $V_{OD}$ | –0.3 to +15 | V |
| Shift register clock voltage | $V_{\phi 1, \phi 2}$ | –0.3 to +15 | V |
| Last-stage shift register clock voltage | $V_{\phi 1L}$, $V_{\phi 2L}$ | –0.3 to +15 | V |
| Reset signal voltage | $V_{\phi R}$ | –0.3 to +15 | V |
| Transfer gate signal voltage | $V_{\phi TG}$ | –0.3 to +15 | V |
| Operating ambient temperature | $T_{opt}$ | –25 to +55 | °C |
| Storage temperature | $T_{stg}$ | –40 to +100 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_a$ = –25 to + 55 °C)

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Output unit drain voltage | $V_{OD}$ | 11.4 | 12.0 | 12.6 | V |
| Shift register clock signal high level | $V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 1LH}$, $V_{\phi 2LH}$ | 4.5 | 5.0 | 5.5 | V |
| Shift register clock signal low level | $V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 1LL}$, $V_{\phi 2LL}$ | –0.3 | 0 | +0.5 | V |
| Reset signal $\phi$R high level | $V_{\phi RBH}$ | 4.5 | 5.0 | 5.5 | V |
| Reset signal $\phi$R low level | $V_{\phi RBL}$ | –0.3 | 0 | +0.5 | V |
| Transfer gate signal high level | $V_{\phi TGH}$ | 4.5 | $V_{\phi 1H}$ | $V_{\phi 1H}$ | V |
| Transfer gate signal low level | $V_{\phi TGL}$ | –0.3 | 0 | +0.5 | V |
| Data rate | $f_{\phi R}$ | 0.5 | 1 | 20 | MHz |

**Remark 1.** Input reset signal $\phi$R to pin 22 via capacitor. Concerning the connection method refer to **APPLICATION EXAMPLE**.

**2.** Operating conditions of reset signal $\phi$R is not the condition at device pins but the conditions of the signal which applied to capacitor.

**3.** When $V_{\phi TGH} > V_{\phi 1H}$, image lag increases.

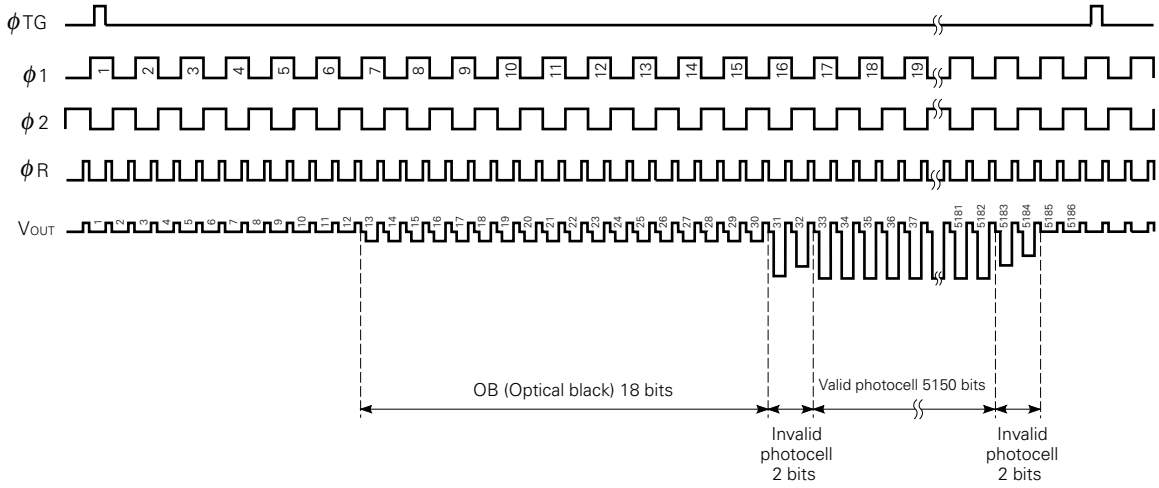
## ELECTRICAL CHARACTERISTICS

($T_a$ = +25 °C, $V_{DD}$ = 12 V, $f_{\phi 1}$ = 0.5 MHz, data rate = 1 MHz, storage time = 10 ms
light source: 3200 K halogen lamp + C500 (infrared cut filter), input clock = 5 $V_{P-P}$)

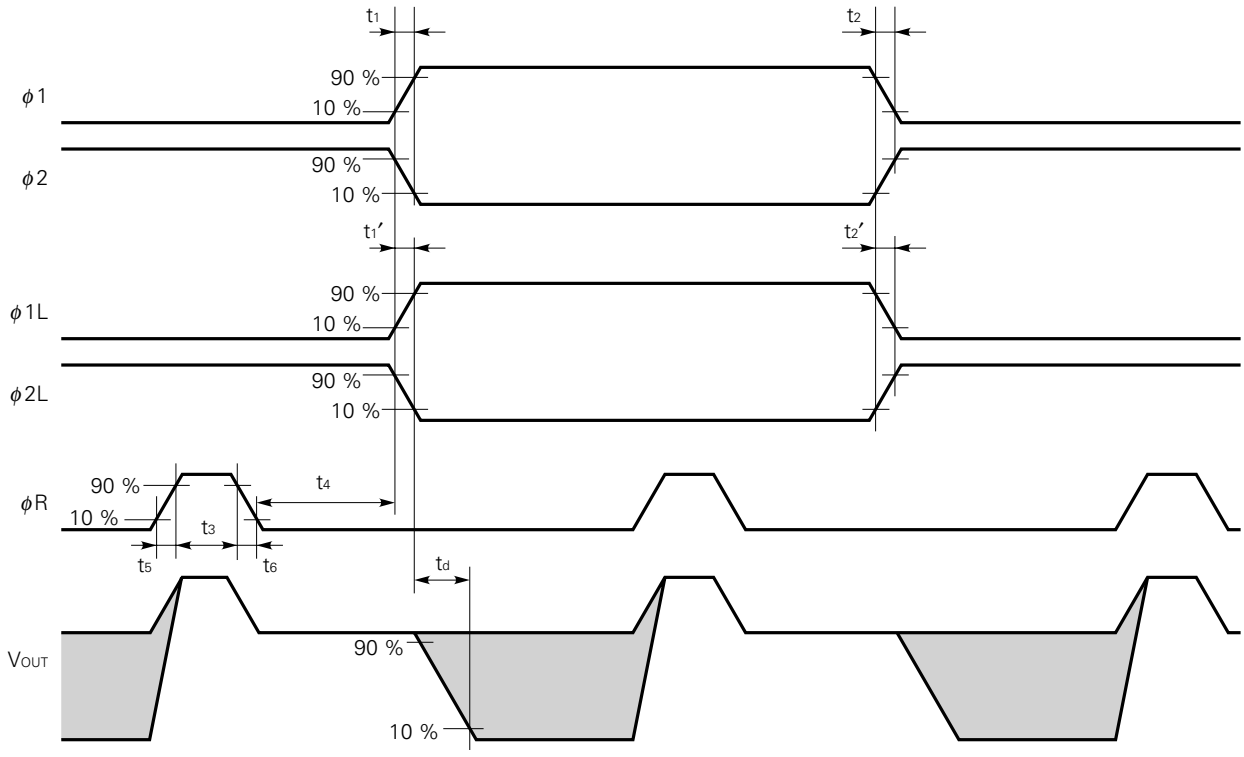
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit | |
|---|---|---|---|---|---|---|---|
| Saturation voltage | $V_{sat}$ | | 1.0 | 1.5 | | V | |
| Saturation exposure | SE | Daylight color fluorescent lamp | | 0.2 | | lx·s | |
| Photo response non-uniformity | PRNU | $V_{OUT}$ = 500 mV | | ±5 | ±10 | % | |
| Average dark signal | ADS | Light shielding | | 1.0 | 3.0 | mV | |
| Dark signal non-uniformity | DSNU | Light shielding | –3 | +3<br>–1 | +6 | mV | |
| Power consumption | $P_W$ | | | 100 | | mW | |
| Output impedance | $Z_O$ | | | 0.2 | 0.5 | kΩ | |
| Response | $R_F$ | Daylight color fluorescent lamp | 6 | 7.5 | 9 | V/lx·s | |
| Response peak wavelength | | | | 550 | | nm | |
| Image lag | IL | $V_{OUT}$ = 1 V | | 0.3 | 1 | % | ★ |
| Offset level | $V_{OS}$ | | 2.0 | 3.0 | 5.0 | V | |
| Input capacity of shift register clock pin | $C_{\phi 1}$<br>$C_{\phi 2}$ | | | 800 | | pF | |
| Input capacity of last-stage shift register clock pin | $C_{\phi 1L}$<br>$C_{\phi 2L}$ | | | 50 | | pF | |
| Input capacity of reset pin | $C_{\phi R}$ | | | 10 | | pF | |
| Input capacity of transfer gate clock pin | $C_{\phi TG}$ | | | 150 | | pF | |
| Output fall delay time | $t_d$ **Note** | Time from 90 % to 10 % of $\phi$2L fall is 5ns. | | 25 | | ns | ★ |
| Register imbalance | RI | $V_{OUT}$ = 500 mV | | 0 | 4 | % | |
| Transfer efficiency | TTE | $V_{OUT}$ = 500 mV, $f_{\phi R1}$ = 20 MHz | 92 | 98 | | % | |
| Dynamic range | DR | $V_{sat}$/DSNU | | 500 | | times | |
| Reset feed-through noise | RFSN | Light shielding | | 250 | 500 | mV | |

**Note** $t_d$ is defined as a time from 10 % of $\phi$2L to 10 % of $V_{OUT}$, output after passing through two steps of emitter follower in the application example. ★

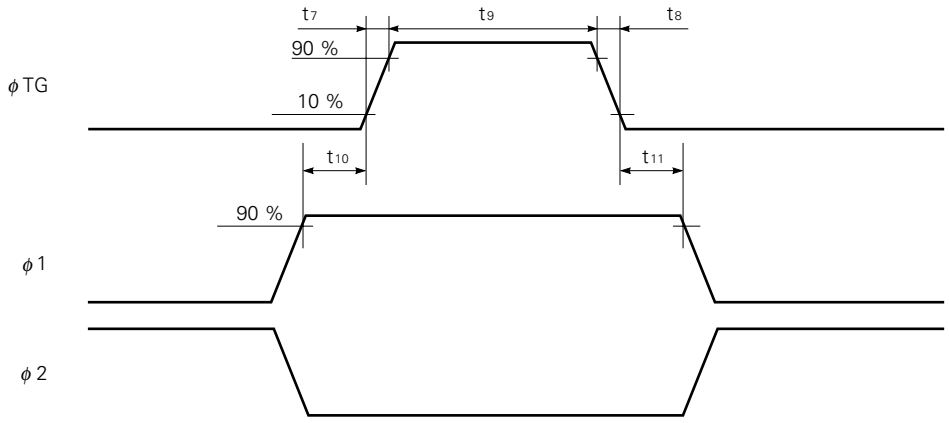
## TIMING CHART 1



**TIMING CHART 2**



## TIMING CHART for φTG, φ1, φ2

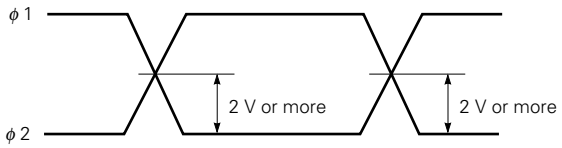



(Unit: ns)

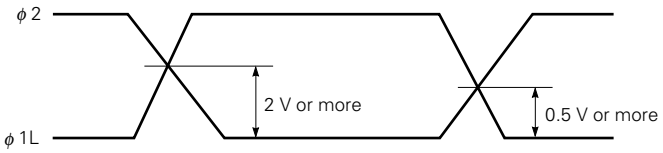
| Parameter | MIN. | TYP. | MAX. |
|---|---|---|---|
| $t_1$, $t_2$ | 0 | 50 | (150) |
| $t_1'$, $t_2'$ | 0 | 5 | (25) |
| $t_3$ | 15 | 50 | (500) |
| $t_4$ | 5 | 20 | (500) |
| $t_5$, $t_6$ | 0 | 20 | (50) |
| $t_7$, $t_8$ | 0 | 50 | (100) |
| $t_9$ | 500 | 1000 | (5000) |
| $t_{10}$, $t_{11}$ | 0 | 100 | (500) |

**Remark** The MAX. in the table above shows the operation range in which the output characteristics are kept almost enough for genaral purpose, does not show the limit above which the μPD3737 is destroied.

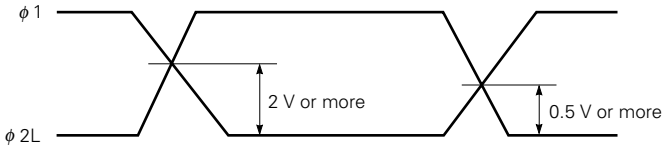
## CROSS POINTS for φ1, φ2




## CROSS POINTS for φ1L, φ2




## CROSS POINTS for φ1, φ2L




**Remark** Adjust cross point of (φ1, φ2), (φ1L, φ2), (φ1, φ2L) by each pin external input resistor.

## DEFINITIONS OF CHARACTERISTIC ITEMS

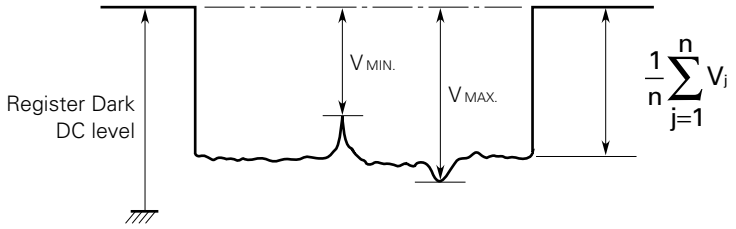
1. Saturation voltage: $V_{sat}$
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure: SE
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity: PRNU
   The peak/bottom ratio to the average output voltage of all the valid bits calculated by the following formula.

$$PRNU\ (\%) = \left( \frac{V_{MAX.} \text{ or } V_{MIN.}}{\frac{1}{n}\sum_{j=1}^{n} V_j} - 1 \right) \times 100$$

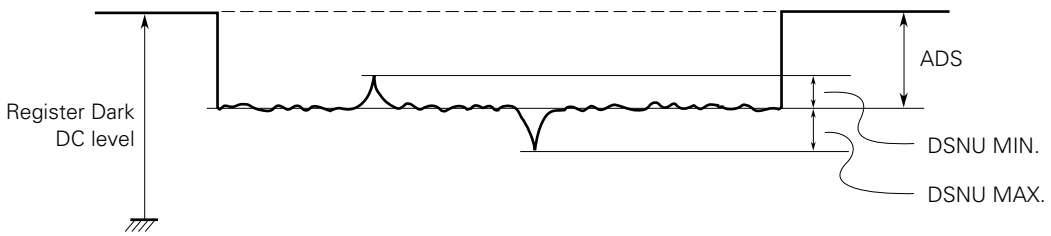
n : Number of valid bits
$V_j$ : Output voltage of each bit




4. Average dark signal: ADS
   Output average voltage in light shielding.

$$ADS(mV) = \frac{1}{n}\sum_{j=1}^{n} V_j$$

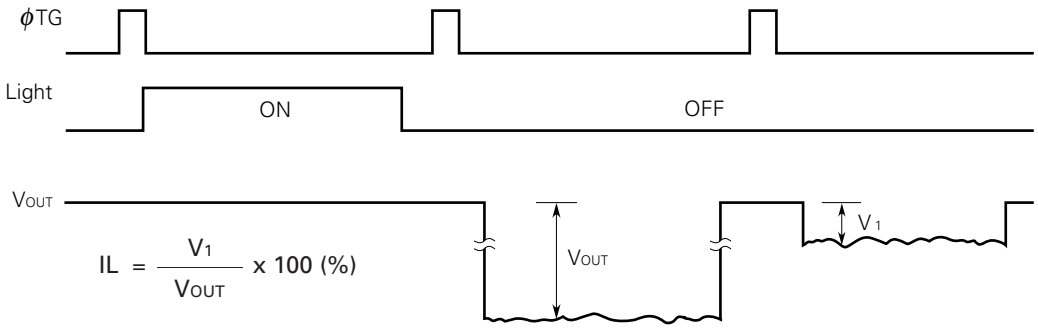
5. Dark signal non-uniformity: DSNU
   The difference between peak or bottom output voltage in light shielding and ADS.



6. Output impedance: $Z_o$
   Output pin impedance viewed from outside.

7. Response: R
   Output voltage divided by exposure (lx·s).
   Note that the response varies with the light source.

8. Image Lag: IL
   The rate between the last output voltage and the next one after read out the data of a line.



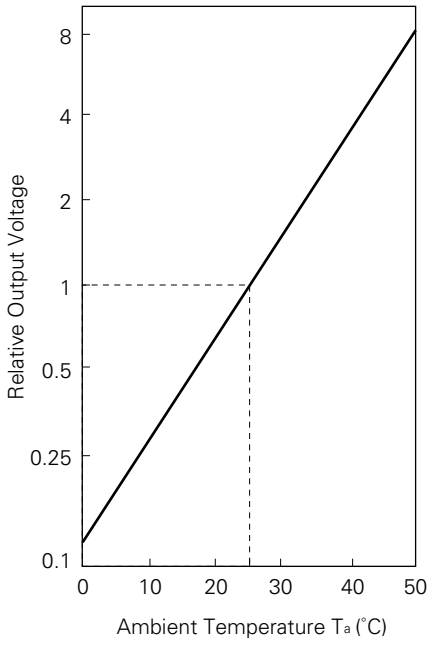

$$IL = \frac{V_1}{V_{OUT}} \times 100\ (\%)$$

9. Register Imbalance: RI
   The rate of the difference between the average of the output voltage of Odd and Even bits, against the average output voltage of all the valid bits.

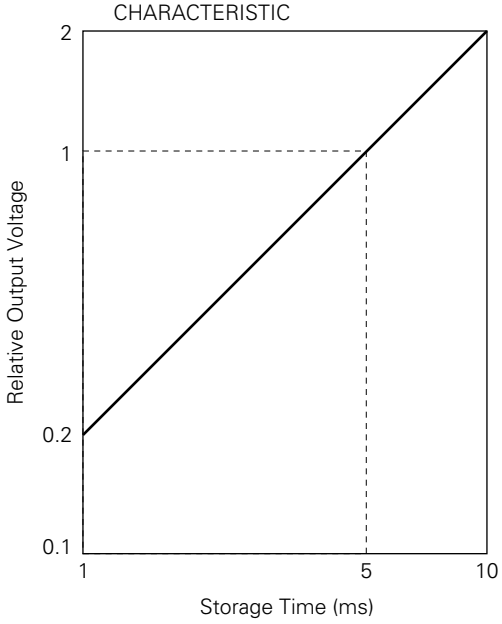
$$RI = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}}\left(V_{2j-1} - V_{2j}\right)\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100\ (\%)$$

## STANDARD CHARACTERISTIC CURVES ($T_a$ = 25 °C)

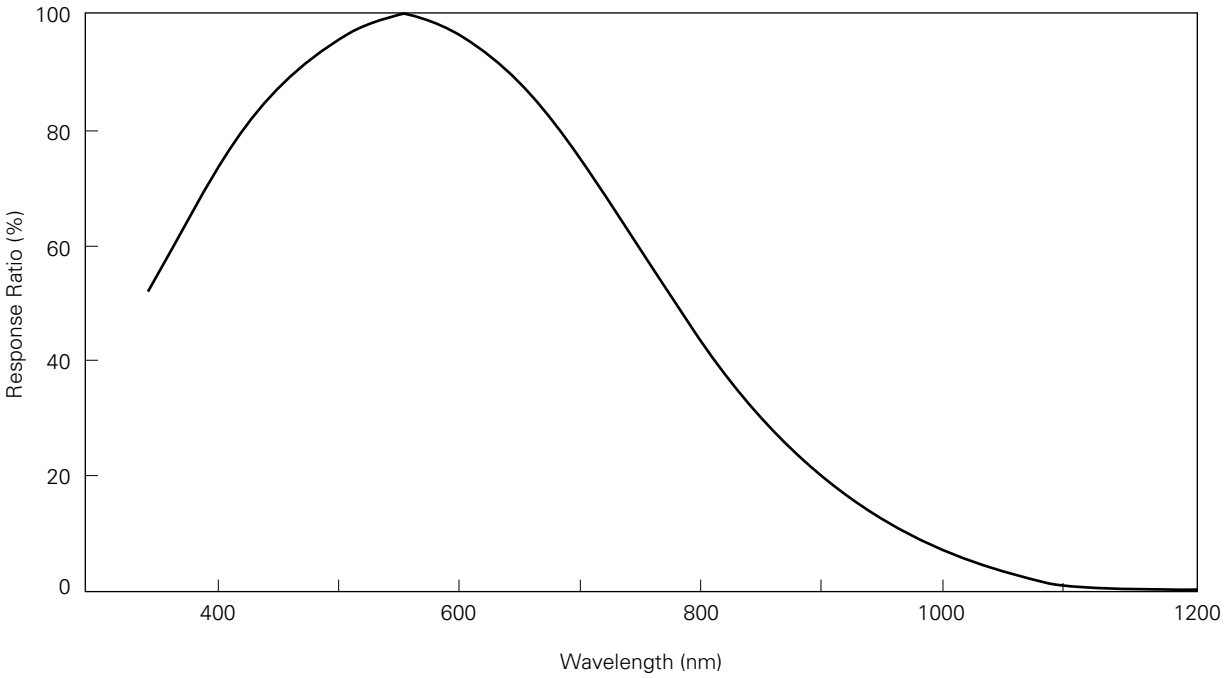
DARK OUTPUT TEMPERATURE CHARACTERISTIC



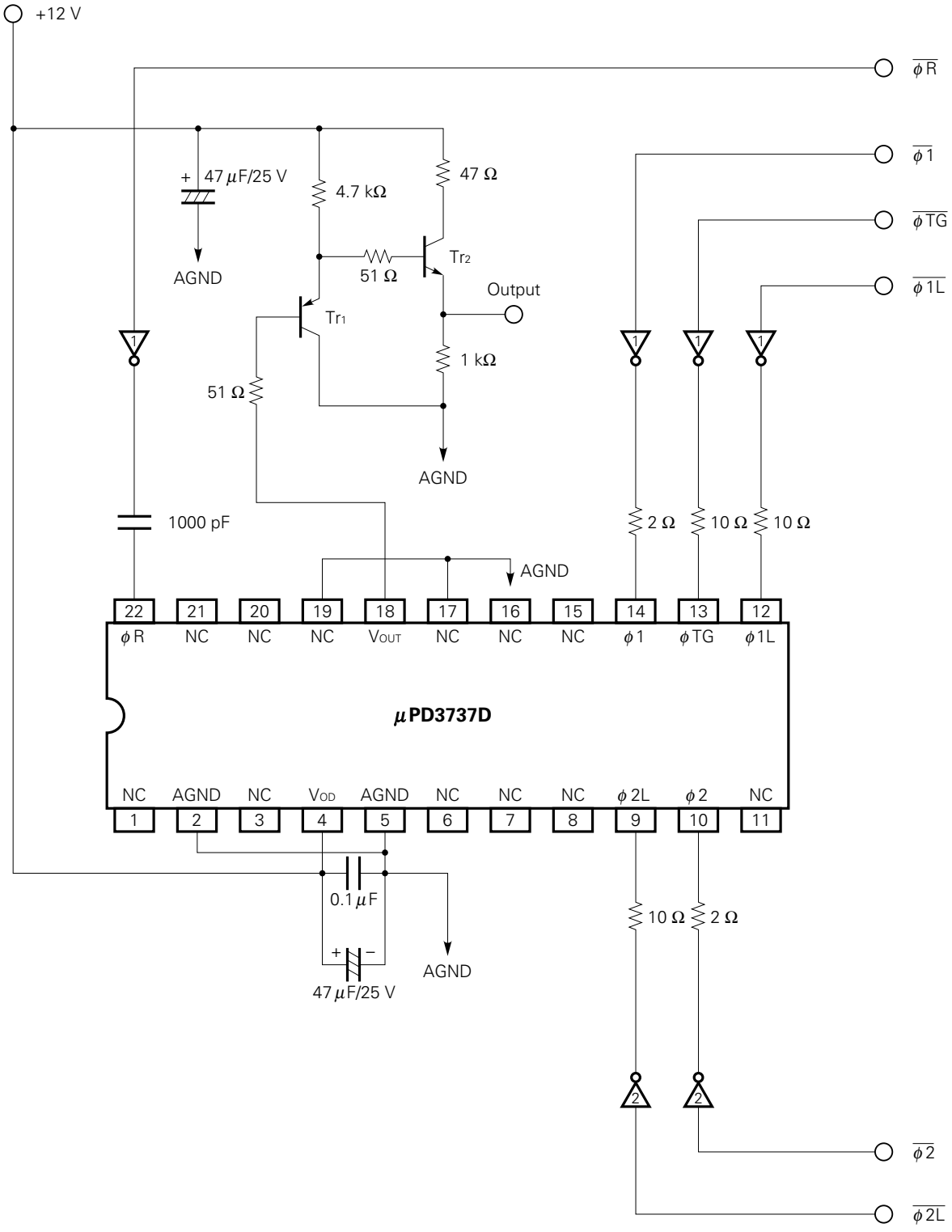

STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC




SPECTRAL RESPONSE CHARACTERISTIC



## APPLICATION EXAMPLE

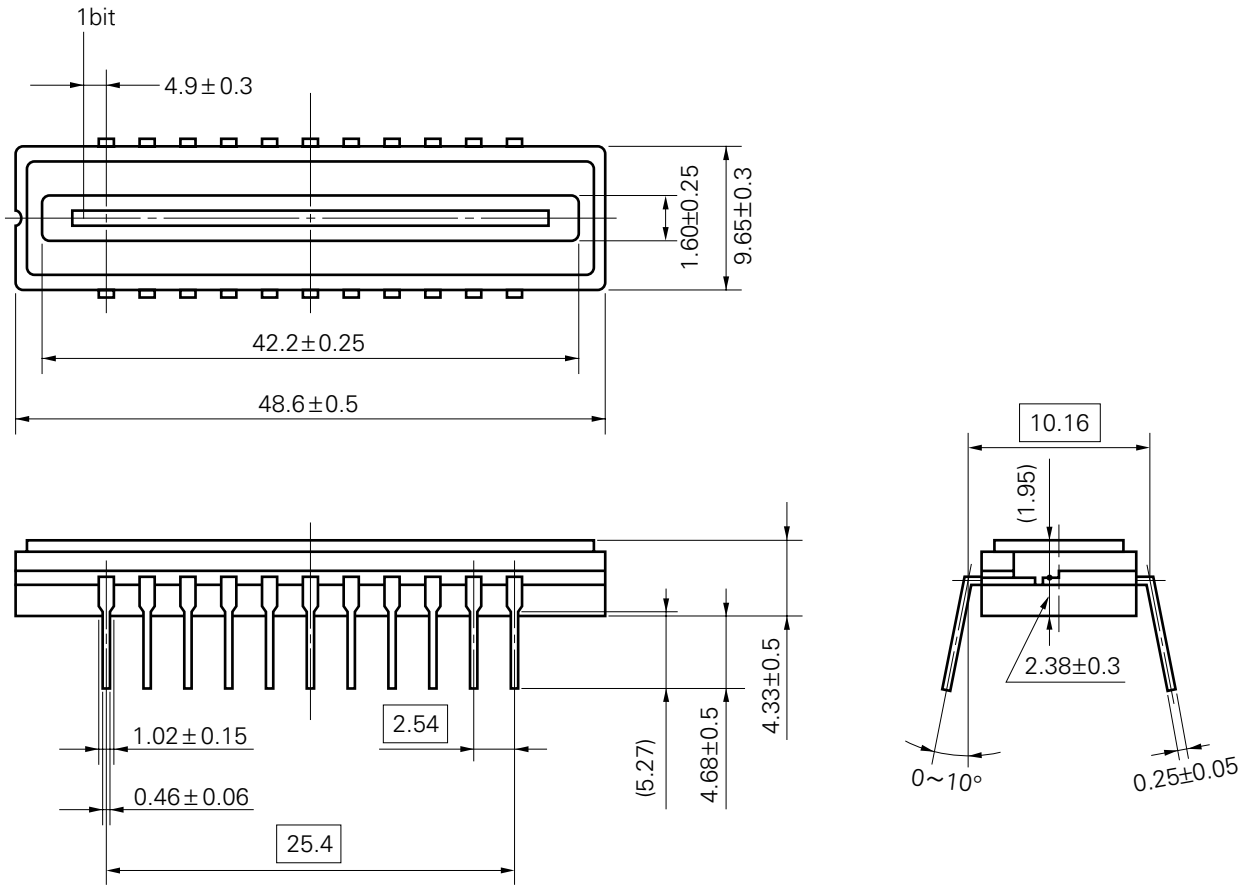



1. 74AC04 $Tr_1$ 2SA1005
2. 74AC04 $Tr_2$ 2SC945

## PACKAGE DIMENSIONS

### CCD LINEAR IMAGE SENSOR 22PIN CERAMIC DIP (CERDIP) (400mil)

(Unit : mm)




| Name | Dimensions | Refractive index |
|---|---|---|
| Glass cap | 47.5×9.25×0.7 | 1.5 |

22D-1CCD-PKG7

## RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207)**.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**Table 1 Type of Through Hole Device**

μPD3737D: CCD LINEAR IMAGE SENSOR 22 PIN CERAMIC DIP (CERDIP) (400 mil)

| Soldering Process | Soldering Conditions |
|---|---|
| Wave soldering<br>(For leads only) | Solder temperature: 260 °C or below,<br>Flow time: 10 seconds or below |
| Partial<br>heating method | Pin temperature: 260 °C or below,<br>Time: 10 seconds or below |

**Caution Do not jet molten solder on the surface of package.**

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

**[MEMO]**

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.



M4 92.6