

NEC

MOS INTEGRATED CIRCUIT

μ PD6325, μ PD6326, μ PD6335, μ PD6336

**QUAD/OCTAL 6BIT D/A CONVERTER
CMOS LSI**

DESCRIPTION

μ PD6325 Serise are 6 bit D/A Converter for control volumn, brightness, contrast, color or tone of TV set. The data are transferring serially from micro-computer.

μ PD6325 Serise Line-up	QUAD D/A	OCTAL D/A
D/A output is consist of Emitter follower buffer	μ PD6325C, 6325G	μ PD6326C
Non buffer output	μ PD6335C, 6335G	μ PD6336C

FEATURES

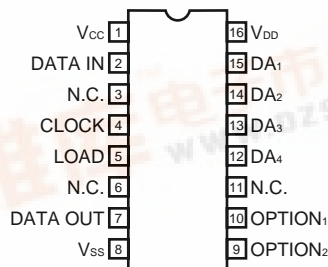
- R-2R ladder D/A
- Serial Data input (DATA IN, CLOCK, LOAD)
- Power supply voltage of interface is 5 V (Vcc) and D/A reference voltage is free (Vcc to 15 V).

ORDERING INFORMATION

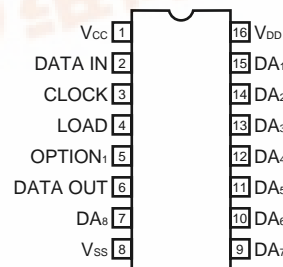
Part No.	Package
μ PD6325C	16-pin plastic DIP (300 mil)
μ PD6325G	16-pin plastic SOP (300 mil)
μ PD6326C	16-pin plastic DIP (300 mil)
μ PD6335C	16-pin plastic DIP (300 mil)
μ PD6335G	16-pin plastic SOP (300 mil)
μ PD6336C	16-pin plastic DIP (300 mil)

PIN CONNECTION DIAGRAM (Top View)

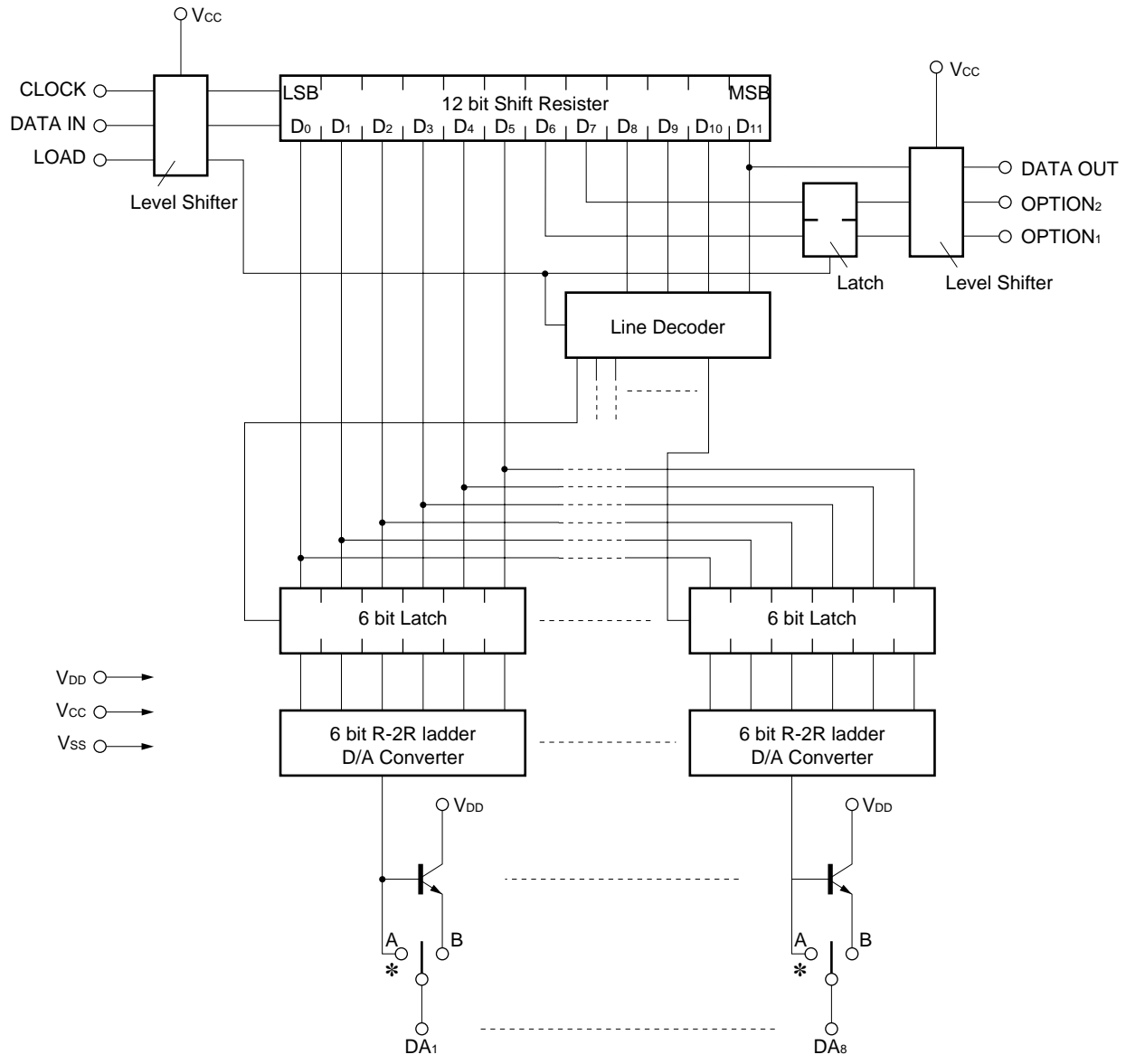
μ PD6325, μ PD6335



μ PD6326, μ PD6336



BLOCK DIAGRAM



*A ----- μ PD6335, μ PD6336
 B ----- μ PD6325, μ PD6326

μ PD6325, μ PD6326 have Quad D/As.

PIN CONFIGURATION

Pin No.		Symbol	Pin Name	Function
μ PD 6325 6335	μ PD 6326 6336			
1	1	V _{CC}	Interface Power Supply	This pin is used to interface with the control IC (ex. micro processor). Supply the voltage high level of the control IC.
2	2	DATA IN	Serial Data Input	Control data input terminal. Data is read in synchronization with the clocks input to the CLOCK terminal.
4	3	CLOCK	Shift Clock Input	Data read clock input terminal. The Data input to the DATA IN terminal is read at the leading edge of the clock.
5	4	LOAD	Load Pulse Input	This terminal is used to input Load signals after inputting serial data. 12 bit data is read after leading edge of a pulse input to the LOAD terminal.
7	6	DATA OUT	Serial Data Output	Serial data output terminal. The final stage data of 12 bit shift register appears on this terminal in synchronization with shift clock.
8	8	V _{SS}	Ground	System ground.
9	–	OPTION ₂	Expansion Output Port	D ₇ the data of the shift register appears on this terminal. (Only μ PD6325 and μ PD6335)
10	5	OPTION ₁	Expansion Output Port	D ₆ the data of the shift register appears on this terminal.
–	7	DA ₈	Analog Output Channel 8	Analog Output
–	9	DA ₇	Analog Output Channel 7	Analog Output
–	10	DA ₆	Analog Output Channel 6	Analog Output
–	11	DA ₅	Analog Output Channel 5	Analog Output
12	12	DA ₄	Analog Output Channel 4	Analog Output
13	13	DA ₃	Analog Output Channel 3	Analog Output
14	14	DA ₂	Analog Output Channel 2	Analog Output
15	15	DA ₁	Analog Output Channel 1	Analog Output
16	16	V _{DD}	Power Supply	Reference Voltage for D/A converters. Analog output voltage range is GND to V _{DD} .

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Supply Voltage	V _{DD} , V _{CC}	-0.5 to +18, V _{CC} ≤ V _{DD}	V
Output Voltage	V _{OUT}	-0.5 to V _{DD} +0.5	V
Input Voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Input Current	I _{IN}	10	mA
Emitter Follower Current	I _{OE}	10	mA
Power Dissipation	P _D	500*/200**	mW
Operating Temperature	T _A	-40 to +85	°C
Storage Temperature	T _{stg}	-65 to +125	°C

*DIP

**SOP

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Supply Voltage	V _{DD}	V _{CC}		15	V	V _{CC} ≤ V _{DD}
Supply Voltage of Interface	V _{CC}	4.5	5.0	5.5	V	V _{CC} ≤ V _{DD}
Low Level Input Voltage	V _{IL}			0.8	V	V _{CC} = 5 V, V _{DD} = 5 to 15 V
High Level Input Voltage	V _{IH}	3.5			V	V _{CC} = 5 V, V _{DD} = 5 to 15 V
Only μ PD6325 & μ PD6326						
Emitter Follower Power Dissipation 1	P _E /unit			5	mW	T _A = 85 °C
Emitter Follower Power Dissipation 2	P _E /unit			15	mW	T _A = 70 °C
Emitter Follower Power Dissipation 3	P _E total			25	mW	T _A = 85 °C
Emitter Follower Power Dissipation 4	P _E total			75	mW	T _A = 70 °C
TIMING CONDITIONS (T _A = -40 to +85 °C, V _{SS} = 0 V, V _{CC} = 5 V, V _{DD} = V _{CC} to 15 V)						
CLOCK High Level Width	t _{CH}	4.0			μs	
CLOCK Low Level Width	t _{CL}	10.0			μs	
CLOCK Rise Time	t _{cr}			1.0	μs	
CLOCK Fall Time	t _{cf}			1.0	μs	
DATA IN Setup Time	t _{Dsetup}	2			μs	
DATA IN Hold Time	t _{Dhold}	10			μs	
Pulse Width, LOAD High	t _{W(Load)}	4			μs	
LOAD Lead Time	t _{Llead}	10			μs	
LOAD Lag Time	t _{Llag}	10			μs	

ELECTRICAL CHARACTERISTICS

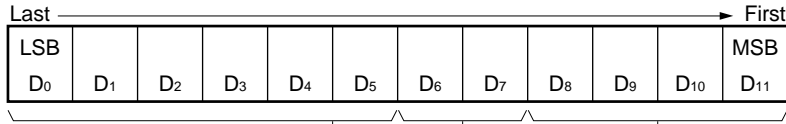
($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V, $V_{CC} = 4.5$ to 5.5 V, $V_{DD} = V_{CC}$ to 15 V)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Current Consumption	I_{DD}			15	mA	No Load, for μ PD6326, 6336
Current Consumption	I_{DD}			10	mA	No Load, for μ PD6325, 6335
Current Consumption of Interface	I_{CC}			10	μ A	No Load of DATA OUT, Static Consumption
Input Leak Current	I_{LEAK}			± 1	μ A	$V_{IN} = V_{CC}$ or V_{SS}
DATA OUT High Level Output Voltage	I_{OH}	-100			μ A	$V_{OH} = V_{DD} - 0.5$ V
DATA OUT Low Level Output Voltage	I_{OL}	100			μ A	$V_{OL} = 0.5$ V
Emitter Follower Leak Current	I_{OLEAK}			20	μ A	for μ PD6325, 6326
Settling Time	$t_{DA\ set}$			10	μ s	Note

Note μ PD6325, 6326: $R_L = 20$ k Ω , $C_L = 50$ pF
 μ PD6335, 6336: No Load.

DATA CONFIGURATION

Data Length is 12 bit.



D/A output CONTROL BIT

D ₁₁	D ₁₀	D ₉	D ₈	Select D/A	Target device
0	0	0	0	Don't Care	μPD6325, 6326 μPD6335, 6336
0	0	0	1	DA ₁	μPD6325, 6326 μPD6335, 6336
0	0	1	0	DA ₂	μPD6325, 6326 μPD6335, 6336
0	0	1	1	DA ₃	μPD6325, 6326 μPD6335, 6336
0	1	0	0	DA ₄	μPD6325, 6326 μPD6335, 6336
0	1	0	1	DA ₅	μPD6326 μPD6336
0	1	1	0	DA ₆	μPD6326 μPD6336
0	1	1	1	DA ₇	μPD6326 μPD6336
1	0	0	0	DA ₈	μPD6326 μPD6336
1	×	×	×	Don't Care	μPD6325, 6326 μPD6335, 6336

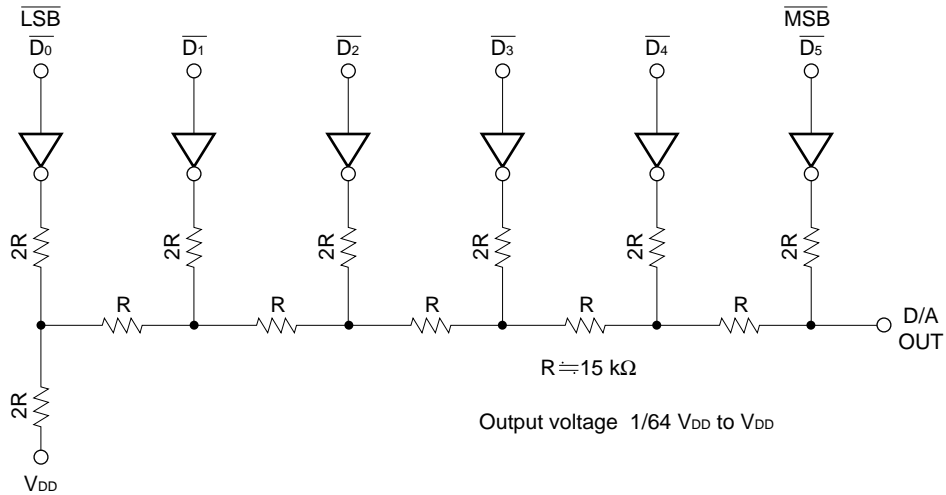
OPTION output CONTROL BIT

D ₇	D ₆	OPTION ₁ out.	OPTION ₂ out.	Note
0	0	L	L	OPTION2 is only μPD6325, 6326
0	1	H	L	OPTION2 is only μPD6325, 6326
1	0	L	H	OPTION2 is only μPD6325, 6326
1	1	H	H	OPTION2 is only μPD6325, 6326

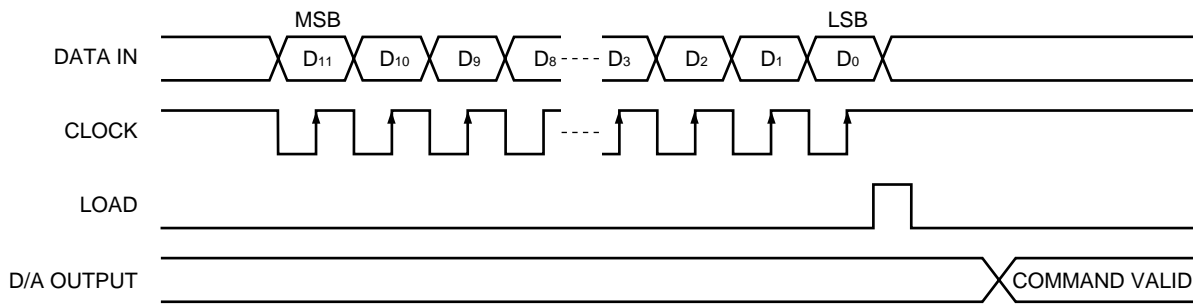
D/A Output Voltage CONTROL BIT

D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Output Voltage
0	0	0	0	0	0	≡ V _{DD} /64
0	0	0	0	0	1	≡ 2 x V _{DD} /64
0	0	0	0	1	0	≡ 3 x V _{DD} /64
0	0	0	0	1	1	≡ 4 x V _{DD} /64
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	≡ 63 x V _{DD} /64
1	1	1	1	1	1	≡ V _{DD}

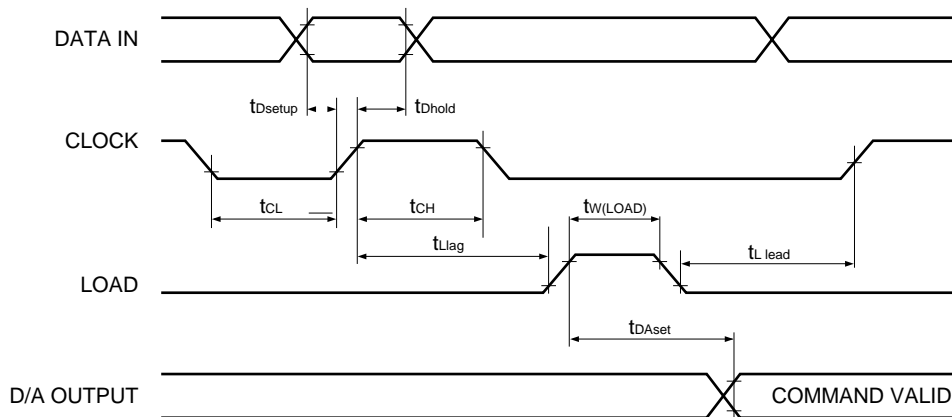
EQUIVALENT CIRCUIT OF 6 bit D/A



TIMING CHART

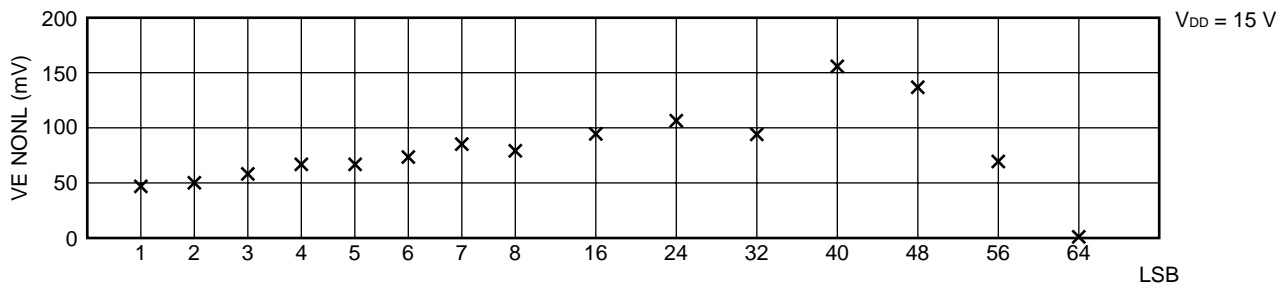
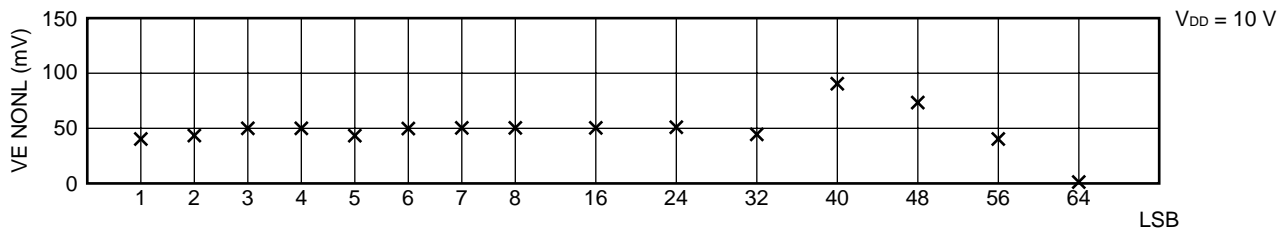
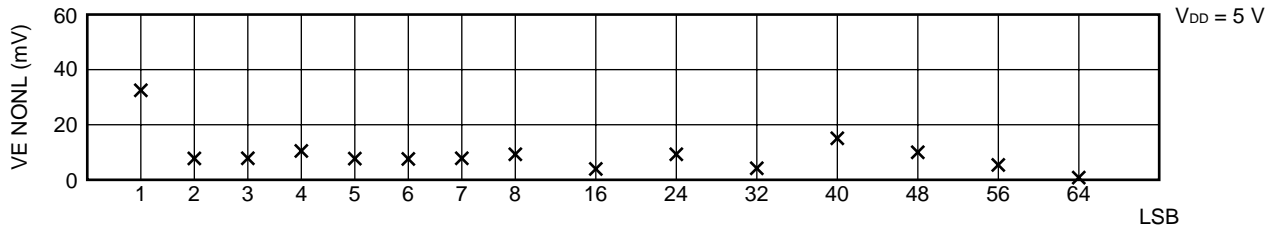


Data is loaded when LOAD is high level.

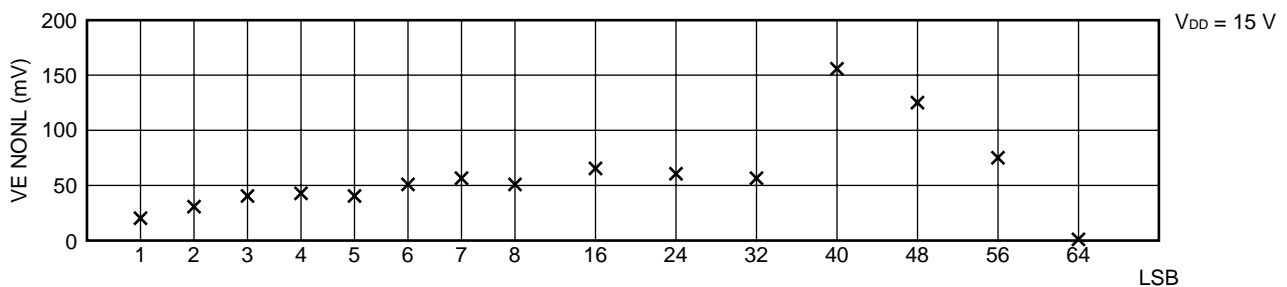
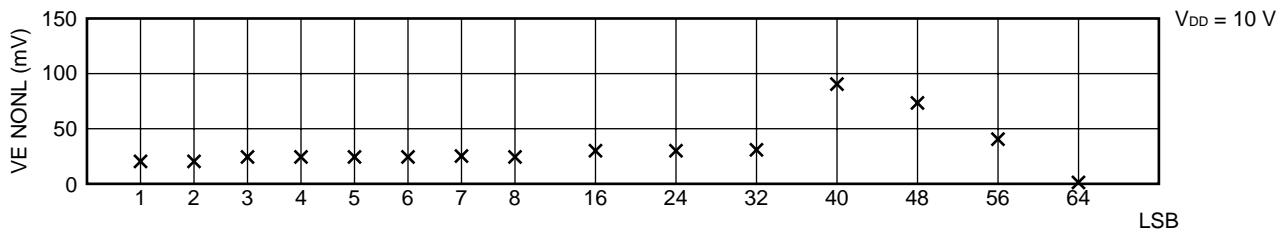
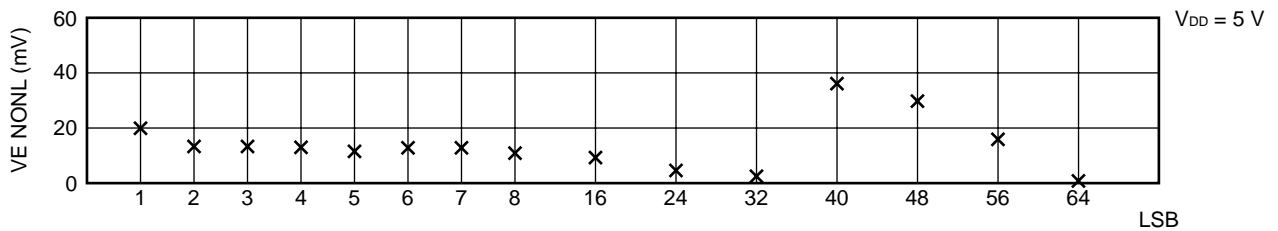


LINIARITY OF D/A OUTPUT (μ PD6335, 6336) (TYP.)

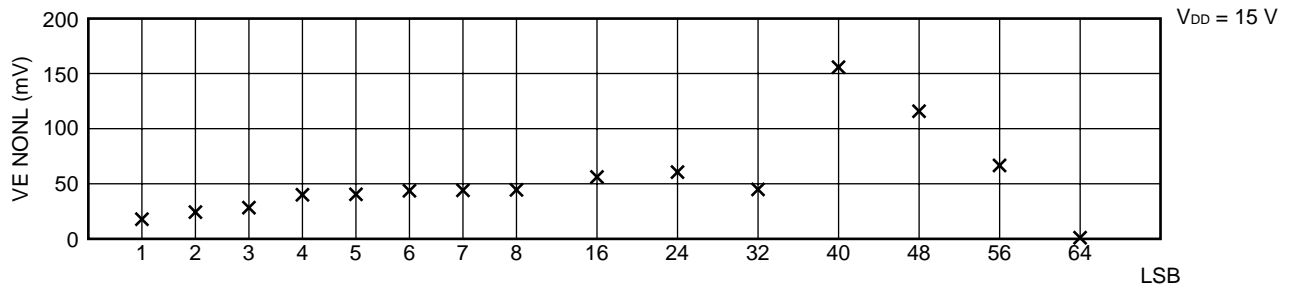
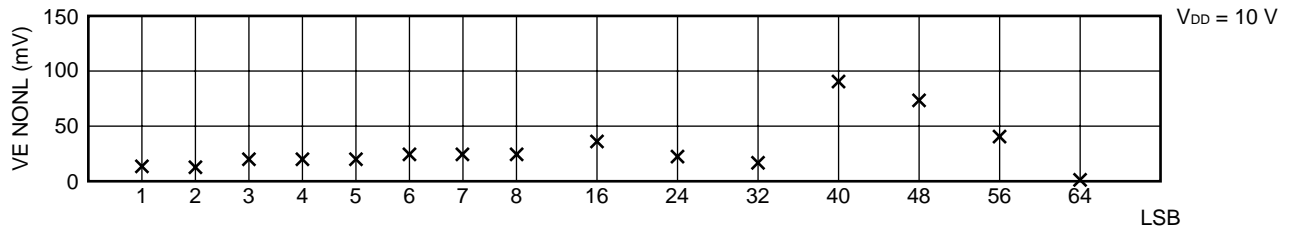
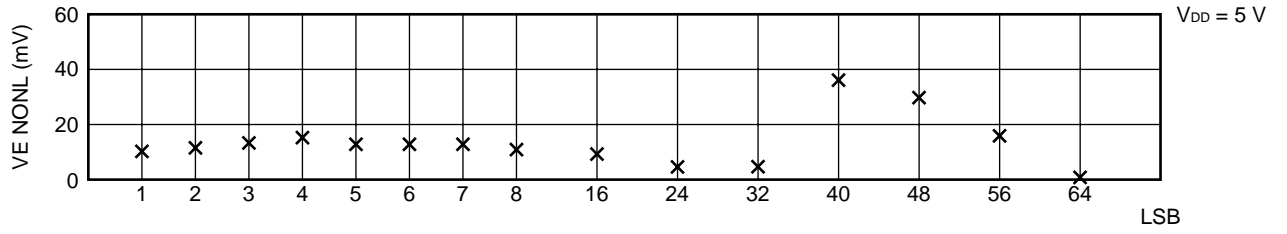
• $T_A = -40\text{ }^\circ\text{C}$



• $T_A = 25\text{ }^\circ\text{C}$



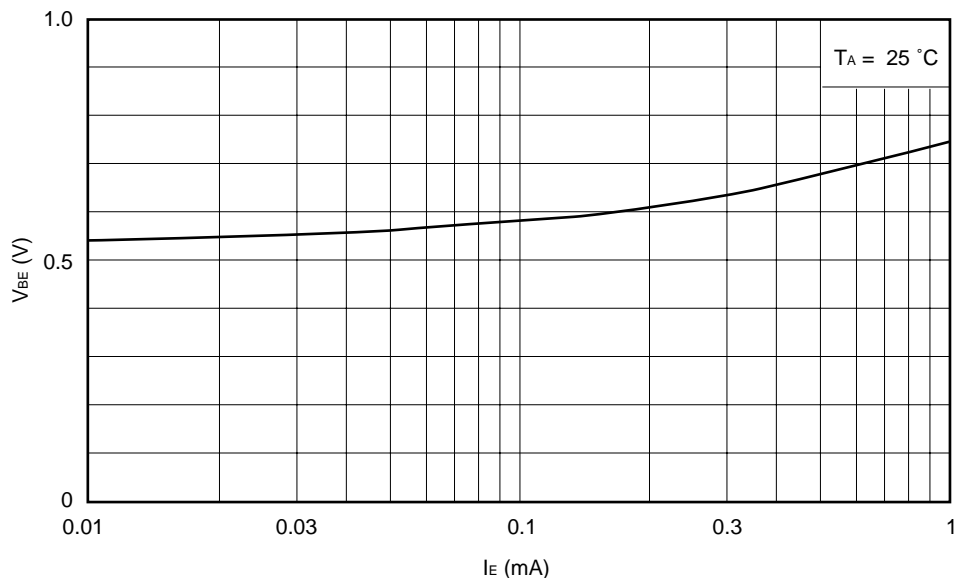
• $T_A = 85\text{ }^\circ\text{C}$



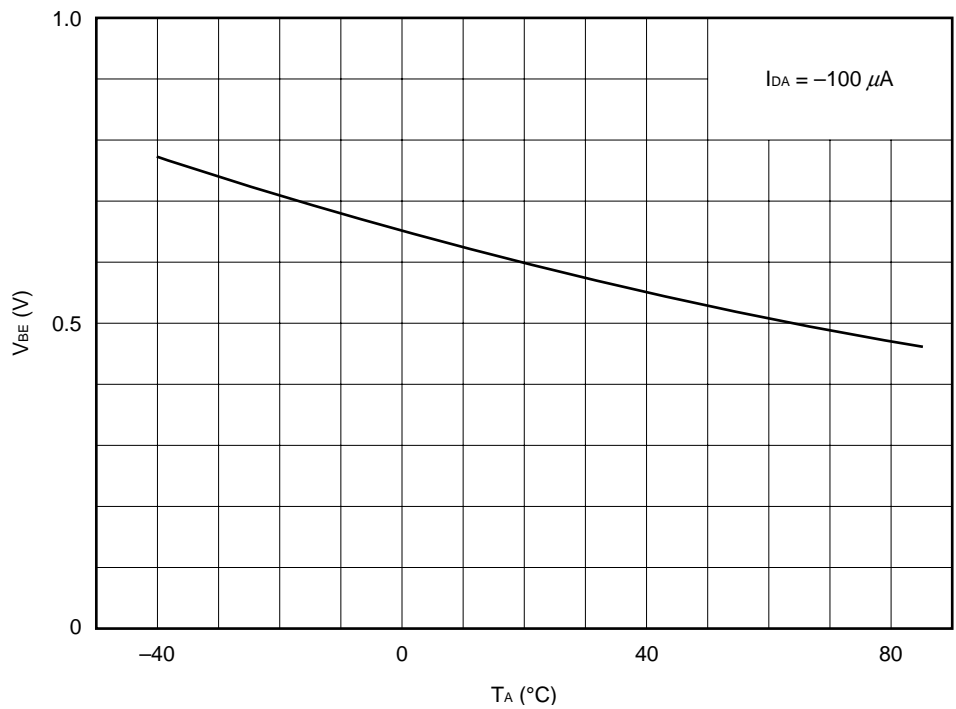
* $VE\ NONL = (MEASUREMENT\ VALUE) - (IDEAL\ VALUE)$

Characteristics of Emitter follower buffer (μ PD6325, 6326)

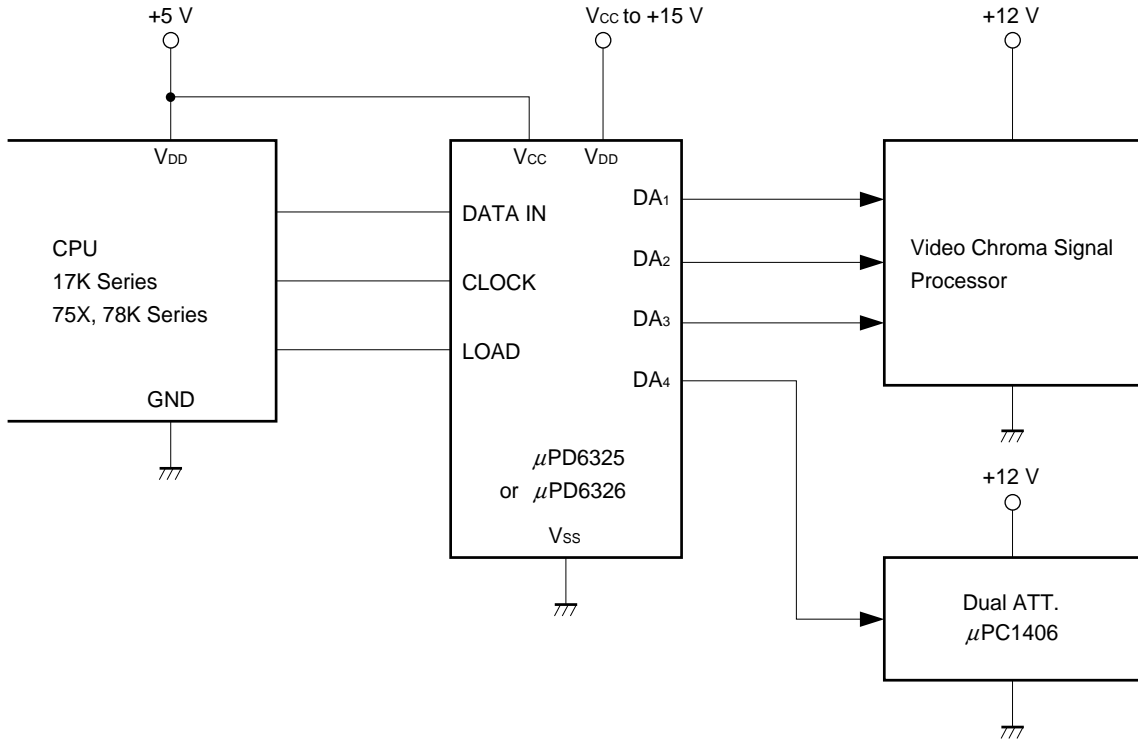
(1) $V_{BE} - I_E$ (including R-2R's resistor)



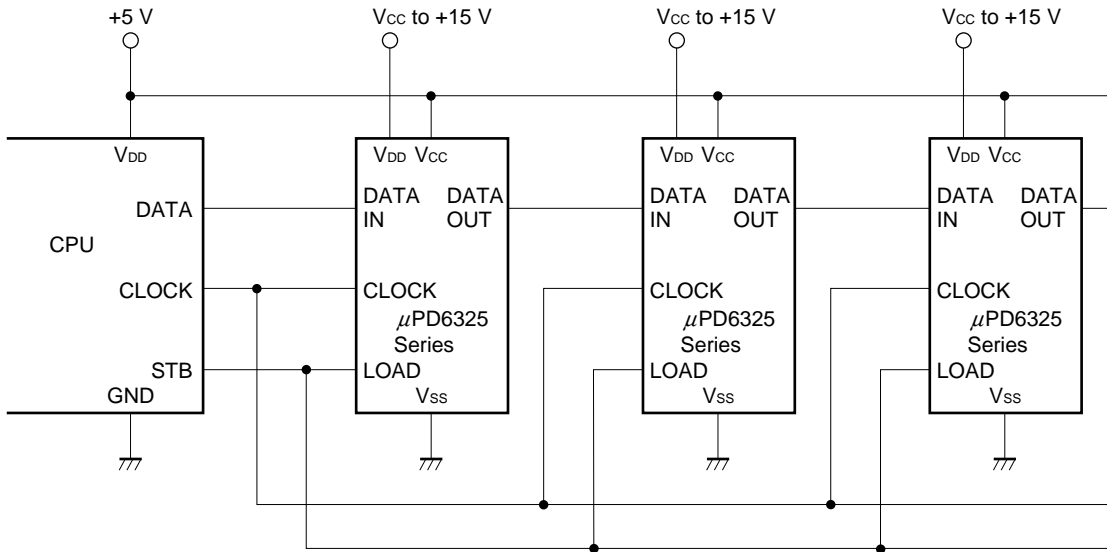
(2) $V_{BE} - T_A$



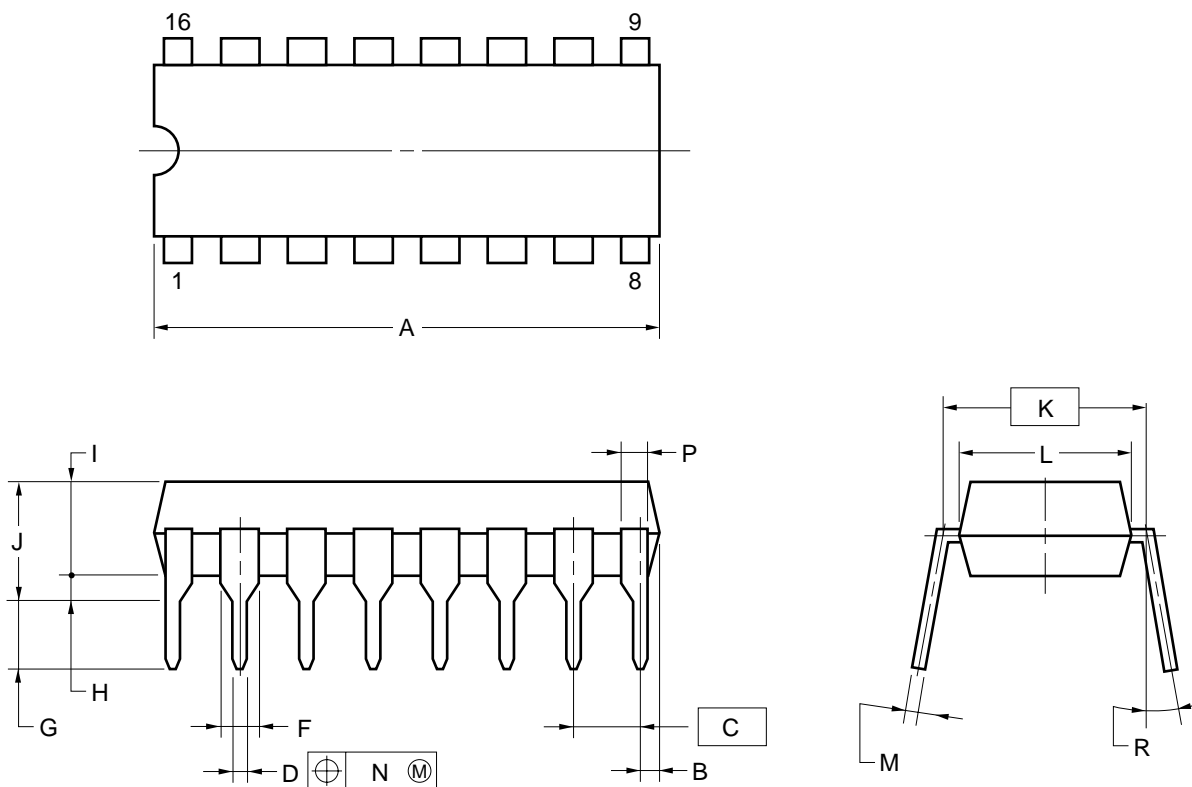
APPLICATION FOR TV SET



APPLICATION FOR CASCADE CONNECTING



16PIN PLASTIC DIP (300 mil)



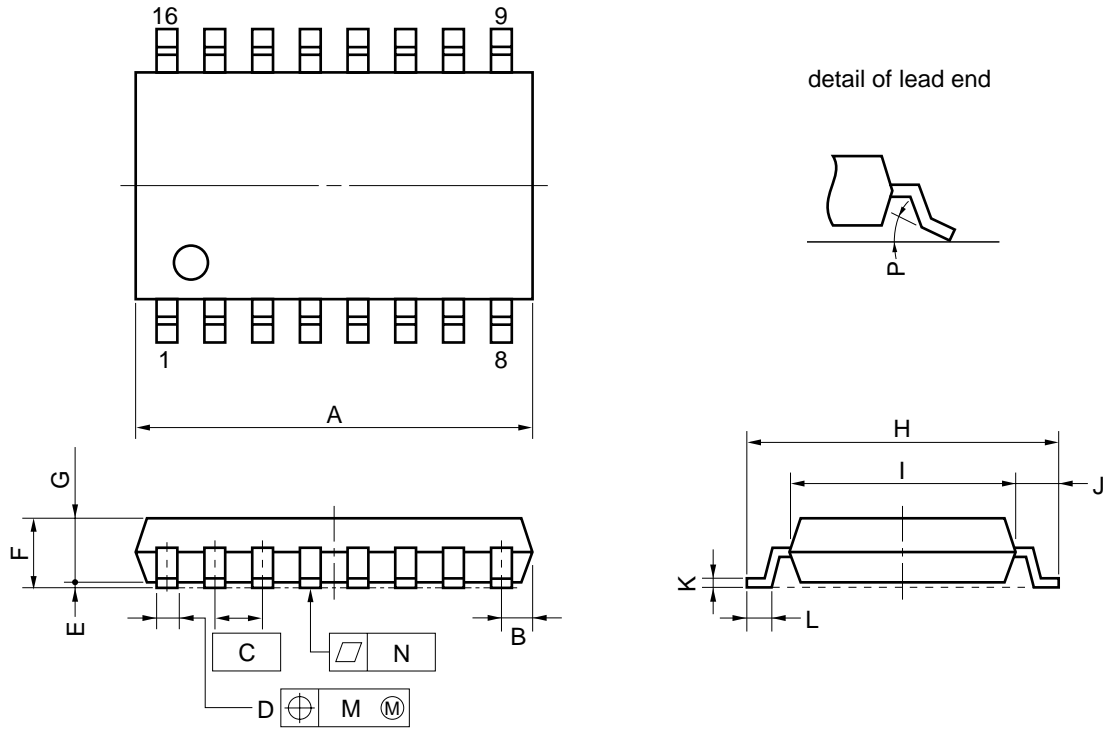
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50±0.10	0.020 ^{+0.004} _{-0.005}
F	1.2 MIN.	0.047 MIN.
G	3.5±0.3	0.138±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 ^{+0.10} _{-0.05}	0.010 ^{+0.004} _{-0.003}
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.
R	0~15°	0~15°

P16C-100-300A,C-1

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 ^{+0.10} _{-0.05}	0.016 ^{+0.004} _{-0.003}
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	0.20 ^{+0.10} _{-0.05}	0.008 ^{+0.004} _{-0.002}
L	0.6±0.2	0.024 ^{+0.008} _{-0.009}
M	0.12	0.005
N	0.10	0.004
P	3°+7° -3°	3°+7° -3°

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	IEI-1212
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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