DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD6379, 6379A, 6379L, 6379AL

2-CHANNEL 16-BIT D/A CONVERTER FOR AUDIO APPLICATION

The μPD6379 and 6379A are 2-channel 16-bit D/A converters for digital audio signal demodulation. These D/A converters employ the resistor string conversion method which has been tested by existing model μPD6376 but they are more compact and require fewer external components than the μPD6376. In addition, low-voltage models, the μPD6379L and 6379AL (minimum operating supply voltage = +3.0 V) are also available for applications in portable systems.

FEATURES

- Resistor string conversion method
- 0-point digital shift circuit
- × 4 oversampling
  Sampling frequency: 200 kHz MAX.
- Signal processing format for 2's complement, MSB first, and backward justification data accommodated
- Left and right in-phase output
- High performance (at V_{DD} = +5.0 V)
  S/N ratio: 100 dB TYP.
  Dynamic range: 96 dB TYP.
- Low-voltage models available
- Bipolar LR clock (LRCK)
- Low power dissipation: 10 mW TYP.
  (with μPD6379L, 6379AL at V_{DD} = +3.3 V)

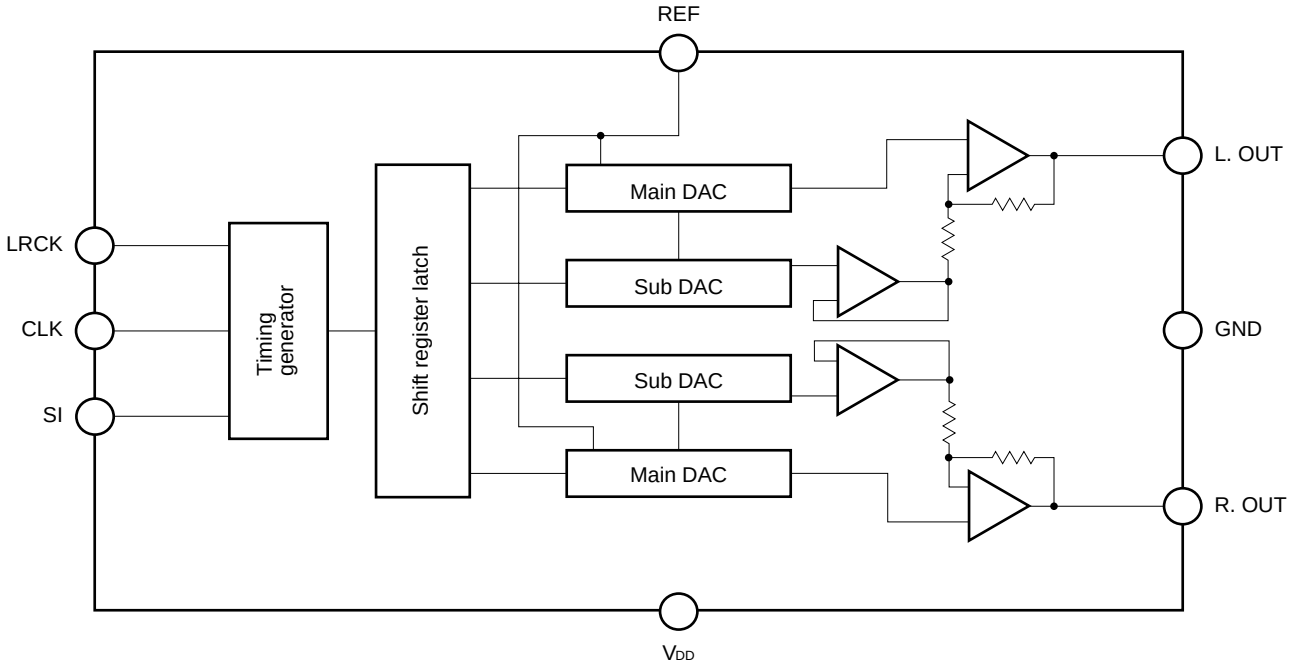
LRCK / Supply voltage	LRCK = L when L-ch data is input	LRCK = H when L-ch data is input
+3.3 V (V_{DD} = +3.0 to 5.5 V)	μPD6379L	μPD6379AL
+5.0 V (V_{DD} = +4.5 to 5.5 V)	μPD6379	μPD6379A

- Few external components
  Internal output operational amplifier
  Only one electrolytic capacitor required for smoothing reference voltage, instead of two capacitors required by existing D/A converters
- Small package: 8-pin plastic SOP (5.72 mm (225))

ORDERING INFORMATION

Part number	Package
μPD6379GR	8-pin plastic SOP (5.72 mm (225))
μPD6379LGR	8-pin plastic SOP (5.72 mm (225))
μPD6379AGR	8-pin plastic SOP (5.72 mm (225))
μPD6379ALGR	8-pin plastic SOP (5.72 mm (225))

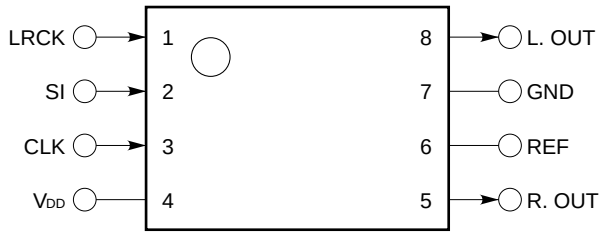
BLOCK DIAGRAM



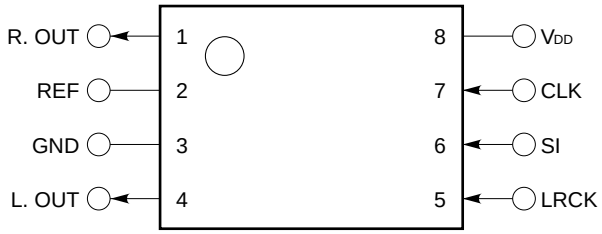
PIN CONFIGURATIONS (Top View)

8-pin plastic SOP (5.72 mm (225))

- **μPD6379GR, 6379LGR**



- **μPD6379AGR, 6379ALGR**



Remark The pin configuration of the μPD6379 and 6379L is different from that of the μPD6379A and 6379AL.

1. PIN FUNCTIONS

Table 1-1 Pin Functions

Pin No.		Name	Symbol	I/O	Function
μPD6379, 6379L	μPD6379A, 6379AL				
1	5	Left/Right Clock	LRCK	Input	Input pin to identify left or right input data. μPD6379, 6379L: Input "L" to this pin when inputting L-ch data to SI pin. μPD6379A, 6379AL: Input "H" to this pin when inputting L-ch data to SI pin.
2	6	Serial Input	SI	Input	Serial data input pin. Input data on 2's complement, MSB first, and backward justification.
3	7	Clock	CLK	Input	Serial input data read clock (bit clock) input pin
4	8	Supply Voltage	V_{DD}	–	Positive power supply pin
5	1	R-ch Output	R. OUT	Output	Right analog signal output pin
6	2	Reference Voltage	REF	–	Reference voltage pin. Connect this pin to GND through capacitor.
7	3	Ground	GND	–	GND pin
8	4	L-ch Output	L. OUT	Output	Left analog signal output pin

2. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	– 0.3 to +7.0	V
Input voltage	V_I	– 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	– 0.3 to V_{DD} + 0.3	V
Permissible package power dissipation	P_D	220 (T_A = 75 °C)	mW
Operating ambient temperature	T_A	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

μPD6379, 6379A

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Logic input voltage (HIGH)	V_{IH}		0.7 V_{DD}		V_{DD}	V
Logic input voltage (LOW)	V_{IL}		0		0.3 V_{DD}	V
Operating ambient temperature	T_A		–20	+25	+75	°C
Output load resistance	R_L	R. OUT, L. OUT pins	5			kΩ
Conversion frequency	f_S				200	kHz
Clock frequency	f_{CLK}				10	MHz
Clock pulse width	t_{SCK}		40			ns
SI, LRCK setup time	t_{DC}		12			ns
SI, LRCK hold time	t_{CD}		12			ns

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V_{DD} = +5 V, f_S = 176.4 kHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES			16		Bit
Total harmonic distortion	THD	f_{IN} = 1 kHz, 0 dB		0.04	0.09	%
Full-scale output voltage	V_{FS}			2.0	2.3	V_{p-p}
S/N ratio	S/N	With A-weight filter	93	100		dB
Dynamic range	D.R	f_{IN} = 1 kHz, –60 dB	89	96		dB
Crosstalk	C.T	One side channel = 0 dB, f_{IN} = 1 kHz	82	96		dB
Current dissipation	I_{DD}	f_{IN} = 1 kHz, 0 dB		5	12	mA

μPD6379L, 6379AL

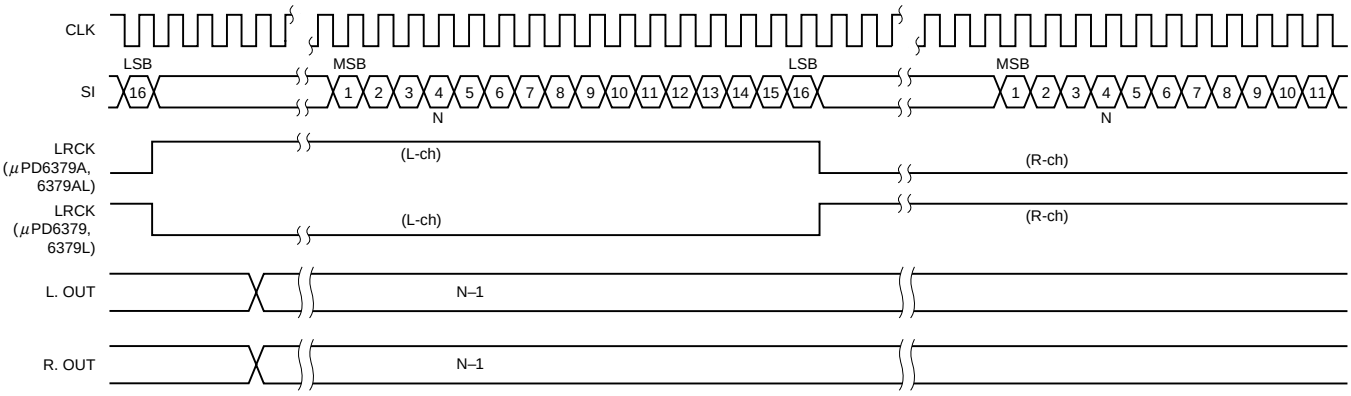
RECOMMENDED OPERATING CONDITIONS

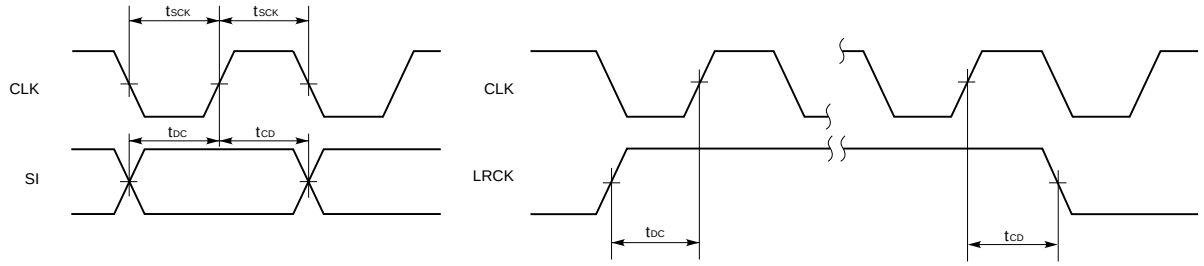
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.0	3.3	5.5	V
Logic input voltage (HIGH)	V_{IH}		0.7 V_{DD}		V_{DD}	V
Logic input voltage (LOW)	V_{IL}		0		0.3 V_{DD}	V
Operating ambient temperature	T_A		–20	+25	+75	°C
Output load resistance	R_L	R. OUT, L. OUT pins	10			kΩ
Conversion frequency	f_S				200	kHz
Clock frequency	f_{CLK}				10	MHz
Clock pulse width	t_{SCK}		40			ns
SI, LRCK setup time	t_{DC}		12			ns
SI, LRCK hold time	t_{CD}		12			ns

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V_{DD} = +3.3 V, f_S = 176.4 kHz)

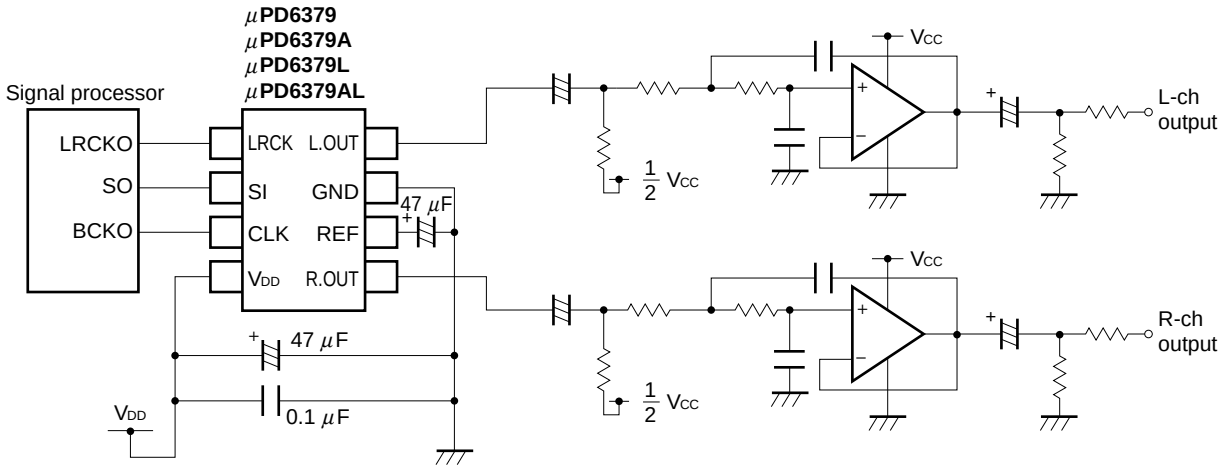
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	RES			16		Bit
Total harmonic distortion	THD	f_{IN} = 1 kHz, 0 dB		0.04	0.09	%
Full-scale output voltage	V_{FS}			1.32	1.52	V_{p-p}
S/N ratio	S/N	With A-weight filter	93	98		dB
Dynamic range	D.R	f_{IN} = 1 kHz, –60 dB	89	93		dB
Crosstalk	C.T	One side channel = 0 dB, f_{IN} = 1 kHz	82	93		dB
Current dissipation	I_{DD}	f_{IN} = 1 kHz, 0 dB		3	6	mA

Timing Chart





3. APPLICATION CIRCUIT EXAMPLE



4. NOTES ON USE

(1) Input signal format

- Input data must be input as 2's complement, MSB first, and backward justification.
  2's complement is a method of expressing both positive numbers and negative numbers as binary numbers. See the table below.

2's Complement (MSB)			(LSB)	Decimal Number	L.OUT, R.OUT Pin Voltage TYP. (V) (Reference Values)Note 1	
					V_{DD} = 5.0 V	V_{DD} = 3.3 VNote 2
0111	1111	1111	1111	+32767	3.0	1.98
0111	1111	1111	1110	+32766	⋮	⋮
⋮				⋮		
0000	0000	0000	0001	+1		
0000	0000	0000	0000	0	2.0	1.32
1111	1111	1111	1111	–1		
⋮				⋮	⋮	⋮
1000	0000	0000	0001	–32767		
1000	0000	0000	0000	–32768	1.0	0.66

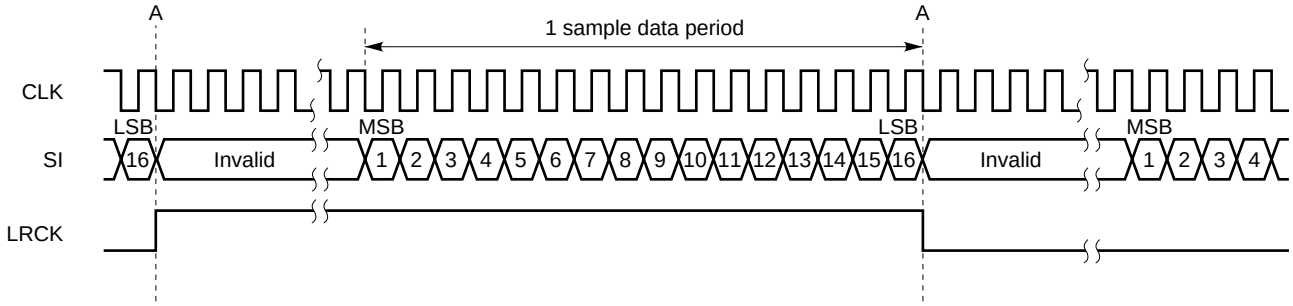
Notes 1. Values differ depending on IC fabrication variations, supply voltage fluctuations, and ambient temperature.

2. μPD6379L, 6379AL

- Make sure that the delimiter of each bit of the data (SI) and the changing timing of LRCK coincide with the falling edge of CLK.
- It is necessary that 16 clocks be input during 1 sample data period (16 bits). Make sure that the time width of 1 bit coincides with one cycle of the clock.
- ★ In the input data, the 16 bits preceding the change point of LRCK (shown in "1 sample data period" in Fig. 4-1, and Fig. 4-2) are considered to be valid data and are incorporated for use in D/A conversion.

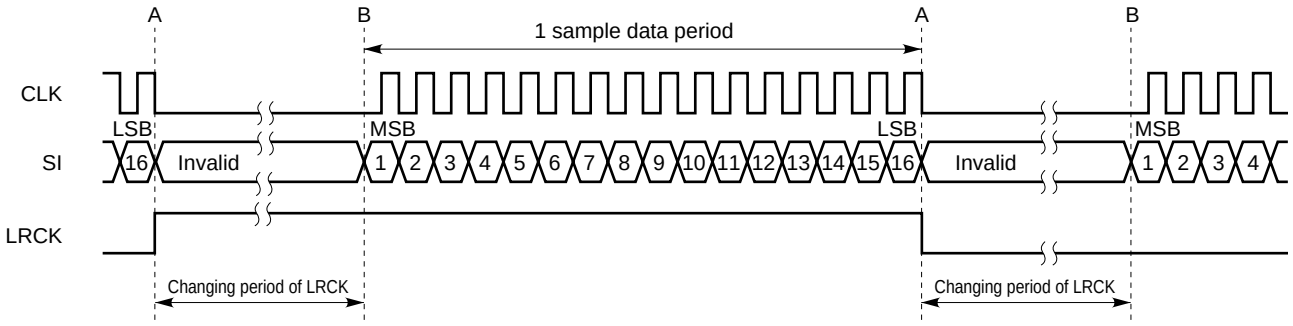
- If the clock is also supplied to CLK while data is not sampled (refer to Fig. 4-1), make sure that the changing timing of LRCK coincides with the falling edge (point A) of CLK after the LSB has been input.

Fig. 4-1 Input Timing Chart (1)



- If the clock is supplied to CLK only while data is sampled (refer to Fig. 4-2), set the changing timing of LRCK in between the falling edge (point A) of CLK after the LSB has been input and the start of inputting the next MSB (point B) (points A and B are included).

Fig. 4-2 Input Timing Chart (2)



★ **(2) Output signal updating timing**

The L.OUT and R.OUT signals are updated after the input of 3.5 clocks following the change point indicating the end of the LRCK pin R-ch data input period. Therefore, when the clock is supplied to CLK only during D/A conversion, the clock must be stopped after the L.OUT and R.OUT signals corresponding to the last input data are output. Be aware that the L.OUT and R.OUT signals corresponding to the last sample data are not output, especially when the clock is supplied to CLK only during a sample data period.

Fig. 4-3 Output Timing Chart (1) (for continuous clocks)

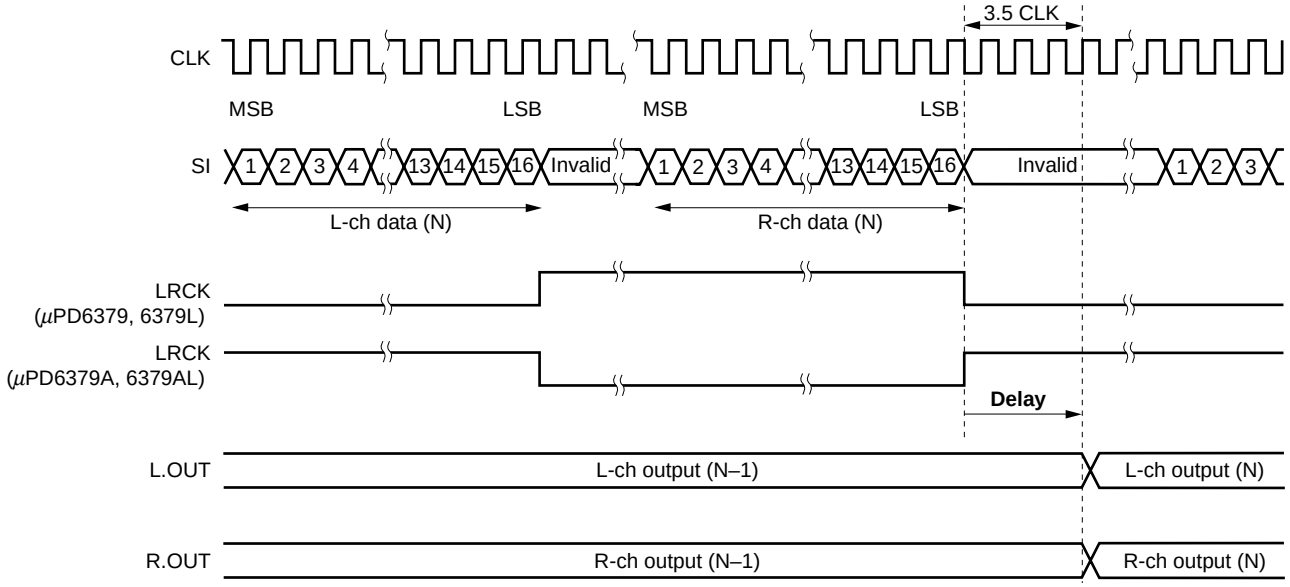
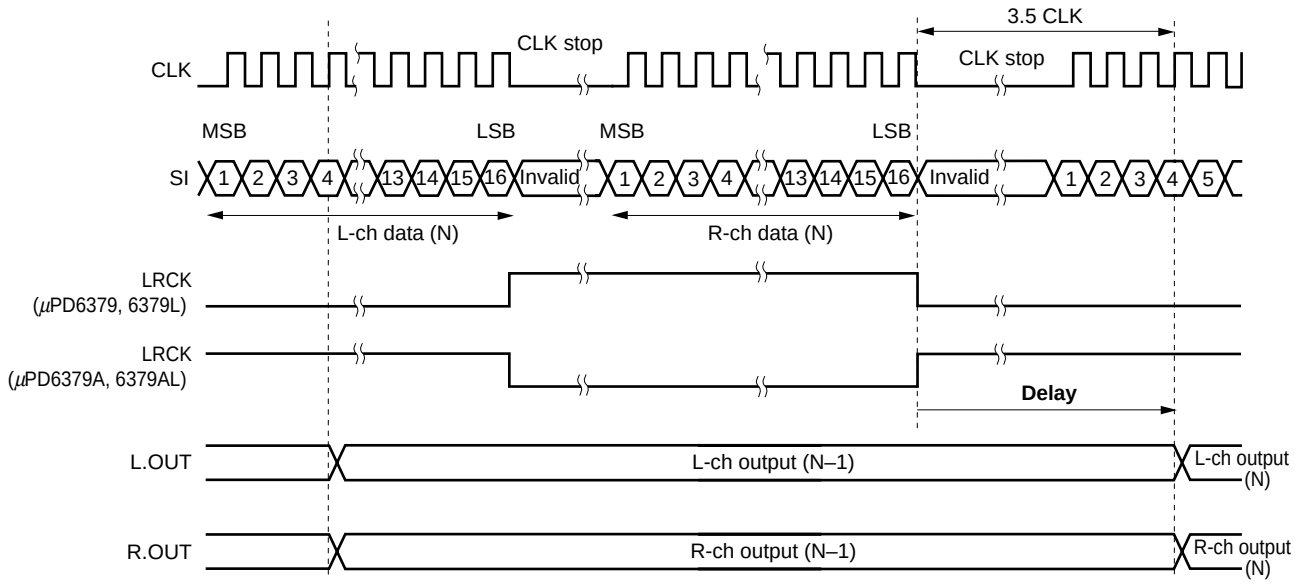


Fig. 4-4 Output Timing Chart (2) (when there is an interval which the clock is stopped)

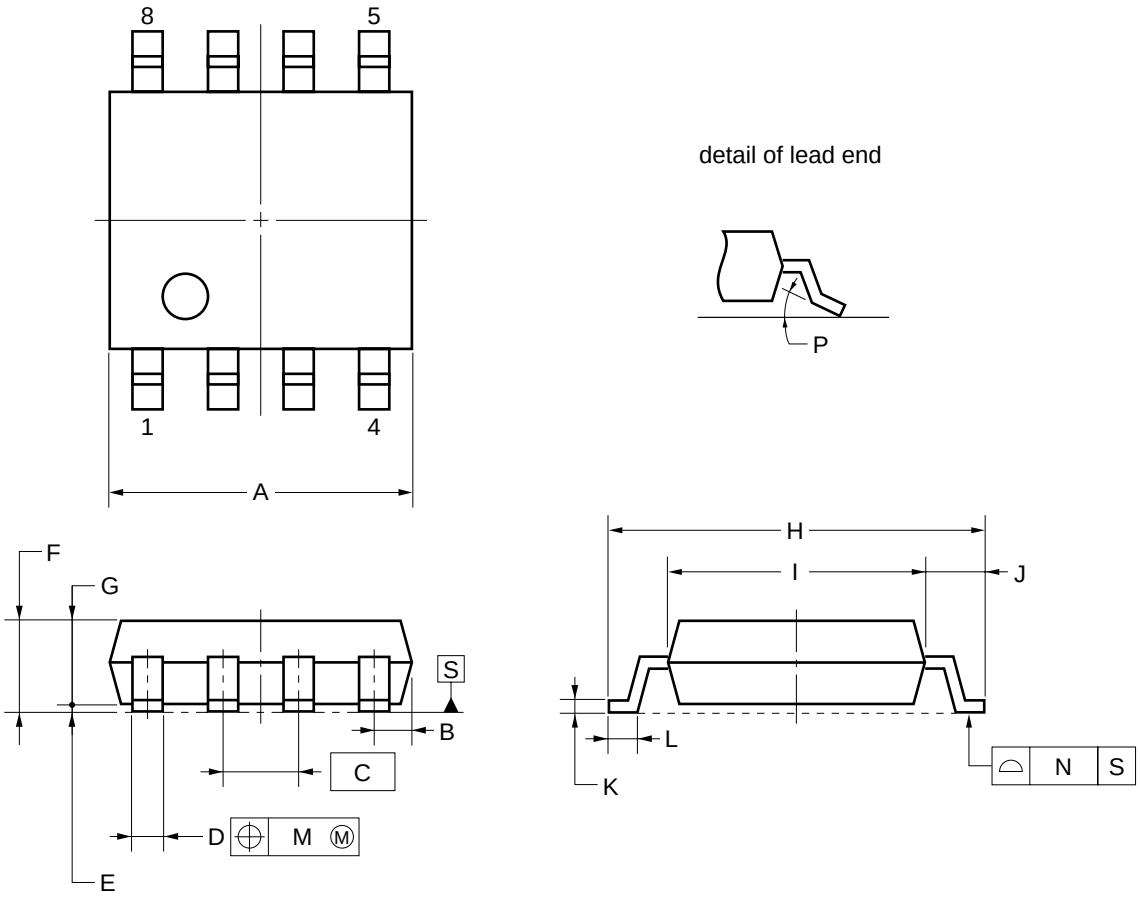


(3) Countermeasures against shock noise

It is recommended that a mute circuit be connected to the next stage of the D/A converter. If a mute circuit is not provided, shock noise may occur when power is applied.

5. PACKAGE DRAWING

8-PIN PLASTIC SOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$5.2^{+0.17}_{-0.20}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S8GM-50-225B-6

6. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the product.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

Table 6-1 Soldering Conditions

μPD6379GR, 6379AGR, 6379LGR, 6379ALGR : 8-pin plastic SOP (5.72 mm (225))

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak temperature of package surface: 235 °C or below, Reflow time: 30 seconds or less (at 210 °C or higher), Number of reflow processes: MAX. 2.	IR35-00-2
VPS	Peak temperature of package surface: 215 °C or below, Reflow time: 40 seconds or less (at 200 °C or higher), Number of reflow processes: MAX. 2.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Pre-heating temperature: 120 °C or below (Package surface), Number of flow processes: MAX. 1.	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Time: 3 seconds or less (Per one side of the device).	—

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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