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DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD6467

ON-SCREEN CHARACTER DISPLAY CMOS IC FOR 512-CHARACTER, 12-ROW, 28-COLUMN, CAMERA-CONTAINED VCR

The μPD6467 is a CMOS LSI for on-screen character display, and can be used in combination with a microcomputer to display the tape counter, time, and date in the view finder of a video camera, or the time of a video tape, messages such as dates on pictures, and channel number on a TV screen.

Characters are displayed in 12 (horizontal) by 18 (vertical) dots. Two or more characters can be combined to display Kanji (Japanese characters) and symbols. This LSI supports color view finders and is provided with three sets of character output signals (RGB output: for color view finder, V_{C1} output: for recording (or monitor pin), V_{C2} output: for monitor pin (or recording)).

In addition, the μPD6467 is also equipped with a power-ON clear function and a video RAM batch clear command so that it can mitigate the workload of the microcomputer.

The command format of this LSI is identical to that of the existing models, the μPD6461, 6462 and 6466, and therefore, the μPD6467 is compatible with the existing models, and the software resources for the existing models can be used.

FEATURES

- Number of display characters : 12 rows, 28 columns (336 characters)
- Types of character : 512 types (ROM). Changeable by using mask code option.
- Character size : Can be expanded up to four-fold in vertical and horizontal directions independently, in units of lines.
- Number of character colors : 8 colors
- Framing : Framing or no framing, or white or black framing selectable in screen units.
- Dot matrix : 12 (horizontal) × 18 (vertical) dot configuration. No gap between adjacent characters.
- Blinking : Blinking can be turned ON/OFF in character units. The blinking ratio is 1:1. The blinking frequency can be selected from about 1 Hz, about 2 Hz, and about 0.5 Hz in screen unit.
- Character color reversing function : The color of the character and that of the background can be reversed.
- Character left and right reverse : Left and right can be reversed for display in character units.
- Background : No background, blank background, or filled background selectable in screen units.
- Blue back function : Blue or white can be selected as the background.
- External dot clock input : Frequency 2-divide function is selectable.
- Signal output : 3 sets (output (1) R, G, B + BLK/V_{C1} + V_{BLK1}/V_{C2} + V_{BLK2} and output (2) R + R_{BLK}/B + B_{BLK}/G + G_{BLK} selectable by command)
  When output (1) is selected, V_{C1} and V_{C2} outputs can be selected from three types.
- Video RAM data clear : Implemented by video RAM batch clear command or by clear function on power-ON.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

• Interface with microcomputer	: 8-bit variable word length serial input (LSB first/MSB first selectable by command)
• Supply voltage	: Supports low voltage (2.0 to 3.6 V)
• Process	: CMOS low power consumption
• Small package size	: 20-pin plastic shrink SOP (225 mil)

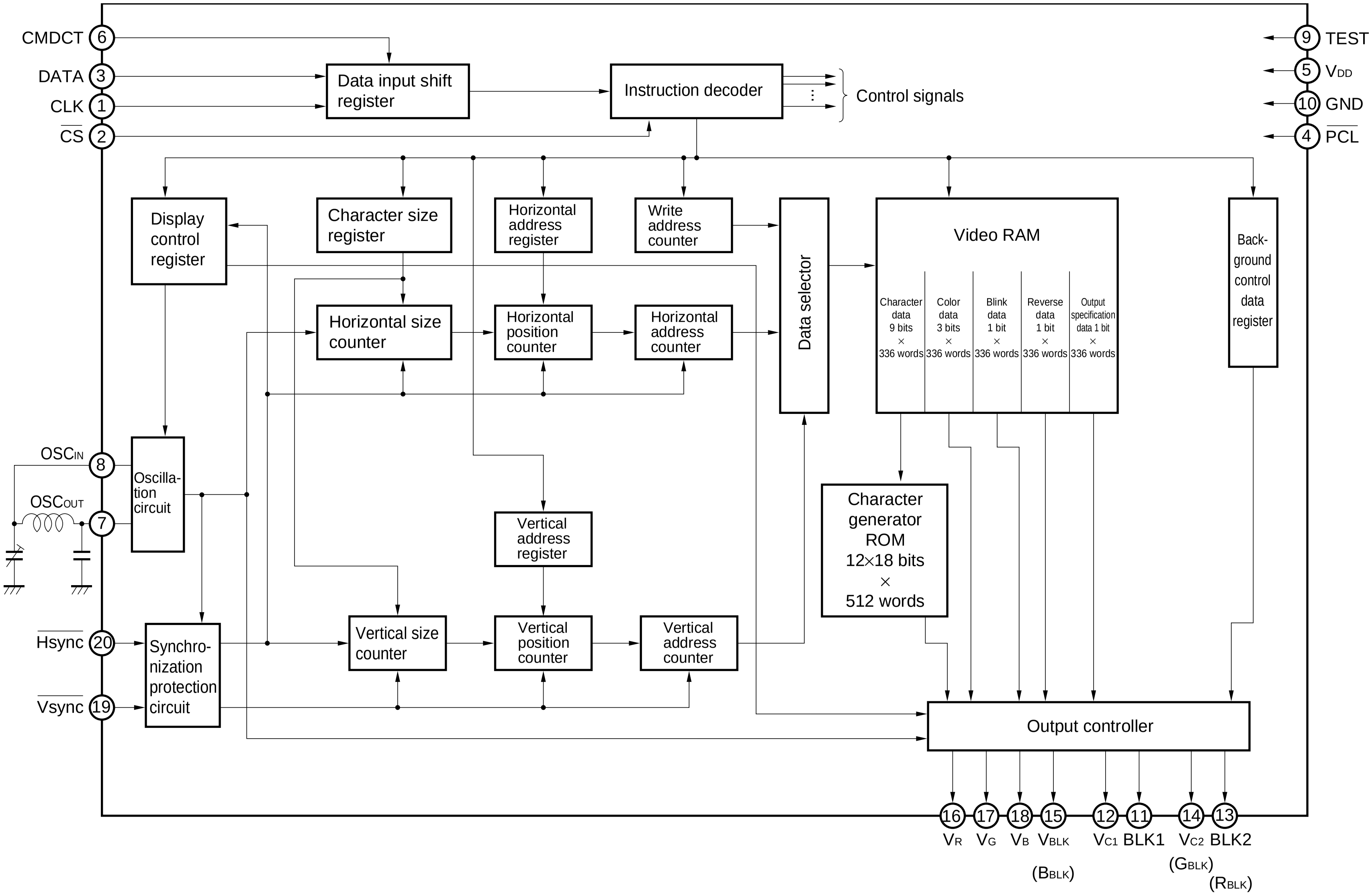
ORDERING INFORMATION

Part Number	Package
μPD6467GR-xxx	20-pin plastic shrink SOP (225 mil)

Remarks **1.** NEC’s standard model is the μPD6467GR-001.
For the details of the character generator ROM, refer to **5. CHARACTER PATTERNS**.

2. xxx indicates a ROM code suffix.

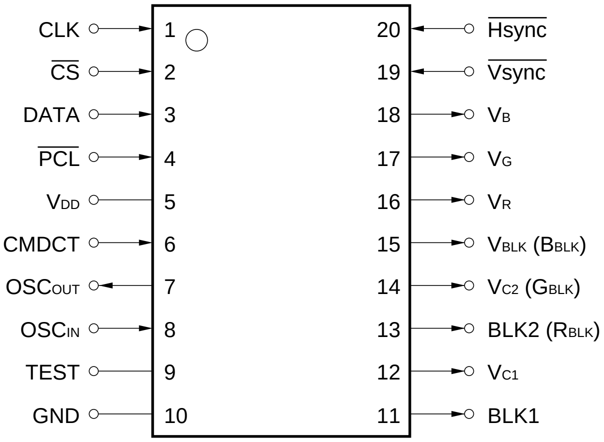
BLOCK DIAGRAM


CMDCT 6
DATA 3
CLK 1
CS 2
Data input shift register
Instruction decoder
Control signals
9 TEST
5 VDD
10 GND
4 PCL
Display control register
Character size register
Horizontal address register
Write address counter
Data selector
Video RAM
Character data 9 bits × 336 words
Color data 3 bits × 336 words
Blink data 1 bit × 336 words
Reverse data 1 bit × 336 words
Output specification data 1 bit × 336 words
Back-ground control data register
Horizontal size counter
Horizontal position counter
Horizontal address counter
OSCIN 8
OSCOUT 7
Oscilla-tion circuit
Vertical address register
Character generator ROM 12×18 bits × 512 words
Hsync 20
Vsync 19
Synchro-nization protection circuit
Vertical size counter
Vertical position counter
Vertical address counter
Output controller
16 VR
17 VG
18 VB
15 VBLK (BBLK)
12 VC1
11 BLK1
14 VC2 (GBLK)
13 BLK2 (RBLK)

Remark Signals in ( ) are set by using an initial status setting command (RGB + RGB compatible blanking).

PIN CONFIGURATION (Top View)

20-pin plastic shrink SOP (225 mil)
μPD6467GR-xxx


CLK
1
CS
2
DATA
3
PCL
4
VDD
5
CMDCT
6
OSCOUT
7
OSCIN
8
TEST
9
GND
10
20
Hsync
19
Vsync
18
VB
17
VG
16
VR
15
VBLK (BBLK)
14
VC2 (GBLK)
13
BLK2 (RBLK)
12
VC1
11
BLK1

Remarks **1.** xxx indicates a ROM code suffix.

2. Signals in ( ) are set by using an initial status setting command (RGB + RGB compatible blanking).

B_{BLK} : Blanking B
BLK1, BLK2 : Blanking Output 1, 2
CLK : Clock
CMDCT : Command Control
$\overline{\text{CS}}$: Chip Select
DATA : Data Input
G_{BLK} : Blanking G
GND : Ground
$\overline{\text{Hsync}}$: Horizontal Synchronous Signal Input
OSC_{IN} : Oscillator Input
OSC_{OUT} : Oscillator Output
$\overline{\text{PCL}}$: Power-ON Clear
R_{BLK} : Blanking R
TEST : Test
V_B : Character Signal Output
V_{BLK} : Blanking Signal Output for V_R, V_G, V_B
V_{C1}, V_{C2} : Character Signal Output 1, 2
V_{DD} : Power Supply
V_G : Character Signal Output
V_R : Character Signal Output
$\overline{\text{Vsync}}$: Vertical Synchronous Signal Input

PIN FUNCTIONS

Pin No.	Pin Symbol[Note]	Pin Name[Note]	Function
1	CLK	Clock input	This pin inputs a clock for reading data. Data input to the DATA pin is read at the rising edge of this clock.
2	$\overline{\text{CS}}$	Chip select input	Serial transfer can be accepted if this pin is made low.
3	DATA	Serial data input	This pin inputs control data. Data is read in synchronization with the clock input to the CLK pin.
4	$\overline{\text{PCL}}$	Power-ON clear	This pin, when high, initializes the internal circuitry of the IC on power application.
5	V_{DD}	Power supply	This pin supplies power.
6	CMDCT	Command specification select	This pin selects whether a command is input with the LSB first or MSB first. When this pin is low, the command is input with the LSB first; when it is high, the command is input with the MSB first. To input the command with the LSB first, this pin may be opened.
7 8	OSC_{OUT} OSC_{IN}	LC oscillation I/O (OSC_{IN}: external clock input)	These are an input and an output pin for an oscillation circuit that generates a dot clock. A coil and capacitor for oscillation are connected to these pins. (If the input of an external clock is selected by the initial status setting command, an external clock (clock synchronized with $\overline{\text{Hsync}}$) is input. OSC_{OUT} is opened at this time.)
9	TEST	Test pin	This pin is used to test the IC. Normally, connect this pin to GND. When the TEST pin is connected to GND, the test mode is not set.
10	GND	Ground pin	Connect this pin to GND of the system.
11	BLK1	Blanking signal output 1	This pin outputs a blanking signal to cut the video signal. It supports output of V_{C1}, and is high-active. (If RGB compatible blanking is selected by a command, this pin outputs the logical sum of R_{BLK}, G_{BLK}, and B_{BLK}.)
12	V_{C1}	Character signal output 1	This pin outputs a character signal, and is high-active. (If RGB compatible blanking is selected by a command, this pin outputs the logical sum of V_R, V_G, and V_B.)
13	BLK2 (R_{BLK})	Blanking signal output 2 (blanking R)	This pin outputs a blanking signal to cut the video signal. It supports output of V_{C2}, and is high-active. (This pin outputs a blanking signal supporting output of V_R and is high-active.)
14	V_{C2} (G_{BLK})	Character signal output 2 (blanking G)	This pin outputs a character signal, and is high-active. (This pin outputs a blanking signal supporting output of V_G and is high-active.)
15	V_{BLK} (B_{BLK})	Blanking signal output (blanking B)	This pin outputs a blanking signal to cut the video signal. It supports output of V_R, V_G, and V_B, and is high-active (this pin outputs a blanking signal supporting output of V_B and is high-active).
16 17 18	V_R V_G V_B	Character signal output	This pin outputs a character signal, and is high-active.
19	$\overline{\text{Vsync}}$	Vertical sync signal input	This pin inputs a vertical sync signal. Input a negative sync signal.
20	$\overline{\text{Hsync}}$	Horizontal sync signal input	This pin inputs a horizontal sync signal. Input a negative sync signal.

Note Signals in ( ) are set by the initial status setting command (RGB + RGB compatible blanking).

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1. INITIAL STATUS SETTING

1.1 Initial Status Setting

The μPD6467 selects the following parameters by using an initial status setting command.

<table>
<tr><th></th><th>Parameter</th><th colspan="4">Selected by:</th></tr>
<tr><td>(1)</td><td>Dot clock</td><td colspan="2">LC oscillation</td><td colspan="2">External clock input</td></tr>
<tr><td>(2)</td><td>Vertical display start position</td><td colspan="2">3-row unit setting</td><td colspan="2">9-row unit setting</td></tr>
<tr><td>(3)</td><td>Pin selection</td><td colspan="2">RGB + V_{C1} + V_{C2}</td><td colspan="2">RGB + RGB compatible BLK
(RGB + 3BLK)</td></tr>
<tr><td>(4)</td><td>Output selection</td><td>Option A</td><td colspan="2">Option B</td><td>Option C</td></tr>
<tr><td>(5)</td><td>Character color reversal specification selection</td><td colspan="2">Black character</td><td colspan="2">White character</td></tr>
<tr><td>(6)</td><td>Function selection</td><td colspan="2">Character blinking</td><td colspan="2">Character left/right reversal</td></tr>
<tr><td>(7)</td><td>External clock frequency selection</td><td colspan="2">×1 frequency mode</td><td colspan="2">×2 frequency mode</td></tr>
</table>

(1) Dot clock

To select a dot clock for character display. If an external clock input is selected, refer to **External Clock Input** in **6. ELECTRICAL CHARACTERISTICS**.

(2) Vertical display start position

To select the setting accuracy of the vertical display start position of the character display area. In 3-row units, the vertical display start position can be set more finely than in 9-row units.

(3) Pin selection

To select the setting of the output pins.

When RGB + V_{C1} + V_{C2} is selected, character signals are output from pins V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, and BLK2. When RGB + 3BLK is selected, character signals are output from pins V_R, V_G, V_B, R_{BLK}, G_{BLK}, B_{BLK}, V_{C1}, and BLK1.

When RGB + V_{C1} + V_{C2} is selected with a video camera with a color view finder, colored characters can be displayed in the view finder. When RGB + 3BLK is selected, character signals can be separated color specification.

(4) Output selection

To set the output format of the character signal where the setting of the output pin is RGB + V_{C1} + V_{C2} (setting the output format of the character signal is invalid where the setting of the output pin is RGB + 3BLK).

When an on-screen character display IC is used in a video camera, some items of information (such as date and title) are displayed on the video tape, and the others (such as battery alarm, focus, and counter indication) are only displayed in the view finder. The μPD6467 can select these items of information in row or half-row units by using the output pin. Select the output format from three types: option A, option B, and option C (when 3BLK is selected, however, be sure to select option B).

(5) Character color reversal specification selection

To select the specifications when the character color is reversed (valid only for RGB output).

- Black character: Outputs an area with dots in black and prohibits framing.
- White character: Outputs an area with dots in white and prohibits framing.

(6) Function selection

To select either of the character blinking or character left/right reversal functions.

(7) External clock frequency selelction

The external clock frequency 2 divided function is built in the μPD6467.

- ×1 frequency mode: External clock frequency is not divided by 2 in the μPD6467.
- ×2 frequency mode: External clock frequency is divided by 2 in the μPD6467.

When the dot clock control bit (OSC) is “1 (External clock input)”, this function is able to use.

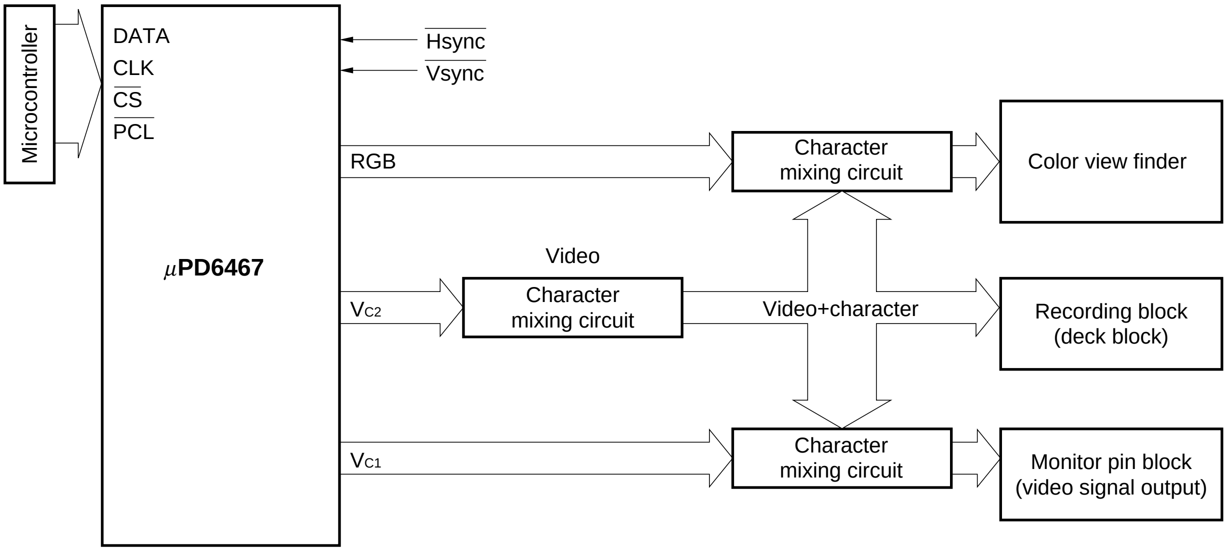
Example If ×2 frequency mode is selected, and the external input frequency is 14 MHz, the internal dot clock frequency is become to 7 MHz.

The default setting assumed on power application is as follows:

(1) Dot clock = LC oscillation
(2) Vertical display start position = 3-row unit
(3) Pin selection = RGB + V_{C1} + V_{C2}
(4) Output selection = Option B
(5) Character color reversal specification selection = Black characters
(6) Function selection = Character blinking
(7) External clock frequency selection = ×1 frequency mode

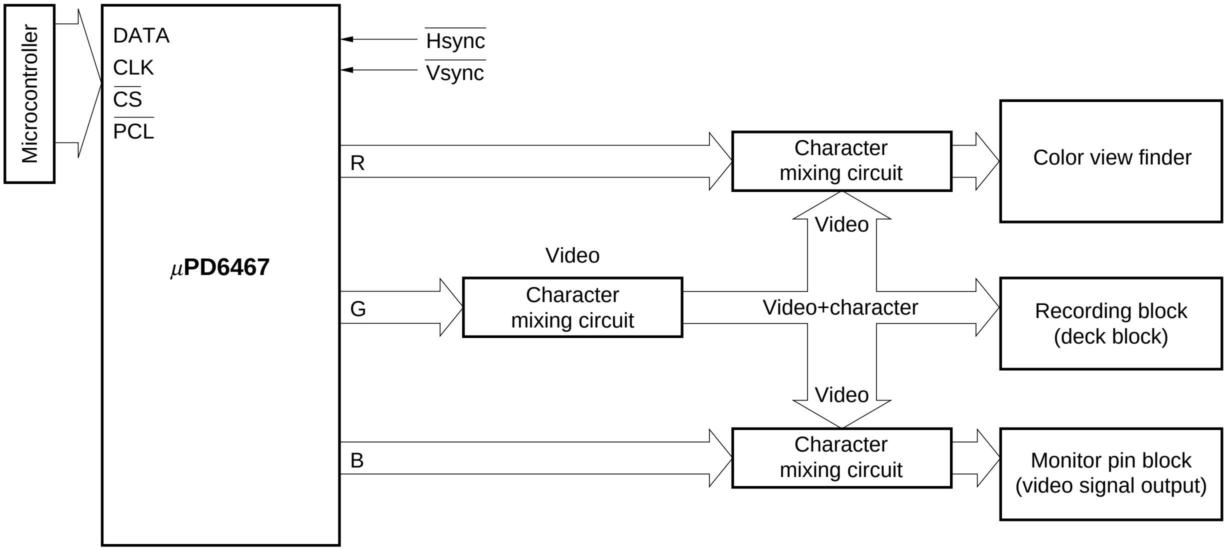
1.2 Application Block Diagram

Example of application in a video camera (1) (in the case of RGB + V_{C1} + V_{C2})
(When V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, and BLK2 pins are used)


Microcontroller
DATA
CLK
CS
PCL
Hsync
Vsync
μPD6467
RGB
VC2
VC1
Video
Character mixing circuit
Character mixing circuit
Character mixing circuit
Video+character
Color view finder
Recording block (deck block)
Monitor pin block (video signal output)

RGB : V_R, V_G, V_B, V_{BLK} V_{C1} : V_{C1}, BLK1 V_{C2} : V_{C2}, BLK2

Example of application in a video camera (2) (RGB + 3BLK (RGB compatible BLK))
(When V_R, V_G, V_B, R_{BLK}, G_{BLK}, and B_{BLK} pins are used)


Microcontroller
DATA
CLK
CS
PCL
Hsync
Vsync
μPD6467
R
G
B
Video
Video
Video
Character mixing circuit
Character mixing circuit
Character mixing circuit
Video+character
Color view finder
Recording block (deck block)
Monitor pin block (video signal output)

R : V_R, R_{BLK} G : V_G, G_{BLK} B : V_B, B_{BLK}

1.3 Display with RGB + V_{C1} + V_{C2} Pins

The μPD6467 has three output options: A, B, and C. The following figure shows the output with each option specified (the output is controlled by an output pin control command (refer to **3.11 Output Pin Control Command**)).

Output pin control command (with MSB first (The command is input from the MSB (D15).)

(because this command is a 2-byte command, input of 16 bits is necessary when this command is input more than once successively.)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	0	0	OD1	OD0	0	0	AR3	AR2	AR1	AR0

Row specification bits				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Specifies row 0.
0	0	0	1	Specifies row 1.
≈	≈	≈	≈	≈
1	0	1	1	Specifies row 11.
Setting prohibited				

Option A

Output pin control bits		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs specified row, V_{C2}: Fixed to low level
0	1	V_{C1}: Fixed to low level, V_{C2}: Outputs specified row

Option B

Output pin control bits		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs all rows, V_{C2}: Fixed to low level
0	1	V_{C1}: Outputs all rows, V_{C2}: Outputs specified row

Option C

Output pin control bits		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs columns 0-27, V_{C2}: Fixed to low level
0	1	V_{C1}: Outputs columns 0-11, V_{C2}: Outputs columns 12-27
1	0	V_{C1}: Outputs columns 12-27, V_{C2}: Outputs columns 0-11
1	1	V_{C1}: Fixed to low level, V_{C2}: Outputs columns 0-27

- **Row specification control**
  Specify whether the character signal is output to the V_{C1} or V_{C2} pin in row units (or 12-column, 16-column units).

- **Output pin control**
  The output of the V_{C1} and V_{C2} pins can be selected from three types, A, B, and C, by using the initial status setting command (the blanking signal is output in the same manner).

Output with option A

Output pin control bit			
OD1	OD0	Pin output	
0	0	V_{C1}: Outputs specified row, V_{C2}: Fixed to low level	(1)
0	1	V_{C1}: Fixed to low level, V_{C2}: Outputs specified row	(2)

	Output	Character signal	Background signal (with background specified)
In the case of (1)	V_{C1} output	Outputs character signal resulting from ORing V_R, V_G, and V_B pins (specified row). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Fixed to low level (specified row)	Outputs background signal to only area specified by V_{C2}
In the case of (2)	V_{C1} output	Fixed to low level (specified row)	Outputs background signal to area other than that specified by V_{C2}
	V_{C2} output	Outputs character specified by V_{C2} (specified row)	Outputs background signal to only area specified by V_{C2}

Output with option B

Output pin control bit			
OD1	OD0	Pin output	
0	0	V_{C1}: Outputs all rows, V_{C2}: Fixed to low level	(1)
0	1	V_{C1}: Outputs all rows, V_{C2}: Outputs specified row	(2)

	Output	Character signal	Background signal (with background specified)
In the case of (1)	V_{C1} output	Outputs character signal resulting from ORing V_R, V_G, and V_B pins (all rows). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Fixed to low level (specified row)	Outputs background signal to only area specified by V_{C2}.
In the case of (2)	V_{C1} output	Outputs character signal resulting from ORing V_R, V_G, and V_B pins (all rows). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Outputs character specified by V_{C2} (specified row).	Outputs background signal to only area specified by V_{C2}.

Output with option C

Output pin control bit			
OD1	OD0	Pin output	
0	0	V_{C1}: Outputs columns 0-27, V_{C2}: Fixed to low level	(1)
0	1	V_{C1}: Outputs columns 0-11, V_{C2}: Outputs columns 12-27	(2)
1	0	V_{C1}: Outputs columns 12-27, V_{C2}: Outputs columns 0-11	(3)
1	1	V_{C1}: Fixed to low level, V_{C2}: Outputs columns 0-27	(4)

	Output	Character signal	Background signal (with background specified)
In the case of (1)	V_{C1} output	Outputs character signal resulting from ORing V_R, V_G, and V_B pins (columns 0-27 of specified row). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Fixed to low level (specified row)	Outputs background signal to only area specified by V_{C2}.
In the case of (2)	V_{C1} output	Outputs character signals resulting from ORing V_R, V_G, and V_B pins (columns 0-11 of specified row). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Outputs character specified by V_{C2} (columns 12-27 of specified row).	Outputs background signal to only area specified by V_{C2}.
In the case of (3)	V_{C1} output	Outputs character signal resulting from ORing V_R, V_G, and V_B pins (columns 12-27 of specified row). However, character specified by V_{C2} is not output.	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Outputs character specified by V_{C2} (columns 0-11 of specified row).	Outputs background signal to only area specified by V_{C2}.
In the case of (4)	V_{C1} output	Fixed to low level (specified row)	Outputs background signal to area other than that specified by V_{C2}.
	V_{C2} output	Outputs character specified by V_{C2} (columns 0-27 of specified row).	Outputs background signal to only area specified by V_{C2}.

The signal of the character specified by V_{C2} is not output from the RGB or V_{C1} output channel, but the background is output as described above.

When the μPD6467 is set to output RGB, V_{C1}, or V_{C2} signal, the following setting can be performed as well as the above output control.

- Independent ON/OFF control of character display of each channel (3-channel independent display ON/OFF command)
- Independent background control of each channel (3-channel background control command)

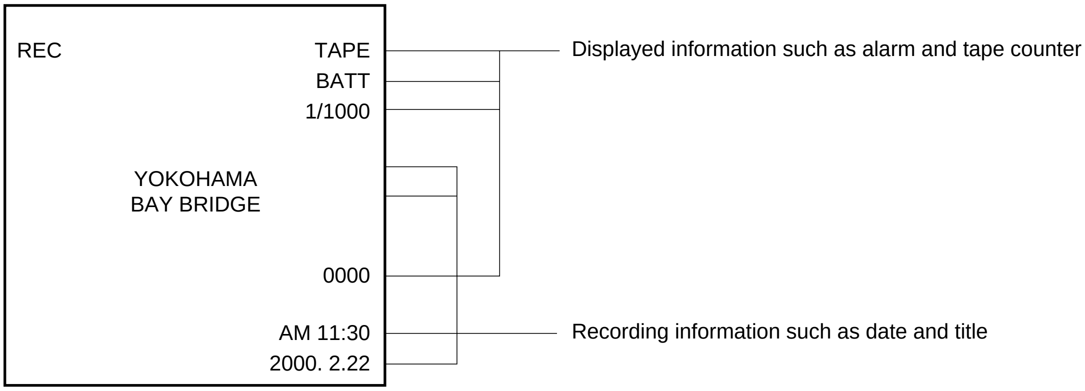
1.3.1 Character signal output with output select option A

Option A

Whether a signal is output to the character signal output pin V_{C1} in row units can be specified by the OD0 bit that selects an output pin. The V_{C2} output can be specified in character units, and the V_{C1} outputs only characters for which the V_{C2} in the rows for which the OD0 bit is set to 1. The character specified by V_{C2} is not output to the RGB and V_{C1} output.

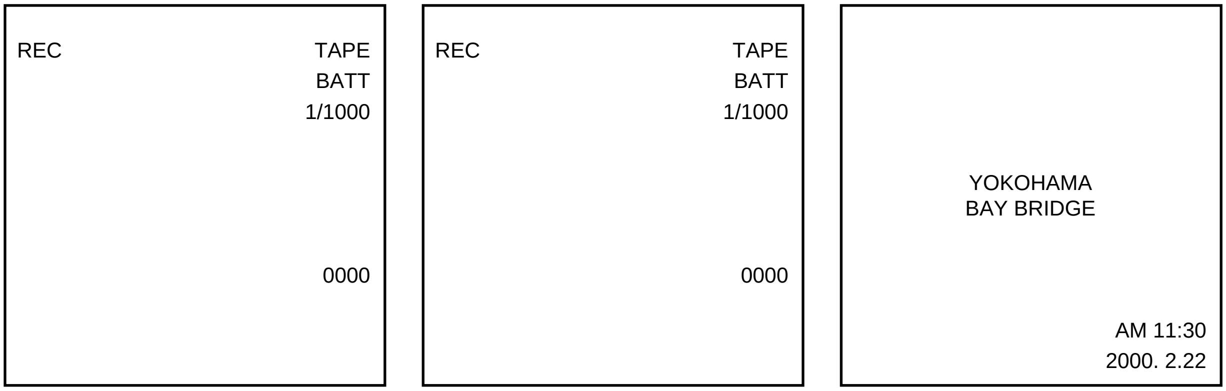
Display example (to use V_{C2} channel for information for recording)

Example of view finder display
(RGB and V_{C2} output)



REC
TAPE
BATT
1/1000
YOKOHAMA
BAY BRIDGE
0000
AM 11:30
2000. 2.22
Displayed information such as alarm and tape counter
Recording information such as date and title

Output example



REC
TAPE
BATT
1/1000
0000
REC
TAPE
BATT
1/1000
0000
YOKOHAMA
BAY BRIDGE
AM 11:30
2000. 2.22

RGB character output
(color character)

- The character specified to V_{C2} is not output.

Character output of V_{C1} channel
(specified row)

- Character information on the row specified by clearing the OD0 bit to 0 is output from V_{C1}. However, the characterspecified by V_{C2} is not output.
- The row specified by setting the OD0 bit to 1 is not output (fixed to low level).

Character output of V_{C2} channel
(specified row, character specified by V_{C2})

- The row specified by clearing the OD0 bit to 0 is not output (fixed to low level).
- Only the character information specified by V_{C2} on the row specified by setting the OD0 bit to 1 is output from V_{C2}.

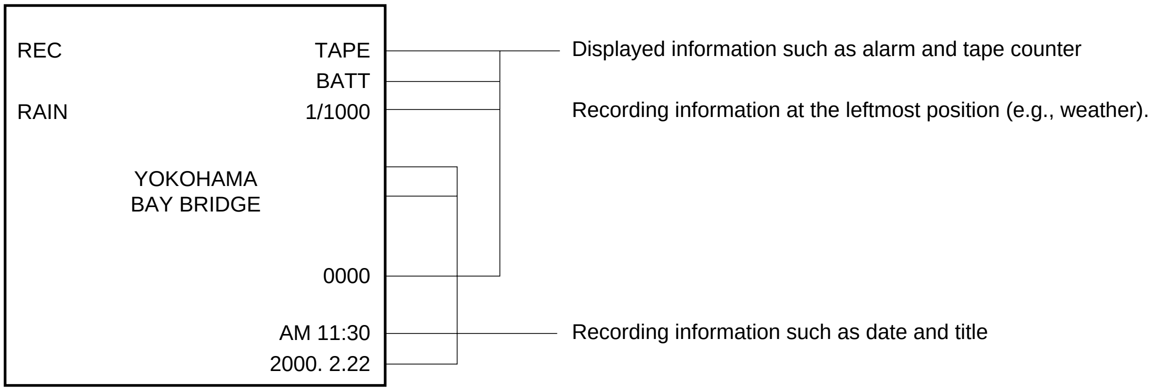
1.3.2 Character signal output with output select option B

Option B

The V_{C1} outputs characters of all rows regardless of setting of the OD0 and OD1 bits. The V_{C2} output can be specified in character units, and the V_{C2} outputs only characters for which the V_{C2} in the rows for which the OD0 bit is set to 1. The character specified to V_{C2} is not output to the RGB and V_{C1} output.

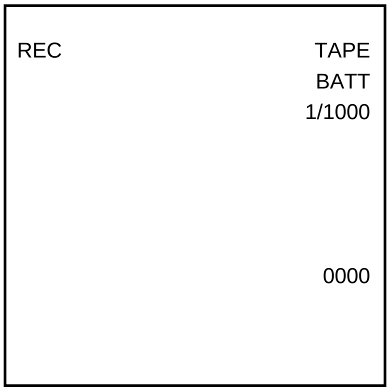
Display example (to use V_{C2} channel for information for recording)

Example of view finder display
(RGB and V_{C2} output)


REC
TAPE
BATT
RAIN
1/1000
YOKOHAMA
BAY BRIDGE
0000
AM 11:30
2000. 2.22
Displayed information such as alarm and tape counter
Recording information at the leftmost position (e.g., weather).
Recording information such as date and title

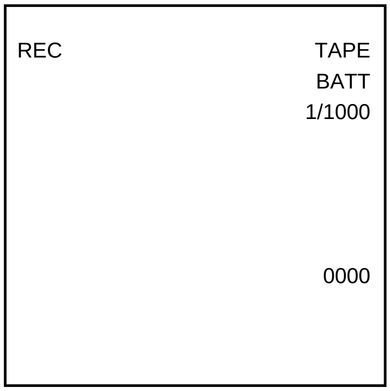
Output example

RGB character output
(color character)


REC
TAPE
BATT
1/1000
0000

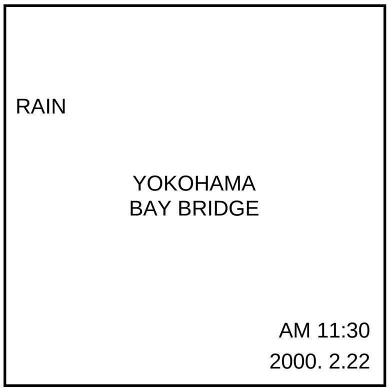
- The character specified to V_{C2} is not output.

Character output of V_{C1} channel
(all rows)


REC
TAPE
BATT
1/1000
0000

- The character information on all the rows is output from V_{C1} regardless of the OD0 bit. However, the character specified to V_{C2} is not output.

Character output of V_{C2} channel
(specified row, character specified to V_{C2})


RAIN
YOKOHAMA
BAY BRIDGE
AM 11:30
2000. 2.22

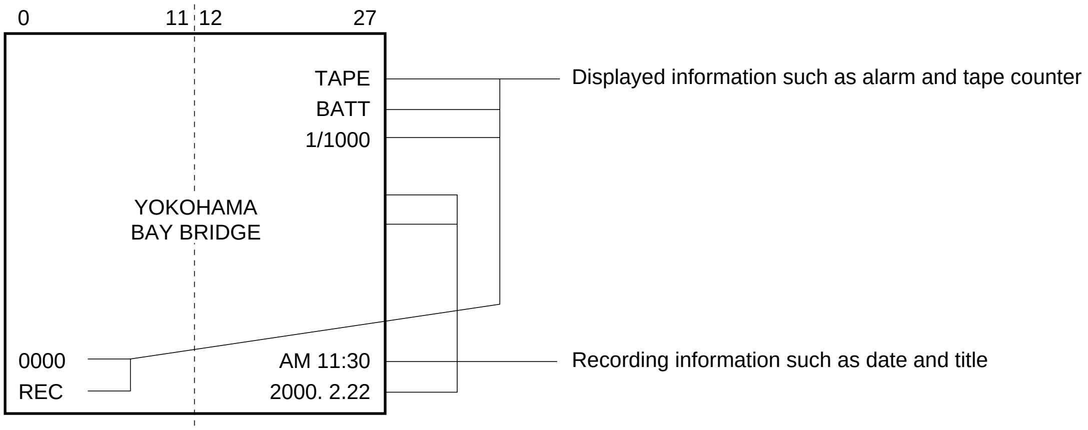
- Only the character information specified to V_{C2} on the row specified by setting the OD0 bit to 1 is output from V_{C2}.
- The character information specified to V_{C2} is not output on the row specified by clearing the OD0 bit to 0 is not output.

1.3.3 Character signal output with output select option C

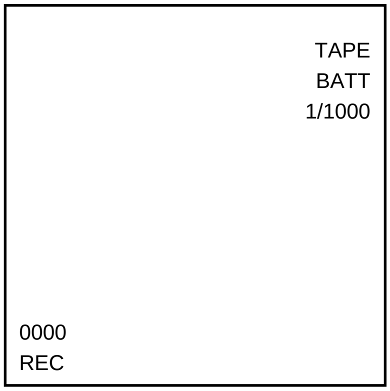
Option C

Columns 0 through 11, and 12 through 27 on each row can be output to the V_{C1} and V_{C2} pins by using the OD0 and OD1 bits of the “output pin control command”.

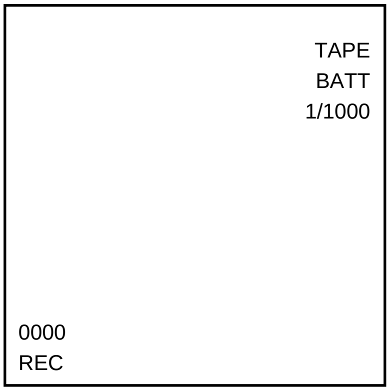
Display example


Example of view finder display
0
11
12
27
TAPE
BATT
1/1000
YOKOHAMA
BAY BRIDGE
0000
REC
AM 11:30
2000. 2.22
Displayed information such as alarm and tape counter
Recording information such as date and title

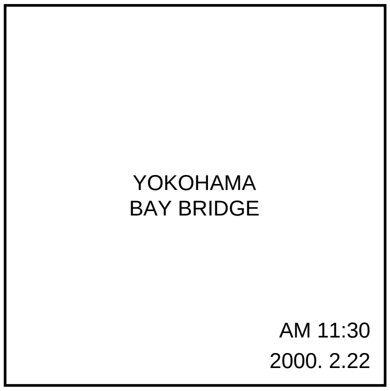
Output example


RGB character output
(color character)
TAPE
BATT
1/1000
0000
REC

- The character specified to V_{C2} is not output.


Character output of V_{C1} channel
(specified row)
TAPE
BATT
1/1000
0000
REC

- In the case of setting OD1 bit to 0, the V_{C1} outputs the characters of columns 0 to 27 in specified rows for which the OD0 bit is set to 0, or the characters of columns 0 to 11 in specified rows for which the OD0 bit is set to 1, excluding the characters for which the V_{C2} specified.
- In the case of setting OD1 bit to 1, the V_{C1} outputs the characters of columns 12 to 27 in specified rows for which the OD0 bit is set to 0, and the rows for which the OD0 bit is set to 1 are not output (the V_{C1} pin is fixed to low level), excluding the characters for which the V_{C2} specified.

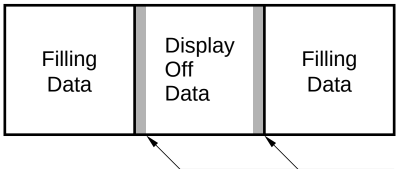

Character output of V_{C2} channel
(character specified by V_{C2})
YOKOHAMA
BAY BRIDGE
AM 11:30
2000. 2.22

- In the case of setting OD0 bit to 0, the V_{C2} outputs the characters of columns 0 to 11 in specified rows for which the OD1 bit is set to 1, and the rows for which the OD1 bit is set to 0 are not output (the V_{C2} pin is fixed to low level).
- In the case of setting OD0 bit to 1, the V_{C2} outputs the characters of columns 12 to 27 in specified rows for which the OD1 bit is set to 0, or the characters of columns 0 to 27 in specified rows for which the OD1 bit is set to 1.

1.3.4 Displaying characters specified by V_{C2}

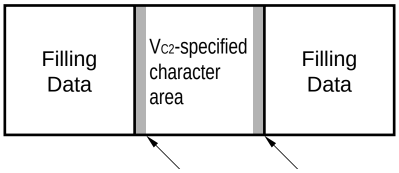
The characters specified by V_{C2} by the display character control command are not output to the RGB and V_{C1} output channels (the RGB and V_{C1} output channels display**Note** the same manner as when Display Off Data is written). Therefore, even if a background is specified by the RGB and V_{C1} output channel (no background/filled background), no background is displayed at the specified portion.

Note The display is slightly different from Display Off Data.

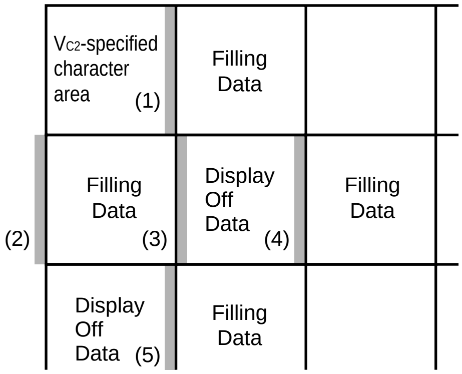


Filling data: Character filling all 12 × 18 dots

- **When Display Off Data is displayed with RGB, V_{C1}, and V_{C2} channel**
  In the case of Display Off Data, framing (or background, if any) of adjacent characters is displayed with the framing or background overlapping the area of Display Off Data by one dot of the minimum size (the framing overlaps the area of Display Off Data, when there are dots at the leftmost or rightmost position of the adjacent character area).



- **Displaying character area specified by V_{C2} with RGB and V_{C1} channels**
  In the case of a character specified by V_{C2}, the framing of the adjacent characters is displayed with the framing overlapping the V_{C2}-specified character area by one dot of the minimum size, but the background does not overlap to the V_{C2}-specified area.
- **Displaying V_{C2}-specified character area with V_{C2} channel**
  Even if the V_{C2}-specified character exists with the V_{C2} output, the framing also overlaps the adjacent character area, but the background does not (the framing overlaps the V_{C2}-specified character area, when there are dots at the leftmost or rightmost position of the adjacent character area).



- **If V_{C2} character specification area exists at the edge of display area**
  (The figure shows the leftmost position of the display area. The same applies to the rightmost position of the display area.)

  ▮ Portion output with framing or background overlapping
  (Width is 1 dot of the minimum character width.)

Portion where framing overlaps	Portion where background overlaps
(1)-(5)	(2)-(5)

The background is not output overlapping the V_{C2}-specified character area.

2. COMMAND

2.1 Command Format

Control commands can be serially input in 8-bit units. The word length of a command is variable.

Three types of commands are available: 1-byte commands that consist of 8 bits including the instruction and data, 2-byte commands, and 2-byte successive commands that can be input in an abbreviated form.

Inputting command data with the MSB first or LSB first can be selected by using the CMDCT pin.

When the CMDCT pin is high, the data is input with the MSB first; when it is low, the data is input with the LSB first.

2.2 Command List

(1) MSB first

1-byte commands (MSB)

Function	D7	D6	D5	D4	D3	D2	D1	D0
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	0	0	0	1	DO	LC	BL1	BL0
Background color/frame color control	0	0	1	0	R	G	B	BFC
3-channel independent display ON/OFF	0	1	1	1	0	DOA	DOB	DOC
Character color reverse ON/OFF	0	1	1	1	1	0	0	BCRE
Blue back ON/OFF	0	1	1	1	1	CLR	0	BB
Character address bank select	0	1	1	1	1	1	1	BC
Output switch control	0	1	0	S3A	S3B	SW4	SW2	SW1

2-byte commands (MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Character display position control	1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0
Write address control	1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0
Output pin control	1	0	0	1	1	1	0	0	OD1	OD0	0	0	AR3	AR2	AR1	AR0
Character size control	1	0	0	1	1	0	SV1	SV0	SH1	SH0	0	0	AR3	AR2	AR1	AR0
3-channel background control	1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC
Initial status setting	1	0	1	1	0	1	ECK	0	0	BR	RS	OP1	OP0	COC	VST	OSC
Test mode[Note]	1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

Note Must not be used.

2-byte successive command (MSB)

Function	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Display character control	1	1	RV	R	G	B	BL	V_{C2}	C7	C6	C5	C4	C3	C2	C1	C0

(2) LSB first

1-byte commands (LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7
Video RAM batch clear	0	0	0	0	0	0	0	0
Display control	BL0	BL1	LC	DO	1	0	0	0
Background color/frame color control	BFC	B	G	R	0	1	0	0
3-channel independent display ON/OFF	DOC	DOB	DOA	0	1	1	1	0
Character color reverse ON/OFF	BCRE	0	0	1	1	1	0	0
Blue back ON/OFF	BB	0	CLR	1	1	1	1	0
Character address bank select	BC	1	1	1	1	1	1	0
Output switch control	SW1	SW2	SW4	S3B	S3A	0	1	0

2-byte commands (LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Character display position control	V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2
Write address control	AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AC4	AR0	AR1	AR2
Output pin control	0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	OD0	OD1
Character size control	SV0	SV1	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	SH0	SH1
3-channel background control	BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0
Initial status setting	0	ECK	1	0	1	1	0	1	OSC	VST	COC	OP0	OP1	RS	BR	0
Test mode[Note]	0	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

Note Must not be used.

2-byte successive command (LSB)

Function	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
Display character control	V_{C2}	BL	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7

2.3 Power-ON Clear Function

Because the internal status of the IC is undefined on power application, execute power-ON clear by lowering the $\overline{\text{PCL}}$ pin for the duration described below.

Command setting on power-ON clear is as follows:

- Clears test mode
- Default setting of initial status (Refer to **3.14 Initial Status Setting Command**.)
- Clears all character data (12 rows, 28 columns) of video RAM (Display Off Data (FEH)). No data blinks.
- Video RAM write address (row 0, digit 0)
- Standard size for all rows as character size (SV1, SV0, SH1, SH0) = (0, 0, 0, 0)
- All rows specified for output pin selection (OD1, OD0) = (0, 0)
- Display OFF, LC oscillation ON, blinking OFF
- Display of each channel OFF
- No background and framing for all three channels
- Character color reversing OFF
- Character left and right reverse OFF
- Blue back OFF
- Low-order (0) bank for character address
- Output switch control is only SW1 = ON, others OFF (S3A, S3B, SW4, SW2, SW1) = (1, 0, 0, 0, 1)

The time required for power-ON clear can be calculated by the following expression. Do not input any command during this time.

t (Time required for power-ON clearing) = t_{PCLL}**Note** + Video RAM clear time

$$= 10\ (\mu s) + 10\ (\mu s) + 12/f_{OSC}\ (\text{MHz}) \times 336$$

$$= 10\ (\mu s) + 10\ (\mu s) + 24/f_{OSC2}\ (\text{MHz}) \times 336$$

f_{OSC} (MHz): LC oscillation frequency or external input clock frequency (when ×1 frequency mode is selected)

f_{OSC2} (MHz): External input clock frequency (when ×2 frequency mode is selected)

Note Refer to **Power-ON Clear Specifications** in **6. ELECTRICAL CHARACTERISTICS**.

To clear the video RAM, the dot clock (OSC_{IN} pin) must be input. Be sure to input the clock when the input of an external clock is selected.

3. DETAILS OF COMMANDS

3.1 Video RAM Batch Clear Command

This command can be used to clear the video RAM with a single command (regardless of whether the MSB or LSB comes first)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0

The following contents are set by the video RAM batch clear command.

- Clears all the character data (Display Off Data (FEH)) of the video RAM (12 rows, 28 columns). No data blinks.
- Video RAM write address: (Row 0, column 0)
- Standard size for all rows as character size (SV1, SV0, SH1, SH0) = (0, 0, 0, 0)
- All rows specified for output pin selection (OD1, OD0) = (0, 0)
- Display OFF, LC oscillation ON, blinking OFF

The time required for clearing the video RAM can be calculated by the following expression. Do not input any command during this time.

t (Time required for video RAM clearing) = Video RAM clear time

$= 10\ (\mu s) + 12/f_{OSC}\ (MHz) \times 336$

$= 10\ (\mu s) + 24/f_{OSC2}\ (MHz) \times 336$

f_{OSC} (MHz): LC oscillation frequency or external input clock frequency (when ×1 frequency mode is selected)

f_{OSC2} (MHz): External input clock frequency (when ×2 frequency mode is selected)

To clear the video RAM, the dot clock (OSC_{IN} pin) must be input. Be sure to input the clock when the input of an external clock is selected.

Remark This command resets the hardware of the IC by inputting a signal to the $\overline{PCL}$ pin. While initializing the IC including clearing the video RAM and the test mode, the video RAM batch clear command executes software reset to initialize the IC, and does not clear the test mode.

3.2 Display Control Command

This command controls the display output, LC oscillation, blinking the characters, and left to right reverse.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	DO	LC	BL1	BL0

With blinking character selected[Note]

Blinking control bit (screen unit)		
BL1	BL0	Function
0	0	Blinking OFF
0	1	Blinking frequency: approx. 2 Hz
1	0	Blinking frequency: approx. 1 Hz
1	1	Blinking frequency: approx. 0.5 Hz

With character left and right reverse selected[Note]

Left to right reverse control bit		
BL1	BL0	Function
–	0	Character left to right reverse OFF
–	1	Character left to right reverse ON

– : “0” or “1”

LC oscillation control bit	
LC	Function
0	LC oscillation OFF
1	LC oscillation ON

Character display ON/OFF control bit	
DO	Function
0	Display OFF
1	Display ON

Note Set with the initial setting command.

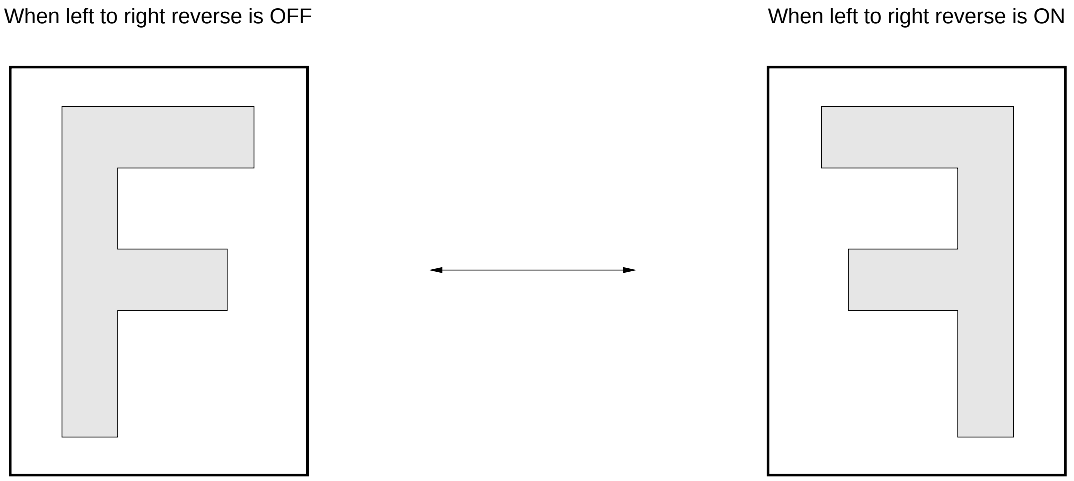
(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BL0	BL1	LC	DO	1	0	0	0

- **Blinking control (screen units)**
  The function selected by the initial setting command is controlled.
  - Blinking control (screen units)
    Whether the characters written to the video RAM blink or not is controlled in screen units. The character specified to blink by the display character control command blinks.
    The blinking ratio is 1:1, and the blinking frequency can be selected from three types.
- **Left to right reverse control**
  The character specified to be reversed left to right by the display character control command is reversed (this is valid only if character left to right reverse is selected by the initial setting command).

Display example of character specified to be reversed left to right (character “F” is displayed)


When left to right reverse is OFF
When left to right reverse is ON

- **LC oscillation control**
  The oscillation circuit can be turned ON/OFF by the oscillation control bit. Oscillation is stopped during the period in which the characters are not displayed, to reduce the power consumption.
  Nothing can be written to the video RAM while the oscillation is stopped. To write data to the video RAM, be sure to turn ON oscillation.

Cautions 1. When LC oscillation is used : Oscillation is synchronized with $\overline{\text{Hsync}}$ when the character display is ON, and is stopped while $\overline{\text{Hsync}}$ is low. When character display is OFF, oscillation continues regardless of $\overline{\text{Hsync}}$.

2. When external clock is input : When an external clock is used, the clock is supplied to the IC's internal circuitry when oscillation is turned ON. When oscillation is OFF, the clock supply to the internal circuitry is stopped.

- **Character display ON/OFF control**

  Character display output can be turned ON/OFF. The display is turned ON/OFF in synchronization with the falling of $\overline{\text{Hsync}}$.

3.3 Background Color/Frame Color Control Command

This command specifies the background color and frame color. This command is valid when filling of the background, blank background, or framing is specified.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	R	G	B	BFC

Frame color control bit

BFC	Function
0	Frame color: Black
1	Frame color: White

Background color control bit

R	G	B	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BFC	B	G	R	0	1	0	0

- **Frame color control**
  The frame color (white/black) can be selected in screen units (RGB output). If the frame is specified with V_{C1} and V_{C2} output, the frame color is fixed to black.

- **Background color control**
  The background color can be selected (from eight colors) in screen units (RGB output). If the background is specified with V_{C1} and V_{C2} output (blank background or filled background), the background color is fixed to black.

3.4 3-Channel Independent Display ON/OFF Command

This command can turn ON/OFF the display of character output of 3 channels independently.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	DOA	DOB	DOC

With support of RGB/V_{C1}/V_{C2} output selected

Control bit		Function
DOA	0	RGB display OFF
	1	RGB display ON
DOB	0	V_{C1} display OFF
	1	V_{C1} display ON
DOC	0	V_{C2} display OFF
	1	V_{C2} display ON

With R/G/B/3BLK output selected

Control bit		Function
DOA	0	Character display OFF
	1	Character display ON
DOB	–	Don't care
DOC	–	Don't care

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
DOC	DOB	DOA	0	1	1	1	0

- Displaying the character signal of the 3 channels (RGB, V_{C1}, and V_{C2}) can be independently turned ON/OFF.
  When RGB + RGB compatible BLK is selected, it is controlled by the display ON/OFF command.
- Turning ON display each output channel by using this command is valid only when the display is turned ON by the display control command.
- If the display is turned OFF by the display control command, the display remains OFF even if it is specified to be ON by this command.

3.5 Character Color Reverse ON/OFF Command

This command specifies reversal of character color in screen units.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) D7	D6	D5	D4	D3	D2	D1	(LSB) D0
0	0	1	1	1	0	0	BCRE

Character color reverse control bit

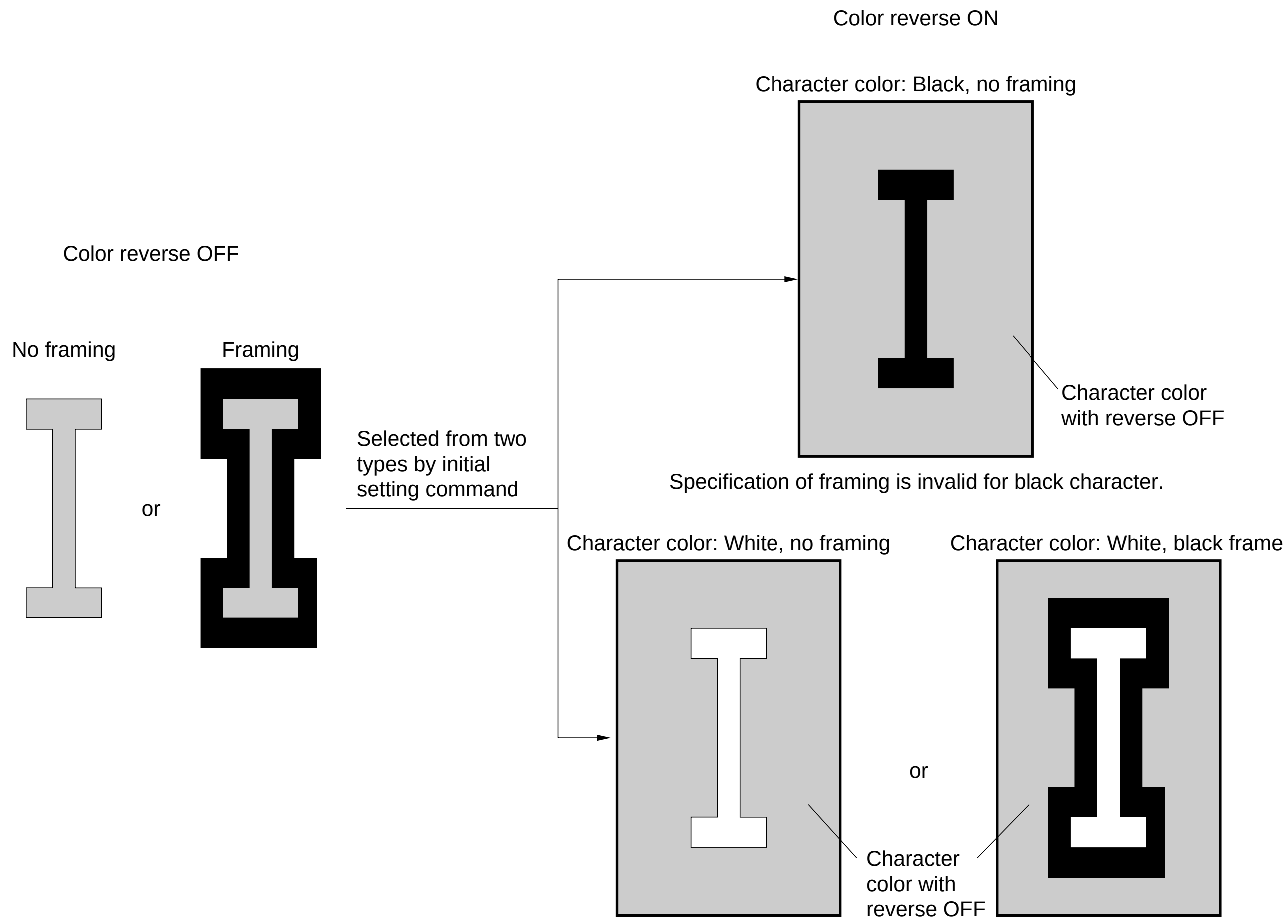
BCRE	Function
0	Character color not reversed
1	Character color reversed

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) D0	D1	D2	D3	D4	D5	D6	(MSB) D7
BCRE	0	0	1	1	1	0	0

The color of the character specified by the display character control command is reversed for the whole screen with the reverse specifications (character color: black or white) specified by the initial status setting command.

Example of display of reversed character (example of reversing character "I")


Color reverse ON
Character color: Black, no framing
Character color with reverse OFF
Specification of framing is invalid for black character.
Color reverse OFF
No framing
Framing
or
Selected from two types by initial setting command
Character color: White, no framing
Character color: White, black frame
or
Character color with reverse OFF

The character color/background color (with blank background or filled background) can be selected from eight types in the case of RGB output when reversing character color is specified to be OFF.
In the case of V_{C1} and V_{C2}, the character color is white and the background color is black.
The Display Off Data is not affected even when inverted.
If Blank Data is reversed, it is filled with the character color originally specified.
The character color and the color of the framing in the above figure are valid with the RGB.
Only black and white are displayed in the case of V_{C1} and V_{C2}.
In the case of V_{C1} and V_{C2}, framing in the character color reverse area is invalid (same as the μPD6461, 6462 and 6466).

3.6 Blue Back ON/OFF Command

This command turns ON/OFF the blue back function in screen units.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	CLR	0	BB

Blue back control bit

BB	Function
0	Blue back OFF
1	Blue back ON

Color specification bit

CLR	Function
0	Blue
1	White

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BB	0	CLR	1	1	1	1	0

By turning ON the blue back function, the character, framing, and area where no background is output are all displayed in blue. This command is valid only for RGB output.

3.7 Character Address Bank Select Command

This command selects the area of the character address specified by the character address specification bit of the display character control command.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	1	BC

Character address bank select control bit

BC	Function
0	Low-order bank (0)
1	High-order bank (1)

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
BC	1	1	1	1	1	1	0

If the low-order bank (0) is specified by the 8-bit data (the second byte of the display character control command) of the character data, character addresses 00H through FFH (common addresses 000H through 0FFH) of the low-order (0) bank are specified. If the high-order bank (1) is specified, character addresses 00H through FFH (common addresses 100H through 1FFH) of the high-order (1) bank are specified.

If FEH is specified at the character address of the display character control command for both banks, the command can be used as the Display Off code. If FFH is specified, it can be used as a 2-byte successive command end code.

3.8 Output Switch Control Command

This command controls ON/OFF of SW1 through SW4, and selects the output format of RGB and V_{C1}.

(1) With MSB first (The command is input from MSB (D7).)

(MSB) (LSB)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	S3A	S3B	SW4	SW2	SW1

SW1 control bit

SW1	Function
0	OFF
1	ON

SW2 control bit

SW2	Function
0	OFF
1	ON

SW4 control bit

SW4	Function
0	OFF
1	ON

SW3 control bit

S3A	S3B	Function
0	0	Controlled by row unit data (OD1) OD1 = 0 : OFF, OD1 = 1 : ON
0	1	
1	0	OFF regardless of OD1
1	1	ON regardless of OD1

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7
SW1	SW2	SW4	S3B	S3A	0	1	0

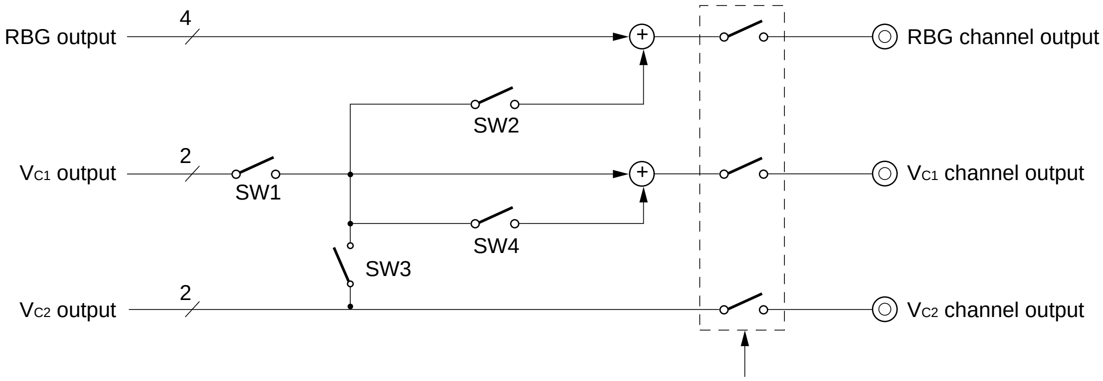
Output format in each switch status

Mode	SW1	SW2	SW4	SW3	RGB	V_{C1}	V_{C2}
1	ON	OFF	OFF	ON	RGB	V_{C1}	V_{C2}
2	ON	OFF	OFF	OFF	RGB	V_{C1}	V_{C2}
3	ON	ON	OFF	ON	RGB+V_{C2}	V_{C1}	V_{C2}
4	ON	ON	OFF	OFF	RGB	V_{C1}	V_{C2}
5	ON	OFF	ON	ON	RGB	V_{C1}+V_{C2}	V_{C2}
6	ON	OFF	ON	OFF	RGB	V_{C1}	V_{C2}
7	ON	ON	ON	ON	RGB+V_{C2}	V_{C1}+V_{C2}	V_{C2}
8	ON	ON	ON	OFF	RGB	V_{C1}	V_{C2}
9	OFF	ON	ON	ON	RGB+V_{C2}	V_{C2}	V_{C2}
10	OFF	ON	ON	OFF	RGB	V_{C1}	V_{C2}
11	OFF	OFF	ON	ON	RGB	V_{C2}	V_{C2}
12	OFF	OFF	ON	OFF	RGB	V_{C1}	V_{C2}
13	OFF	OFF	OFF	ON	RGB	V_{C1}	V_{C2}
14	OFF	OFF	OFF	OFF	RGB	V_{C1}	V_{C2}
15	OFF	ON	OFF	ON	RGB+V_{C2}	V_{C1}	V_{C2}
16	OFF	ON	OFF	OFF	RGB	V_{C1}	V_{C2}

Caution **The V_{C2} character is output by each channel as follows. The V_{C2} outputs only V_{C2} regardless of the status of SW1 to SW4 (same as μPD6461, 6462 and 6466).**

- **If RGB channel is RGB, RGB + V_{C2} : Not controlled at all by output pin control command.**
- **If V_{C1} channel is V_{C1}, V_{C1} + V_{C2} : Output pins at V_{C1} side are controlled.**
- **If V_{C1} channel is V_{C2} : Output pins at V_{C2} side are controlled.**

Image of Internal output and Terminal output



These switches are controlled by 3-channel independent display ON/OFF command.

3.9 Character Display Position Control Command

This command can be used to set the character display start position in 32 steps in units of 3 dots in the horizontal direction, and in 32 steps in units of 3 rows in the vertical direction (because this command is a 2-byte command, input of 16 bits is necessary when this command is input more than once successively).

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	V4	V3	V2	V1	V0	H4	H3	H2	H1	H0

Horizontal display start position control bit					
H4	H3	H2	H1	H0	Function
0	0	0	0	0	Time from rising of $\overline{\text{Hsync}}$ (μs) $(22+3\times0)/f_{OSC}$ (MHz) $(45+6\times0)/f_{OSC2}$ (MHz)
0	0	0	0	0	Time from rising of $\overline{\text{Hsync}}$ (μs) $(22+3\times1)/f_{OSC}$ (MHz) $(45+6\times1)/f_{OSC2}$ (MHz)
≈	≈	≈	≈	≈	≈
1	1	1	1	1	Time from rising of $\overline{\text{Hsync}}$ (μs) $(22+3\times31)/f_{OSC}$ (MHz) $(45+6\times31)/f_{OSC2}$ (MHz)

Remark f_{OSC} : LC oscillation frequency or external input clock frequency (×1 frequency mode)

f_{OSC2}: External input clock frequency (×2 frequency mode)

Vertical display start position control bit					
V4	V3	V2	V1	V0	Function
0	0	0	0	0	3H×0+2H (9H×0+2H) from rising of $\overline{\text{Vsync}}$
0	0	0	0	1	3H×1+2H (9H×1+2H) from rising of $\overline{\text{Vsync}}$
≈	≈	≈	≈	≈	≈
1	1	1	1	1	3H×31+2H from rising of $\overline{\text{Vsync}}$

Remarks 1. H: row

2. ( ): If 9H unit is selected by the initial status setting command.

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
V3	V4	0	0	0	0	0	1	H0	H1	H2	H3	H4	V0	V1	V2

- **Horizontal display start position control**

  (1) In case of LC oscillation or Exernal input clock ×1 frequency mode

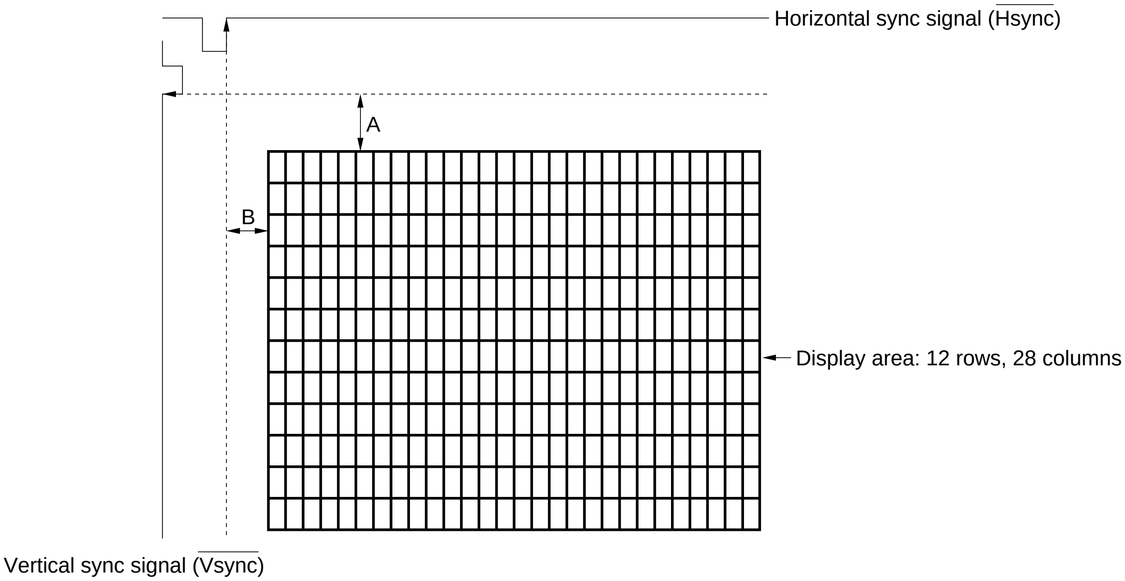
  The horizontal display start position can be set in 32 steps in units of 3 dots ($3/f_{OSC}$ (MHz)) 22 clocks ($22/f_{OSC}$ (MHz)) after the rising of the horizontal sync signal input to the $\overline{\text{Hsync}}$ pin (f_{OSC}: LC oscillation frequency or external input clock frequency).

  (2) In case of External input clock ×2 frequency mode

  The horizontal display start position can be set in 32 steps in units of 3 dots ($6/f_{OSC2}$ (MHz)) 45 clocks ($22/f_{OSC2}$ (MHz)) after the rising of the hirizontal sync signal input to the $\overline{\text{Hsync}}$ pin.

- **Vertical display start position control**

  The vertical display start position can be set in 32 steps in units of 3 or 9 rows (refer to **3.14 Initial Status Setting Command**) from the rising of the vertical sync signal input to the $\overline{\text{Vsync}}$ pin.


Horizontal sync signal (Hsync)
A
B
Display area: 12 rows, 28 columns
Vertical sync signal (Vsync)

A : $\underline{3H} \times (2^4V_4 + 2^3V_3 + 2^2V_2 + 2^1V_1 + 2^0V_0) + 2H$

9H if 9H unit is selected by the initial status setting command.

B : (1) In case of LC oscillation or External input clock ×1 frequency mode

$$\frac{3}{f_{OSC}(\text{MHz})} \times (2^4H_4 + 2^3H_3 + 2^2H_2 + 2^1H_1 + 2^0H_0) + \frac{22}{f_{OSC}(\text{MHz})}$$

(2) External input clock ×2 frequency mode

$$\frac{6}{f_{OSC2}(\text{MHz})} \times (2^4H_4 + 2^3H_3 + 2^2H_2 + 2^1H_1 + 2^0H_0) + \frac{45}{f_{OSC2}(\text{MHz})}$$

f_{OSC} : LC oscillation frequency or external input clock frequency (×1 frequency mode)
f_{OSC2}: External input clock frequency (×2 frequency mode)
H : row

3.10 Write Address Control Command

This command is used to specify a write address when characters are written to the display area (video RAM) of 12 rows and 28 columns (because this command is a 2-byte command, input of 16 bits is necessary when this command is input more than once successively).

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	AR3	AR2	AR1	AR0	AC4	AC3	AC2	AC1	AC0

Write column address control bit

AC4	AC3	AC2	AC1	AC0	Function
0	0	0	0	0	Sets column 0
0	0	0	0	1	Sets column 1
≈	≈	≈	≈	≈	≈
1	1	0	1	1	Sets column 27
Setting prohibited					

Write row address control bit

AR3	AR2	AR1	AR0	Function
0	0	0	0	Sets row 0
0	0	0	1	Sets row 1
≈	≈	≈	≈	≈
1	0	1	1	Sets row 11
Setting prohibited				

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
AR3	0	0	1	0	0	0	1	AC0	AC1	AC2	AC3	AC4	AR0	AR1	AR2

- **Write column address control**
  One row consists of 28 columns in the horizontal direction. Specify to which column data is to be written.

- **Write row address control**
  One column consists of 12 rows in the vertical direction. Specify to which row data is to be written.

3.11 Output Pin Control Command

This command selects the format of pin output of the option (A, B, or C) specified by the initial status setting command (because this is a 2-byte command, input of 16 bits is necessary if this command is input more than once successively).

Remark This command is invalid when RGB + RGB compatible BLK output is selected.

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	0	0	OD1	OD0	0	0	AR3	AR2	AR1	AR0

Row specification bit				
AR3	AR2	AR1	AR0	Function
0	0	0	0	Sets row 0
0	0	0	1	Sets row 1
≈	≈	≈	≈	≈
1	0	1	1	Sets row 11
Setting prohibited				

Option A

Output pin control bit		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs specified row, V_{C2}: Fixed to low level
0	1	V_{C1}: Fixed to low level, V_{C2}: Outputs specified row

Option B

Output pin control bit		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs all rows, V_{C2}: Fixed to low level
0	1	V_{C1}: Outputs all rows, V_{C2}: Outputs specified row

Option C

Output pin control bit		
OD1	OD0	Pin output
0	0	V_{C1}: Outputs columns 0-27, V_{C2}: Fixed to low level
0	1	V_{C1}: Outputs columns 0-11, V_{C2}: Outputs columns 12-27
1	0	V_{C1}: Outputs columns 12-27, V_{C2}: Outputs columns 0-11
1	1	V_{C1}: Fixed to low level, V_{C2}: Outputs columns 0-27

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	1	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	OD0	OD1

- **Row specification control**
  Specify to which of the V_{C1} or V_{C2} pin the character signal is to be output in row units (or 12-column, 16-column units).

- **Output pin control**
  Output of the V_{C1} and V_{C2} pin can be selected from A, B, or C by using the initial status setting command (the blanking signal is output in the same manner).

3.12 Character Size Control Command

The character size can be specified in row units (independently in the horizontal and vertical directions. Because this is a 2-byte command, input of 16 bits is necessary when this command is input more than once successively).

(1) With MSB first (The command is input from MSB (D15).)

(MSB) … (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	SV1	SV0	SH1	SH0	0	0	AR3	AR2	AR1	AR0

Row specification control bit

AR3	AR2	AR1	AR0	Function
0	0	0	0	Sets row 0
0	0	0	1	Sets row 1
≈	≈	≈	≈	≈
1	0	1	1	Sets row 11
Setting prohibited				

Horizontal character size control bit

SH1	SH0	Function
0	0	1 dot = 1t dots (horizontal standard size)
0	1	1 dot = 2t dots (horizontal ×2 size)
1	0	1 dot = 3t dots (horizontal ×3 size)
1	1	1 dot = 4t dots (horizontal ×4 size)

Vertical character size control bit

SV1	SV0	Function
0	0	1 dot = 1H (vertical standard size)
0	1	1 dot = 2H (vertical ×2 size)
1	0	1 dot = 3H (vertical ×3 size)
1	1	1 dot = 4H (vertical ×4 size)

Remark $1\text{t dots } (\mu\text{s}) = \dfrac{1}{f_{\text{OSC}}\ (\text{MHz})} = \dfrac{2}{f_{\text{OSC2}}\ (\text{MHz})}$

f_{OSC} : LC oscillation frequency or external input clock frequency (×1 frequency mode)

f_{OSC2} : External input clock frequency (×2 frequency mode)

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) … (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
SV0	SV1	0	1	1	0	0	1	AR0	AR1	AR2	AR3	0	0	SH0	SH1

- **Row specification control**
  The character size is specified in row units. Which row is specified is controlled.

- **Character size control**
  Four steps (16 types) of character size can be selected in the vertical and horizontal directions independently.

3.13 3-Channel Background Control Command

This command can be used to independently specify the background for the output of the 3 channels (because this command is a 2-byte command, input of 16 bits is necessary when this command is input more than once successively).

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	1	BA1	BA0	BFA	BB1	BB0	BFB	BC1	BC0	BFC

V_{C2} output

V_{C2} background control bit		
BC1	BC0	Function
0	0	No background
0	1	Blank background
1	0	Must not be specified
1	1	Filled background

V_{C2} framing control bit	
BFC	Function
0	Framing OFF
1	Framing ON

V_{C1} output

V_{C1} background control bit		
BB1	BB0	Function
0	0	No background
0	1	Blank background
1	0	Must not be specified
1	1	Filled background

V_{C1} framing control bit	
BFB	Function
0	Framing OFF
1	Framing ON

RGB output

RGB background control bit		
BA1	BA0	Function
0	0	No background
0	1	Blank background
1	0	Must not be specified
1	1	Filled background

RGB framing control bit	
BFA	Function
0	Framing OFF
1	Framing ON

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

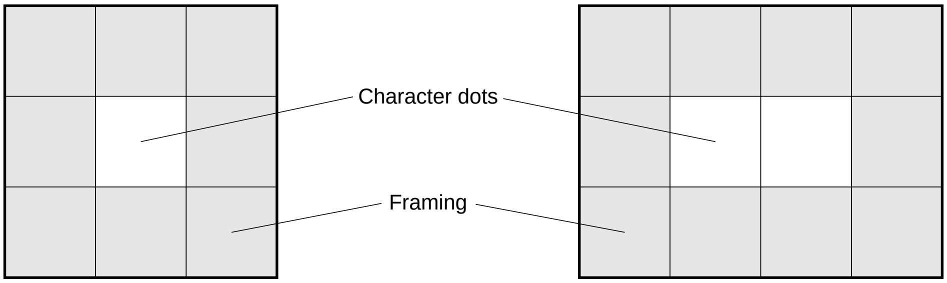
(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
BA1	1	0	0	1	1	0	1	BFC	BC0	BC1	BFB	BB0	BB1	BFA	BA0

- **Framing control**

  Whether a character is framed is specified in screen units.

  Framing: If the rightmost or leftmost dots of the dot matrix forming a character are used, the frame is displayed in the adjacent character display area. If the rightmost or leftmost dots of the dot matrix are not used, the frame is displayed on the left or the right of, above, or upper or lower left or right of the character. Even when the top or bottom dot is used, framing does not overlap the line above or below. Dots other than those at the top or bottom of the dot matrix are framed vertically, horizontally, and diagonally.



  The size of the framing is fixed to one dot of the minimum size even if the character size changes.

- **Background control**

  No background, blank background, or filled background can be selected in screen units. The background color is selected by the background color/framing color control command.

  No background : Only character data is output.
  Blank background : The background is displayed in the display area of the characters written to the video RAM and the portion overlapping by one dot of the minimum size from the rightmost and leftmost position of that area.
  Filled background : In addition to the area where the background is displayed in the blank background mode above, the background is displayed in the areas other than the character display area.

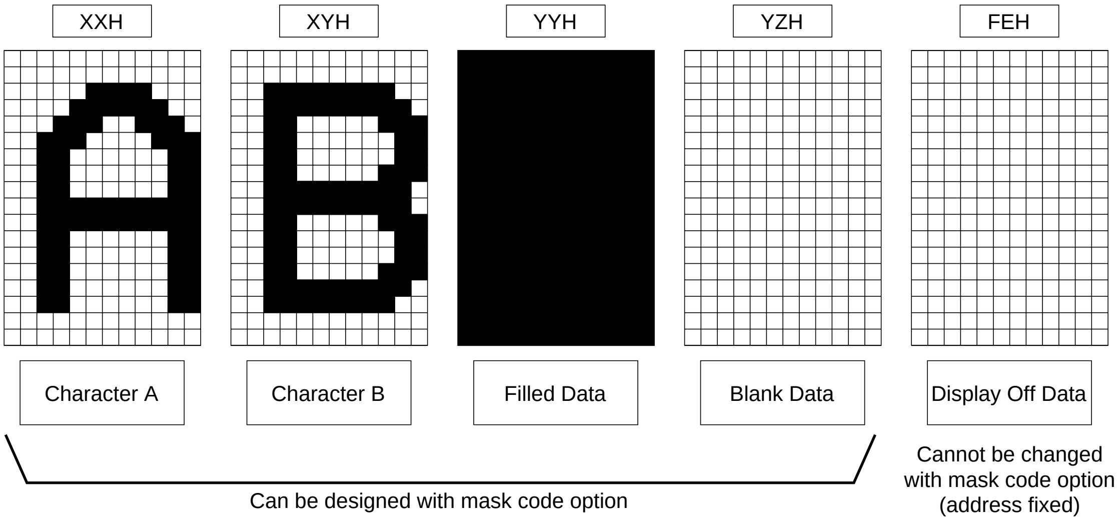
- **Background and frame display in the case of RGB + V_{C1} + V_{C2} output**

  The portion of the character for which V_{C2} is specified by the display character control command is not output to the RGB and V_{C1} channels. Therefore, even if a background (blank background or filled background) is specified for the RGB or V_{C1} output, no background is displayed in the V_{C2}-specified area. In addition, no background is displayed at the portion of the character other than those specified by V_{C2} in the case of V_{C2} output (for the details of display of V_{C2}-specified character area for RGB and V_{C1} output, refer to **1.3 Display with RGB + V_{C1} + V_{C2} Pins** and **1.3.4 Displaying characters specified by V_{C2}**).

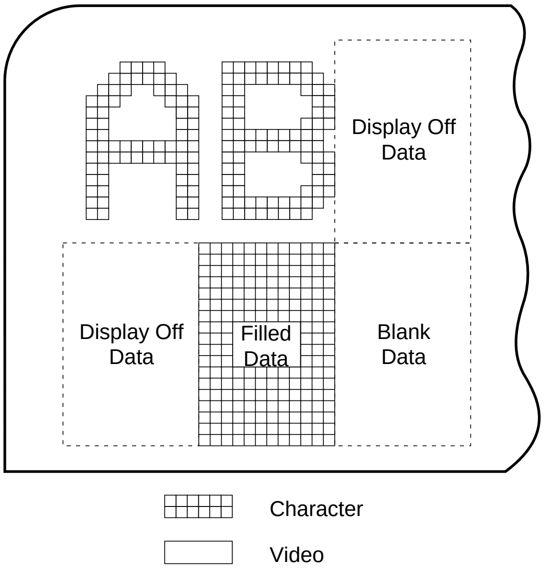
  When RGB + RGB compatible BLK output is selected, only the background control bit of RGB output is valid, and the background control bit of V_{C1} output and V_{C2} output is invalid (when RGB + RGB compatible BLK output is selected, the V_{C2} output pin is not used. The V_{C1} channel outputs the logical sum of the RGB output).

Display format of background and frame

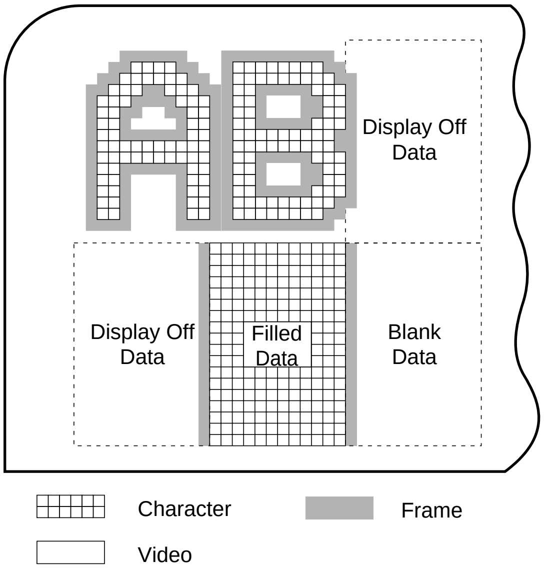
Display example with character


XXH
XYH
YYH
YZH
FEH
Character A
Character B
Filled Data
Blank Data
Display Off Data
Can be designed with mask code option
Cannot be changed with mask code option (address fixed)

No background + no frame

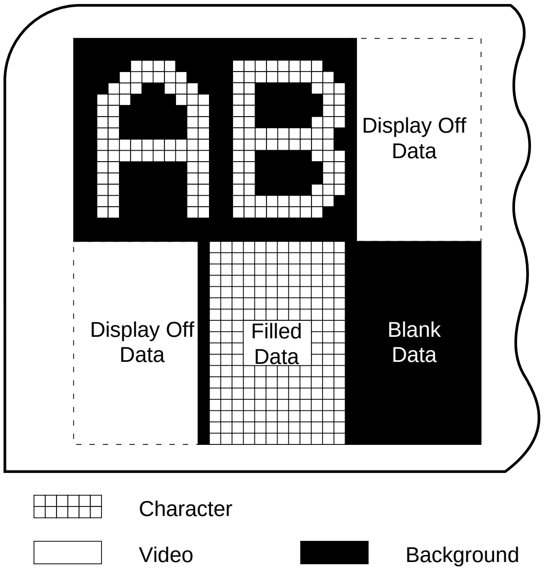

Display Off Data
Display Off Data
Filled Data
Blank Data
Character
Video

No background + frame

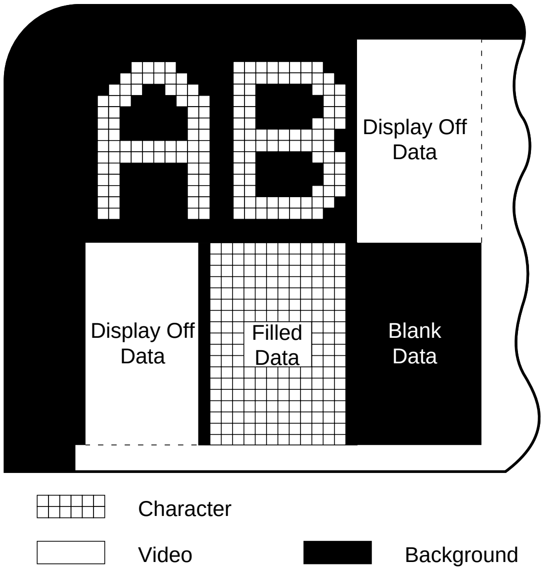

Display Off Data
Display Off Data
Filled Data
Blank Data
Character
Frame
Video

Eight colors can be selected for the character and background, and two colors (black and white) can be selected for the frame, in screen units.

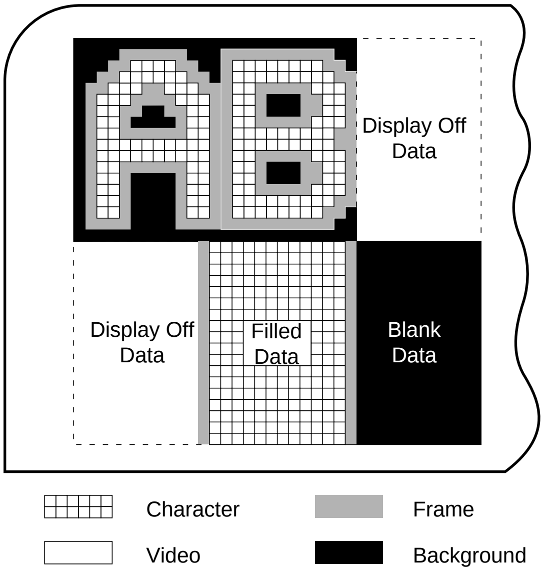
Blank background + no frame


Display Off
Data
Display Off
Data
Filled
Data
Blank
Data
Character
Video
Background

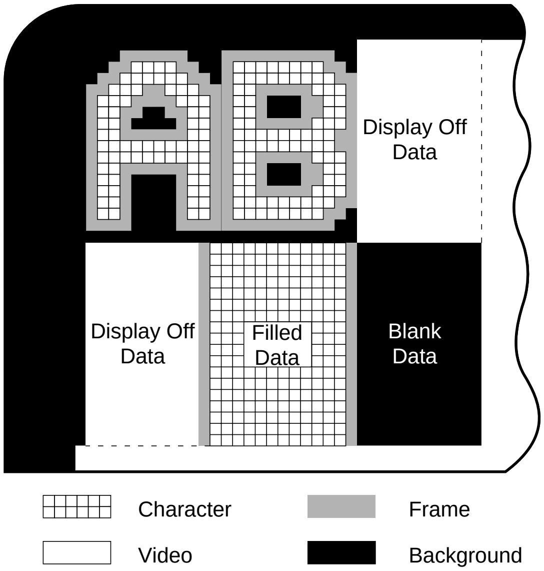
Filled background + no frame


Display Off
Data
Display Off
Data
Filled
Data
Blank
Data
Character
Video
Background

Blank background + frame


Display Off
Data
Display Off
Data
Filled
Data
Blank
Data
Character
Frame
Video
Background

Filled background + frame


Display Off
Data
Display Off
Data
Filled
Data
Blank
Data
Character
Frame
Video
Background

3.14 Initial Status Setting Command

This command initializes the operation mode.

Execute this command first on power application.

To change the initial setting, be sure to execute this command with the display OFF.

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	1	ECK	0	0	BR	RS	OP1	OP0	COC	VST	OSC

Dot clock control bit	
OSC	Function
0	LC oscillation
1	External clock input

Vertical display start position control bit	
VST	Function
0	Vertical display start position setting unit = 3 rows
1	Vertical display start position setting unit = 9 rows

Pin selection control bit	
COC	Function
0	RGB + V_{C1} + V_{C2}
1	RGB + RGB compatible BLK (3BLK)

Output selection control bit		
OP1	OP0	Function
0	0	Option A
0	1	Option B
1	0	Option C
1	1	Must not be specified

Character color reverse control bit	
RS	Function
0	Character color: Black (frame specification is invalid)
1	Character color: White (frame specification is valid)

Function selection bit	
BR	Function
0	Character blinks
1	Character left to right reverse

External clock frequency selection bit	
ECK	Function
0	×1 frequency mode
1 Note	×2 frequency mode

Note When the dot clock control bit (OSC) is "1 (External clock input)", the external clock frequency selection bit (ECK) is able to set "1". When OSC is "0", ECK should be set "0".

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	ECK	1	0	1	1	0	1	OSC	VST	COC	OP0	OP1	RS	BR	0

This command sets the information selected by a mask code option in the μPD6461 and 6462.
The default setting is as follows:

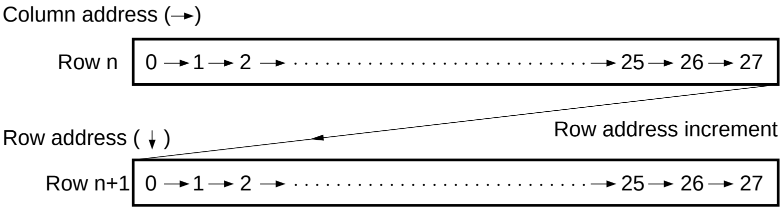
OSC = 0 : LC oscillation
VST = 0 : 3-row units
COC = 0 : RGB + V_{C1} + V_{C2}
(OP1, OP0) = (0, 1) : Option B
RS = 0 : Black character
BR = 0 : Character blinks
ECK = 0 : External input clock ×1 frequency mode

3.15 Display Character Control Command

This command specifies the character data to be written to the video RAM, blinking data, and character color.

When inputting this command, turn ON LC oscillation (if the oscillation is OFF, characters cannot be written to the video RAM).

This command is a 2-byte successive command. To write character data successively without changing the blinking data, character color, and character address bank, the second character and those that follow can be input in the abbreviated form by using only the low-order 8 bits (D7 through D0). In this case, the write column address is automatically incremented (If a character is written to the 27th column, the next write address is automatically incremented to column 0 (leftmost) on one row below. If characters have been written to the 27th column on the 11th row, the next write address is automatically incremented to column 0 on row 0).



(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	RV	R	G	B	BL	V_{C2}	C7	C6	C5	C4	C3	C2	C1	C0

Character specification bit

C7	C6	C5	C4	C3	C2	C1	C0	Function
0	0	0	0	0	0	0	0	Outputs data of 00H
0	0	0	0	0	0	0	1	Outputs data of 01H
≈	≈	≈	≈	≈	≈	≈	≈	≈
1	1	1	1	1	1	1	0	Outputs FEH (Display Off Data)
1	1	1	1	1	1	1	1	FFH (2-byte successive command end code)

V_{C2} output specification bit

V_{C2}	Function
0	V_{C2} specification OFF
1	V_{C2} specification ON

With character blinking selected[Note]

Blinking control bit (character units)

BL	Function
0	Character does not blink.
1	Character blinks.

With character left and right reverse selected[Note]

Left and right reverse character control bit

BL	Function
0	Left and right reverse character specification OFF
1	Left and right reverse character specification ON

Character color specification bit

R	G	B	Function
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White

Character color reverse specification bit

RV	Function
0	Character color reverse specification OFF
1	Character color reverse specification ON

Note Set these bits with the initial setting command.

(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
V_{C2}	RB	B	G	R	RV	1	1	C0	C1	C2	C3	C4	C5	C6	C7

- **Character specification**
  Specify the addresses of the 256 types of characters in each bank. Note, however, that addresses FEH and FFH are respectively fixed to Display Off Data and a 2-byte successive command end code (these addresses are also fixed when characters are changed by using a mask code option, and no characters can be stored to these addresses). The design of the characters can be created by using a mask code option.

- **V_{C2} output specification**
  The character output from the V_{C2} pin can be specified in character units. The character specified by V_{C2} is not output from the RGB output or V_{C1} output channel (this specification is invalid when RGB + RGB compatible BLK output selected).

- **Blinking control (character units)Note**
  Whether the character written to the video RAM blinks is specified in character units. Blinking is turned ON/OFF in screen units by using the character display control command (refer to **3.2 Display Control Command**).

- **Left to right reverse character specificationNote**
  Left to right reverse can be turned ON/OFF in character units (this specification is valid when left and right reverse is turned ON by the display control command).

  Note Character blinking or character left to right reverse, whichever selected by the initial setting command, is valid.

- **Character color control**
  A character color can be set in units of one character (valid for RGB output only. The color is fixed for the V_{C1} and V_{C2} output).

- **Character color reverse specification**
  It can be specified whether the color of a character can be reversed or not, in character units. Turning ON/OFF the character color reverse is specified in screen units by the character color reverse ON/OFF command (refer to **3.5 Character Color Reverse ON/OFF Command**).

3.16 Test Mode

This command is used to test the IC and must not be used for any other purposes.

The IC cannot be set in the test mode when the TEST pin (pin 9) is connected to GND.

(1) With MSB first (The command is input from MSB (D15).)

(MSB) (LSB)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

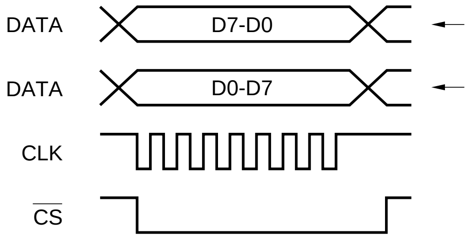
(2) With LSB first (Use of each bit is the same as (1). The command is input from LSB (D0).)

(LSB) (MSB)

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
0	0	0	0	1	1	0	1	T0	T1	T2	T3	T4	T5	T6	T7

4. TRANSFERRING COMMANDS

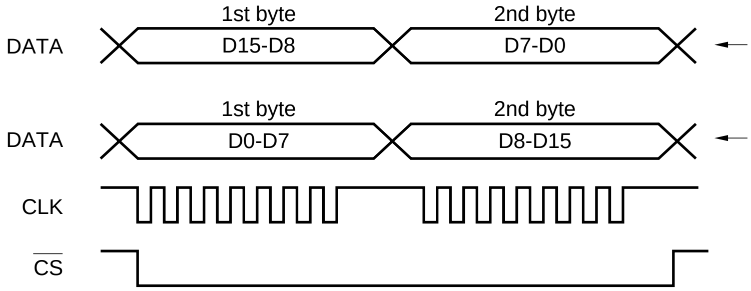
4.1 1-Byte Command


DATA
D7-D0
DATA
D0-D7
CLK
$\overline{\text{CS}}$

With MSB first: The command is input from bit D7.

With LSB first: The command is input from bit D0.

4.2 2-Byte Command

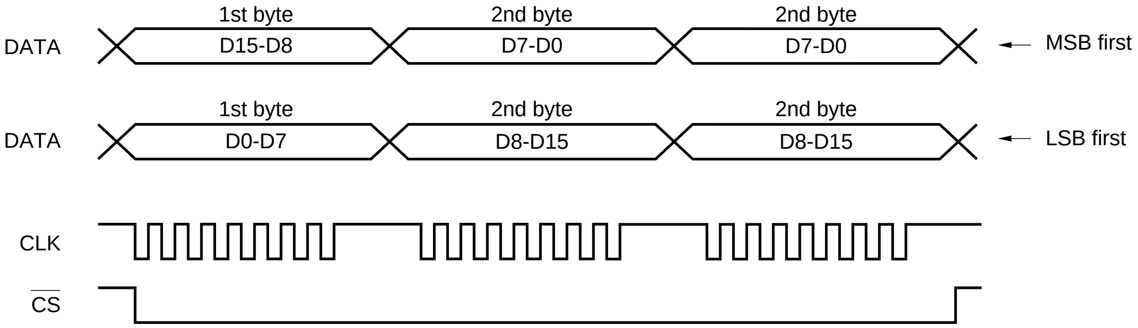

1st byte
2nd byte
DATA
D15-D8
D7-D0
1st byte
2nd byte
DATA
D0-D7
D8-D15
CLK
$\overline{\text{CS}}$

With MSB first
1st byte: D15-D8
2nd byte: D7-D0

With LSB first
1st byte: D0-D7
2nd byte: D8-D15

When transferring a 2-byte command, do not make $\overline{\text{CS}}$ high and keep it low between the first and second bytes.

4.3 2-Byte Successive Commands



The 2-byte successive command writes characters to the video RAM. To successively write characters without changing the blinking data, reverse specification data, and V_{C2} specification data, first transfer the first byte and then transfer the second byte (character address).

To change the contents of the above data, change the contents of the data and then input the command from the first byte after terminating the 2-byte successive command once (by either making $\overline{\text{CS}}$ high or transferring the 2-byte successive command end code).

However, the command cannot be transferred successively across banks.

When the low-order bank is selected, the command can be transferred successively in a character address range of 000H to 0FFH; when the high-order bank is selected, the character address range is from 100H to 1FFH.

It is recommended that characters that are frequently used be stored to both the high-order and low-order banks.

To write a character that across the banks, complete successive transfer once, and then transfer the command from the first byte after changing the bank.

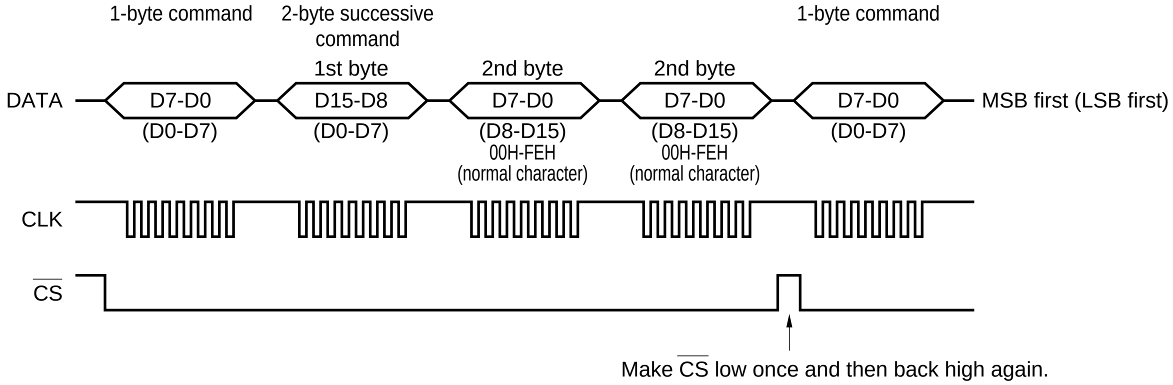
4.4 Successive Input of Command

Transfer each of the 1-byte, 2-byte, and 2-byte successive commands from a microcontroller to the μPD6467 as follows.

To transfer a 1-byte or 2-byte command, or a 2-byte successive command with blinking data changed after a 2-byte successive command has been transferred, either make $\overline{CS}$ high once, or transfer FFH (2-byte successive command end code) at the end of the 2-byte successive command. In the latter case, it is not necessary to make $\overline{CS}$ high.

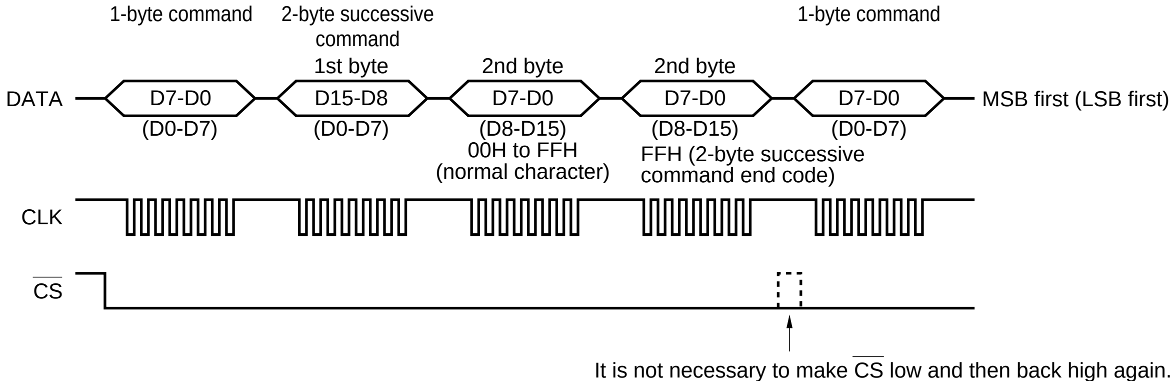
4.4.1 When 2-byte successive command end code is not used

Example 1-byte command → 2-byte successive command → 1-byte command


1-byte command
2-byte successive command
1st byte
2nd byte
2nd byte
1-byte command
DATA
D7-D0
D15-D8
D7-D0
D7-D0
D7-D0
MSB first (LSB first)
(D0-D7)
(D0-D7)
(D8-D15)
(D8-D15)
(D0-D7)
00H-FEH (normal character)
00H-FEH (normal character)
CLK
CS
Make CS low once and then back high again.

4.4.2 When 2-byte successive command end code is used

Example 1-byte command → 2-byte successive command → 1-byte command


1-byte command
2-byte successive command
1st byte
2nd byte
2nd byte
1-byte command
DATA
D7-D0
D15-D8
D7-D0
D7-D0
D7-D0
MSB first (LSB first)
(D0-D7)
(D0-D7)
(D8-D15)
(D8-D15)
(D0-D7)
00H to FFH (normal character)
FFH (2-byte successive command end code)
CLK
CS
It is not necessary to make CS low and then back high again.

Remark By using the 2-byte successive command end code, the $\overline{CS}$ pin may remain low. However, it is recommended to make $\overline{CS}$ pin high to improve the noise immunity.

5. CHARACTER PATTERNS

The μPD6467 can display 512 character patterns, including alphanumeric characters, Kanji characters, and symbols, which are stored in the character generator ROM. Each pattern in the character generator ROM can be modified by specifying a mask code option. However, the Display Off Data at character address FEH and 2-byte continuous command end code at FFH cannot be modified because they are fixed in both high-order (1) and low-order (0) banks. Therefore, no character pattern can be input at these addresses.

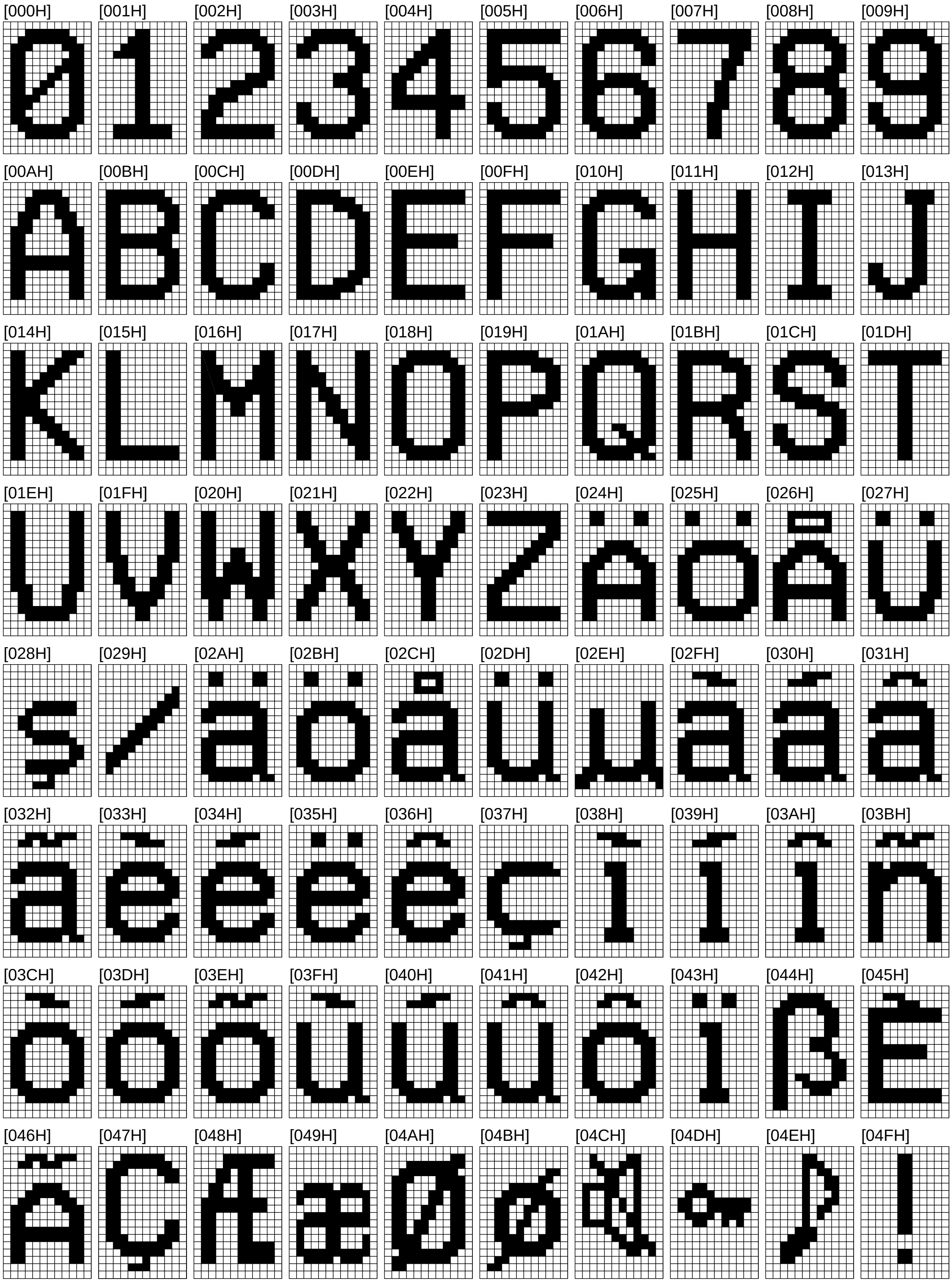
When none of the 12 × 18 dots are filled for a character pattern at addresses 000H to 0FDH and 100H to 1FDH, the character pattern is called Blank Data. Character address FEH in both banks is called Display Off Data. Blank Data and Display Off Data are represented in the same way (with no dots filled) in character patterns (of the μPD6467GR-001) shown on the following pages, but they are different as follows:

Character Code	Display of Character Area in Each Background Mode		
	No background	Minimum background	Overall background
Blank Data	Displays image	Displays background	Displays background
Display Off Data	Displays image	Displays image only (without background)	Displays image only (without background)

You cannot specify Display Off Data for addresses other than FEH when using a mask code option. Blank Data, however, can be specified at any address from 000H to 0FDH or 100H to 1FDH (address 0FFH and 1FFH cannot be used because they are fixed to the 2-byte continuous command end code).

The character patterns of the μPD6467GR-001 (NEC's standard model) are shown on the following pages.

μPD6467GR-001 Character Patterns



[000H] [001H] [002H] [003H] [004H] [005H] [006H] [007H] [008H] [009H]

[00AH] [00BH] [00CH] [00DH] [00EH] [00FH] [010H] [011H] [012H] [013H]

[014H] [015H] [016H] [017H] [018H] [019H] [01AH] [01BH] [01CH] [01DH]

[01EH] [01FH] [020H] [021H] [022H] [023H] [024H] [025H] [026H] [027H]

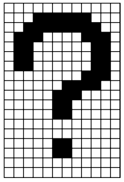
[028H] [029H] [02AH] [02BH] [02CH] [02DH] [02EH] [02FH] [030H] [031H]

[032H] [033H] [034H] [035H] [036H] [037H] [038H] [039H] [03AH] [03BH]

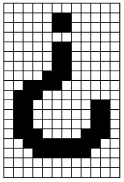
[03CH] [03DH] [03EH] [03FH] [040H] [041H] [042H] [043H] [044H] [045H]

[046H] [047H] [048H] [049H] [04AH] [04BH] [04CH] [04DH] [04EH] [04FH]

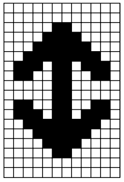
[050H]



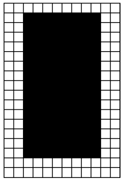
[051H]



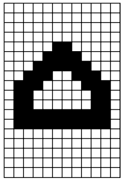
[052H]



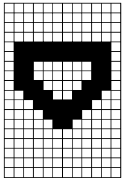
[053H]



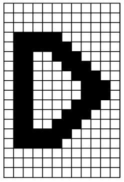
[054H]



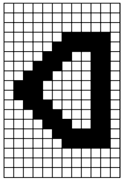
[055H]



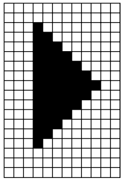
[056H]



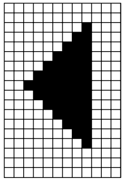
[057H]



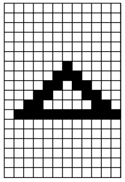
[058H]



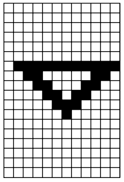
[059H]



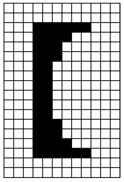
[05AH]



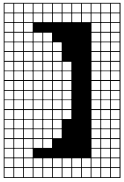
[05BH]



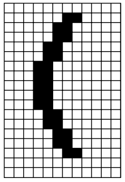
[05CH]



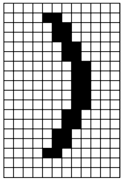
[05DH]



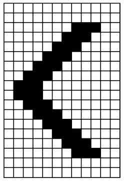
[05EH]



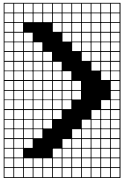
[05FH]



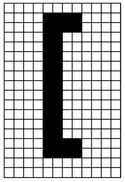
[060H]



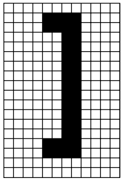
[061H]



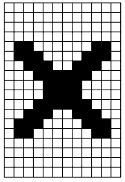
[062H]



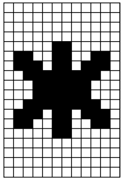
[063H]



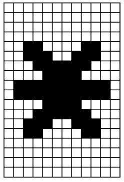
[064H]



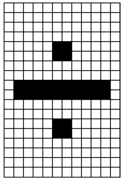
[065H]



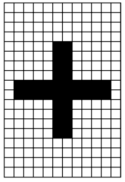
[066H]



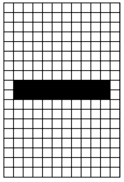
[067H]



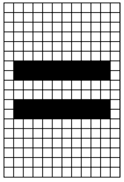
[068H]



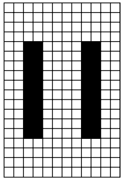
[069H]



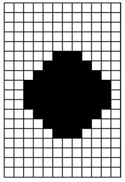
[06AH]



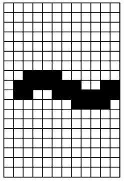
[06BH]



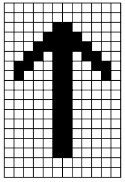
[06CH]



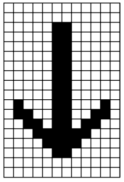
[06DH]



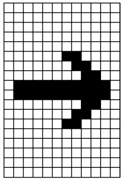
[06EH]



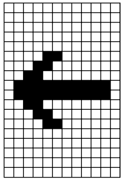
[06FH]



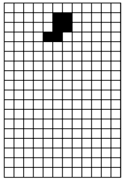
[070H]



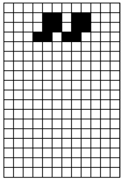
[071H]



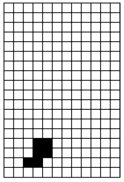
[072H]



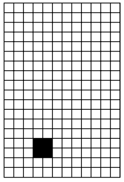
[073H]



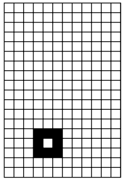
[074H]



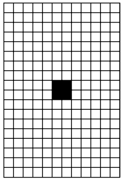
[075H]



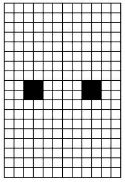
[076H]



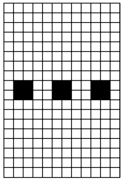
[077H]



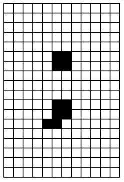
[078H]



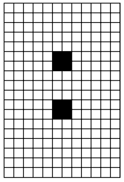
[079H]



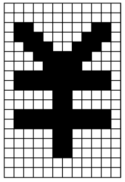
[07AH]



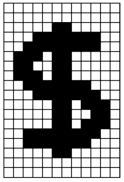
[07BH]



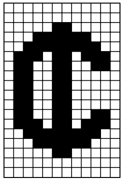
[07CH]



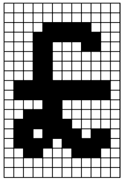
[07DH]



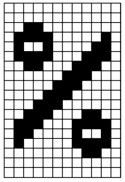
[07EH]



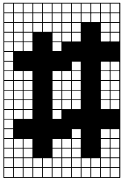
[07FH]



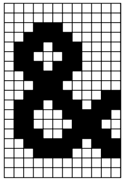
[080H]



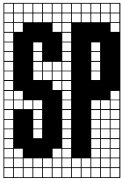
[081H]



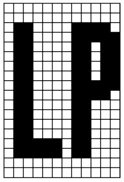
[082H]



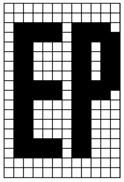
[083H]



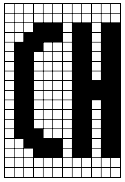
[084H]



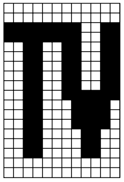
[085H]



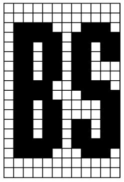
[086H]



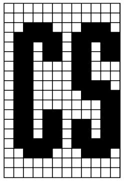
[087H]



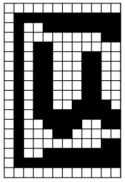
[088H]



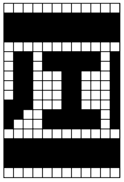
[089H]



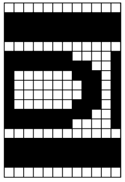
[08AH]



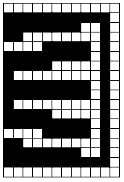
[08BH]



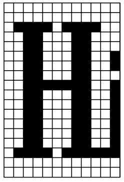
[08CH]



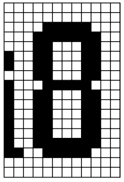
[08DH]



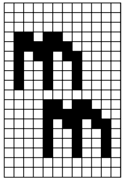
[08EH]



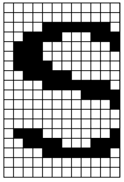
[08FH]



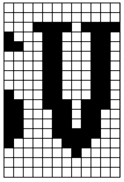
[090H]



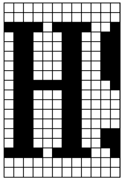
[091H]



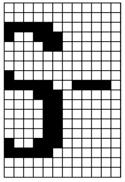
[092H]



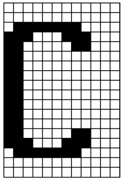
[093H]



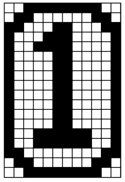
[094H]



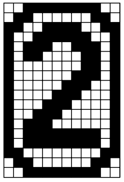
[095H]



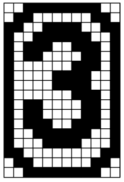
[096H]



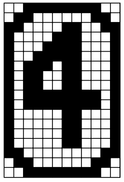
[097H]



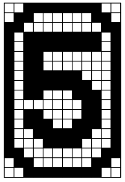
[098H]



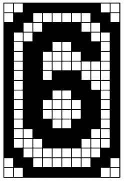
[099H]



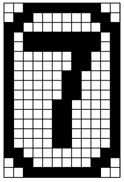
[09AH]



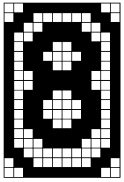
[09BH]



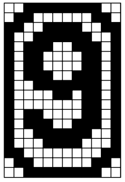
[09CH]



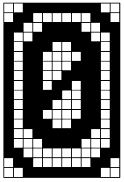
[09DH]

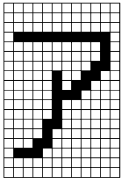
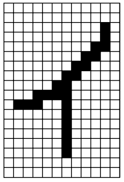
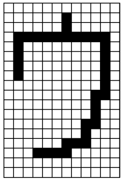
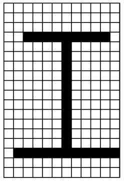
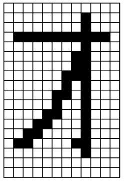
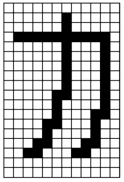
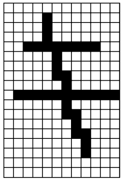
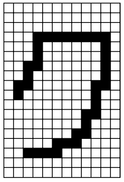
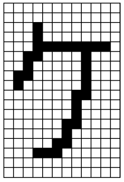
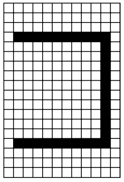


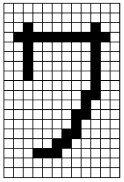
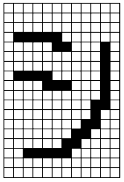
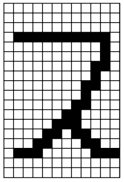
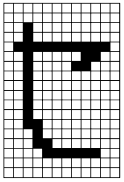
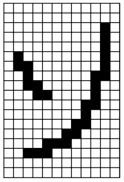
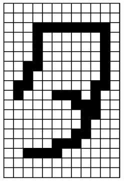
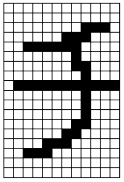
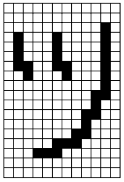
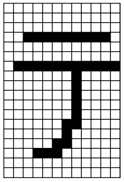
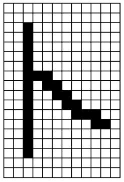
[09EH]

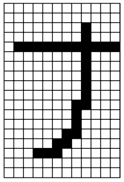
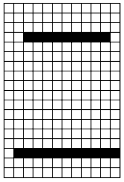
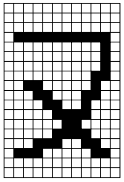
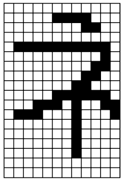
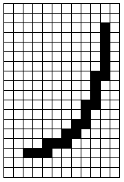
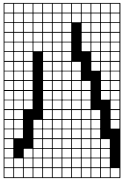
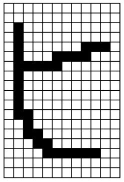
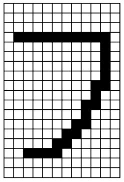
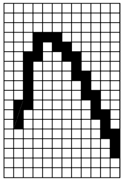
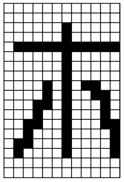


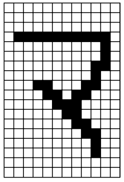
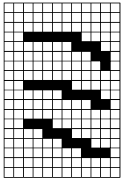
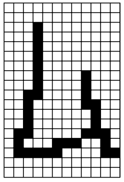
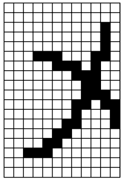
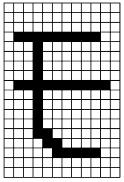
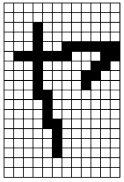
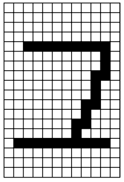
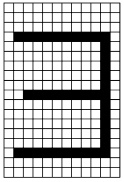
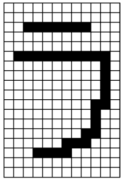
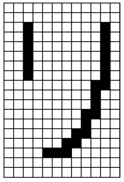
[09FH]

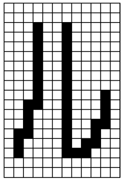
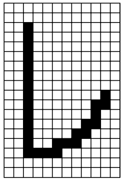
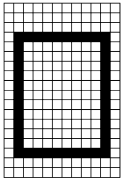
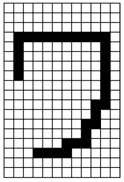
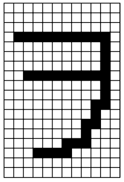
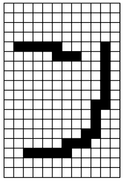
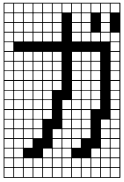
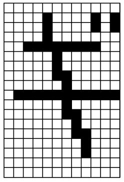
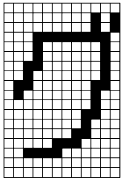
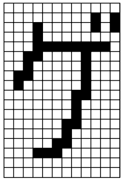


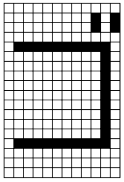
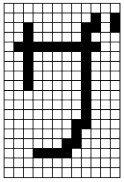
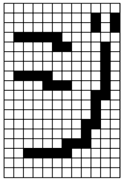
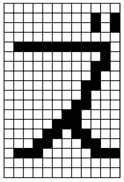
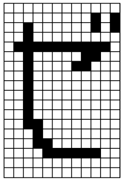
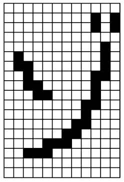
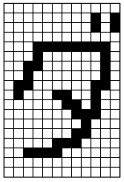
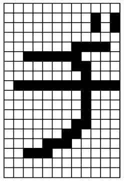
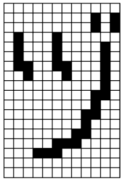
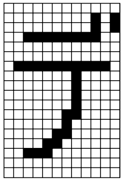
[0A0H]

[0A1H]

[0A2H]

[0A3H]

[0A4H]

[0A5H]

[0A6H]

[0A7H]

[0A8H]

[0A9H]


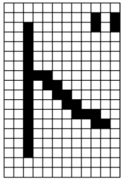
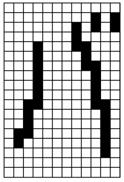
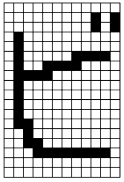
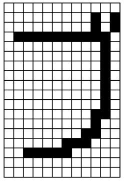
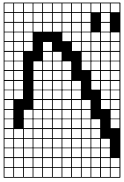
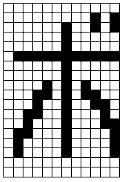
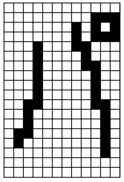
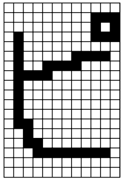
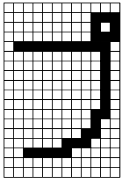
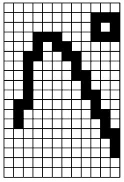
[0AAH]

[0ABH]

[0ACH]

[0ADH]

[0AEH]

[0AFH]

[0B0H]

[0B1H]

[0B2H]

[0B3H]


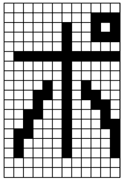
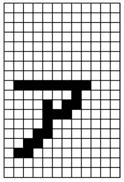
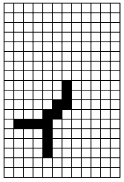
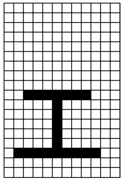
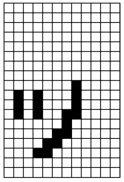
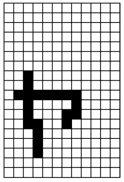
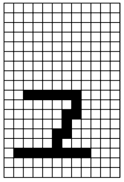
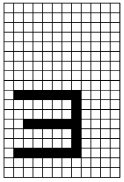
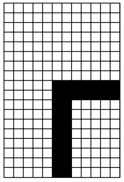
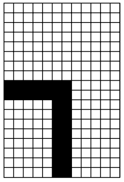
[0B4H]

[0B5H]

[0B6H]

[0B7H]

[0B8H]

[0B9H]

[0BAH]

[0BBH]

[0BCH]

[0BDH]


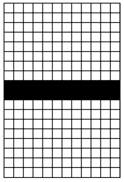
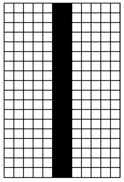
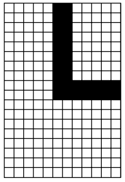
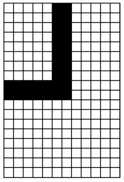
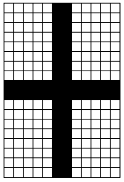
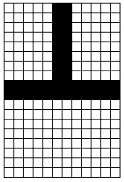
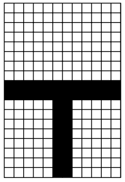
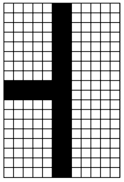
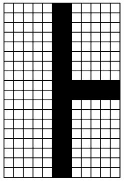
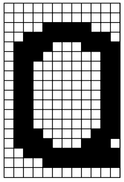
[0BEH]

[0BFH]

[0C0H]

[0C1H]

[0C2H]

[0C3H]

[0C4H]

[0C5H]

[0C6H]

[0C7H]


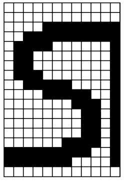
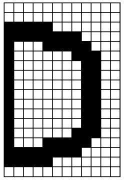
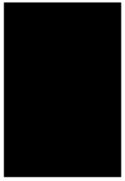
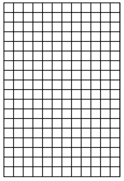
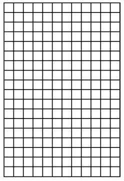
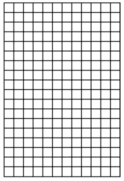
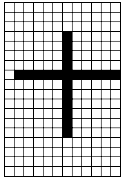
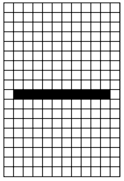
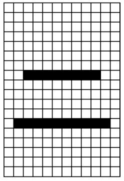
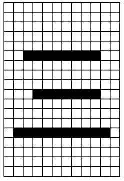
[0C8H]

[0C9H]

[0CAH]

[0CBH]

[0CCH]

[0CDH]

[0CEH]

[0CFH]

[0D0H]

[0D1H]


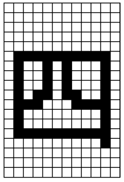
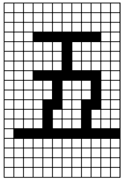
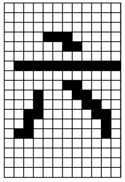
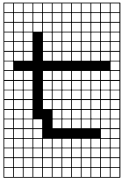
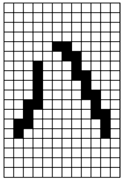
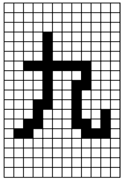
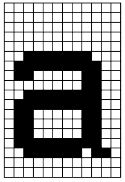
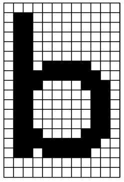
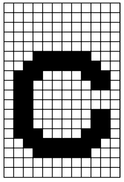
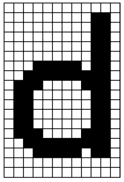
[0D2H]

[0D3H]

[0D4H]

[0D5H]

[0D6H]

[0D7H]

[0D8H]

[0D9H]

[0DAH]

[0DBH]


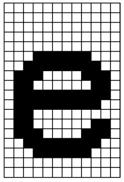
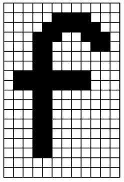
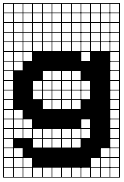
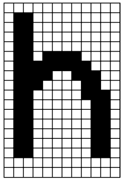
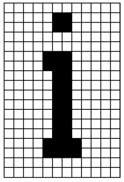
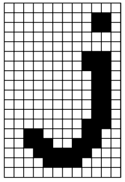
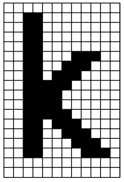
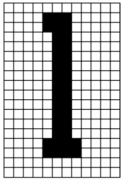
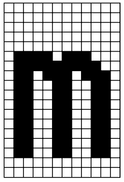
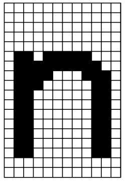
[0DCH]

[0DDH]

[0DEH]

[0DFH]

[0E0H]

[0E1H]

[0E2H]

[0E3H]

[0E4H]

[0E5H]


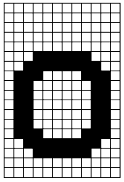
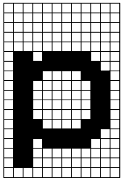
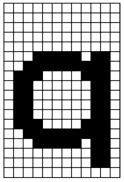
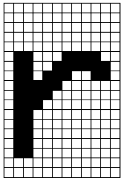
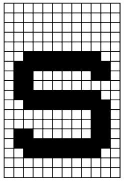
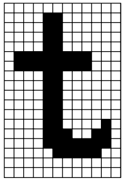
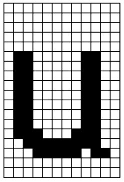
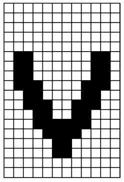
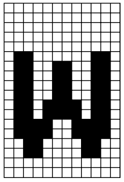
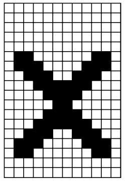
[0E6H]

[0E7H]

[0E8H]

[0E9H]

[0EAH]

[0EBH]

[0ECH]

[0EDH]

[0EEH]

[0EFH]


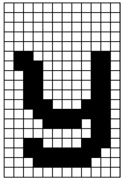
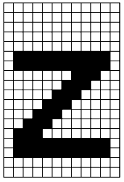
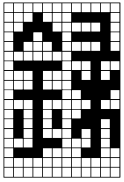
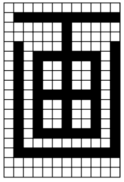
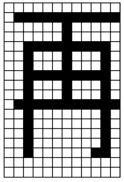
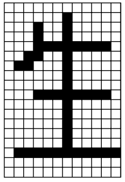
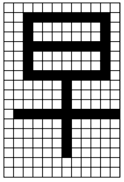
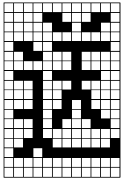
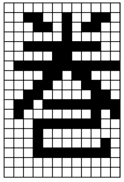
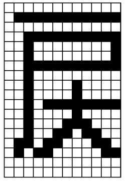
[0F0H]

[0F1H]

[0F2H]

[0F3H]

[0F4H]

[0F5H]

[0F6H]

[0F7H]

[0F8H]

[0F9H]


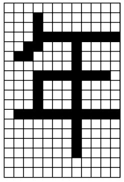
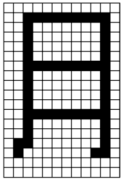
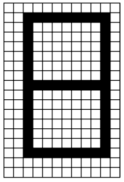
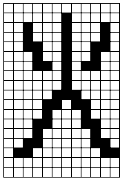
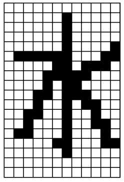
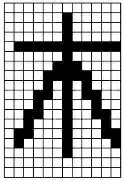
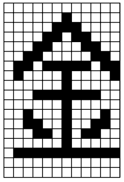
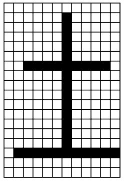
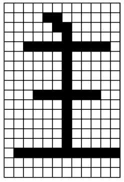
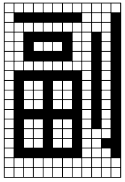
[0FAH]

[0FBH]

[0FCH]

[0FDH]Note 1

[0FEH]Note 2

[0FFH]Note 3

[100H]

[101H]

[102H]

[103H]


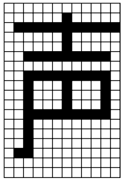
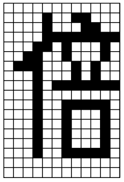
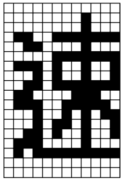
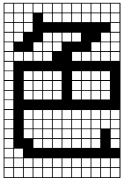
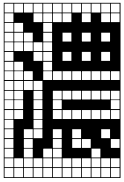
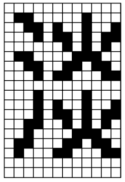
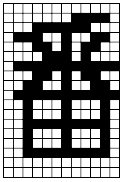
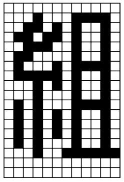
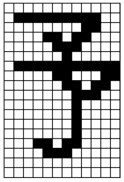
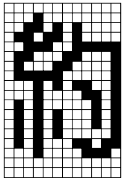
[104H]

[105H]

[106H]

[107H]

[108H]

[109H]

[10AH]

[10BH]

[10CH]

[10DH]


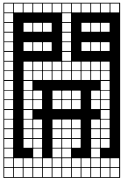
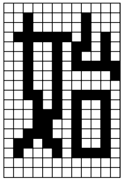
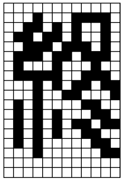
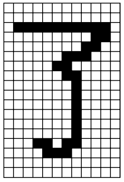
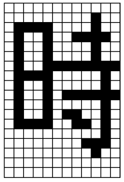
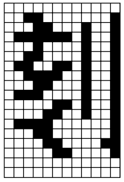
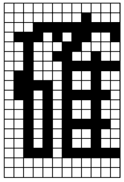
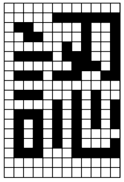
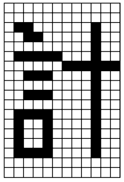
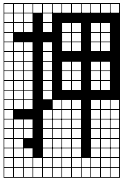
[10EH]

[10FH]

[110H]

[111H]

[112H]

[113H]

[114H]

[115H]

[116H]

[117H]


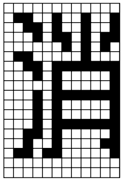
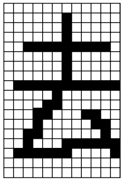
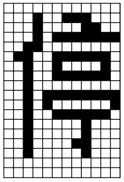
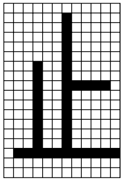
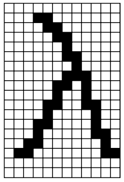
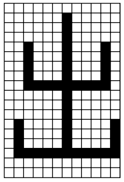
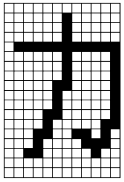
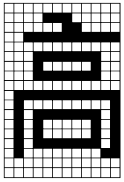
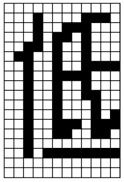
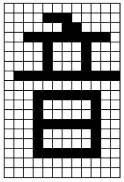
[118H]

[119H]

[11AH]

[11BH]

[11CH]

[11DH]

[11EH]

[11FH]

[120H]

[121H]


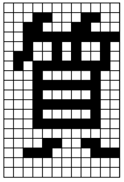
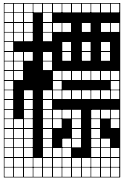
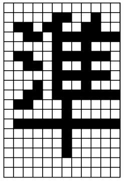
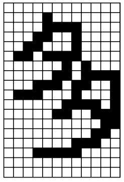
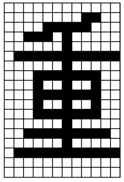
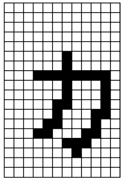
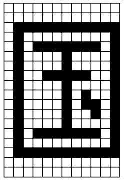
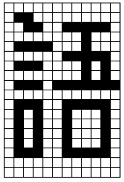
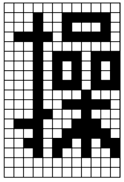
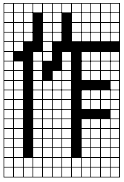
[122H]

[123H]

[124H]

[125H]

[126H]

[127H]

[128H]

[129H]

[12AH]

[12BH]


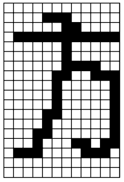
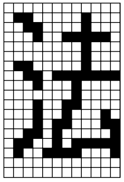
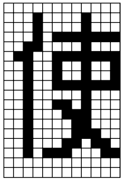
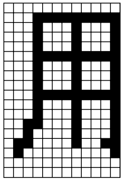
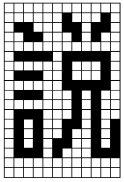
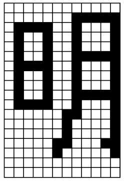
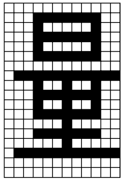
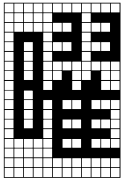
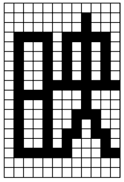
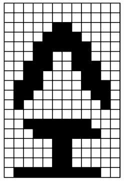
[12CH]

[12DH]

[12EH]

[12FH]

[130H]

[131H]

[132H]

[133H]

[134H]

[135H]


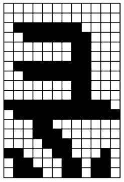
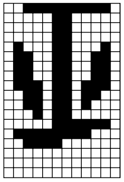
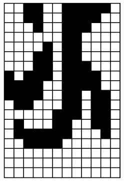
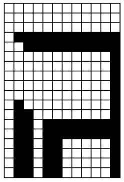
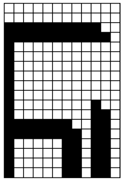
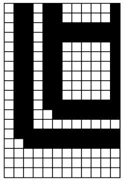
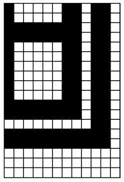
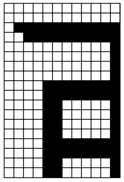
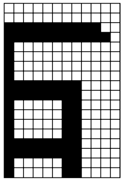
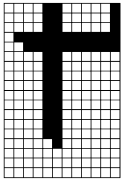
[136H]

[137H]

[138H]

[139H]

[13AH]

[13BH]

[13CH]

[13DH]

[13EH]

[13FH]


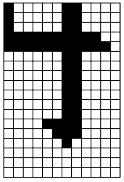
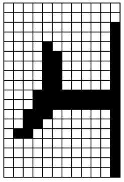
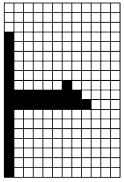
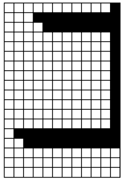
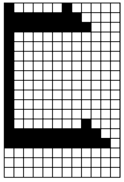
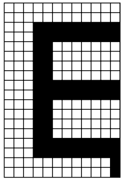
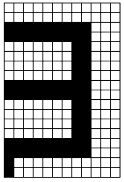
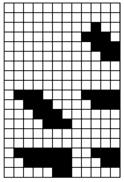
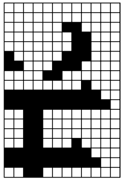
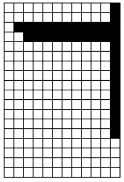
[140H]

[141H]

[142H]

[143H]

[144H]

[145H]

[146H]

[147H]

[148H]

[149H]


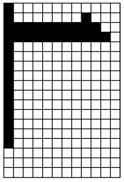
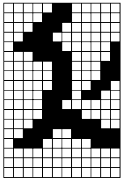
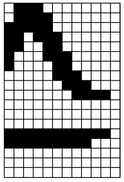
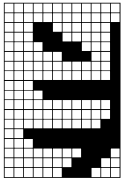
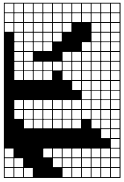
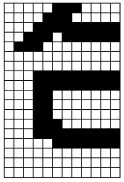
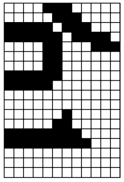
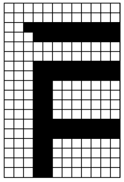
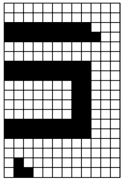
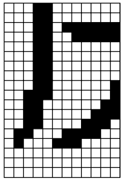
[14AH]

[14BH]

[14CH]

[14DH]

[14EH]

[14FH]

[150H]

[151H]

[152H]

[153H]


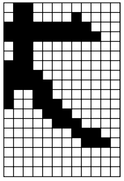
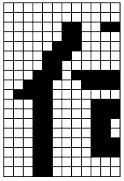
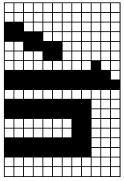
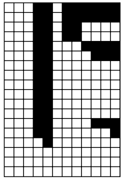
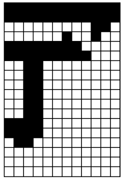
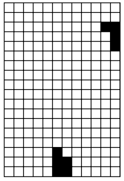
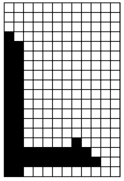
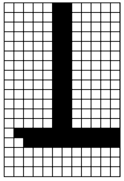
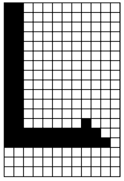
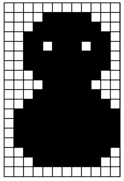
[154H]

[155H]

[156H]

[157H]

[158H]

[159H]

[15AH]

[15BH]

[15CH]

[15DH]


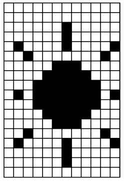
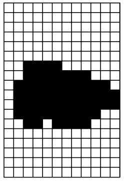
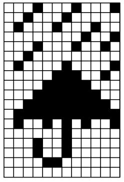
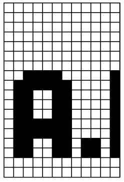
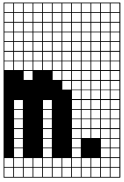
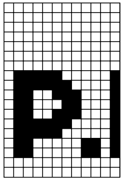
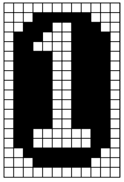
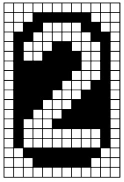
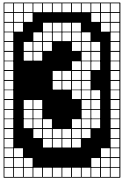
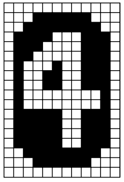
[15EH]

[15FH]

[160H]

[161H]

[162H]

[163H]

[164H]

[165H]

[166H]

[167H]


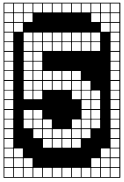
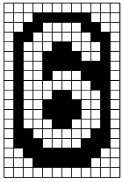
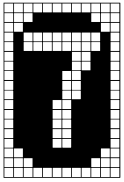
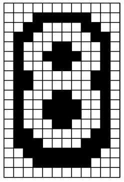
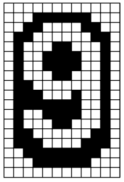
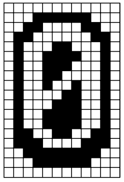
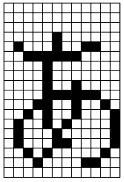
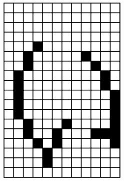
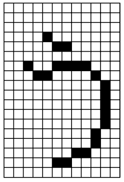
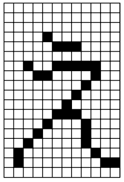
[168H]

[169H]

[16AH]

[16BH]

[16CH]

[16DH]

[16EH]

[16FH]

[170H]

[171H]


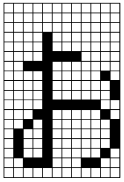
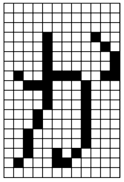
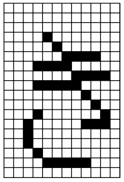
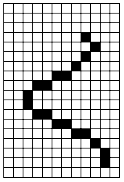
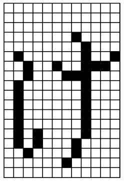
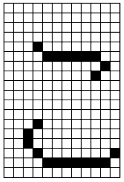
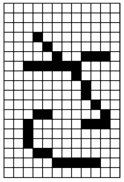
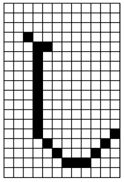
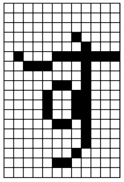
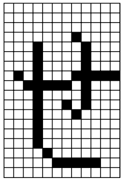
[172H]

[173H]

[174H]

[175H]

[176H]

[177H]

[178H]

[179H]

[17AH]

[17BH]


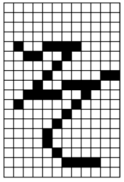
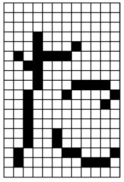
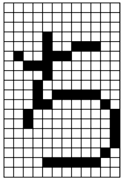
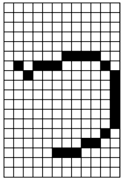
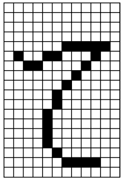
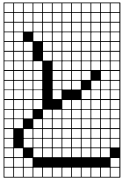
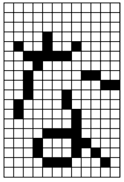
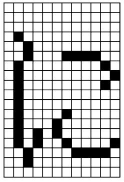
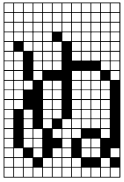
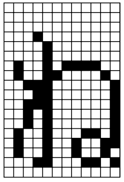
[17CH]

[17DH]

[17EH]

[17FH]

[180H]

[181H]

[182H]

[183H]

[184H]

[185H]


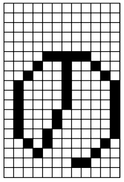
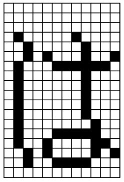
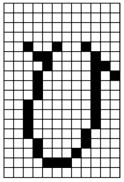
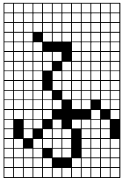
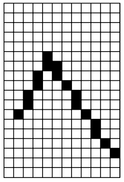
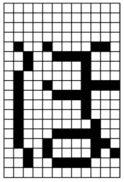
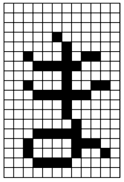
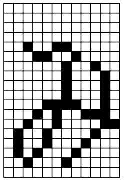
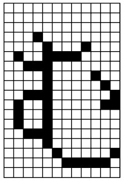
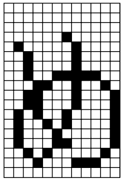
[186H]

[187H]

[188H]

[189H]

[18AH]

[18BH]

[18CH]

[18DH]

[18EH]

[18FH]


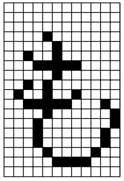
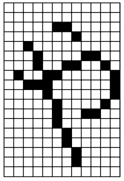
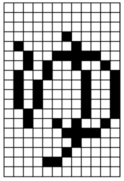
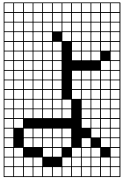
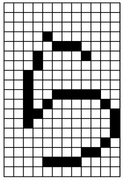
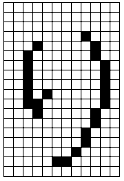
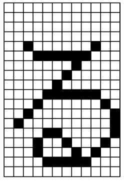
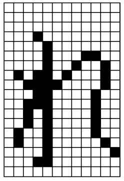
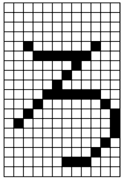
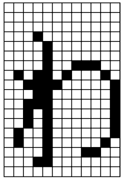
[190H]

[191H]

[192H]

[193H]

[194H]

[195H]

[196H]

[197H]

[198H]

[199H]


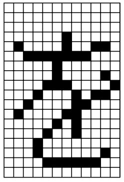
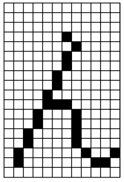
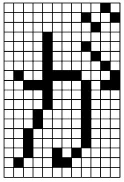
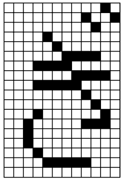
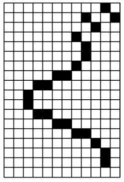
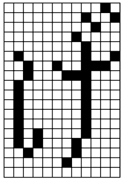
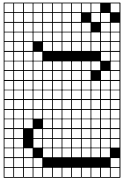
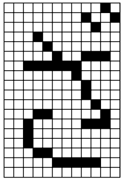
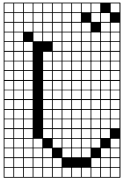
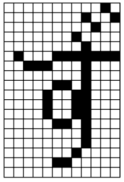
[19AH]

[19BH]

[19CH]

[19DH]

[19EH]

[19FH]

[1A0H]

[1A1H]

[1A2H]

[1A3H]


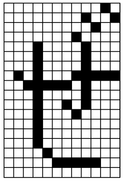
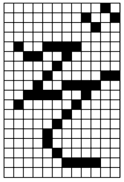
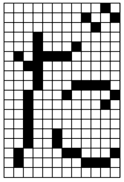
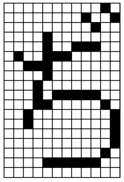
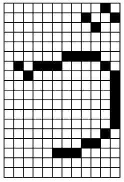
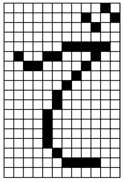
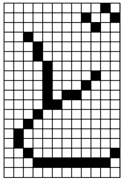
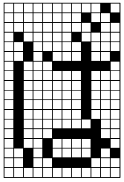
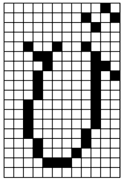
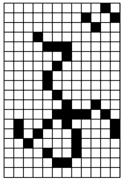
[1A4H]

[1A5H]

[1A6H]

[1A7H]

[1A8H]

[1A9H]

[1AAH]

[1ABH]

[1ACH]

[1ADH]


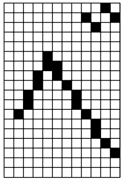
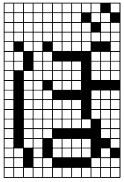
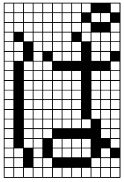
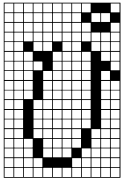
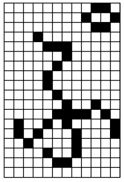
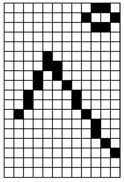
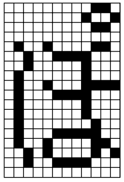
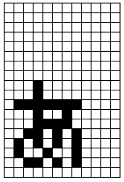
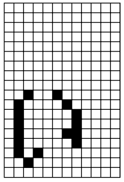
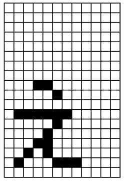
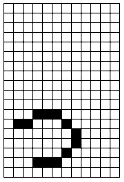
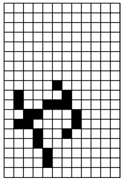
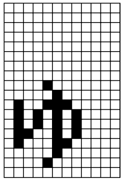
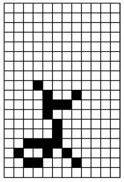
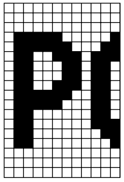
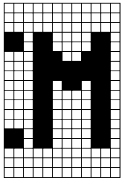
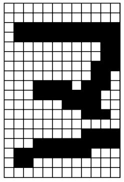
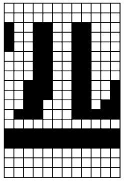
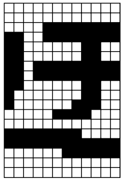
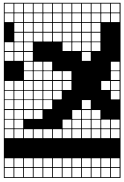
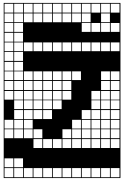
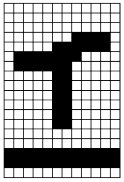
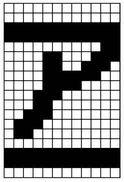
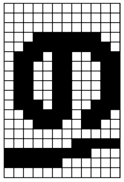
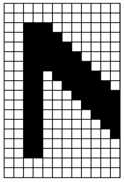
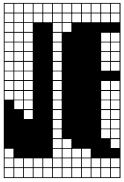
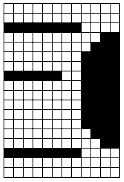
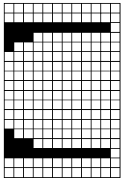
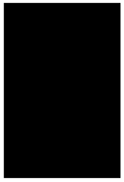
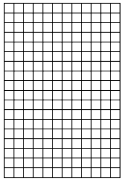
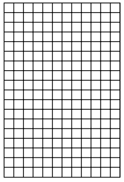
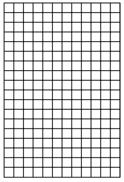
[1AEH]

[1AFH]

[1B0H]

[1B1H]

[1B2H]

[1B3H]

[1B4H]

[1B5H]

[1B6H]

[1B7H]


[1B8H]

[1B9H]

[1BAH]

[1BBH]

[1BCH]

[1BDH]

[1BEH]

[1BFH]

[1C0H]

[1C1H]


[1C2H]

[1C3H]

[1C4H]

[1C5H]

[1C6H]

[1C7H]

[1C8H]

[1C9H]

[1CAH]

[1CBH]


[1CCH]

[1CDH]

[1CEH]

[1CFH]

[1D0H]

[1D1H]

[1D2H]

[1D3H]

[1D4H]

[1D5H]


[1D6H]

[1D7H]

[1D8H]

[1D9H]

[1DAH]

[1DBH]

[1DCH]

[1DDH]

[1DEH]

[1DFH]


[1E0H]

[1E1H]

[1E2H]

[1E3H]

[1E4H]

[1E5H]

[1E6H]

[1E7H]

[1E8H]

[1E9H]

[1EAH]

[1EBH]

[1ECH]

[1EDH]

[1EEH]

[1EFH]

[1F0H]

[1F1H]

[1F2H]

[1F3H]

[1F4H]

[1F5H]

[1F6H]

[1F7H]

[1F8H]

[1F9H]

[1FAH]

[1FBH]

[1FCH]

[1FDH]Note 1

[1FEH]Note 2

[1FFH]Note 3


Notes **1.** Blank data

2. Display Off Data (character addresses are fixed)

3. 2-byte continuous input end code (character addresses are fixed)

Remark 0xxH indicates character address of the low-order (0) bank, and 1xxH indicates that of the high-order (1) bank.

6. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage V_{DD}	V_{DD}		–0.5 to + 4.6	V
Input pin voltageV_{IN}	V_{IN}		–0.3 to V_{DD} + 0.3	V
Output pin voltage	V_{OUT}		–0.3 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–20 to +75	°C
Storage temperature	T_{stg}		–40 to +125	°C
Power dissipation	P_D	T_A = +75 °C	270	mW
Output current	I_O		±5	mA

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Range

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage range	V_{DD}	Dot clock: LC oscillation	2.7		3.6	V
		Dot clock: External input	2.0		3.6	
Oscillation frequency (LC oscillation)	f_{OSC}	V_{DD} = 2.7 to 3.6 V	6.0		8.0	MHz
External dot clock frequency (×1 frequency mode)	f_{OSC}	V_{DD} = 2.0 to 3.6 V	4.0		8.0	MHz
External dot clock frequency (×2 frequency mode)	f_{OSC2}	V_{DD} = 2.0 to 3.6 V	8.0		16.0	MHz
Operating ambient temperature	T_A		–20		+75	°C

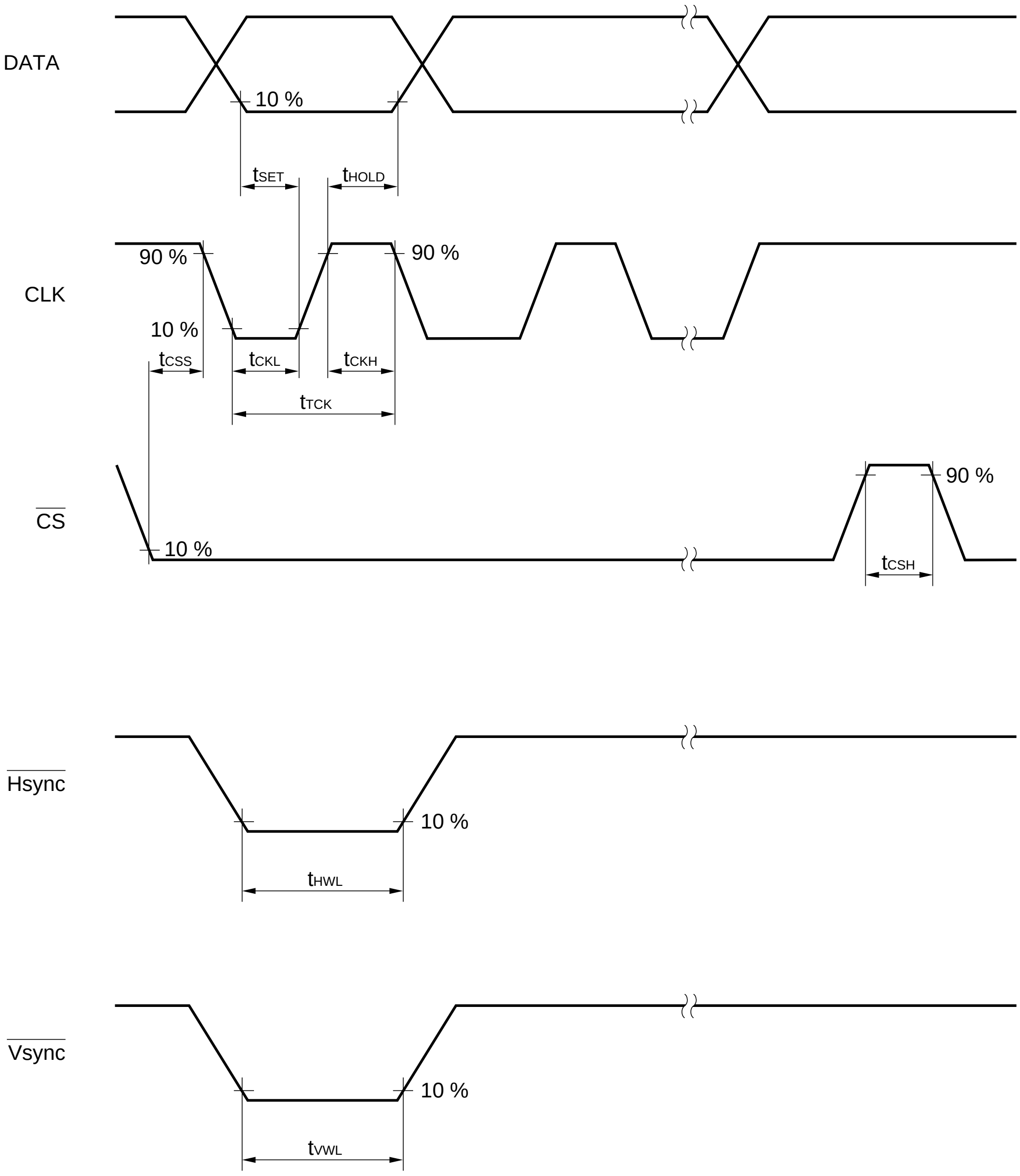
Electrical Characteristics (T_A = –20 to + 75 °C, unless otherwise specified, V_{DD} = 2.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage range	V_{DD}		2.0	3.3	3.6	V
Current consumption 1	I_{DD}	f_{OSC} = 8.0 MHz, V_{DD} = 3.3 V			5	mA
Current consumption 2	I_{DD}	f_{OSC} = 8.0 MHz, V_{DD} = 2.0 V			4	mA
Control input high-level voltage	V_{CIH}		0.7 V_{DD}			V
Control input low-level voltage	V_{CIL}				0.3 V_{DD}	V
Signal output high-level voltage	V_{OSH}	I_{OSH} = –1.0 mA (V_{DD} = 3.3 V)	0.9 V_{DD}			V
Signal output low-level voltage	V_{OSL}	I_{OSL} = 1.0 mA (V_{DD} = 3.3 V)			0.1 V_{DD}	V

Remark Control input : DATA, CLK, $\overline{\text{CS}}$, $\overline{\text{PCL}}$, $\overline{\text{Hsync}}$, $\overline{\text{Vsync}}$, CMDCT
Signal output : V_R, V_G, V_B, V_{C1}, V_{C2}, V_{BLK}, BLK1, BLK2 (R_{BLK}, G_{BLK}, B_{BLK})
( ): Set by initial status setting command

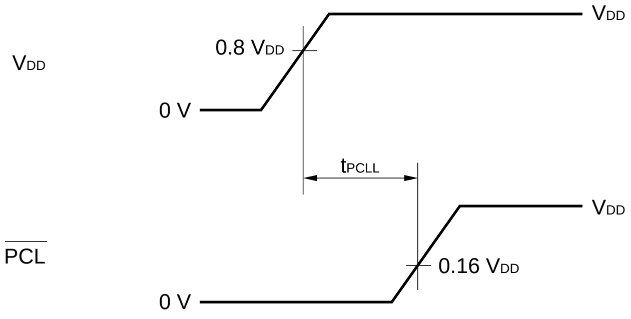
Recommended Operation Timing (T_A = –20 to +75 °C, V_{DD} = 2.0 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Setup time	t_{SET}		200			ns
Hold time	t_{HOLD}		200			ns
Minimum clock low-level width	t_{CKL}		300			ns
Minimum clock high-level width	t_{CKH}		300			ns
Clock cycle	t_{TCK}		700			ns
$\overline{CS}$ setup time	t_{CSS}		300			ns
$\overline{CS}$ hold time	t_{CSH}		400			ns
Minimum $\overline{Hsync}$ low-level width	t_{HWL}		4			μs
Minimum $\overline{Vsync}$ low-level width	t_{VWL}		8			μs


DATA
10 %
tSET
tHOLD
90 %
CLK
10 %
90 %
tCSS
tCKL
tCKH
tTCK
CS
10 %
90 %
tCSH
Hsync
10 %
tHWL
Vsync
10 %
tVWL

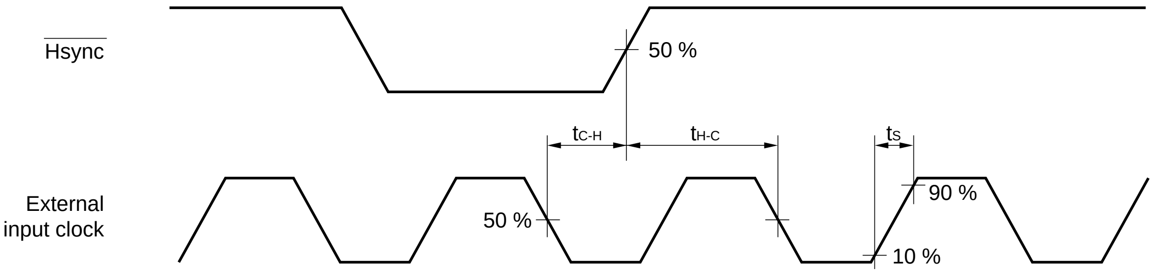
Power-ON Clear Specifications

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{PCL}}$ pin low retention period	t_{PCLL}		10			μs


VDD
VDD
0.8 VDD
0 V
tPCLL
VDD
$\overline{\text{PCL}}$
0.16 VDD
0 V

External clock input

External clock input timing (valid when selected by initial status setting command)


$\overline{\text{Hsync}}$
50 %
t_{C-H}
t_{H-C}
t_S
External input clock
50 %
90 %
10 %

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
External clock falling → sync signal rise time	t_{C-H}		20			ns
Sync signal rise time → external clock falling	t_{H-C}		20			ns
t_S (rising slew rate)	t_S				**Note**	ns

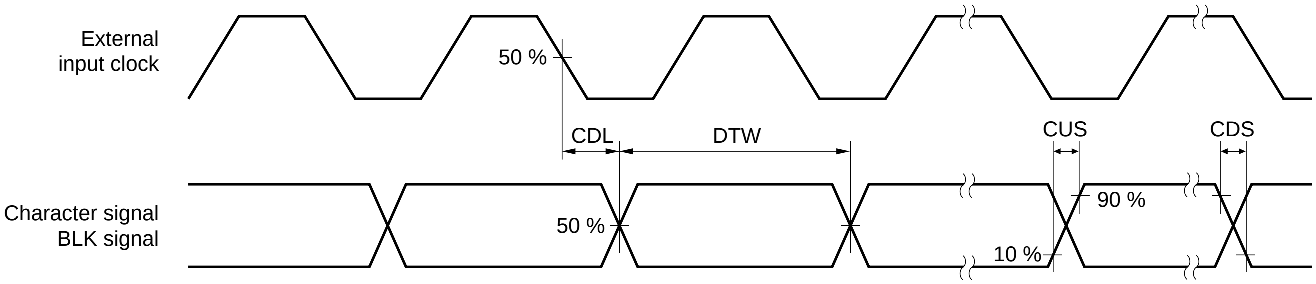
Note 10% of cycle of external clock

Example Where the external clock frequency is 8 MHz
Clock cycle = 125 ns
t_S = 12.5 ns (MAX.) because 125 ns × 10% (MAX.)

Remarks
1. Always keep the phase relation between the rising of $\overline{\text{Hsync}}$ and external input clock.
2. Make sure that noise of greater than 100 ns is not superimposed on the input of $\overline{\text{Hsync}}$.
3. Keep the OSC_{OUT} pin open when the external clock is input.

Character and BLK Signal Output

Characters and BLK signal are output in synchronization with the falling of the dot clock.



Output Timing (T_A = –20 to +75 °C, output load capacitance = 10 pF, pins: V_R, V_G, V_B, V_{BLK}, V_{C1}, BLK1, V_{C2}, BLK2, (R_{BLK}, G_{BLK}, B_{BLK}))

( ): Set by initial status setting command

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Character/BLK signal output delay	CDL	V_{DD} = 3.0 V	5	10	30	ns
Character/BLK signal output delay	CDL	V_{DD} = 2.0 V	10	15	50	ns
Character/BLK signal rise time	CUS	V_{DD} = 3.0 V	1		10	ns
Character/BLK signal rise time	CUS	V_{DD} = 2.0 V	1		25	ns
Character/BLK signal falling	CDS	V_{DD} = 3.0 V	1		10	ns
Character/BLK signal falling	CDS	V_{DD} = 2.0 V	1		25	ns
Minimum size of 1 dot width	DTW	V_{DD} = 3.0 V, External input clock ×1 frequency mode	$(1/f_{OSC})–5$		$(1/f_{OSC})+5$	ns
		V_{DD} = 3.0 V, External input clock ×2 frequency mode	$(2/f_{OSC2})–5$		$(2/f_{OSC2})+5$	ns
Minimum size of 1 dot width	DTW	V_{DD} = 2.0 V, External input clock ×1 frequency mode	$(1/f_{OSC})–5$		$(1/f_{OSC})+5$	ns
		V_{DD} = 2.0 V, External input clock ×2 frequency mode	$(2/f_{OSC2})–5$		$(2/f_{OSC2})+5$	ns

Remark f_{OSC} : External input clock frequency (×1 frequency mode) (MHz)
f_{OSC2}: External input clock frequency (×2 frequency mode) (MHz)

Command Successive Input Permissible Time

Successively input commands under the following timing conditions:

(T_A = –20 to +75 °C, V_{DD} = 2.0 to 3.6 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Command successive input enable time	T1	Common to all commands			2.0			μs
	T2	Video RAM write command	Display ON	LC oscillation	**Note 1**			μs
				External clock	**Note 2**			
			Display OFF		**Note 3**			μs

Notes 1. (1) $2.0 + (14/f_{OSC}) \times S1 + 19/f_{OSC} + (1/f_{OSC}) \times S2 + t_{HWL}$

(2) $2.0 + (19/f_{OSC}) \times S$

S : Character size (×1 (MIN.) to ×4)
S1 : Horizontal character size before $\overline{\text{Hsync}}$
S2 : Horizontal character size before $\overline{\text{Hsync}}$
t_{HWL} : $\overline{\text{Hsync}}$ width

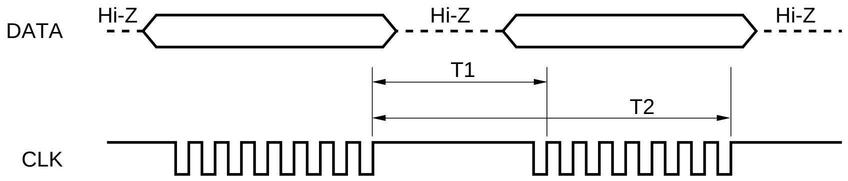
Because the clock is not supplied to the internal circuitry during LC oscillation and $\overline{\text{Hsync}}$, if $\overline{\text{Hsync}}$ is input while the video RAM write command is executed, the width directly influences the execution time (1). If $\overline{\text{Hsync}}$ is not input in the middle, the execution time is as (2) above.
Whether (1) or (2) is longer in time depending on the horizontal character size before and after $\overline{\text{Hsync}}$ and $\overline{\text{Hsync}}$ width is not known. The longer time is the permissible minimum time.

2. $2.0 + 31/f_{OSC}$ or $2.0 + 62/f_{OSC2}$ (S = 1)
$2.0 + (19/f_{OSC}) \times S$ or $2.0 + (38/f_{OSC2}) \times S$ (S = 2, 3, 4)

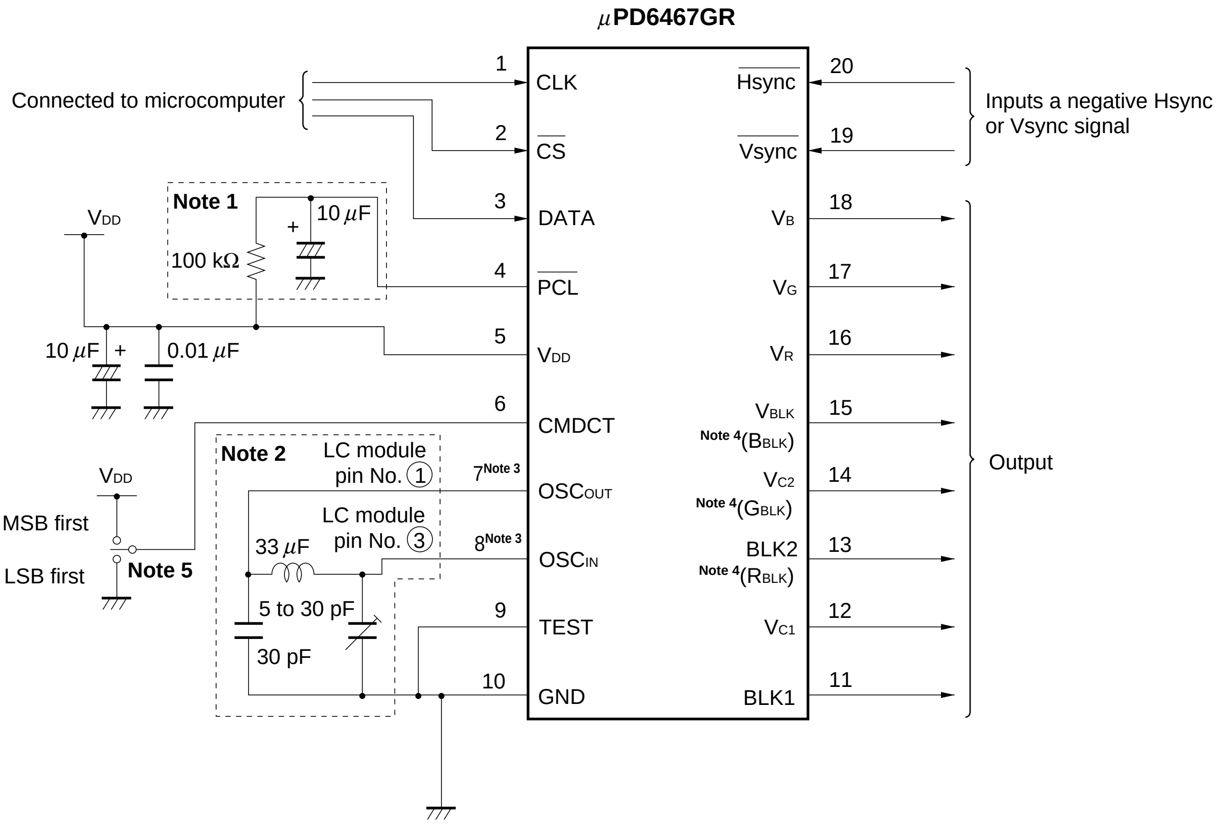
3. $2.0 + 19/f_{OSC}$ or $2.0 + 38/f_{OSC2}$

Remark f_{OSC} : LC oscillation frequency or external input clock frequency (when ×1 frequency mode is selected) (MHz)
f_{OSC2} : External input clock frequency (when ×2 frequency mode is selected) (MHz)

The restriction of T2 is not applied to the commands other than the video RAM write command if the clock cycle for control satisfies the specifications.



7. APPLICATION CIRCUIT EXAMPLE


μPD6467GR
Connected to microcomputer
1 CLK
2 CS
3 DATA
4 PCL
5 VDD
6 CMDCT
7Note 3 OSCOUT
8Note 3 OSCIN
9 TEST
10 GND
20 Hsync
19 Vsync
18 VB
17 VG
16 VR
15 VBLK Note 4(BBLK)
14 VC2 Note 4(GBLK)
13 BLK2 Note 4(RBLK)
12 VC1
11 BLK1
Inputs a negative Hsync or Vsync signal
Output
Note 1
100 kΩ
10 μF
VDD
10 μF
0.01 μF
Note 2
LC module pin No. ①
LC module pin No. ③
33 μF
5 to 30 pF
30 pF
VDD
MSB first
LSB first
Note 5

Notes 1. CR constant must be satisfied with Power-ON Clear Specification (refer to **6. ELECTRICAL CHARACTERISTICS**).

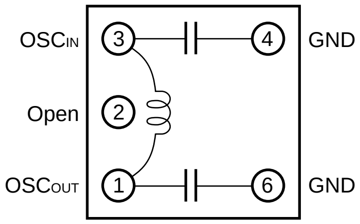
2. This circuit can reduce the number of external components and facilitates the adjustment of oscillation frequency, using LC module (part number: Q285NCIS-11181, manufactured by Toko, Inc., pin connection: Figure A.)

3. Connect these pins as follows when inputting external clock:
OSC$_{IN}$ pin: external clock input, OSC$_{OUT}$ pin: open

4. Signals in ( ) are set by using an initial status setting command (RGB + RGB compatible blanking).

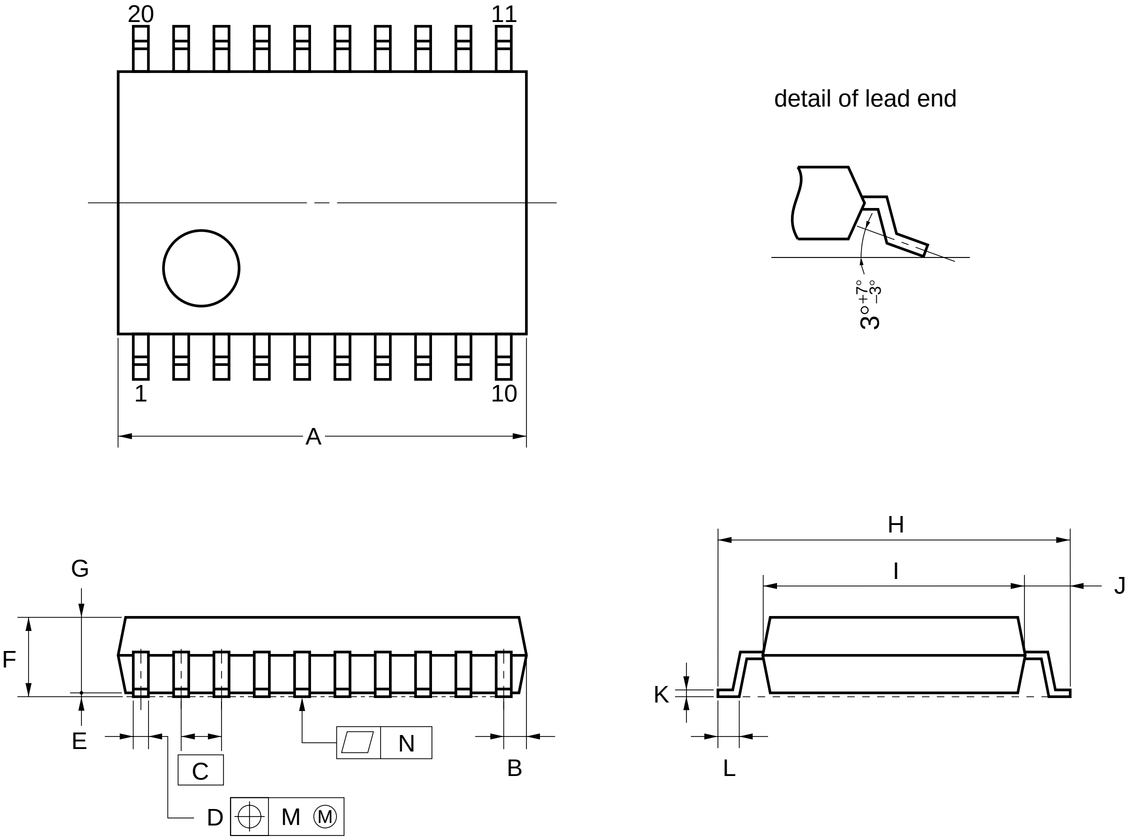
5. When this connection is open, LSB first is selected.

Figure A. Q285NCIS-11181 Pin Connections (Bottom View)


OSCIN ③
④ GND
Open ②
OSCOUT ①
⑥ GND

8. PACKAGE DRAWING

20 PIN PLASTIC SHRINK SOP (225 mil)


20
11
1
10
A
detail of lead end
3°+7° −3°
G
F
E
C
D
M
M
N
B
H
I
J
K
L

NOTE
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	7.00 MAX.	0.276 MAX.
B	0.575 MAX.	0.023 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	$0.22^{+0.10}_{-0.05}$	$0.009^{+0.004}_{-0.002}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.5±0.1	0.059±0.004
H	6.4±0.2	0.252±0.008
I	4.4±0.1	0.173±0.004
J	1.0±0.2	0.039±0.008
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	0.020±0.008
M	0.10	0.004
N	0.15	0.006

9. RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface mount devices

μPD6467GR-xxx: 20-pin plastic shrink SOP (225 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution **Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.**

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated “quality assurance program“ for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
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