



Description

The μPD7003 is a high speed, high performance, low power, 8-bit analog-to-digital Converter designed to be easily interfaced to the 8080 and 8086, 8- and 16-bit microprocessors. Using the parallel conversion technique, the μPD7003 features a conversion speed of 4 μs and eliminates the need of sample and hold circuits in most applications. The μPD7003 is also capable of running under DMA control using a DMA controller such as the μPD8257. Available in a 24-pin ceramic/plastic DIP, the μPD7003 is the ideal converter for high speed 8-bit designs.

Features

- High speed conversion (250 k samples/sec. max.)
- Input consists of 255/1 matched autozeroed comparators
- No missing codes over temperature range
- Linearity ±1.25 LSB max.
- Three-state outputs
- Overrange output
- Operates from single +5 V supply
- Low power consumption (50 mW)

Ordering Information

| Part Number | Package | Operating Temperature Range |
|-------------|-------------|-----------------------------|
| μPD7003C | Plastic DIP | -20°C to +70°C |

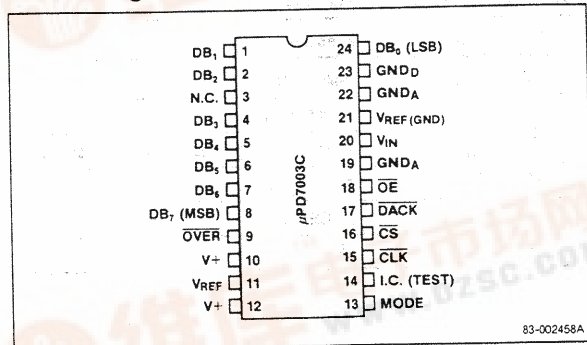
Absolute Maximum Ratings

T_A = 25°C

| | |
|-----------------------|-------------------|
| Operating Temperature | -20 to +70°C |
| Storage Temperature | -65 to +125°C |
| All Input Voltages | -0.3 to V+ +0.3 V |
| Power Supply | -0.3 to +7 V |
| Power Dissipation | 300 mW |
| Analog GND Voltage | ±0.3 V |

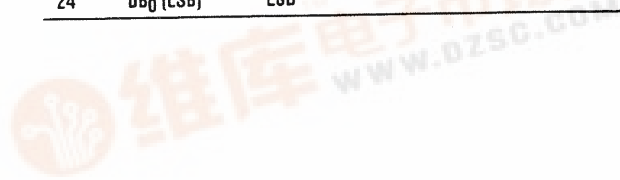
Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

| Pin | Name | Function |
|-----|-----------------------|---|
| 1 | DB ₁ | 7th bit output |
| 2 | DB ₂ | 6th bit output |
| 3 | NC | Non connection |
| 4 | DB ₃ | 5th bit output |
| 5 | DB ₄ | 4th bit output |
| 6 | DB ₅ | 3th bit output |
| 7 | DB ₆ | 2th bit output |
| 8 | DB ₇ | MSB output |
| 9 | OVER | Ovrerrange output |
| 10 | V+ | Power supply (+5 V) |
| 11 | VREF | Reference voltage input (positive) |
| 12 | V+ | Power supply (+5 V) |
| 13 | MODE | MODE control (note 1) |
| 14 | TEST | Low: Device test (used for inspecting the device) High: Conversion |
| 15 | CLK | Low: Previous data output High: Quantizing |
| 16 | CS | Chip select |
| 17 | DACK | DMA Acknowledge |
| 18 | OE | Low: Data output High: High impedance |
| 19 | AGND | Analog ground |
| 20 | V _{IN} | Voltage input |
| 21 | VREF(GND) | GND for VREF |
| 22 | AGND | Analog ground |
| 23 | GND | Digital ground |
| 24 | DB ₀ (LSB) | LSB |



Pin Identification (Cont.)

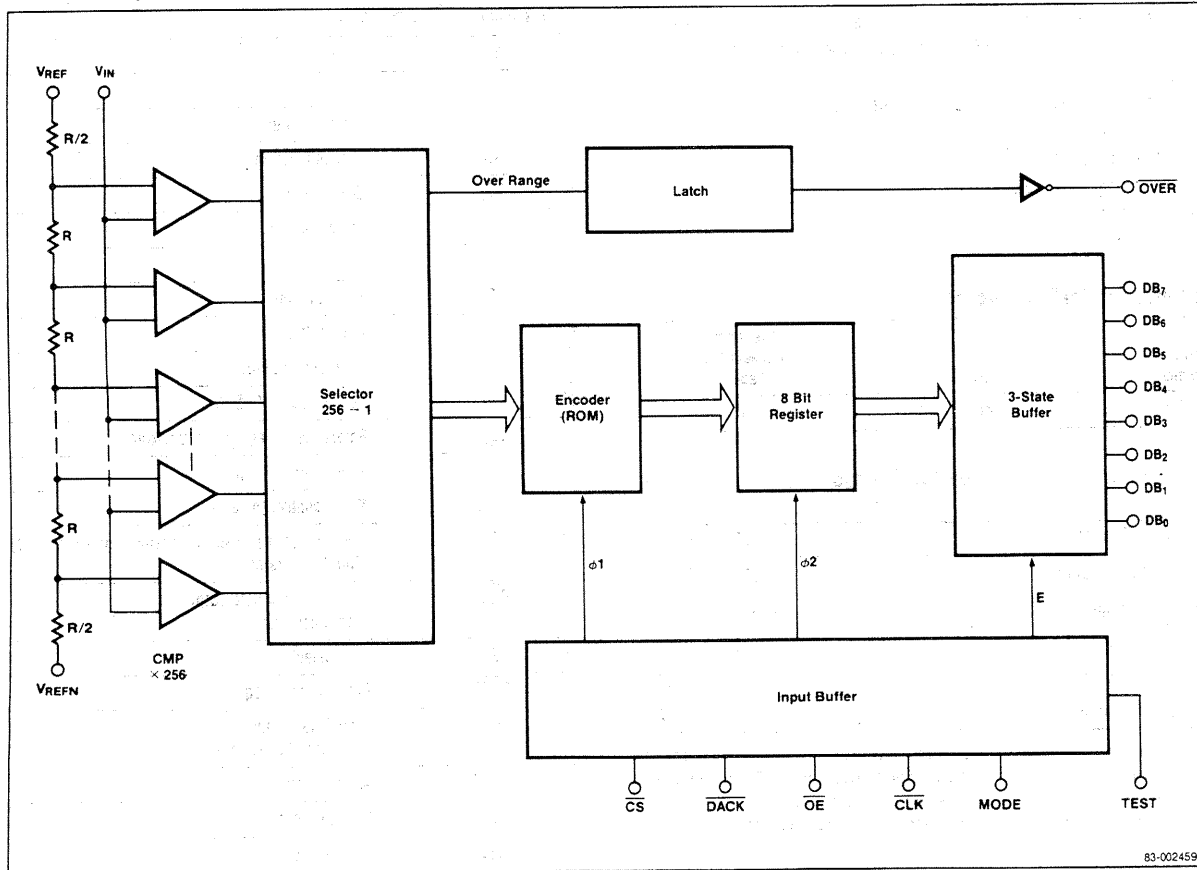
| Pin | Name | Function |
|-----|-------------------|---|
| 19 | GND _A | Analog ground |
| 20 | V _{SIN} | Analog input |
| 21 | V _{REFN} | Reference voltage input (negative) (Note 2) |
| 22 | GND _A | Analog ground |
| 23 | GND _D | Digital Ground |
| 24 | DB0 | LSB output |

Notes: 1.

| Mode | Inputs | |
|------|--------|----------------------------------|
| | OE | 8-Bit Register |
| 1 | 1 | Data refreshed with every CONV ! |
| | 0 | |
| 0 | 1 | |
| | 0 | No change |

2. Tie to the analog ground unless external zero adjustment required.

Block Diagram



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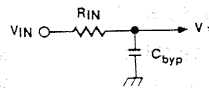
DC Characteristics

$T_A = +25^\circ\text{C}$, $V_+ = V_{REF} = 5.0 \pm 0.25\text{ V}$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|--------------------------------|-----------|--------|------|------|---------------|--|
| | | Min. | Typ. | Max. | | |
| Power Supply Current | I_{CC} | | 6.0 | 18.0 | mA | $t_{CY} = 4.0\ \mu\text{s}$, $t_{WLC} = 2.0\ \mu\text{s}$ Note 1 |
| High Level Output Voltage | V_{OH} | 2.8 | | | V | $I_O = -2.0\ \text{mA}$ |
| Low Level Output Voltage | V_{OL} | | | 0.4 | V | $I_O = -1.0\ \text{mA}$ |
| Digital Input Leakage Current | I_{ILK} | | 1 | 10 | μA | $0\text{ V} \leq V_{IN} \leq V_+$ |
| Digital Output Leakage Current | I_{OLK} | | 1 | 10 | μA | $0\text{ V} \leq V_O \leq V_+$ |
| Reference Input Current | I_{REF} | 1.19 | 1.79 | 3.57 | mA | $\overline{CLK} = \text{H or L}$ Note 1 |
| Analog Input Resistance | R_{IN} | 1 | 35 | | k Ω | $V_{EN} = 2.5\ \text{V}$, $t_{CY} = 4\ \mu\text{s}$, $t_{WLC} = 2\ \mu\text{s}$ Note 2 |
| Reference Input Capacitance | C_{REF} | | 100 | | pF | $f_{clk} = 1\ \text{MHz}$; unmeasured pins returned to Ground |
| Analog Input Capacitance | C_{IN} | | 100 | | pF | $f_{clk} = 1\ \text{MHz}$; unmeasured pins returned to Ground |
| Power Dissipation | P_D | | | 50 | mW | $t_{CY} = 4.0\ \mu\text{s}$, $t_{WLC} = 2.0\ \mu\text{s}$ |

Notes: 1. This means DC current. Tie the bypass capacitors (electrolytic capacitor $\geq 10\ \mu\text{F}$, ceramic capacitor $\approx 0.01\ \mu\text{F}$) to V_+ and V_{REF} pins, in order to absorb rush current ($\approx 10\ \text{mA}$).

2. DC input equivalent circuit is shown below.



Tie the bypass capacitor ($> 0.01\ \mu\text{F}$) to the analog input pin. 3 mA peak current flows into this pin.

AC Characteristics

$T_A = 25 \pm 2^\circ\text{C}$; $V_+ = 5.0\ \text{V}$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|------------------------|-------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Output Delay Time | t_{QEO} | 100 | 350 | | ns | $\overline{OE} \uparrow \rightarrow \text{DO}$ |
| | t_{QCO} | 150 | 450 | | ns | $\overline{CONV} \uparrow \rightarrow \text{DO}$ |
| | t_{QSO} | 100 | 350 | | ns | $\overline{CS} \uparrow \rightarrow \text{DO}$ |
| | t_{QCOVR} | 100 | 350 | | ns | $\overline{CONV} \uparrow \rightarrow \text{OVER}$ |
| Delay Time to Floating | t_{FEO} | 70 | 200 | | ns | $\overline{OE} \uparrow \rightarrow \text{DO}$ |
| | t_{FSO} | 150 | 450 | | ns | $\overline{CS} \uparrow \rightarrow \text{DO}$ |

Conversion Characteristics

$T_A = 25 \pm 2^\circ\text{C}$; $V_+ = V_{REF} = 5.0\ \text{V}$;
 $t_{CY} = 4.0\ \mu\text{s}$; $t_{WLC} = 2.0\ \mu\text{s}$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|--|--------|--------|------|------------|-----------------------|--|
| | | Min. | Typ. | Max. | | |
| Resolution | RES | 8 | 8 | 8 | Bits | -20°C to $+80^\circ\text{C}$ |
| Nonlinearity | NL | | | ± 1.25 | LSB | |
| Full Scale Error | | | | ± 1.00 | LSB | |
| Full Scale Error Temperature Coefficient | | | 20 | | ppm/ $^\circ\text{C}$ | |
| Zero Scale Error | | -0.75 | | +0.75 | LSB | |
| Zero Scale Error Temperature Coefficient | | | 20 | | ppm/ $^\circ\text{C}$ | |

Note: $\mu\text{PD7003C}$: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$.

Recommended Operating Conditions

T_A = 0°C to 70°C: μPD7003C,

T_A = -20°C to +80°C: μPD7003D

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|----------------------------------|-------------------|--------|------|---------|---------|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | V+ | 4.75 | 5.0 | 5.25 | V | |
| Reference Input Voltage | V _{REF} | 4.0 | V+ | V+ | V | |
| Analog Input Voltage | V _{IN} | -0.1 | | V+ +0.1 | V | |
| High Level Logic Input | V _{IH} | 2.4 | | V+ | V | |
| Low Level Logic Input | V _{IL} | -0.1 | | 0.8 | V | |
| Sampling Rate | | 10 | | 250k | times/s | |
| Conversion Cycle Time | t _{CY} | 4.0 | | 100 | μs | |
| CONV High Level Width | t _{WHC} | 2.0 | | | μs | |
| CONV Low Level Width | t _{WLC} | 2.0 | | | μs | |
| CONV Setup Time | t _{SCE} | 0 | | Note 1 | ns | $\overline{\text{CONV}} \downarrow \rightarrow \overline{\text{OE}} \downarrow$ |
| CS Setup Time | t _{SSE} | 100 | | | ns | $\overline{\text{CS}} \downarrow \rightarrow \overline{\text{OE}} \downarrow$ |
| CS Hold Time | t _{HES} | 0 | | | ns | $\overline{\text{OE}} \uparrow \rightarrow \overline{\text{CS}} \uparrow$ |
| OE Setup Time | t _{SEC} | 600 | | | ns | $\overline{\text{OE}} \downarrow \rightarrow \overline{\text{CONV}} \downarrow$ |
| OE Hold Time | t _{HCE} | 400 | | | ns | $\overline{\text{CONV}} \uparrow \rightarrow \overline{\text{OE}} \downarrow$ |
| OE Low Level Width | t _{WLE} | 400 | | Note 2 | ns | |
| Digital Input Rise and Fall Time | t _{r, f} | | | 50 | ns | |

- Notes: 1. t_{SCE} (ns) ≤ t_{CY} (ns) - t_{WLE} (ns) - 100 (ns).
 2. t_{WLE} (ns) ≤ t_{CY} (ns) - t_{SCE} (ns) - 100 (ns).

Converter Operation

Referring to the block diagram, the reference voltage is set externally to some desired level which references the individual internal components such that V_{REF} is divided equally by 256 resistors in a ladder/divider configuration. The applied voltage to V_{IN} is then compared to the reference level and the individual samples are sent to the selector section where the individual signals are multiplexed to form an address data word. The data word is then further encoded to form the final 8-bit data byte by the encoder ROM, and stored in the 8-bit register until the Output Enable Command. Then the data is sent to the data bus via a three-state buffer.

Mode Select

There are two modes of operation for the μPD7003. Figure 1 shows the timing diagram for mode "0" where the converter is operating in continuous output mode. The analog input is sampled when the clock is in the "low" state. When the clock is in the "high" state the conversion from analog-to-digital takes place and the resultant data is output on the next falling edge of the clock pulse and the cycle is repeated.

The second mode (Mode 1) is shown in figure 2. In this mode of operation, one conversion takes place while the clock is in the "low" state and the resultant data is held as long as output enable and Chip Select (CS) or DMA Acknowledge (DACK) are "low." Data refresh is inhibited until CS and DACK are recycled.

MODE = "HIGH"

Data is refreshed on the falling edge of CLK, loaded during the "low" clock state, and converted and output during the "high" clock state.

MODE = "LOW"

Data is loaded and converted when Output Enable is "low" and refreshed only when OE makes the transition from high to low again.

Note that in either case data will only be accepted and output when OE and CS or DACK are active ("low"). Output enable should not be changed during the intervals shown in figure 3. The timing for output enable change versus clock transition is 600 ns before and 500 ns after the rising or falling edge of CLK any attempt to change OE during these periods will be inhibited.

Timing Waveforms

Figure 1. (MODE;0)

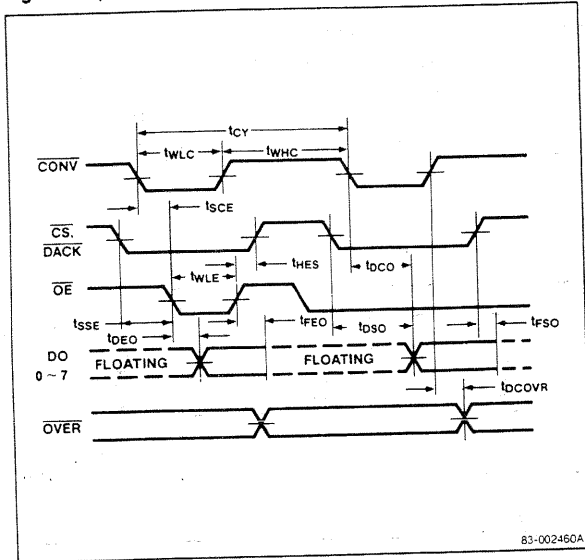


Figure 2. (MODE;1)

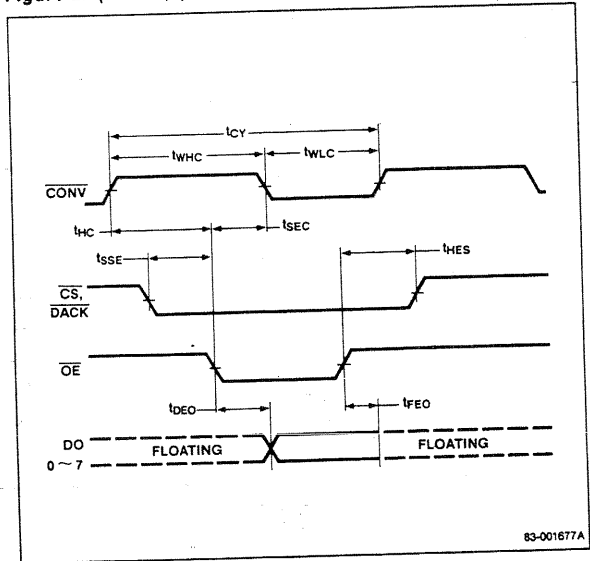
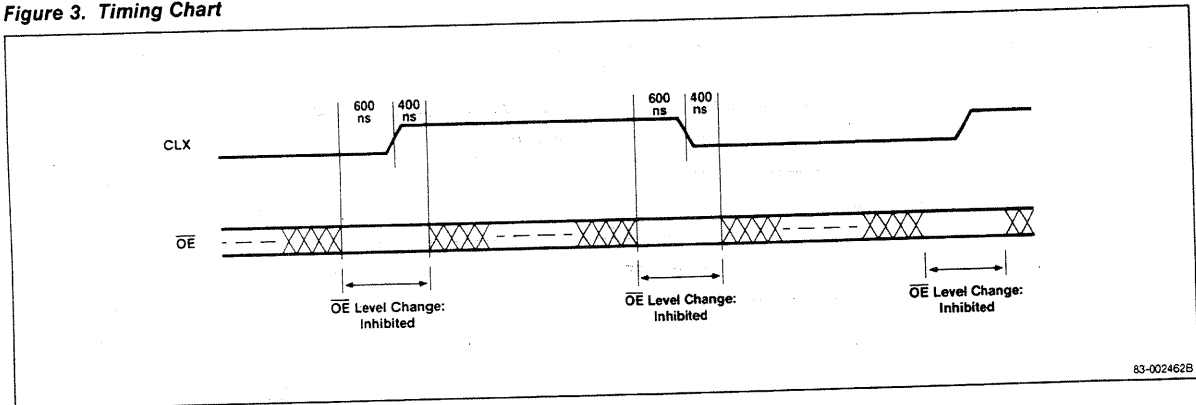
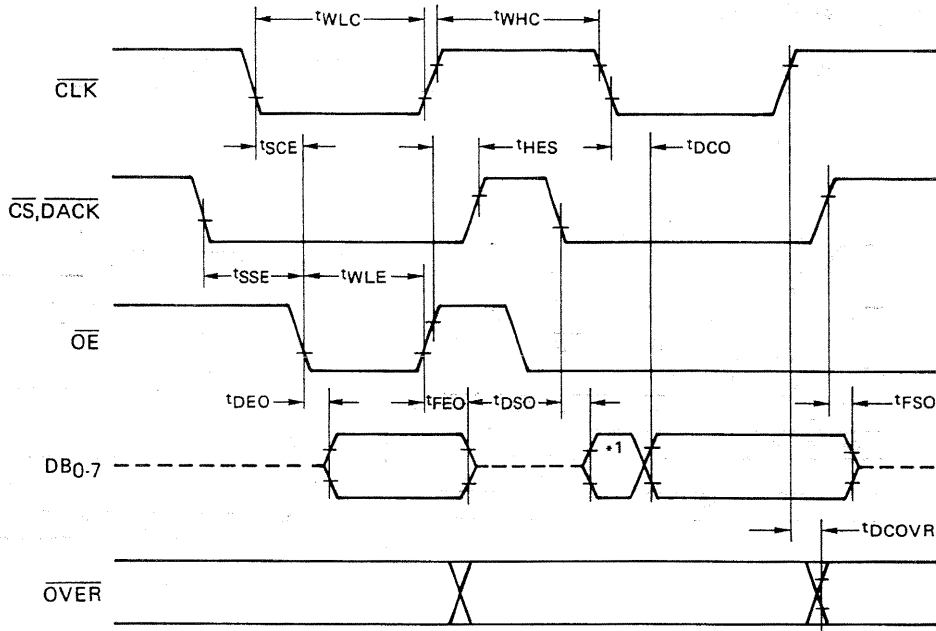


Figure 3. Timing Chart



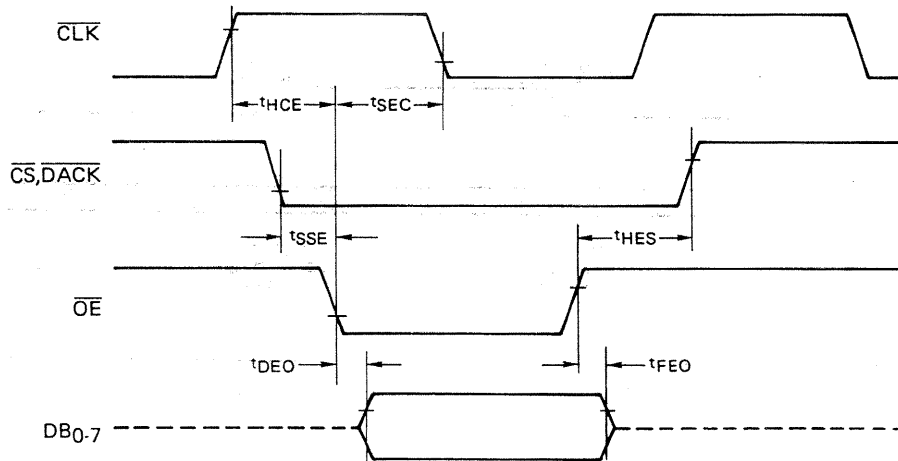
TIMING DIAGRAMS

1. CONTINUOUS OUTPUT MODE



*1: The last conversion Data are output.

2. LATCH OUTPUT MODE



OPERATION OF INTERNAL CIRCUIT BLOCK

1. COMPARATOR

Reference voltage (V_{REF}) is divided by 256 resistors, and 256 comparators simultaneously compare analog input voltage (V_{IN}) with the divided voltages.

2. SELECTOR, ENCODER

Selector accepts the outputs of comparators, and detects the position of comparator which corresponds to analog input voltage.

The encoder generates an 8 bit code by translating the output data from selector.

When the analog input voltage (V_{IN}) is higher than the reference voltage (V_{REF}), the selector generates an over range signal (OVER).

3. 8-BIT LATCH

This register temporarily stores 8-Bit data from encoder.

4. LOGIC CONTROL

This circuit block generates internal control signals according to external control signals.

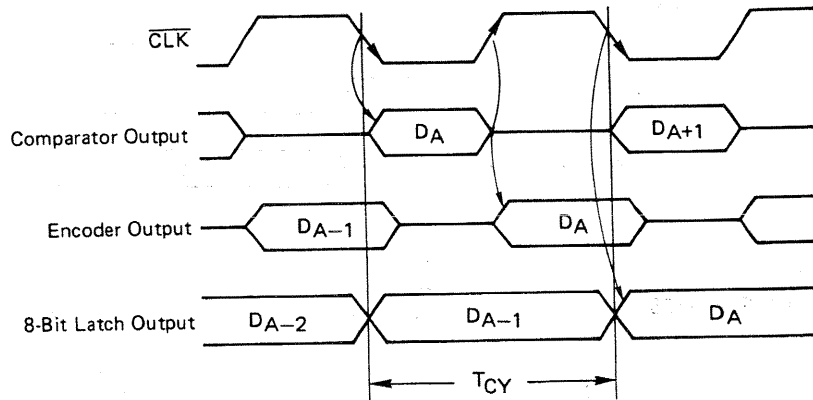
OPERATION MODES

According to the different conversion output, two modes of operation are available.

1. CONTINUOUS OUTPUT MODE (MODE = H)

The actual conversion time of μPD7003 is shortened by using pipeline processing mode.

INTERNAL TIMING

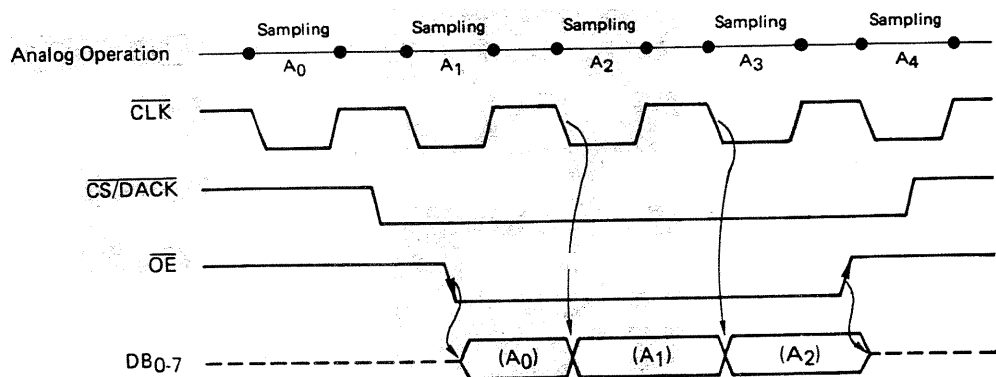


The pipeline processing consists of 3 steps:

- Comparing by comparators,
- Generating 8-Bit data in selector and encoder,
- Holding conversion data in 8-Bit latch.

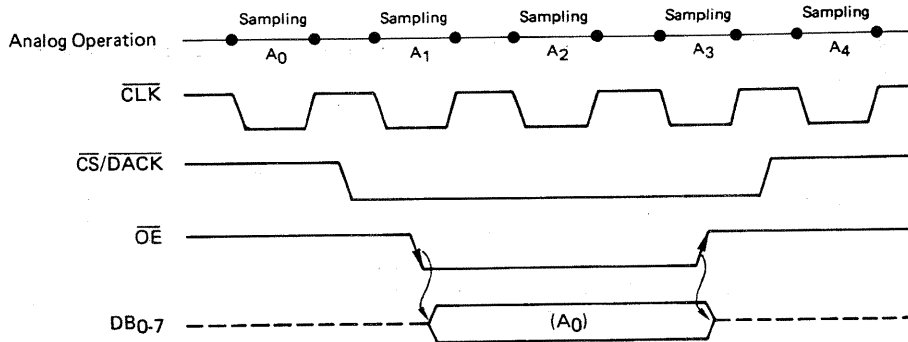
Analog input signals are sampled at the low level interval of $\overline{\text{CLK}}$. The conversion data are output at the subsequent falling edge of CLK.

CONTINUOUS OUTPUT MODE TIMING

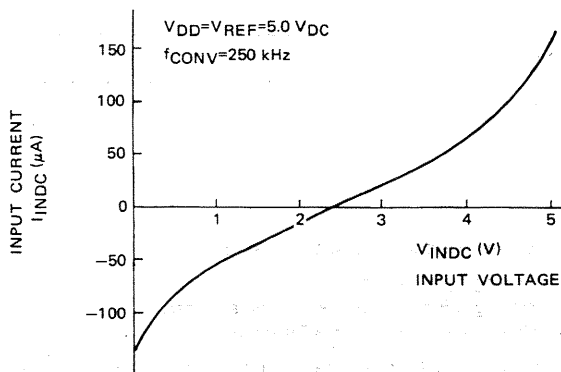


2. LATCH OUTPUT MODE (MODE = L)

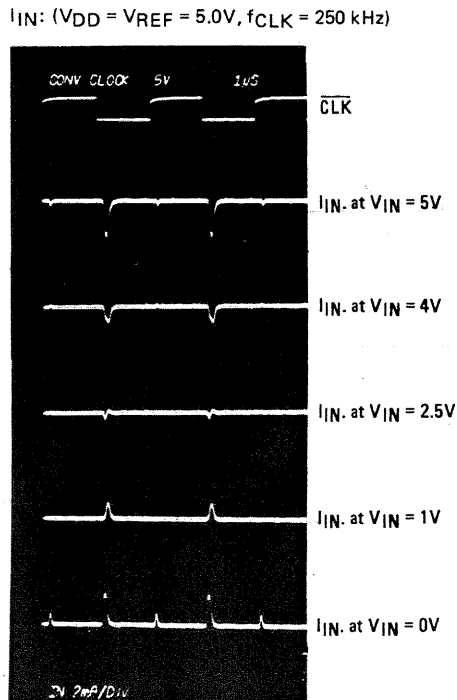
In this mode, μPD7003 operates the same A/D conversion operation as continuous output mode, but with an additional 8-Bit latch operation. In latch output mode, updating of 8-Bit latch data is inhibited at the low level interval of \overline{OE} , and holding the last latched data.



INPUT CHARACTERISTICS

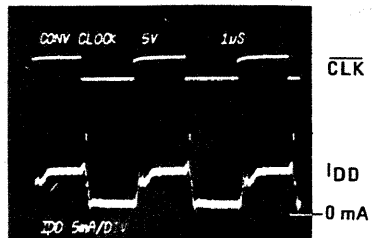


INPUT CURRENT WAVEFORMS



POWER SUPPLY CURRENT WAVEFORMS

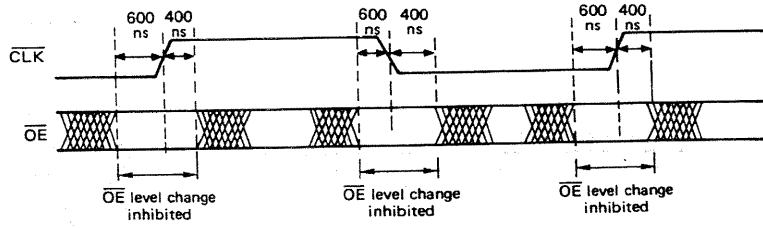
I_{DD} ($V_{DD} = V_{REF} = 5.0$ V, $f_{CONV} = 250$ kHz)



APPLICATION HINTS

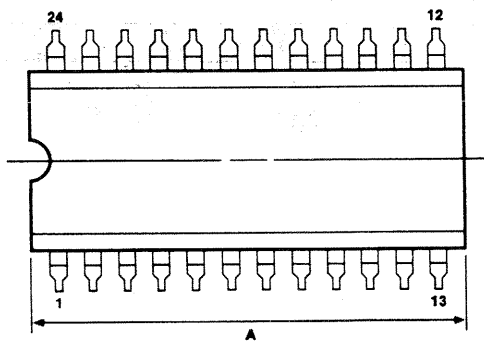
Note 1: Data of A₁ and A₂ are not held.

Note 2: Please do not change the level of \overline{OE} signal during the intervals shown below.

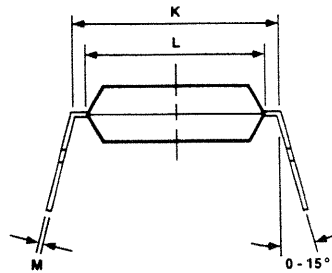
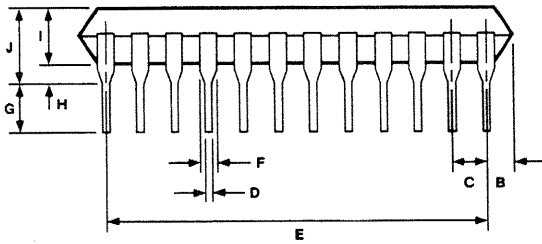


Packaging Information

24-Pin Plastic Package (600 mil)



| Item | Millimeters | Inches |
|------|--------------------|----------------------|
| A | 33.02 max | 1.3 max |
| B | 2.54 max | .10 max |
| C | 2.54 [TP] | .10 [TP] |
| D | .5 ± .10 | .02 + .004 - .005 |
| E | 27.94 | 1.1 |
| F | 1.2 min | .047 min |
| G | 3.6 ± .3 | .138 ± .012 |
| H | .51 min | .02 min |
| I | 4.31 max | .17 max |
| J | 5.72 max | .226 max |
| K | 15.24 [TP] | .60 [TP] |
| L | 13.2 | .52 |
| M | .25 + .10 - .05 | .01 + .004 - .003 |



- Notes: 1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
 2. Item "K" to center of leads when formed parallel.

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