



## Ultra Fast USB 2.0 SD/MMC Flash Media Controller

### PRODUCT FEATURES

### Datasheet

#### General Description

The SMSC USB2244/USB2244i is a USB 2.0 compliant, high speed Bulk Only Mass Storage Class Peripheral Controller intended for reading and writing to SD/MMC Flash Media Cards.

The SMSC USB2244/USB2244i is a fully integrated, single chip solution capable of ultra high performance operation. Average sustained transfer rates exceeding 35MB/s are possible if the media and host can support those rates. Provisions to read/write secure media formats is also provided.

#### General Features

- 36-pin QFN (6x6mm) lead-free RoHS compliant package
- Hardware-controlled data flow architecture for all self-mapped media
- Pipelined hardware support for access to non-self-mapped media
- Product name with "i" denotes the version that supports the industrial temperature range of -40°C to 85°C
- Support included for secure media format on a licensed, customized basis
  - SD Secure

#### Hardware Features

- Single Chip Flash Media Reader/Writer
  - Secure Digital 2.0
    - HS-SD, HC-SD, TransFlash™ and reduced form factor media
    - MultiMediaCard Specification 4.2
      - 1/4/8 bit MMC
  - SDIO and MMC Streaming Mode support
  - Extended configuration options
    - Socket switch polarities, etc.
  - Media Activity LED
  - GPIO configuration and polarity
    - Up to 8 GPIOs for special function use: LED indicators, power control to memory devices, etc. The number of actual GPIO's depends on the implementation configuration used.
    - One GPIO with up to 200 mA drive
- On Board 24MHz Crystal Driver Circuit
- Internal Card Power FET
  - 200mA
  - "Fold-back" short circuit current protected
- 8051 8-bit microprocessor
  - 60MHz - single cycle execution
  - 64KB ROM; 14KB RAM
- Internal Regulator for 1.8V core operation
- Optimized pinout improves signal routing, easing implementation and allowing for improved signal integrity

#### Mask Programmable Features

- VID/PID/Language ID
- 28-character Manufacturer ID and Product string
- 12-hex digit (max) Serial Number string
- Customizable Vendor specific data LED blink interval or duration

#### Software Features

- Optimized for low latency interrupt handling
- Reduced memory footprint
- Please see the USB2244/USB2244i Software Release Notes for additional Software Features.

#### Applications

- Flash Media Card Reader/Writer
- Printers
- Desktop and Mobile PCs
- Consumer A/V
- Media Players/Viewers
- Vista ReadyBoost™
- Compatible with Microsoft Vista, Windows XP, Windows ME, Windows 2K SP4, Apple OSx, and Linux Mass Storage Class Drivers



Ultra Fast USB 2.0 SD/MMC Flash Media Controller

Datasheet

**ORDER NUMBER:**

**USB2244/USB2244i-AEZG-XX for 36 pin, QFN Lead-Free RoHS Compliant Package**

**“XX” in the order number indicates the internal ROM firmware revision level.  
Please contact your SMSC sales representative for more information.**



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

Copyright © 2008 SMSC or its subsidiaries. All rights reserved.

Circuit diagrams and other information relating to SMSC products are included as a means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. Although the information has been checked and is believed to be accurate, no responsibility is assumed for inaccuracies. SMSC reserves the right to make changes to specifications and product descriptions at any time without notice. Contact your local SMSC sales office to obtain the latest specifications before placing your product order. The provision of this information does not convey to the purchaser of the described semiconductor devices any licenses under any patent rights or other intellectual property rights of SMSC or others. All sales are expressly conditional on your agreement to the terms and conditions of the most recently dated version of SMSC's standard Terms of Sale Agreement dated before the date of your order (the "Terms of Sale Agreement"). The product may contain design defects or errors known as anomalies which may cause the product's functions to deviate from published specifications. Anomaly sheets are available upon request. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer. Copies of this document or other SMSC literature, as well as the Terms of Sale Agreement, may be obtained by visiting SMSC's website at <http://www.smsc.com>. SMSC is a registered trademark of Standard Microsystems Corporation ("SMSC"). Product names and company names are the trademarks of their respective holders.

SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES, INCLUDING WITHOUT LIMITATION ANY AND ALL IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE, AND AGAINST INFRINGEMENT AND THE LIKE, AND ANY AND ALL WARRANTIES ARISING FROM ANY COURSE OF DEALING OR USAGE OF TRADE. IN NO EVENT SHALL SMSC BE LIABLE FOR ANY DIRECT, INCIDENTAL, INDIRECT, SPECIAL, PUNITIVE, OR CONSEQUENTIAL DAMAGES; OR FOR LOST DATA, PROFITS, SAVINGS OR REVENUES OF ANY KIND; REGARDLESS OF THE FORM OF ACTION, WHETHER BASED ON CONTRACT; TORT; NEGLIGENCE OF SMSC OR OTHERS; STRICT LIABILITY; BREACH OF WARRANTY; OR OTHERWISE; WHETHER OR NOT ANY REMEDY OF BUYER IS HELD TO HAVE FAILED OF ITS ESSENTIAL PURPOSE, AND WHETHER OR NOT SMSC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

## Table of Contents

---

<b>Chapter 1 Acronyms .....</b>	<b>6</b>
<b>Chapter 2 Block Diagram .....</b>	<b>7</b>
<b>Chapter 3 Pin Table.....</b>	<b>8</b>
3.1    36-Pin Package .....	8
<b>Chapter 4 Pin Configuration .....</b>	<b>9</b>
<b>Chapter 5 Pin Descriptions .....</b>	<b>10</b>
5.1    Pin Descriptions .....	10
5.2    Buffer Type Descriptions .....	12
<b>Chapter 6 Pin Reset State Table.....</b>	<b>13</b>
6.1    36-Pin Reset States .....	14
<b>Chapter 7 DC Parameters.....</b>	<b>15</b>
7.1    Maximum Guaranteed Ratings.....	15
7.2    Recommended Operating Conditions.....	16
7.3    DC Electrical Characteristics .....	17
7.4    Capacitance .....	19
<b>Chapter 8 AC Specifications.....</b>	<b>20</b>
8.1    Oscillator/Clock.....	20
<b>Chapter 9 Package Outline .....</b>	<b>21</b>
<b>Chapter 10 GPIO Usage .....</b>	<b>22</b>

## List of Figures

Figure 2.1	USB2244/USB2244i Block Diagram .....	7
Figure 4.1	USB2244/USB2244i 36 Pin QFN Diagram .....	9
Figure 6.1	Pin Reset States .....	13
Figure 6.2	Legend for Pin Reset States Table .....	13
Figure 7.1	Supply Rise Time Model .....	16
Figure 8.1	Typical Crystal Circuit .....	20
Figure 8.2	Formula to Find Value of C1 and C2 .....	20
Figure 9.1	USB2244/USB2244i 36-QFN, 6x6mm Body, 0.5mm Pitch .....	21

## List of Tables

Table 3.1	USB2244/2244i 36-Pin QFN Package.	8
Table 5.2	USB2244/2244i 36-Pin QFN Pin Descriptions.	10
Table 5.3	USB2244/USB2244i Buffer Type Descriptions	12
Table 6.1	USB2244/USB2244i Pin Reset States	14
Table 7.1	Pin Capacitance.	19
Table 10.1	USB2244/USB2244i GPIO Usage (ROM Rev 0x00)	22

## Chapter 1 Acronyms

**MMC:** MultiMediaCard

**PLL:** Phase-Locked Loop

**QFN:** Quad Flat no Leads

**RoHS:** Restriction of Hazardous Substances Directive

**SD:** Secure Digital

**SDIO:** Secure Digital Input/Output

**SDC:** Secure Digital Controller

**SIE:** Serial Interface Engine

\*Note: In order to develop, make, use, or sell readers and/or other products using or incorporating any of the SMSC devices made the subject of this document or to use related SMSC software programs, technical information and licenses under patent and other intellectual property rights from or through various persons or entities, including without limitation media standard companies, forums, and associations, and other patent holders may be required. These media standard companies, forums, and associations include without limitation the following: Sony Corporation (Memory Stick, Memory Stick Pro); SD3 LLC (Secure Digital); MultiMedia Card Association (MultiMediaCard); the SSFDC Forum (SmartMedia); the Compact Flash Association (Compact Flash); and Fuji Photo Film Co., Ltd., Olympus Optical Co., Ltd., and Toshiba Corporation (xD-Picture Card). SMSC does not make such licenses or technical information available; does not promise or represent that any such licenses or technical information will actually be obtainable from or through the various persons or entities (including the media standard companies, forums, and associations), or with respect to the terms under which they may be made available; and is not responsible for the accuracy or sufficiency of, or otherwise with respect to, any such technical information.

SMSC's obligations (if any) under the Terms of Sale Agreement, or any other agreement with any customer, or otherwise, with respect to infringement, including without limitation any obligations to defend or settle claims, to reimburse for costs, or to pay damages, shall not apply to any of the devices made the subject of this document or any software programs related to any of such devices, or to any combinations involving any of them, with respect to infringement or claimed infringement of any existing or future patents related to solid state disk or other flash memory technology or applications ("Solid State Disk Patents"). By making any purchase of any of the devices made the subject of this document, the customer represents, warrants, and agrees that it has obtained all necessary licenses under then-existing Solid State Disk Patents for the manufacture, use and sale of solid state disk and other flash memory products and that the customer will timely obtain at no cost or expense to SMSC all necessary licenses under Solid State Disk Patents; that the manufacture and testing by or for SMSC of the units of any of the devices made the subject of this document which may be sold to the customer, and any sale by SMSC of such units to the customer, are valid exercises of the customer's rights and licenses under such Solid State Disk Patents; that SMSC shall have no obligation for royalties or otherwise under any Solid State Disk Patents by reason of any such manufacture, use, or sale of such units; and that SMSC shall have no obligation for any costs or expenses related to the customer's obtaining or having obtained rights or licenses under any Solid State Disk Patents.

**SMSC MAKES NO WARRANTIES, EXPRESS, IMPLIED, OR STATUTORY, IN REGARD TO INFRINGEMENT OR OTHER VIOLATION OF INTELLECTUAL PROPERTY RIGHTS. SMSC DISCLAIMS AND EXCLUDES ANY AND ALL WARRANTIES AGAINST INFRINGEMENT AND THE LIKE.**

No license is granted by SMSC expressly, by implication, by estoppel or otherwise, under any patent, trademark, copyright, mask work right, trade secret, or other intellectual property right.

\*\*To obtain this software program the appropriate SMSC Software License Agreement must be executed and in effect. Forms of these Software License Agreements may be obtained by contacting SMSC.

## Chapter 2 Block Diagram

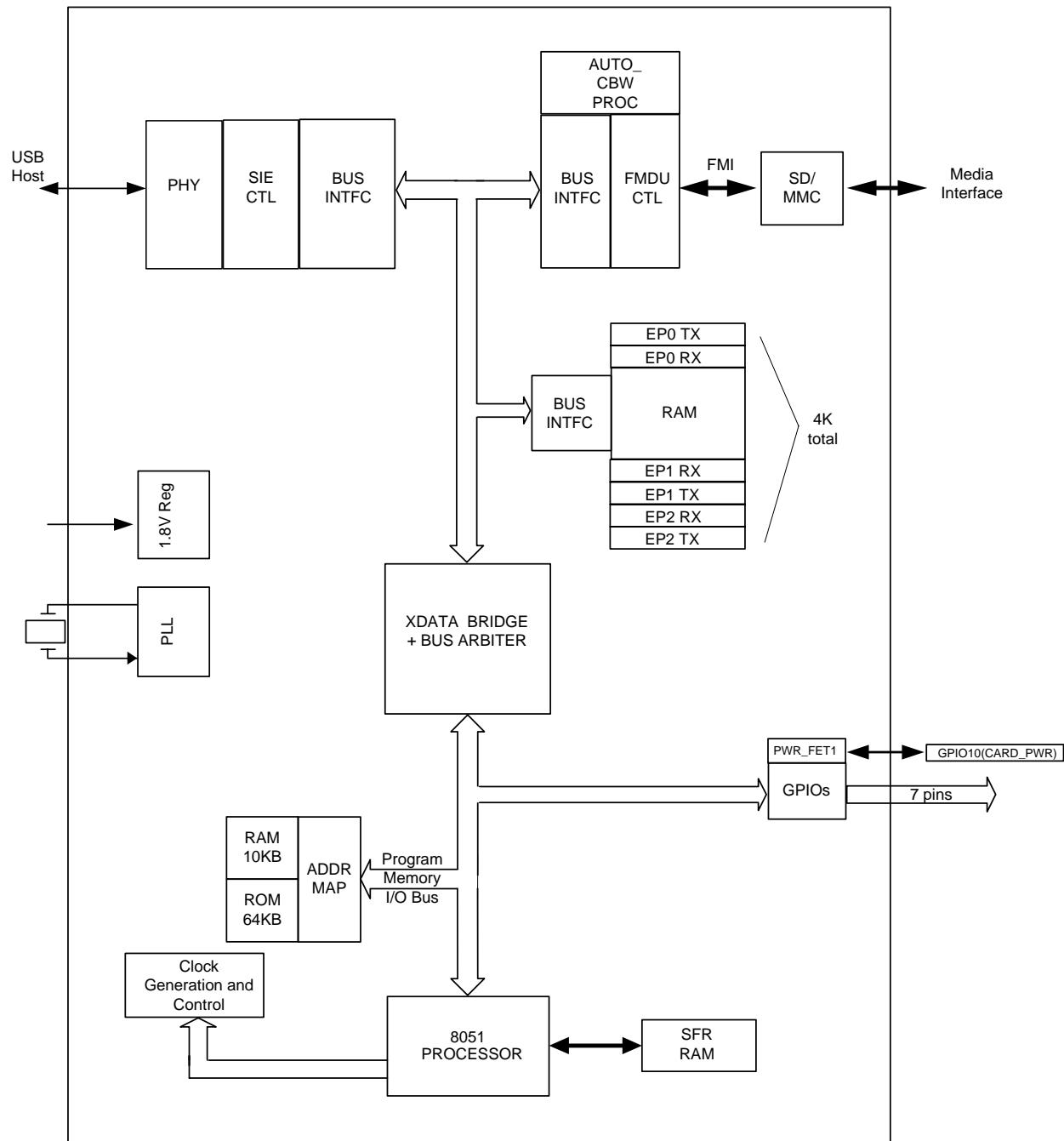


Figure 2.1 USB2244/USB2244i Block Diagram

## Chapter 3 Pin Table

### 3.1 36-Pin Package

Table 3.1 USB2244/2244i 36-Pin QFN Package

SD/MMC INTERFACE (12 Pins)			
SD_D0	SD_D1	SD_D2	SD_D3
SD_D4	SD_D5	SD_D6	SD_D7
SD_CLK	SD_CMD	SD_WP	GPIO15 (SD_nCD)
USB INTERFACE (7 PINS)			
USB+	USB-	RBIAS	
XTAL1 (CLKIN)	XTAL2	VDDA33	VDD18PLL
MISC (13 PINS)			
GPIO1 (LED1)	GPIO2 / RXD / SDA	GPIO4	GPIO7 / TXD / SCK
GPIO10 (CRD_PWR)	GPIO12	GPIO14	(4) NC
TEST	nRESET		
DIGITAL, POWER (4 PINS)			
(3)VDD33	VDD18		
TOTAL 36			

## Chapter 4 Pin Configuration

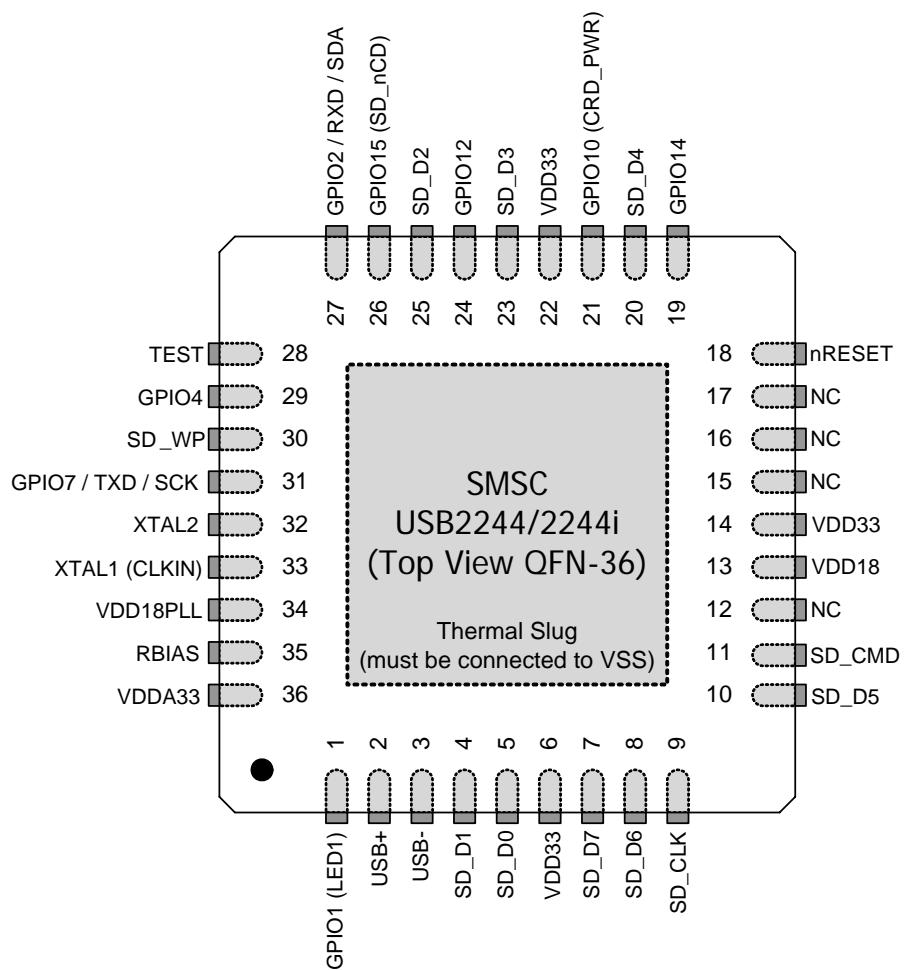


Figure 4.1 USB2244/USB2244i 36 Pin QFN Diagram

## Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

### 5.1 Pin Descriptions

Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
<b>SECURE DIGITAL INTERFACE</b>				
SD Data	SD_D[7:0]	7 8 10 20 23 25 4 5	I/O12PU	The bi-directional signals should have weak pull-up resistors. The register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE_CTL
SD Clock	SD_CLK	9	O12	This is an output clock signal to SD/MMC device.  The clock frequency is software configurable.
SD Command	SD_CMD	11	I/O12PU	This is a bi-directional signal that connects to the CMD signal of SD/MMC device. The bi-directional signal should have an internal weak pull-up resistor.  The pull-up register can be controlled by: SD_MMC_INTF_EN bit of SDC_MODE_CTL
SD Write Protect	SD_nWP	30	I/O12	This pin is designated as the Secure Digital card mechanical write detect pin.
SD Card Detect GPIO	GPIO15 (SD_nCD)	26	I/O12	This is a GPIO designated as the Secure Digital card detection pin.
<b>USB INTERFACE</b>				
USB Bus Data	USB+ USB-	2 3	I/O-U	These pins connect to the USB bus data signals.
USB Transceiver Bias	RBIAS	35	I-R	A 12.0k , 1.0% resistor is attached from VSSA to this pin in order to set the transceiver's internal bias currents.

Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions (continued)

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
24MHz Crystal or external clock input	XTAL1 (CLKIN)	33	ICLKx	This pin can be connected to one terminal of the crystal or it can be connected to an external 24 clock when a crystal is not used.
24MHz Crystal	XTAL2	32	OCLKx	This is the other terminal of the crystal, or it can be left open when an external clock source is used to drive XTAL1(CLKIN). It may not be used to drive any external circuitry other than the crystal circuit.
3.3V Analog Power	VDDA33	36		3.3V Analog Power
1.8V PLL Power	VDD18PLL	34		This pin is the 1.8V Power for the PLL. +1.8V Filtered analog power for internal PLL. This pin must have a 1.0 $\mu$ F(or greater) $\pm 20\%$ (ESR <0.1 $\Omega$ ) capacitor to VSS.
<b>MISC</b>				
General Purpose I/O	GPIO1 (LED1)	1	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.  In addition, as an output, the GPIO1 can use output controlled by the LED1_GPIO1 register.
General Purpose I/O	GPIO2 / RXD / SDA	27	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			I	RXD: In addition to the above, the signal can be used as input to the RXD of UART in the device, when the TXD_RXD_SEL bit in UTIL_CONFIG1 register is cleared to "0".
			I/O12	SDA: This is the data pin when used with an external serial EEPROM.
General Purpose I/O	GPIO4	29	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
General Purpose I/O	GPIO7 / TXD / SCK	31	I/O12	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
			O12	TXD: In addition, as an output, the GPIO7 can be used as an output TXD of UART in the device, when the GPIO2/TXD bit in UTIL_CONFIG register is set to "1"
			O12	SCK: This is the clock output when used with an external EEPROM.
General Purpose I/O	GPIO10 (CRD_PWR)	21	I/O200	GPIO: This pin may be used either as input, edge sensitive interrupt input, or output.
				CRD_PWR: Card Power drive of 3.3V @ either 100mA or 200mA.
General Purpose I/O	GPIO14	19	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output.
RESET Input	nRESET	18	IS	This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 $\mu$ s wide.

**Table 5.2 USB2244/2244i 36-Pin QFN Pin Descriptions (continued)**

NAME	SYMBOL	36-PIN QFN	BUFFER TYPE	DESCRIPTION
TEST Input	TEST	28	I	This signal is used for testing the chip. User should normally tie this pin low externally if the test function is not used.
No Connects	NC			No Connect. No trace or signal should be routed/attached to these pins.
<b>DIGITAL / POWER</b>				
+1.8V Core power	VDD18	13		All VDD18 pins must be connected together on the circuit board.  +1.8V core power. This pin must have a $1.0\mu F$ (or greater) $\pm 20\%$ (ESR $<0.1\Omega$ ) capacitor to VSS.
3.3V Power & Regulator Input.	VDD33	6 14 22		3.3V Power & Regulator Input.
Ground	VSS	SLUG		Ground Reference

## 5.2 Buffer Type Descriptions

**Table 5.3 USB2244/USB2244i Buffer Type Descriptions**

BUFFER	DESCRIPTION
I	Input.
IS	Input with Schmitt trigger.
I/O12	Input/Output buffer with 12mA sink and 12mA source.
I/O200	Input/Output buffer 12mA with FET disabled, 100/200mA source only when the FET is enabled.
I/O12PU	Input/Output buffer with 12mA sink and 12mA source with a pull-up resistor.
O12	Output buffer with 12mA source.
ICLKx	XTAL clock input.
OCLKx	XTAL clock output.
I/O-U	Analog Input/Output Defined in USB specification.
I-R	RBIAS.

## Chapter 6 Pin Reset State Table

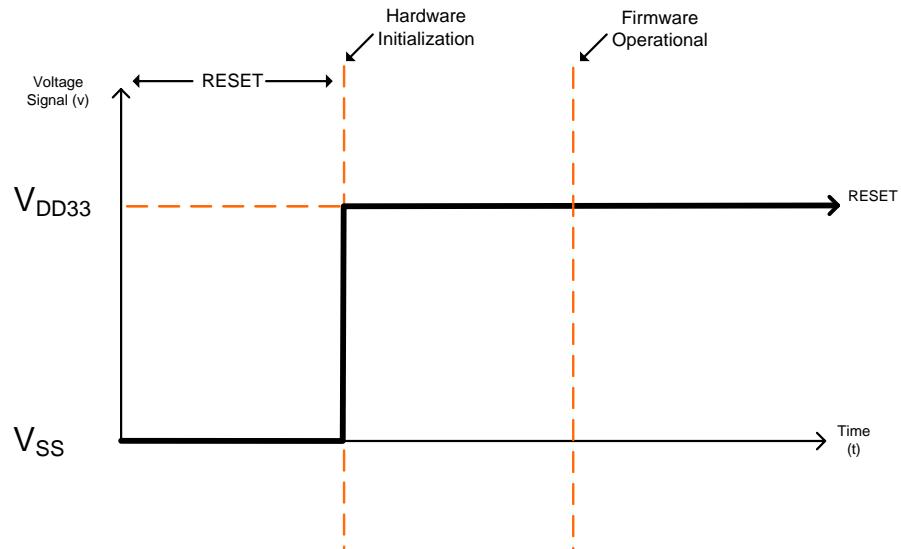


Figure 6.1 Pin Reset States

LEGEND	
yes	hardware enables function
--	hardware disables function
z	hardware disables output driver
pu	hardware enables pullup
pd	hardware enables pulldown
hw	hardware controls function, but state is protocol dependent
(fw)	firmware controls function through registers
VDD	hardware supplies power through pin, applicable only to CARD_PWR pins
none	hardware disables pad

Figure 6.2 Legend for Pin Reset States Table

## 6.1 36-Pin Reset States

Table 6.1 USB2244/USB2244i Pin Reset States

PIN	PIN NAME	RESET STATE				Post-Reset State SD Mode			
		FUNCTION	OUT- PUT	PU/ PD	IN- PUT	FUNCTION	OUT- PUT	PU/ PD	IN- PUT
8	SD_D6	none	z	--	--	SD_D6	hw	pu	yes
7	SD_D7	none	z	--	--	SD_D7	hw	pu	yes
5	SD_D0	none	z	--	--	SD_D0	hw	pu	yes
4	SD_D1	none	z	--	--	SD_D1	hw	pu	yes
30	SD_WP	SD_WP	0	--	--	SD_WP	(fw)	(fw)	(fw)
25	SD_D2	none	z	--	--	SD_D2	hw	pu	yes
23	SD_D3	none	z	--	--	SD_D3	hw	pu	yes
20	SD_D4	none	z	--	--	SD_D4	hw	pu	yes
9	SD_CLK	none	z	--	--	SD_CLK	hw	--	yes
10	SD_D5	none	z	--	--	SD_D5	hw	pu	yes
11	SD_CMD	none	z	--	--	SD_CMD	hw	pu	yes
19	GPIO14	GPIO	z	pu	yes				
26	GPIO15 (SD_nCD)	GPIO	z	pu	yes				
24	GPIO12	GPIO	z	pu	yes				
27	GPIO2 / RXD / SDA	GPIO	0	--	--	RXD	z	pu	yes
29	GPIO4	GPIO	0	--	--				
31	GPIO7 / TXD / SCK	GPIO	0	--	--	TXD	hw	--	--
21	GPIO10(CARD_PWR)	GPIO	z	--	--	PWR	VDD	--	--
28	TEST	TEST	z	--	yes				
18	nRESET	nRESET	z	--	yes				
1	GPIO1 (LED1)	GPIO1	0	--	--				
17:15	NC	none	z	--	--	none	z	--	--
12	NC	none	z	--	--	none	z	--	--
2	USB+	USB+	z	--	--				
3	USB-	USB-	z	--	--				
35	RBIAS								
33	XTAL1 (CLKIN)								
32	XTAL2								

## Chapter 7 DC Parameters

### 7.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	$T_A$	-55	150	°C	
Lead Temperature			325	°C	Soldering < 10 seconds
3.3V supply voltage	$V_{DD33}$ , $V_{DDA33}$	-0.5	4.0	V	
Voltage on USB+ and USB- pins		-0.5	$(3.3V \text{ supply voltage} + 2) \leq 6$	V	
Voltage on GPIO10		-0.5	$V_{DD33} + 0.3$	V	When internal power FET operation of this pin is enabled, this pin may be simultaneously shorted to ground or any voltage up to 3.63V indefinitely, without damage to the device as long as $V_{DD33}$ and $V_{DDA33}$ are less than 3.63V and $T_A$ is less than 70°C.
Voltage on any signal pin		-0.5	$V_{DD33} + 0.3$	V	
Voltage on XTAL1		-0.5	4.0	V	
Voltage on XTAL2		-0.5	$V_{DD18} + 0.3$	V	

**Note 7.1** Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied.

**Note 7.2** When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

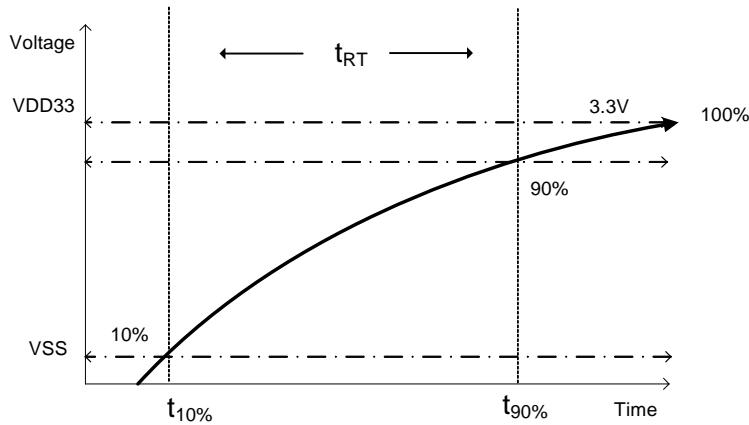


Figure 7.1 Supply Rise Time Model

## 7.2 Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
<b>Operating Temperature</b>					
Commercial Part	$T_A$	0	70	°C	
Industrial Part	$T_A$	-40	85	°C	
3.3V supply voltage	$V_{DD33}$ , $V_{DDA33}$	3.0	3.6	V	(Note 7.3)
3.3V supply rise time	$t_{RT}$	0	400	μs	
Voltage on USB+ and USB- pins		-0.3	5.5	V	If any 3.3V supply voltage drops below 3.0V, then the MAX becomes: $(3.3V \text{ supply voltage}) + 0.5 \leq 5.5$
Voltage on any signal pin		-0.3	$V_{DD33}$	V	
Voltage on XTAL1		-0.3	$V_{DDA33}$	V	
Voltage on XTAL2		-0.3	$V_{DD18}$	V	

**Note 7.3** A 3.3V regulator with an output tolerance of 1% must be used if the output of the internal power FET's must support a 5% tolerance.

## 7.3 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>I, IPU, IPD Type Input Buffer</b>						
Low Input Level	$V_{IL}$			0.8	V	TTL Levels
High Input Level	$V_{IH}$	2.0			V	
Pull Down	PD		72		$\mu$ A	
Pull Up	PU		58		$\mu$ A	
<b>IS Type Input Buffer</b>						
Low Input Level	$V_{IL}$			0.8	V	TTL Levels
High Input Level	$V_{IH}$	2.0			V	
Hysteresis	$V_{HYSI}$		420		mV	
<b>ICLK Input Buffer</b>						
Low Input Level	$V_{ILCK}$			0.5	V	
High Input Level	$V_{IHCK}$	1.4			V	
Input Leakage	$I_{IL}$	-10		+10	$\mu$ A	$V_{IN} = 0$ to $V_{DD33}$
<b>Input Leakage</b>						
(All I and IS buffers)						
Low Input Leakage	$I_{IL}$	-10		+10	$\mu$ A	$V_{IN} = 0$
High Input Leakage	$I_{IH}$	-10		+10	$\mu$ A	$V_{IN} = V_{DD33}$
<b>O12 Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 12mA$ @ $V_{DD33} = 3.3V$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -12mA$ @ $V_{DD33} = 3.3V$
Output Leakage	$I_{OL}$	-10		+10	$\mu$ A	$V_{IN} = 0$ to $V_{DD33}$ (Note 7.4)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
<b>I/O12, I/O12PU &amp; I/O12PD Type Buffer</b>						
Low Output Level	$V_{OL}$			0.4	V	$I_{OL} = 12\text{mA} @ V_{DD33} = 3.3\text{V}$
High Output Level	$V_{OH}$	$V_{DD33} - 0.4$			V	$I_{OH} = -12\text{mA} @ V_{DD33} = 3.3\text{V}$
Output Leakage	$I_{OL}$	-10		+10	$\mu\text{A}$	$V_{IN} = 0$ to $V_{DD33}$ (Note 7.4)
Pull Down	PD		72		$\mu\text{A}$	
Pull Up	PU		58		$\mu\text{A}$	
<b>IO-U (Note 7.5)</b>						
<b>I-R (Note 7.6)</b>						
<b>I/O200 Integrated Power FET for GPIO10</b>						
High Output Current Mode	$I_{OUT}$	200			mA	$V_{dropFET} = 0.46\text{V}$
Low Output Current Mode (Note 7.7)	$I_{OUT}$	100			mA	$V_{dropFET} = 0.23\text{V}$
On Resistance (Note 7.7)	$R_{DSON}$			2.1	$\Omega$	$I_{FET} = 70\text{mA}$
Output Voltage Rise Time	$t_{DSON}$			800	$\mu\text{s}$	$C_{LOAD} = 10\mu\text{F}$
Supply Current Unconfigured	$I_{CCINIT}$		80	90	mA	
Supply Current Active Full Speed	$I_{CC}$		110	140	mA	
High Speed	$I_{CC}$		135	165	mA	
Supply Current Suspend	$I_{CSBY}$		350	700	$\mu\text{A}$	
Industrial Temperature Suspend	$I_{CSBYI}$		350	900	$\mu\text{A}$	

**Note 7.4** Output leakage is measured with the current pins in high impedance.

**Note 7.5** See The USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics

**Note 7.6** RBIAS is a 3.3V tolerant analog pin.

**Note 7.7** Output current range is controlled by program software, software disables FET during short circuit condition.

**Note 7.8** The assignment of each Integrated Card Power FET to a designated Card Connector is controlled by both firmware and the specific board implementation. Firmware will default to

the settings listed in [Table 10.1, “USB2244/USB2244i GPIO Usage \(ROM Rev 0x00\),” on page 22.](#)

**Note 7.9** The 3.3V supply should be at least at 75% of its operating condition before the 1.8V supply is allowed to ramp up.

## 7.4 Capacitance

$T_A = 25^\circ\text{C}$ ;  $f_c = 1\text{MHz}$ ;  $V_{DD}, V_{DDP} = 1.8V$

**Table 7.1 Pin Capacitance**

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	$C_{XTAL}$			2	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	$C_{IN}$			10	pF	
Output Capacitance	$C_{OUT}$			20	pF	

## Chapter 8 AC Specifications

### 8.1 Oscillator/Clock

Crystal: Parallel Resonant, Fundamental Mode, 24 MHz  $\pm$  100ppm.

External Clock: 50% Duty cycle  $\pm$  10%, 24 MHz  $\pm$  100ppm, Jitter  $<$  100ps rms.

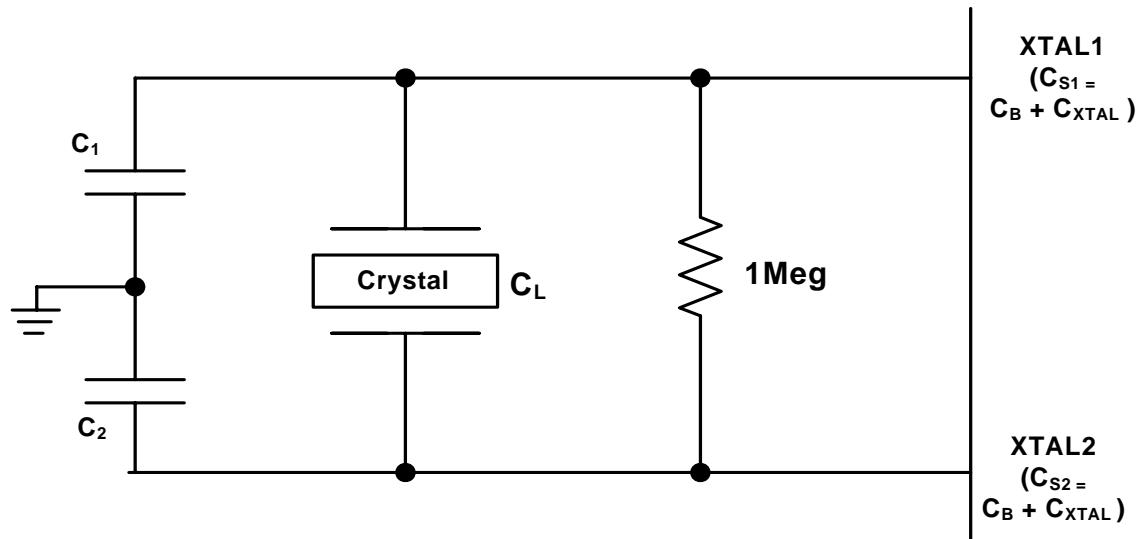


Figure 8.1 Typical Crystal Circuit

**Note:**  $C_B$  equals total board/trace capacitance.

$$\frac{(C_1 + C_{S1}) \times (C_2 + C_{S2})}{(C_1 + C_{S1} + C_2 + C_{S2})} = C_L$$

Figure 8.2 Formula to Find Value of  $C_1$  and  $C_2$

## Chapter 9 Package Outline

Ultra Fast USB 2.0 SD/MMC Flash Media Controller

### Datasheet

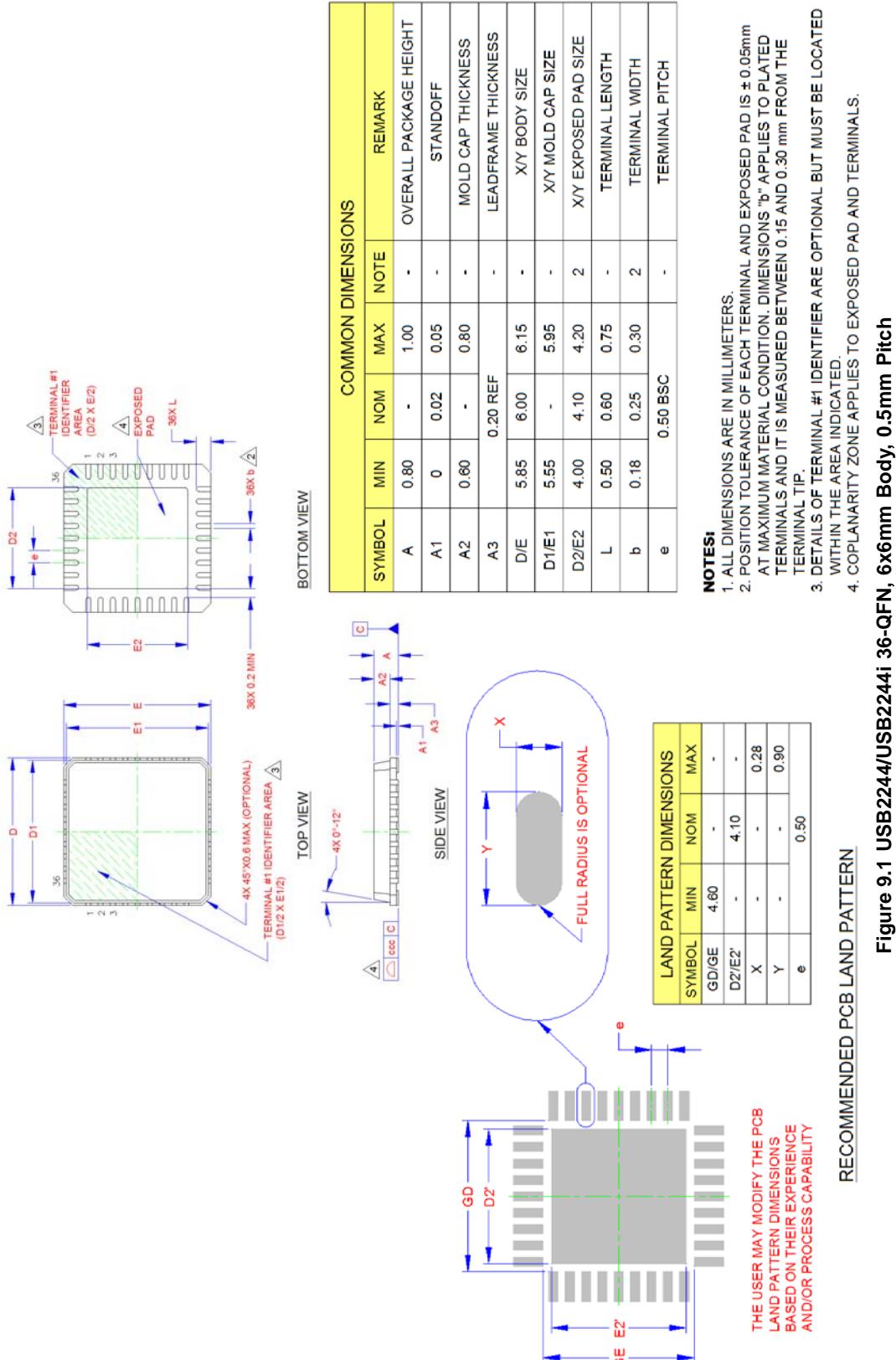


Figure 9.1 USB2244/USB2244i 36-QFN, 6x6mm Body, 0.5mm Pitch

## Chapter 10 GPIO Usage

Table 10.1 USB2244/USB2244i GPIO Usage (ROM Rev 0x00)

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED1	LED indicator
GPIO2	H	RXD / SDA	Receive Port of Debugger / Serial EEPROM Data
GPIO4	USER	GPIO	User defined
GPIO7	H	TXD / SCK	Transmit Port of Debugger / Serial EEPROM Clock
GPIO10	L	CRD_PWR	Card Power Control
GPIO12	USER	GPIO	User defined
GPIO14	USER	GPIO	User defined
GPIO15	L	SD_nCD	Secure Digital card detect