

UTC UT136FE

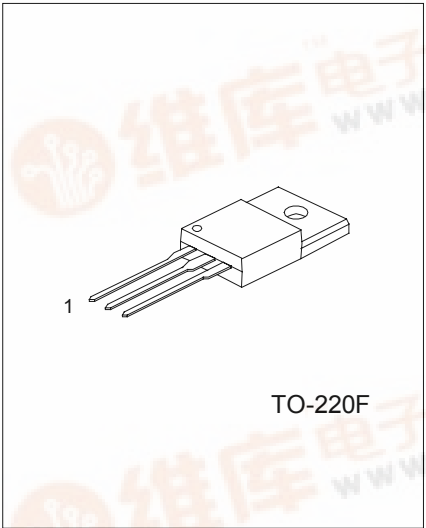
TRIAC

TRIACS

DESCRIPTION

Glass passivated sensitive gate triacs in a full pack,plastic envelop, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages UT136FE-5 UT136FE-6 UT136FE-8	V_{DRM}	500* 600* 800	V
RMS on-state current full sine wave; $T_{hs} \leq 92^{\circ}C$	$I_T(RMS)$	4	A
Non-repetitive peak on-state current Full sine wave; $T_j = 125^{\circ}C$ prior to surge; with reapplied $V_{DRM}(max)$ $t = 20ms$ $t = 16.7 ms$	I_{TSM}	25 27	A
I^2t for fusing ($t = 10 ms$)	I^2t	3.1	A^2s
Repetitive rate of rise of on-state current after triggering $I_{TM} = 6 A$; $I_G = 0.2A$; $dI_G / dt = 0.2A / \mu s$ T2+ G+ T2+ G- T2- G- T2- G+	dI_T / dt	50 50 50 10	$A / \mu s$
Peak gate voltage	V_{GM}	5	V
Peak gate current	I_{GM}	2	A
Peak gate power	P_{GM}	5	W
Average gate power (over any 20 ms period)	$P_{G(AV)}$	0.5	W
Storage temperature	T_{stg}	$-40 \sim 150$	$^{\circ}C$
Operating junction temperature	T_j	125	$^{\circ}C$

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed $3A/\mu s$.

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UNISONIC TECHNOLOGIES CO., LTD.



ISOLATION LIMITING VALUE & CHARACTERISTIC (T_{HS}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Repetitive peak voltage from all three terminals to external heatsink (R.H. ≤ 65%, clean and dustfree)	Visol			1500	V
Capacitance from MT2 to external heatsink (f=1MHz)	Cisol		12		pF

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to heatsink (Full or half cycle) with heatsink compound without heatsink compound	R _{th j-hs}			5.5 7.2	K/W
Thermal resistance Junction to ambient (In free air)	R _{th j-a}		55		K/W

STATIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	I _{GT}	V _D = 12 V; I _T = 0.1 A T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching current	I _L	V _D = 12 V; I _{GT} = 0.1 A T2+ G+ T2+ G- T2- G- T2- G+		3.0 10 2.5 4.0	15 20 15 20	mA
Holding current	I _H	V _D = 12 V; I _{GT} = 0.1 A		2.2	15	mA
On-state voltage	V _T	I _T = 5 A		1.4	1.7	V
Gate trigger voltage	V _{GT}	V _D = 12 V; I _T = 0.1 A		0.7	1.5	V
		V _D = 400 V; I _T = 0.1 A; T _J = 125°C	0.25	0.4		V
Off-state leakage current	I _D	V _D = V _{DRM(max)} ; T _J = 125 °C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of Off-state voltage	dV _D /dt	V _{DM} = 67% V _{DRM(max)} ; T _J = 125°C; exponential waveform; gate open circuit		50		V/μs
Gate controlled turn-on time	t _{gt}	I _{TM} = 6 A; V _D = V _{DRM(max)} ; I _G = 0.1 A; dI _G /dt = 5 A/μs		2		μs

TYPICAL CHARACTERISTICS

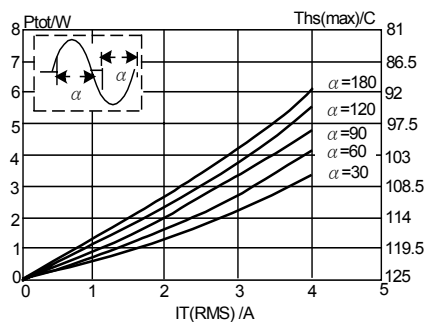


Fig. 1. Maximum on-state dissipation P_{tot} , versus rms on-state current, $I_T(RMS)$, where α = conduction angle.

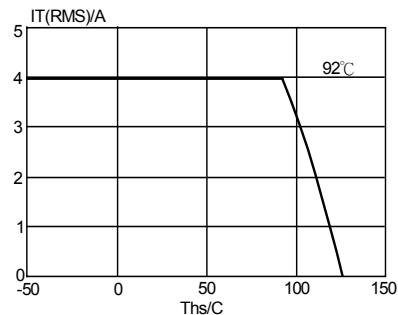


Fig. 4. Maximum permissible rms current $I_T(RMS)$, versus heatsink temperature T_{hs} .

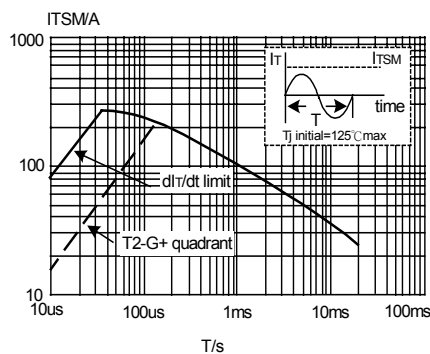


Fig. 2. Maximum Permissible non-repetitive peak on-state Current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20\text{ms}$.

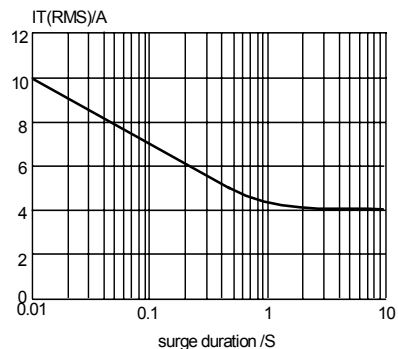


Fig. 5. Maximum permissible repetitive rms on-state current $I_T(RMS)$, versus surge duration, for sinusoidal current, $f=50\text{Hz}$; $T_{hs} \leq 92^\circ\text{C}$.

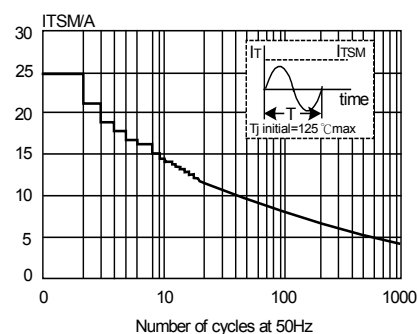


Fig. 3. Maximum Permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f=50\text{Hz}$.

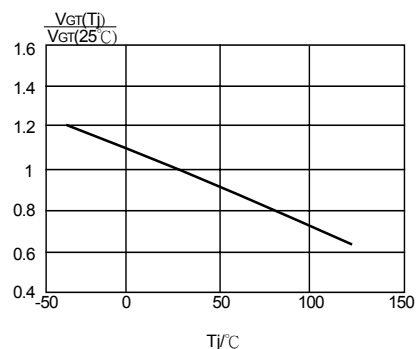


Fig. 6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

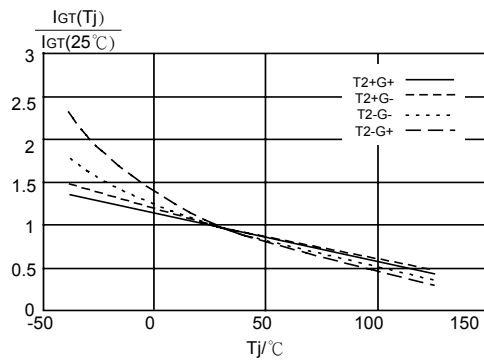


Fig. 7. Normalised gate trigger Current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

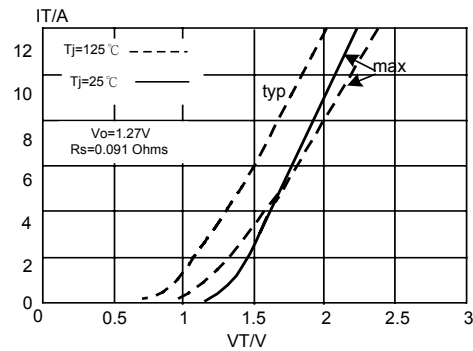


Fig. 10. Typical and maximum on-state characteristic.

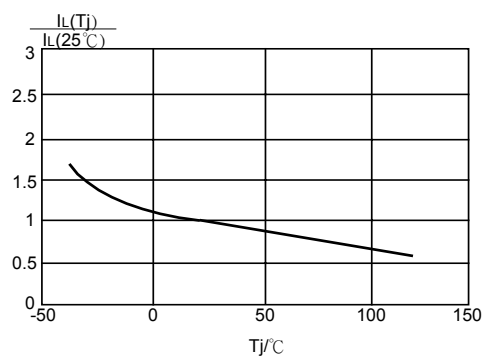


Fig. 8. Normalised latching Current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j .

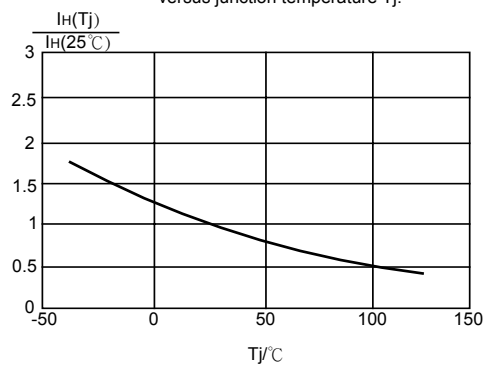


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

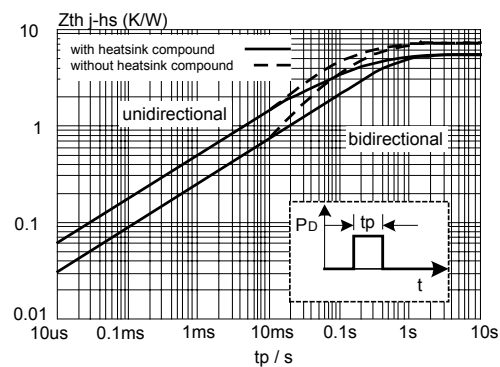


Fig. 11. Transient thermal impedance Z_{thj-mb} , versus pulse width t_p .

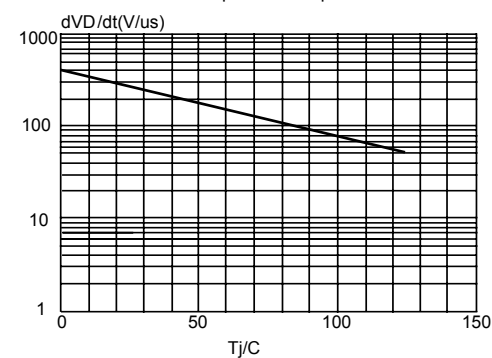


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_d/dt versus junction temperature T_j .

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