Standard Products

UT7C138/139 4Kx8/9 Radiation-Hardened Dual-Port Static RAM with Busy Flag

Data Sheet

January 2002

FEATURES

- ❑ 45ns and 55ns maximum address access time
- ❑ Asynchronous operation for compatibility with industry-standard 4K x 8/9 dual-port static RAM
- ❑ CMOS compatible inputs, TTL/CMOS compatible output levels
- ❑ Three-state bidirectional data bus
- ❑ Low operating and standby current
- ❑ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0E6 rads(Si)
  - Memory Cell LET threshold: 85 MeV-cm^2/mg
  - Latchup immune (LET >100 MeV-cm^2/mg)
- ❑ QML Q and QML V compliant part
- ❑ Packaging options:
  - 68-lead Flatpack
  - 68-pin PGA
- ❑ 5-volt operation
- ❑ Standard Microcircuit Drawing 5962-96845

INTRODUCTION

The UT7C138 and UT7C139 are high-speed radiation-hardened CMOS 4K x 8 and 4K x 9 dual-port static RAMs. Arbitration schemes are included on the UT7C138/139 to handle situations when multiple processors access the same memory location. Two ports provide independent, asynchronous access for reads and writes to any location in memory. The UT7C138/139 can be utilized as a stand-alone 32/36-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. For applications that require depth expansion, the $\overline{BUSY}$ pin is open-collector allowing for wired OR circuit configuration. An M/$\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications, and status buffering.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port.

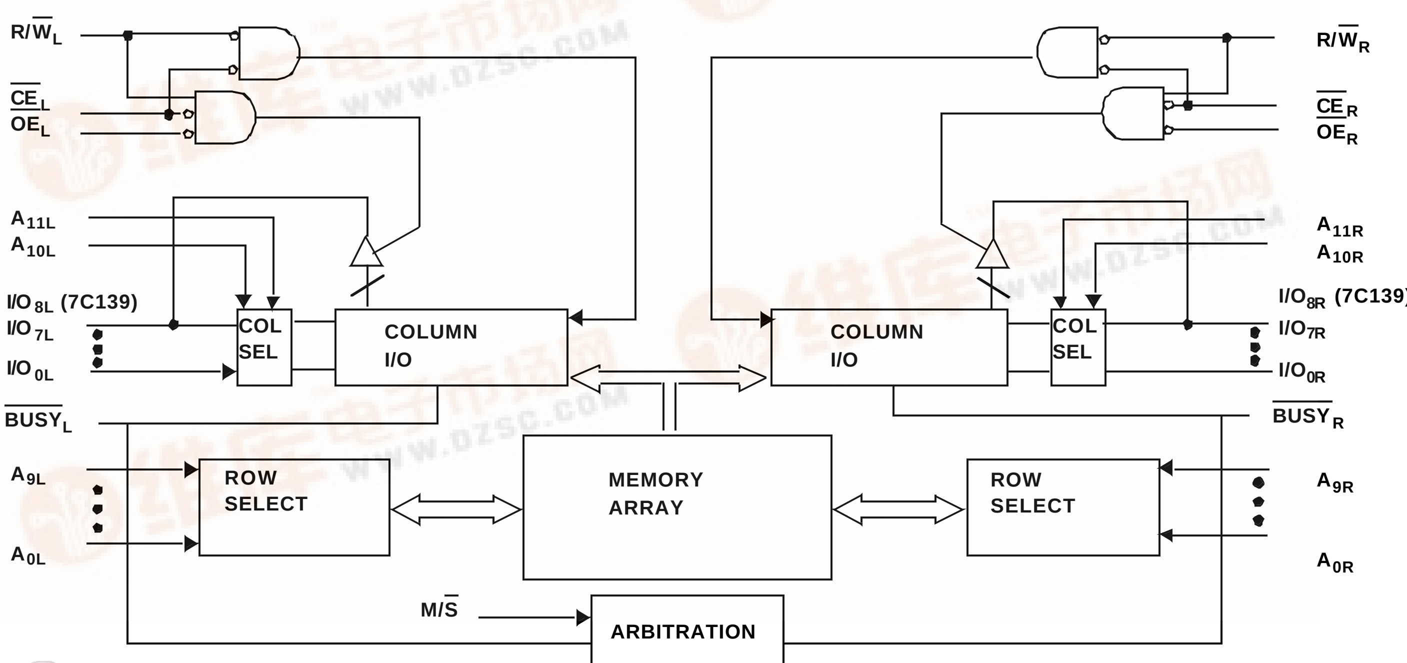


Figure 1. Logic Block Diagram

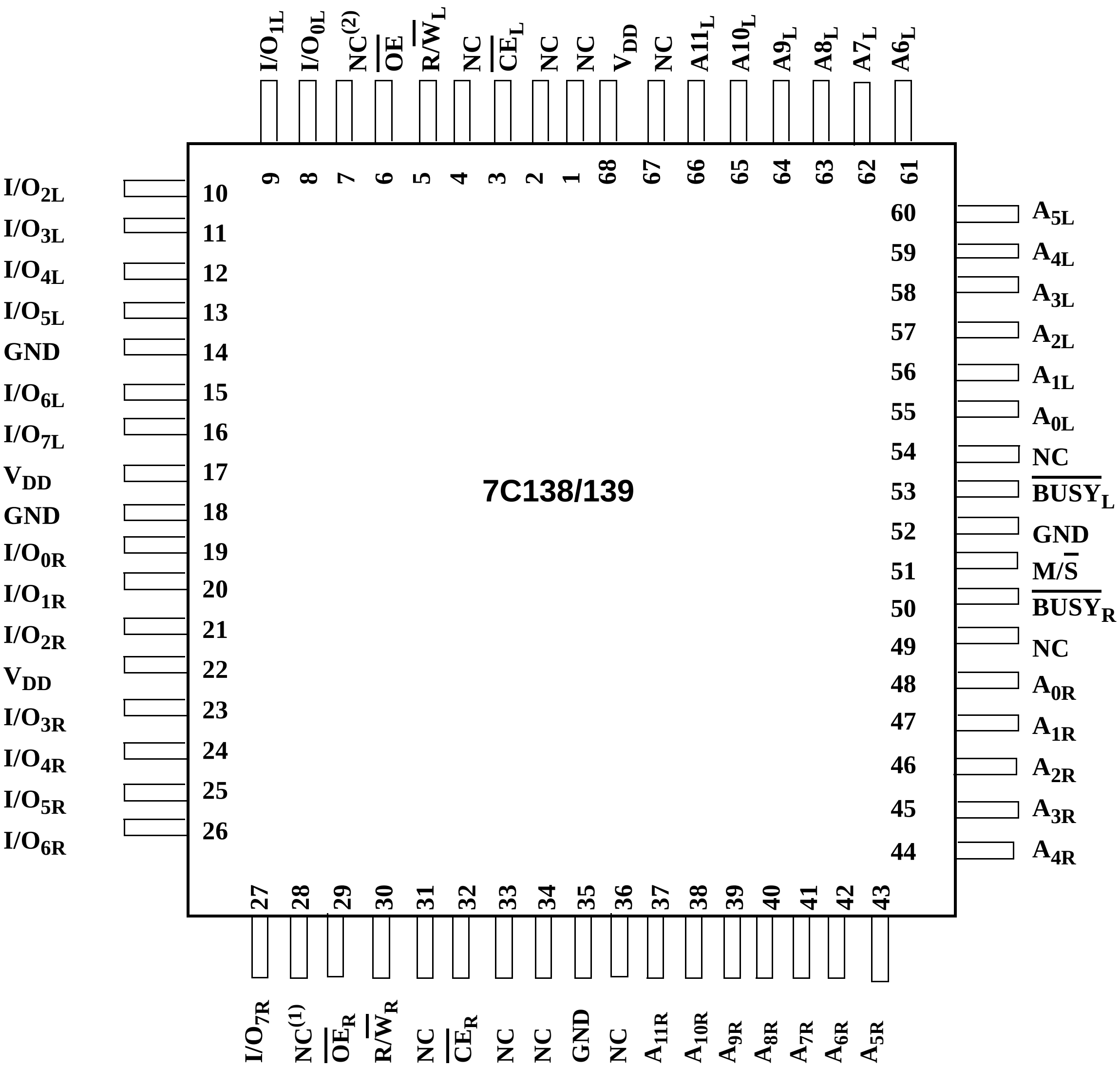


Figure 2a. DPRAM Pinout (68-Flatpack)
(top view)

Notes:
1. I/O8R on the7C139
2. I/O8L on the 7C139

11		**B11** A_{5L}	**C11** A_{4L}	**D11** A_{2L}	**E11** A_{0L}	**F11** $\overline{BUSY}_L$	**G11** $M/\overline{S}$	**H11** NC	**J11** A_{1R}	**K11** A_{3R}	
10	**A10** A_{7L}	**B10** A_{6L}	**C10** A_{3L}	**D10** A_{1L}	**E10** NC	**F10** GND	**G10** $\overline{BUSY}_R$	**H10** A_{0R}	**J10** A_{2R}	**K10** A_{4R}	**L10** A_{5R}
9	**A9** A_{9L}	**B9** A_{8L}								**K9** A_{7R}	**L9** A_{6R}
8	**A8** A_{11L}	**B8** A_{10L}								**K8** A_{9R}	**L8** A_{8R}
7	**A7** V_{DD}	**B7** NC								**K7** A_{11R}	**L7** A_{10R}
6	**A6** NC	**B6** NC				**7C138/139**				**K6** GND	**L6** NC
5	**A5** NC	**B5** $\overline{CE}_L$								**K5** NC	**L5** NC
4	**A4** $\overline{OE}_L$	**B4** $R/\overline{W}_L$								**K4** NC	**L4** $\overline{CE}_R$
3	**A3** I/O_{0L}	**B3** NC(2)								**K3** $\overline{OE}_R$	**L3** $R/\overline{W}_R$
2	**A2** I/O_{1L}	**B2** I/O_{2L}	**C2** I/O_{4L}	**D2** GND	**E2** I/O_{7L}	**F2** GND	**G2** I/O_{1R}	**H2** V_{DD}	**J2** I/O_{4R}	**K2** I/O_{7R}	**L2** NC(1)
1		**B1** I/O_{3L}	**C1** I/O_{5L}	**D1** I/O_{6L}	**E1** V_{DD}	**F1** I/O_{0R}	**G1** I/O_{2R}	**H1** I/O_{3R}	**J1** I/O_{5R}	**K1** I/O_{6R}	
	A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**J**	**K**	**L**

Figure 2b: DPRAM Pinout (68 PGA)
(top view)

Notes:
1. I/O8R on the7C139
2. I/O8L on the 7C139

PIN NAMES

LEFT PORT	RIGHT PORT	DESCRIPTION
$I/O_{0L\text{-}7L(8L)}$	$I/O_{0R\text{-}7R(8R)}$	Data Bus Input/Output
$A_{0L\text{-}11L}$	$A_{0R\text{-}11R}$	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag Input/Output
$M/\overline{S}$		Master or Slave Select
V_{DD}		Power
GND		Ground

The UT7C138/139 consists of an array of 4K words of 8 or 9 bits of dual-port SRAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a $\overline{BUSY}$ pin is provided on each port. With the M/$\overline{S}$ pin, the UT7C138/139 can function as a master ($\overline{BUSY}$ pins are outputs) or as a slave ($\overline{BUSY}$ pins are inputs). Each port is provided with its own output enable control ($\overline{OE}$), which allows data to be read from the device.

WRITE CYCLE

A combination of R/$\overline{W}$ less than V_{IL} (max), and $\overline{CE}$ less than V_{IL} (max), defines a write cycle. The state of $\overline{OE}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{OE}$ is greater than V_{IH} (min), or when R/$\overline{W}$ is less than V_{IL} (max).

WRITE OPERATION

Write Cycle 1, the Write Enable-controlled Access shown in figure 4a, is defined by a write terminated by R/$\overline{W}$ going high with $\overline{CE}$ active. The write pulse width is defined by t_{PWE} when the write is initiated by R/$\overline{W}$, and by t_{SCE} when the write is initiated by $\overline{CE}$ going active. Unless the outputs have been previously placed in the high-impedance state by $\overline{OE}$, the user must wait t_{HZOE} before applying data to the eight/nine bidirectional pins I/O(0:7/0:8) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access shown in figure 4b, is defined by a write terminated by $\overline{CE}$ going inactive. The write pulse width is defined by t_{PWE} when the write is initiated by R/$\overline{W}$, and by t_{SCE} when the write is initiated by $\overline{CE}$ going active. For the R/$\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{OE}$, the user must wait t_{HZWE} before applying data to the eight/nine bidirectional pins I/O(0:7/0:8) to avoid bus contention.

If a location is being written by one port and the opposite port attempts to read that location, a port-to-port flow through delay must be met before the data is read on the output. Data will be valid on the port wishing to read the location ($t_{BZA} + t_{BDD}$) after the data is written on the other port (see figure 5a).

READ OPERATION

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted (see figures 3a and 3b).

MASTER/SLAVE

A M/$\overline{S}$ pin is provided in order to expand the word width by configuring the device as either a master or a slave. The $\overline{BUSY}$ output of the master is connected to the $\overline{BUSY}$ input of the slave. Writing of slave devices must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation. When presented as a HIGH input, the M/$\overline{S}$ pin allows the device to be used as a master and, therefore, the $\overline{BUSY}$ line is an output. $\overline{BUSY}$ can then be used to send the arbitration outcome to a slave. When presented as a LOW input, the M/$\overline{S}$ pin allows the device to be used as a slave, and, therefore, the $\overline{BUSY}$ pin is an input.

Table 1. Non-Contending Read/Write

INPUTS			OUTPUTS	
$\overline{CE}$	**R/$\overline{W}$**	**$\overline{OE}$**	**I/O_{0-7}**	**OPERATION**
H	X	X	High Z	Power Down
X	X	H	High Z	I/O Lines Disabled
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	X	X	---	Illegal Condition

RADIATION HARDNESS

The UT7C138/139 incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Table 2. Radiation Hardness Design Specifications[1]

Total Dose	1.0E6	rads(Si)
LET Threshold	85	MeV-cm^2/mg
Neutron Fluence[2]	3.0E14	n/cm^2
Memory Device Cross Section @ LET = 120MeV-cm^2/mg	$\leq$ 1.376E^{-2} (4Kx8) $\leq$ 1.548E^{-2} (4Kx9)	cm^2

Notes:
1. The DPRAM will not latchup during radiation exposure under recommended operating conditions.
2. Not tested for CMOS technology.

ABSOLUTE MAXIMUM RATINGS[1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5 to (V_{DD} + 0.3)V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	2.0W
T_J	Maximum junction temperature[2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case[3]	3.3°C/W
I_I	DC input current	±10 mA

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Maximum junction temperature may be increased to +175°C during burn-in and steady-static life.
3. Test per MIL-STD-883, Method 1012, infinite heat sink.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_{DD} = 5.0V ±10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage	(CMOS)	$0.7V_{DD}$		V
V_{IL}	Low-level input voltage	(CMOS)		$0.3V_{DD}$	V
V_{OL}	Low-level output voltage	I_{OL} = 8mA, V_{DD} = 4.5V (TTL)		0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)		0.05	V
V_{OH}	High-level output voltage	I_{OH} = -4mA, V_{DD} = 4.5V (TTL)	2.4		V
V_{OH}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)	4.45		V
C_{IN}[1]	Input capacitance	f = 1MHz @ 0V		25	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz @ 0V		25	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-10	10	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{G}$ = 5.5V	-10	10	µA
I_{OS}[2,3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
$I_{DD}(OP)$[4,5]	Supply current operating (both ports) @ 22.2MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		300	mA
$I_{DD}(OP)$[4,6]	Supply current operating (single port) @ 22.2 MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		150	mA
$I_{DD}(OP)$[4,5]	Supply current operating (both ports) @ 18.2MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		275	mA
$I_{DD}(OP)$[4,6]	Supply current operating (single port) @ 18.2 MHz	CMOS inputs (I_{OUT} = 0) V_{DD} = 5.5V		138	mA
$I_{DD}(SB)$[4]	Supply current standby	CMOS inputs (I_{OUT} = 0) $\overline{CE}$ = V_{DD} - 0.5, V_{DD} = 5.5V		1	mA

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. V_{IH} = 5.5V, V_{IL} = 0V.
5. I_{DD} (OP) derates at 6.4mA/MHz.
6. I_{DD} (OP) derates at 3.4mA/MHz.

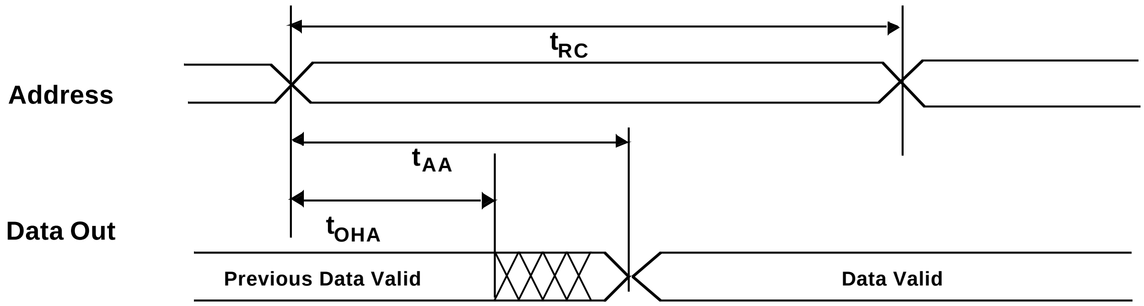
AC CHARACTERISTICS READ CYCLE [1,2]

(V_{DD} = 5.0V±10%)

SYMBOL	PARAMETER	7C138 - 45 7C139 - 45 MIN	 MAX	7C138 - 55 7C139 - 55 MIN	 MAX	UNIT
t_{RC}	Read cycle time	45		55		ns
t_{AA}	Address to data valid[2]		45		55	ns
t_{OHA}	Output hold from address change	5		5		ns
t_{ACE}	$\overline{CE}$ LOW to data valid[2]		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid[2]		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z		20		20	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z	0		0		ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z		20		20	ns

Notes:

1. Test conditions assume signal transition time of 5ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0.5V to V_{DD}-0.5V, and output loading of the specified I_{OL}/I_{OH} and 50-pF load capacitance.
2. AC test conditions use $V_{OH}/V_{OL}=V_{DD}/2 \pm 500mV$.

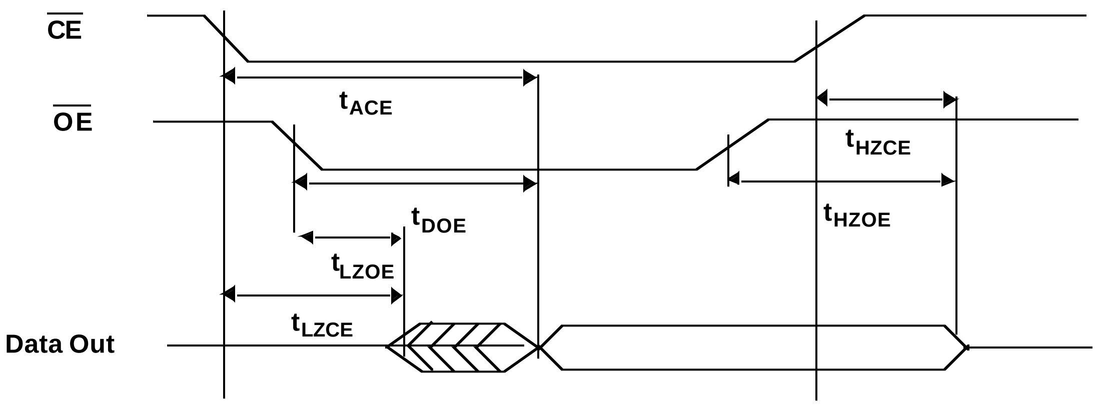


Assumptions:

1.R/W is HIGH for read cycle

2.Device is continuously selected $\overline{CE}$=LOW and $\overline{OE}$=LOW

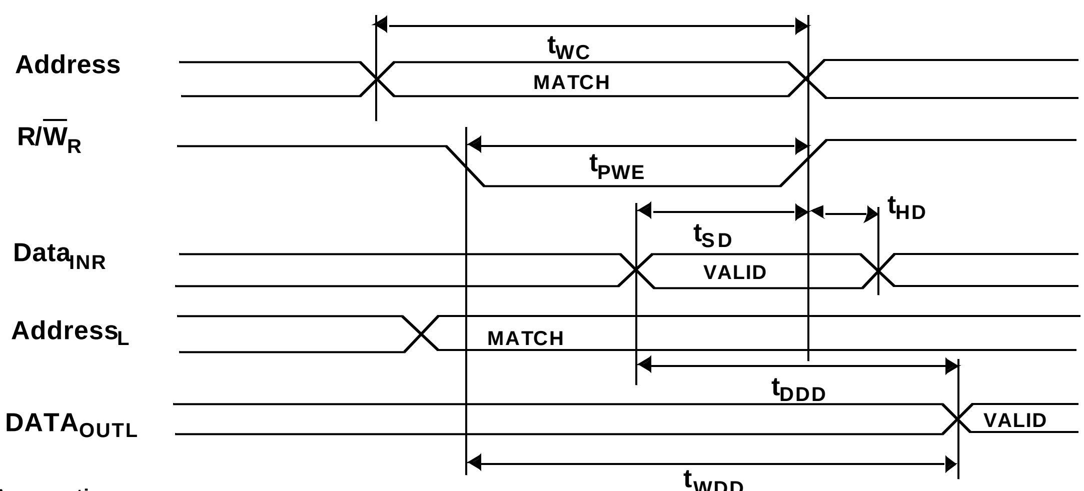
Figure 3a. Read Cycle 1



Assumptions:

1. Address valid prior to or coincident with $\overline{CE}$ transition LOW
2. R/W is HIGH for read cycle

Figure 3b. Read Cycle 2



Assumptions:

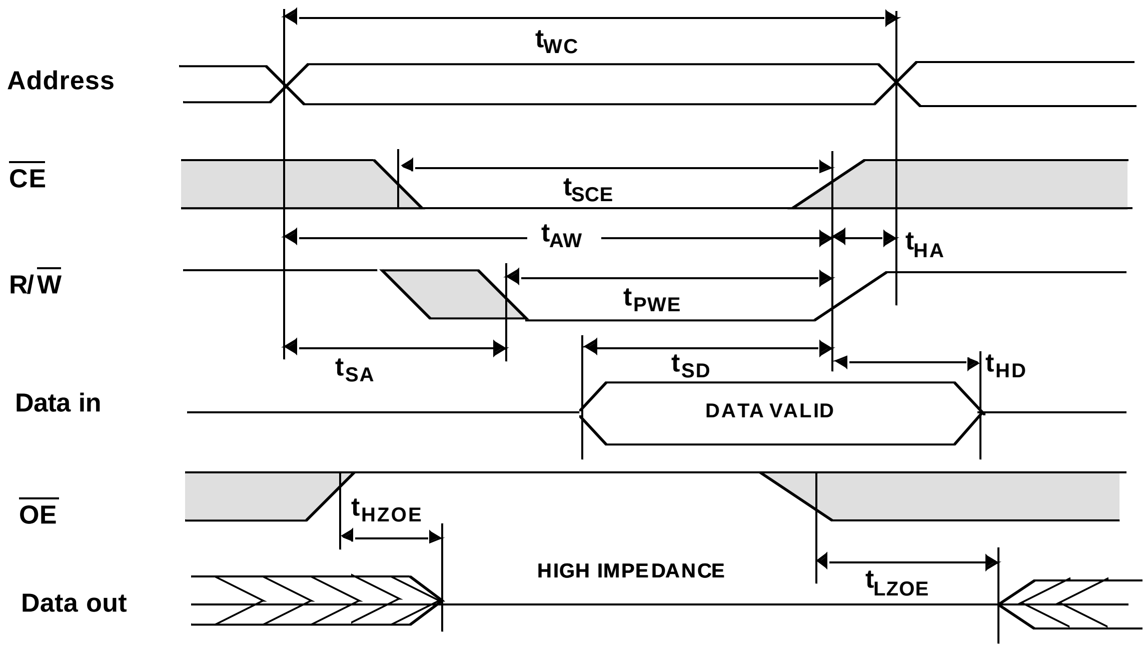
1. BUSY = HIGH for the writing port
2. $CE_L = CE_R$ = LOW

Figure 3c. Read Timing with Port-to-Port Delay

AC CHARACTERISTICS WRITE CYCLE[1]
(V_{DD} = 5.0V±10%)

SYMBOL	PARAMETER	7C138 - 45 7C139 - 45 MIN	MAX	7C138 - 55 7C139 - 55 MIN	MAX	UNIT
t_{WC}	Write cycle time	45		55		ns
t_{SCE}	$\overline{CE}$ LOW to write end	40		50		ns
t_{AW}	Address set-up to write end	40		50		ns
t_{HA}	Address hold from write end	0		0		ns
t_{SA}	Address set-up to write start	0		0		ns
t_{PWE}	Write pulse width	40		50		ns
t_{SD}	Data set-up to write end	40		50		ns
t_{HD}	Data hold from write end	0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to high Z		20		20	ns
t_{LZWE}	R/$\overline{W}$ HIGH to low Z	0		0		ns
t_{WDD}	Write pulse to data delay	95		105		ns
t_{DDD}	Write data valid to read data valid	95		105		ns
t_{WHWL}	Write disable time	5		5		ns

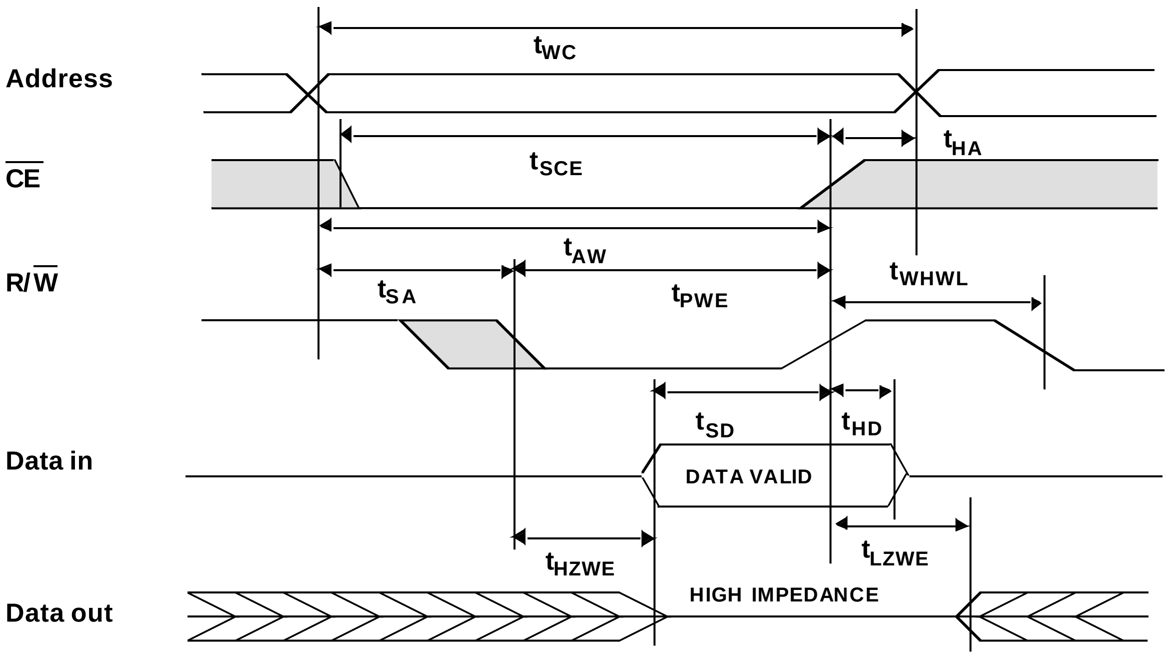
Notes:
1. For information on part-to-part delay through DPRAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform (see figure 3c).



Assumptions:

1. The internal write time of memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
3. R/$\overline{W}$ must be HIGH during all address transactions.

Figure 4a. Write Cycle 1: $\overline{OE}$ Three-States Data I/Os (Either Port)



Assumptions:

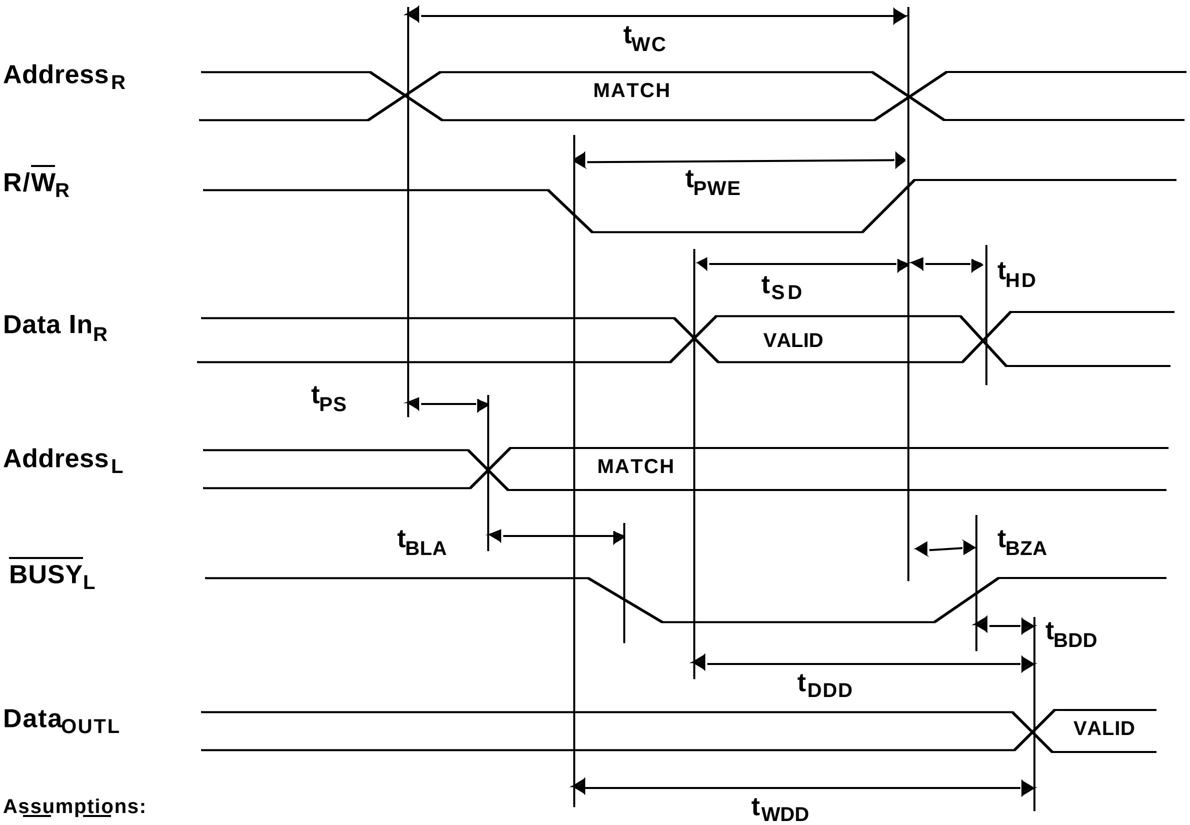
1. The internal write time of memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initialize a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. R/$\overline{W}$ must be HIGH during all address transactions.
3. Data I/O pins enter high impedance even if $\overline{OE}$ is held LOW during write.

Figure 4b. Write Cycle 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)

AC CHARACTERISTICS BUSY CYCLE [1]
(V_{DD} = 5.0V±10%)

SYMBOL	PARAMETER	7C138 - 45 7C139 - 45 MIN	MAX	7C138 - 55 7C139 - 55 MIN	MAX	UNIT
t_{BLA}	$\overline{\text{BUSY}}$ LOW from address match		25		30	ns
t_{BZA}	$\overline{\text{BUSY}}$ HIGH-Z from address mismatch		25		30	ns
t_{BLC}	$\overline{\text{BUSY}}$ LOW from $\overline{\text{CE}}$ LOW		25		30	ns
t_{BZC}	$\overline{\text{BUSY}}$ HIGH from $\overline{\text{CE}}$ HIGH		25		30	ns
t_{PS}[2,3]	Port set-up for priority	5		5		ns
t_{WB}	R/$\overline{\text{W}}$ LOW after $\overline{\text{BUSY}}$ LOW	0		0		ns
t_{WH}	R/$\overline{\text{W}}$ HIGH after $\overline{\text{BUSY}}$ HIGH	40		50		ns
t_{BDD}	$\overline{\text{BUSY}}$ HIGH to data valid		45		55	ns

Notes:
1. Test conditions assume signal transition time of 5ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0.5V to V_{DD}-0.5V, and output loading of the specified I_{OL}/I_{OH} and 50-pF load capacitance.
2. Violation of t_{PS} (with addresses matching) results in at least one of the two busy output signals asserting, only one port remains busy.
3. When violating t_{PS}, the busy signal asserts on one port or the other; there is no guarantee on which port the busy signal asserts.



Assumptions:

1. $\overline{CE_L} = \overline{CE_R}$ = LOW

Figure 5a. Read Timing with $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$=HIGH)

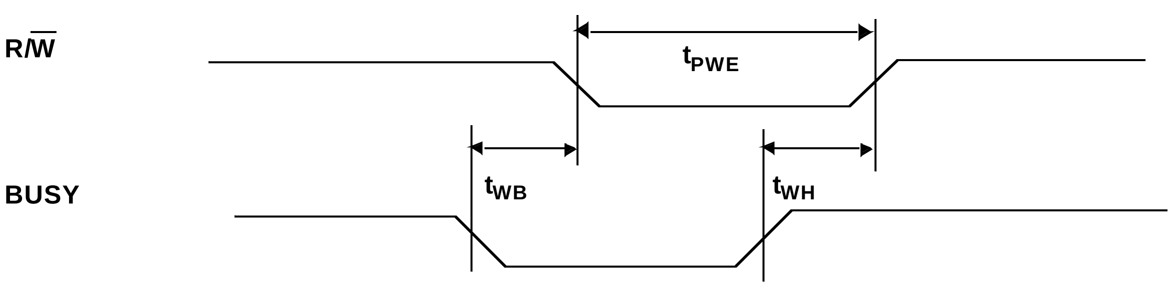
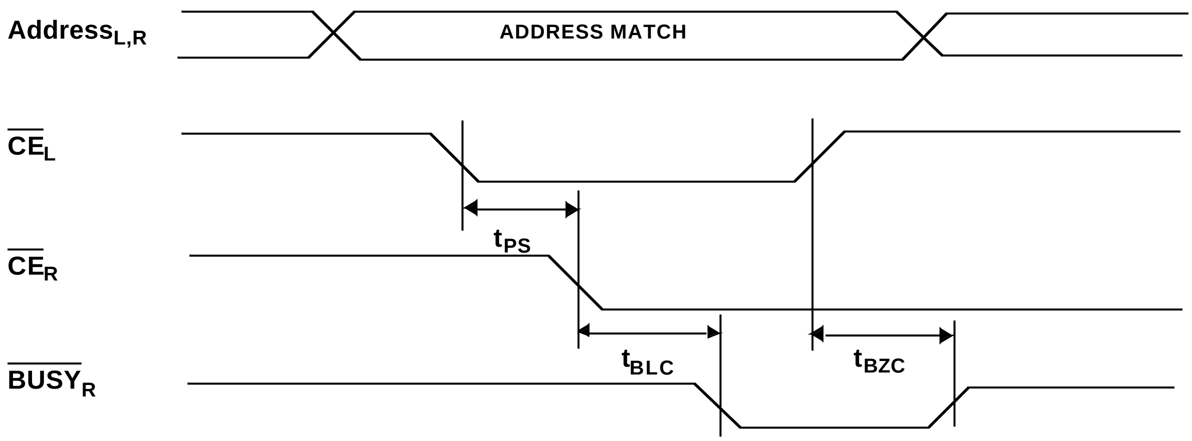
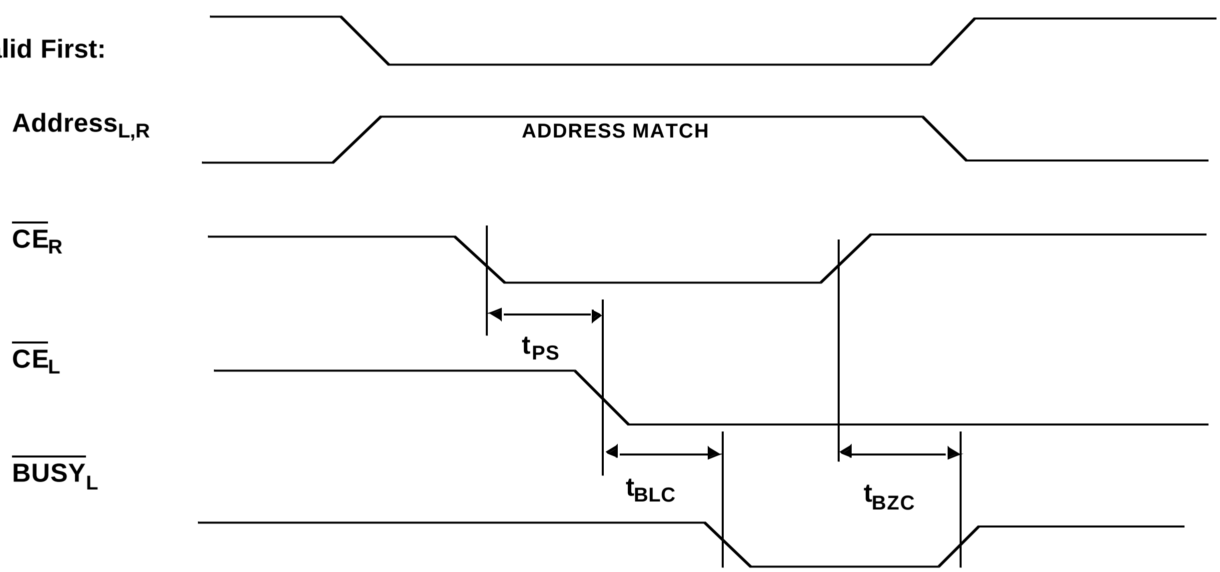


Figure 5b. Write Timing with $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$=LOW)

$\overline{CE}_L$ Valid First:



$\overline{CE}_R$ Valid First:

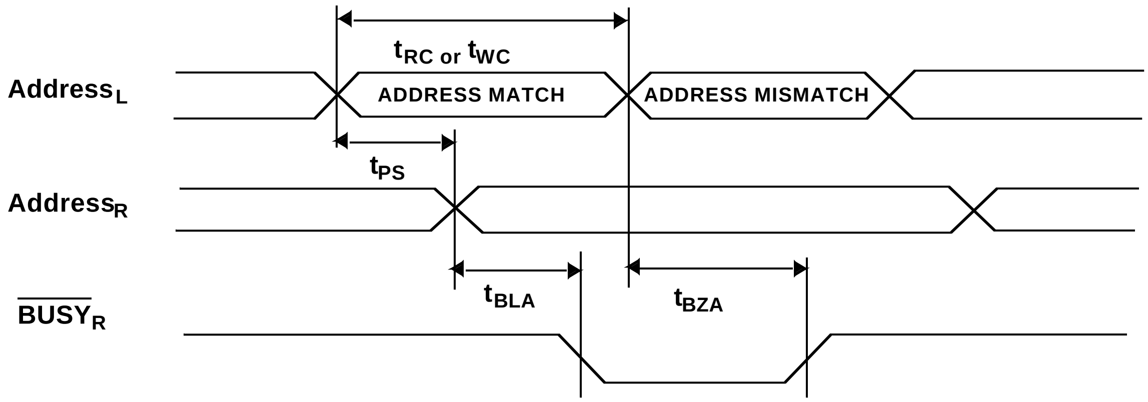


Assumptions:

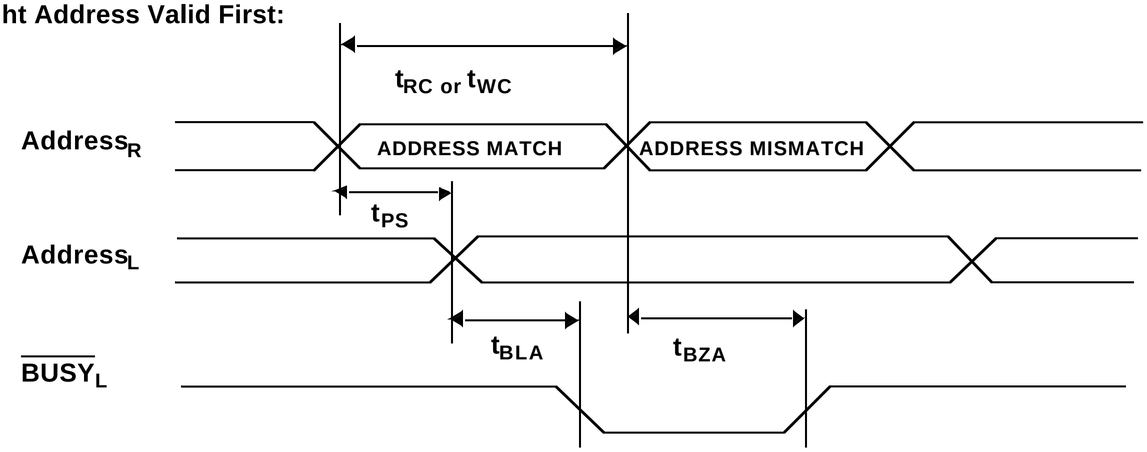
1. If t_{PS} is violated, the $\overline{BUSY}$ signal will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted.

Figure 5c. BUSY Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

Left Address Valid First:



Right Address Valid First:



Assumptions:

1. If t_{PS} is violated, the $\overline{\text{BUSY}}$ signal will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted.

Figure 5d. BUSY Timing Diagram No. 2 (Address Arbitration)

DATA RETENTION CHARACTERISTICS (Pre-Radiation)
(T_C = 25°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM V_{DD} @ 2.5V	UNIT
V_{DR}	V_{DD} for data retention	2.5	--	V
I_{DDR}[1]	Data retention current	--	400	µA
t_{EFR}[1,2]	Chip deselect to data retention time	0		ns
t_R[1,2]	Operation recovery time	t_{WC} or t_{RC}		ns

Notes:
1. CE equals V_{DR}, all other inputs equal V_{DR} or V_{SS}.
2. Guaranteed but not tested.

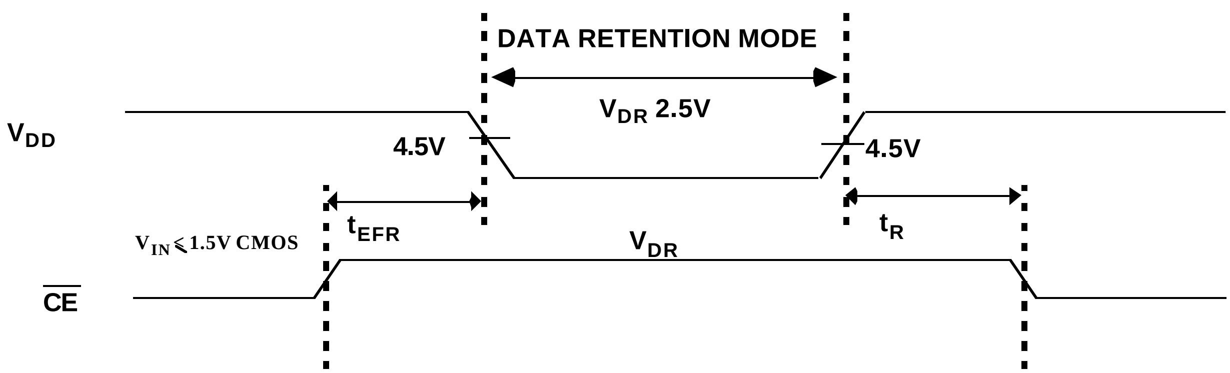
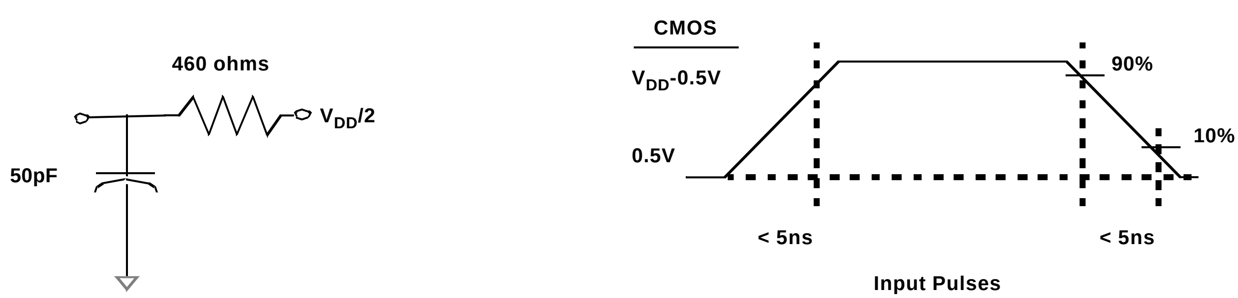
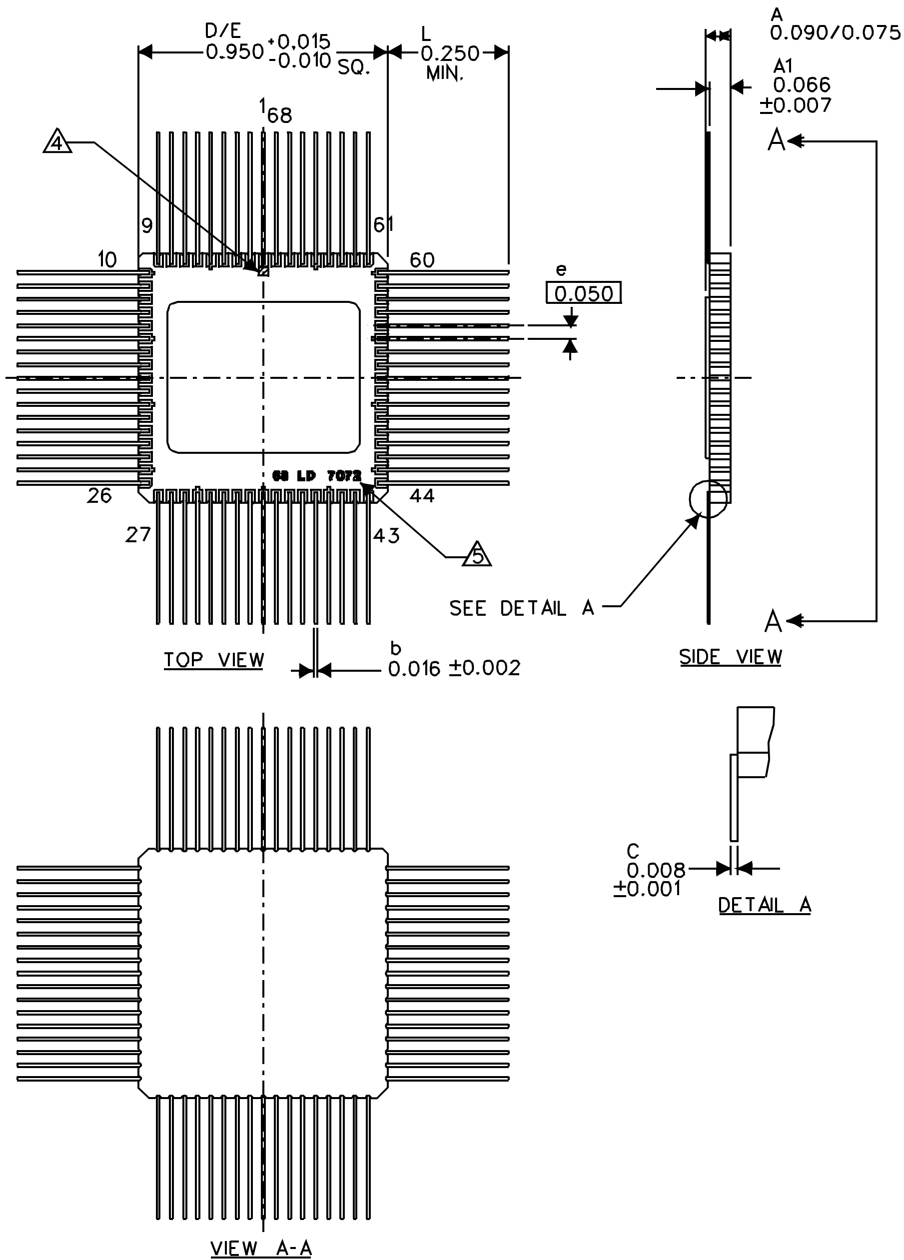


Figure 6. Low V_{DD} Data Retention Waveform



Notes:
1. 50pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point (CMOS input = V_{DD}/2).

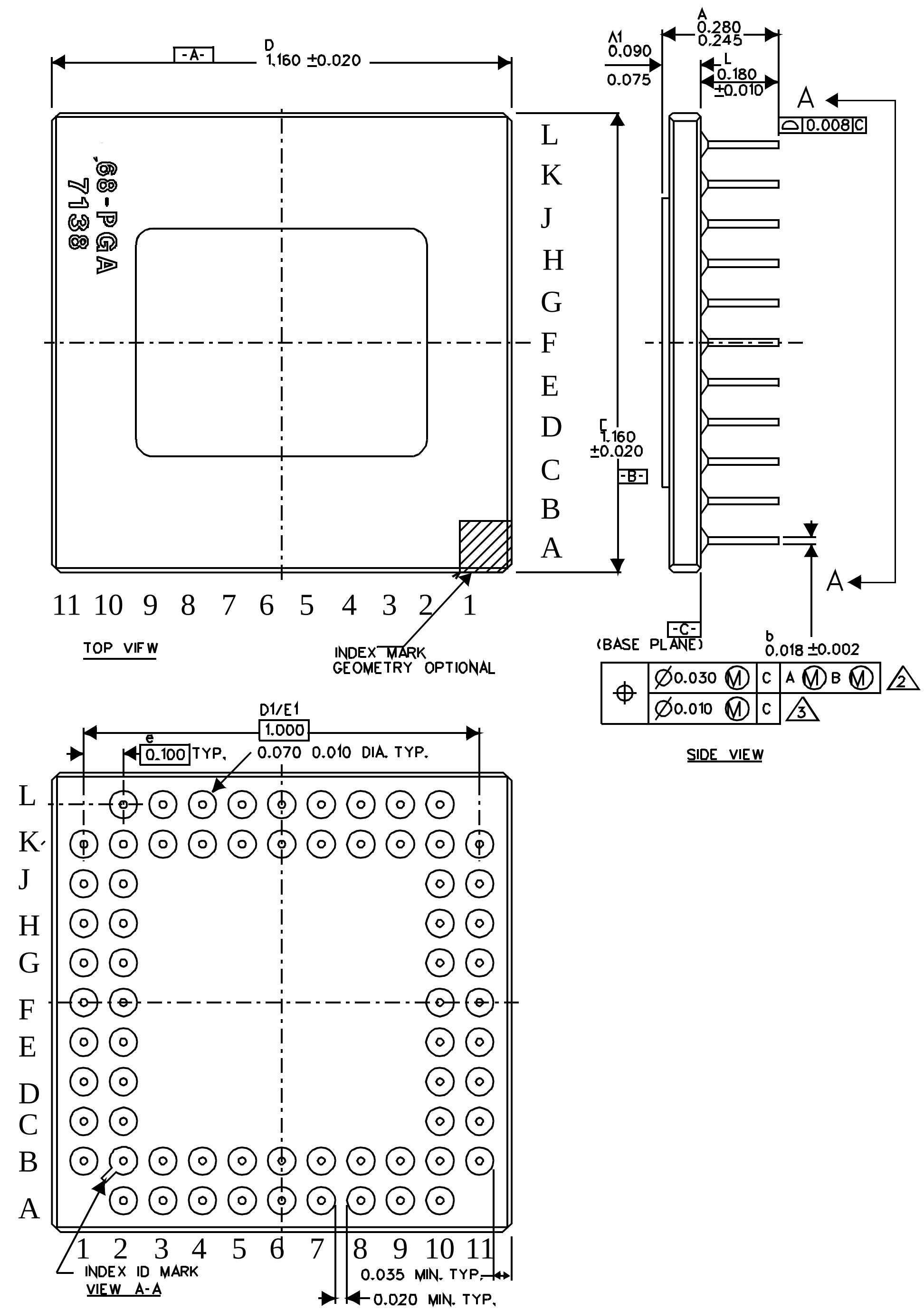
Figure 7. AC Test Loads and Input Waveforms



Notes:

1. All package finishes are per MIL-PRF-38535.
2. Letter designations are for cross-reference to MIL-STD-1835.
3. All leads increase max limit by 0.003 measured at the center of the flat, when lead finish A (solder) is applied.
4. ID mark: Configuration is optional.
5. Lettering is not subject to marking criteria.
6. Total weight is approximately 4.5 grams.

Figure 8. 68-lead Flatpack



Notes:

1. All packages finishes are per MIL-PRF-38535.
2. True position applies at base plane (Datum C).
3. True position applies at pin tips.
4. Letter designations are for cross-reference to MIL-STD-1835.
5. Total weight is approximately 7.0 grams.

Figure 9. 68-pin PGA

ORDERING INFORMATION

UT7C138/UT7C139 Dual-Port SRAM: SMD

5962 * 96845 * * * *

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Case Outline:
(X) = 68-pin PGA
(Y) = 68-lead Flatpack

Class Designator:
(Q) = Class Q
(V) = Class V

Device Type
(01) = 4Kx8, CMOS Compatible Inputs, 45ns
(02) = 4Kx9, CMOS Compatible Inputs, 45ns
(03) = 4Kx8, CMOS Compatible Inputs, 55ns
(04) = 4Kx9, CMOS Compatible Inputs, 55ns

Drawing Number: 96845

Total Dose:
(H) = 1E6 rads(Si)
(G) = 5E5 rads(Si)
(F) = 3E5 rads(Si)
(R) = 1E5 rads(Si)

Federal Stock Class Designator: No options

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an “X” is specified when ordering, part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

UT7C138/UT7C139 Dual-Port SRAM

UT **** * ** * * * *

Total Dose:
( ) = None

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Screening:
(C) = Military Temperature Range flow
(P) = Prototype flow

Package Type:
(G) = 68-lead PGA
(W) = 68-lead Flatpack

Access Time:
(45) = 45ns access time
(55) = 55ns access time

Device Type Modifier:
(C) = CMOS-compatible Inputs, 5.0V operation

Device Type:
(7C138) = 4Kx8 Dual-Port SRAM
(7C139) = 4Kx9 Dual-Port SRAM

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an “X” is specified when ordering, then the part marking will match the lead finish and will be either “A” (solder) or “C” (gold).
3. Military Temperature Range flow per UTMC Manufacturing Flows Document. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototypes are produced to UTMC’s prototype flow and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed. Lead finish is GOLD only.

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