VMX51C900

Datasheet *Rev 1.2*

Versa Mix 8051 MCU with LCD Controller and ADC

Overview

The VMX51C900 is an 8-bit microcontroller with 8KB of Flash memory, 256 bytes of RAM and based on the architecture of the standard 80C51 microcontroller.

The VMX51C900 includes extra features such as a 4 Channel 8-bit A/D Converter, 2 PWM outputs and 14 segment x 4 common LCD driver. The VMX51C900 hardware features make it a versatile and cost-effective controller for a wide range of embedded applications.

The Flash memory can be programmed using a parallel programmer available from Ramtron. Support is also available from 3rd party commercial programmer manufacturers.

The VMX51C900 is available in PLCC-44, QFP-44 and DIP-40 packages and operates over the industrial temperature range.

Features

- 80C51/80C52 pin compatible
- 8KB on-chip Flash memory
- 256 Bytes on-chip data RAM
- 4 8-bit I/O ports and 1 4-bit I/O port
- 4-Channel, 8-bit A/D Converter
- LCD Driver: 14-Segment x 4-Common
- 2-PWM Outputs
- UART serial port
- 3 16-bit Timers/Counters
- Watchdog Timer
- BCD arithmetic + 8-bit Unsigned Multiply and Division
- 2 levels of Interrupt Priority and nested Interrupts
- Power saving modes
- Low EMI (ALE disable)
- Code protection function
- Operates at a clock frequency of up to 25MHz
- Industrial Temperature range (-40°C to +85°C)
- 5V version available

FIGURE 1: VMX51C900 BLOCK DIAGRAM

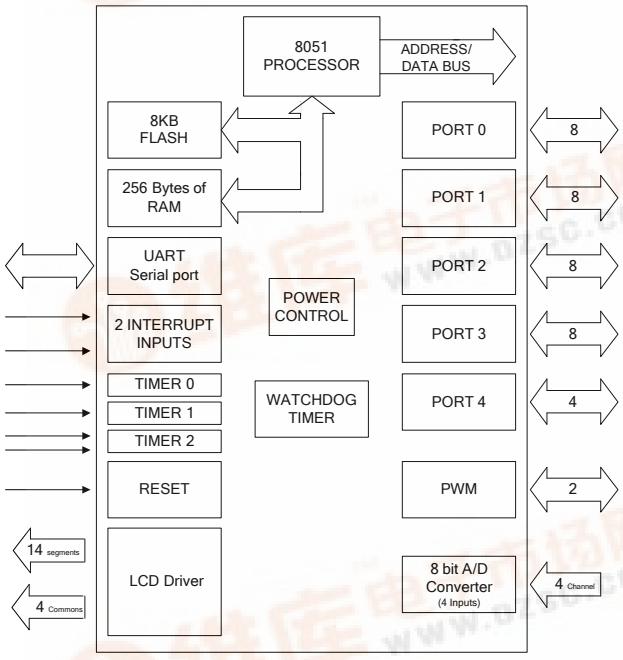
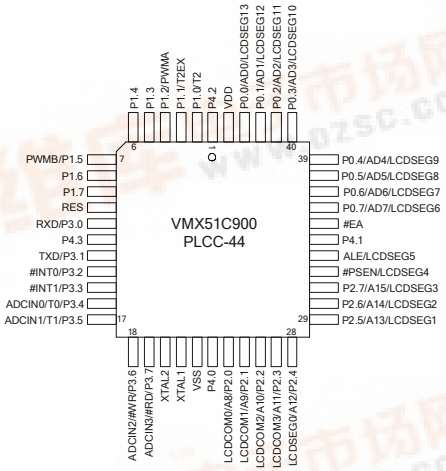
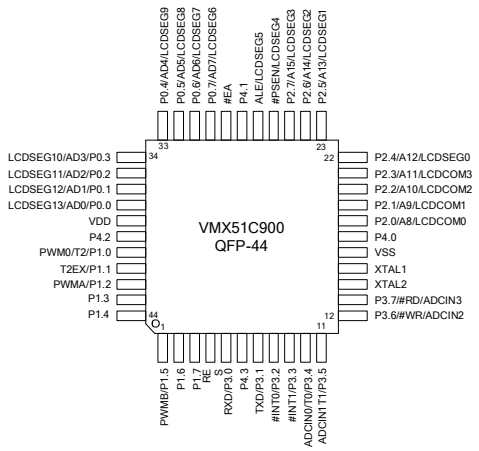


FIGURE 2: VMX51C900 PLCC-44 AND QFP-44 PIN OUT DIAGRAMS





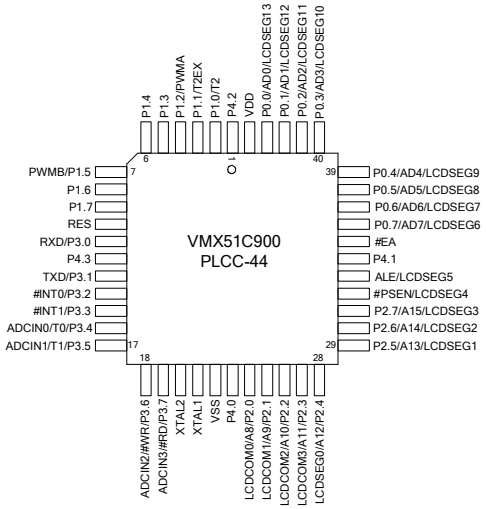
	A9	O	Bit 9 of Ext. Memory Address
26	LCDCOM2	-	LCD Driver Common 2
	P2.2	I/O	Bit 2 of Port 2
	A10	O	Bit 10 of Ext. Memory Address
27	LCDCOM3	-	LCD Driver Common 3
	P2.3	I/O	Bit 3 of Port 2 &
	A11	O	Bit 11 of Ext. Memory Address
28	LCDSEG0	-	LCD Segment 0
	P2.4	I/O	Bit 4 of Port 2
	A12	O	Bit 12 of Ext. Memory Address
29	LCDSEG1	-	LCD Segment 1
	P2.5	I/O	Bit 5 of Port 2
	A13	O	Bit 13 of External Memory Address
30	LCDSEG2	-	LCD Segment 2
	P2.6	I/O	Bit 6 of Port 2
	A14	O	Bit 14 of External Memory Address

Pin Descriptions for PLCC-44

TABLE 1: PIN DESCRIPTIONS FOR PLCC-44

PLCC - 44	Name	I/O	Function
1	P4.2	I/O	Bit 2 of Port 4
2	T2	I	Timer 2 Clock Out
	P1.0	I/O	Bit 0 of Port 1
3	T2EX	I	Timer 2 Control
	P1.1	I/O	Bit 1 of Port 1
4	P1.2	I/O	Bit 2 of Port 1
	PWMA	O	PWM Channel A
5	P1.3	I/O	Bit 3 of Port 1
6	P1.4	I/O	Bit 4 of Port 1
7	PWMB	O	PWM Channel B
	P1.5	I/O	Bit 5 of Port 1
8	P1.6	I/O	Bit 6 of Port 1
9	P1.7	I/O	Bit 7 of Port 1
10	RES	I	Reset
11	RXD	I	Receive Data
	P3.0	I/O	Bit 0 of Port 3
12	P4.3	I/O	Bit 3 of Port 4
13	TXD	O	Transmit Data &
	P3.1	I/O	Bit 1 of Port 3
14	#INT0	I	External Interrupt 0
	P3.2	I/O	Bit 2 of Port 3
15	#INT1	I	External Interrupt 1
	P3.3	I/O	Bit 3 of Port 3
16	ADCIN0	Ain	ADC input 0
	T0	I	Timer 0
	P3.4	I/O	Bit 4 of Port 3
17	ADCIN1	Ain	ADC input 1
	T1	I	Timer 1 & 3
	P3.5	I/O	Bit 5 of Port
18	ADCIN2	Ain	ADC input 2
	#WR	O	Ext. Memory Write
	P3.6	I/O	Bit 6 of Port 3
19	ADCIN3	Ain	ADC input 3
	#RD	O	Ext. Memory Read
	P3.7	I/O	Bit 7 of Port 3
20	XTAL2	O	Oscillator/Crystal Output
21	XTAL1	I	Oscillator/Crystal In
22	VSS	-	Ground
23	P4.0	I/O	Bit 0 of Port 4
24	LCDCOM0	-	LCD Driver Common 0
	P2.0	I/O	Bit 0 of Port 2
	A8	O	Bit 8 of Ext. Memory Address
25	LCDCOM1	-	LCD Driver Common 1
	P2.1	I/O	Bit 1 of Port 2

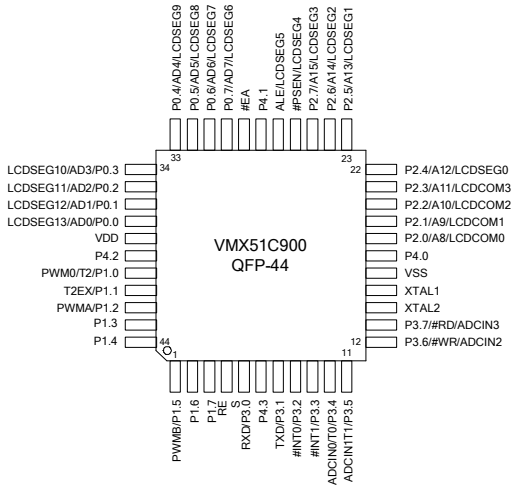
PLCC - 44	Name	I/O	Function
31	LCDSEG3	-	LCD Segment 3
	P2.7	I/O	Bit 7 of Port 2
	A15	O	Bit 15 of External Memory Address
32	LCDSEG4	-	LCD Segment 4
	#PSEN	O	Program Store Enable
33	LCDSEG5	-	LCD Segment 5
	ALE	O	Address Latch Enable
34	P4.1	I/O	Bit 1 of Port 4
35	#EA	I	External Access
36	LCDSEG6	-	LCD Segment 6
	P0.7	I/O	Bit 7 Of Port 0
	AD7	I/O	Data/Address Bit 7 of Ext. Memory
37	LCDSEG7	-	LCD Segment 7
	P0.6	I/O	Bit 6 of Port 0
	AD6	I/O	Data/Address Bit 6 of Ext. Memory
38	LCDSEG8	-	LCD Segment 8
	P0.5	I/O	Bit 5 of Port 0
	AD5	I/O	Data/Address Bit 5 of Ext. Memory
39	LCDSEG9	-	LCD Segment 9
	P0.4	I/O	Bit 4 of Port 0
	AD4	I/O	Data/Address Bit 4 of Ext. Memory
40	LCDSEG10	-	LCD Segment 10
	P0.3	I/O	Bit 3 Of Port 0
	AD3	I/O	Data/Address Bit 3 of Ext. Memory
41	LCDSEG11	-	LCD Segment 11
	P0.2	I/O	Bit 2 of Port 0
	AD2	I/O	Data/Address Bit 2 of Ext. Memory
42	LCDSEG12	-	LCD Segment 12
	P0. 1	I/O	Bit 1 of Port 0 & Data
	AD1	I/O	Address Bit 1 of Ext. Memory
43	LCDSEG13	-	LCD Segment 13
	P0.0	I/O	Bit 0 Of Port 0 & Data
	AD0	I/O	Address Bit 0 of Ext. Memory
44	VDD	-	5V supply


P1.4
P1.3
P1.2/PWMA
P1.1/T2EX
P1.0/T2
P4.2
VDD
P0.0/AD0/LCDSEG13
P0.1/AD1/LCDSEG12
P0.2/AD2/LCDSEG11
P0.3/AD3/LCDSEG10
6
1
40
PWMB/P1.5
7
39
P1.6
P1.7
RES
RXD/P3.0
P4.3
TXD/P3.1
#INT0/P3.2
#INT1/P3.3
ADCIN0/T0/P3.4
ADCIN1/T1/P3.5
17
29
18
28
VMX51C900
PLCC-44
P0.4/AD4/LCDSEG9
P0.5/AD5/LCDSEG8
P0.6/AD6/LCDSEG7
P0.7/AD7/LCDSEG6
#EA
P4.1
ALE/LCDSEG5
#PSEN/LCDSEG4
P2.7/A15/LCDSEG3
P2.6/A14/LCDSEG2
P2.5/A13/LCDSEG1
ADCIN2/#WR/P3.6
ADCIN3/#RD/P3.7
XTAL2
XTAL1
VSS
P4.0
LCDCOM0/A8/P2.0
LCDCOM1/A9/P2.1
LCDCOM2/A10/P2.2
LCDCOM3/A11/P2.3
LCDSEG0/A12/P2.4

Pin Descriptions for QFP-44

TABLE 2: PIN DESCRIPTIONS FOR QFP-44

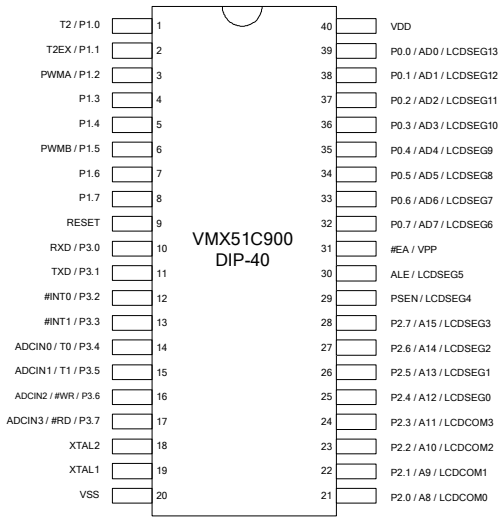
PLCC - 44	Name	I/O	Function
1	PWMB	O	PWM Channel B
	P1.5	I/O	Bit 5 of Port 1
2	P1.6	I/O	Bit 6 of Port 1
3	P1.7	I/O	Bit 7 of Port 1
4	RES	I	Reset
5	RXD	I	Receive Data
	P3.0	I/O	Bit 0 of Port 3
6	P4.3	I/O	Bit 3 of Port 4
7	TXD	O	Transmit Data &
	P3.1	I/O	Bit 1 of Port 3
8	#INT0	I	External Interrupt 0
	P3.2	I/O	Bit 2 of Port 3
9	#INT1	I	External Interrupt 1
	P3.3	I/O	Bit 3 of Port 3
10	ADCIN0	Ain	ADC input 0
	T0	I	Timer 0
	P3.4	I/O	Bit 4 of Port 3
11	ADCIN1	Ain	ADC input 1
	T1	I	Timer 1 & 3
	P3.5	I/O	Bit 5 of Port
12	ADCIN2	Ain	ADC input 2
	#WR	O	Ext. Memory Write
	P3.6	I/O	Bit 6 of Port 3
13	ADCIN3	Ain	ADC input 3
	#RD	O	Ext. Memory Read
	P3.7	I/O	Bit 7 of Port 3
14	XTAL2	O	Oscillator/Crystal Output
15	XTAL1	I	Oscillator/Crystal In
16	VSS	-	Ground
17	P4.0	I/O	Bit 0 of Port 4
18	LCDCOM0	-	LCD Driver Common 0
	P2.0	I/O	Bit 0 of Port 2
	A8	O	Bit 8 of Ext. Memory Address
19	LCDCOM1	-	LCD Driver Common 1
	P2.1	I/O	Bit 1 of Port 2
	A9	O	Bit 9 of Ext. Memory Address
20	LCDCOM2	-	LCD Driver Common 2
	P2.2	I/O	Bit 2 of Port 2
	A10	O	Bit 10 of Ext. Memory Address
21	LCDCOM3	-	LCD Driver Common 3
	P2.3	I/O	Bit 3 of Port 2 &
	A11	O	Bit 11 of Ext. Memory Address
22	LCDSEG0	-	LCD Segment 0
	P2.4	I/O	Bit 4 of Port 2
	A12	O	Bit 12 of Ext. Memory Address
23	LCDSEG1	-	LCD Segment 1
	P2.5	I/O	Bit 5 of Port 2
	A13	O	Bit 13 of External Memory Address
24	LCDSEG2	-	LCD Segment 2
	P2.6	I/O	Bit 6 of Port 2
	A14	O	Bit 14 of External Memory Address
25	LCDSEG3	-	LCD Segment 3
	P2.7	I/O	Bit 7 of Port 2
	A15	O	Bit 15 of External Memory Address
26	LCDSEG4	-	LCD Segment 4
	#PSEN	O	Program Store Enable
27	LCDSEG5	-	LCD Segment 5
	ALE	O	Address Latch Enable
28	P4.1	I/O	Bit 1 of Port 4
29	#EA	I	External Access
30	LCDSEG6	-	LCD Segment 6
	P0.7	I/O	Bit 7 Of Port 0
	AD7	I/O	Data/Address Bit 7 of Ext. Memory
31	LCDSEG7	-	LCD Segment 7
	P0.6	I/O	Bit 6 of Port 0
	AD6	I/O	Data/Address Bit 6 of Ext. Memory
32	LCDSEG8	-	LCD Segment 8
	P0.5	I/O	Bit 5 of Port 0
	AD5	I/O	Data/Address Bit 5 of Ext. Memory
33	LCDSEG9	-	LCD Segment 9
	P0.4	I/O	Bit 4 of Port 0
	AD4	I/O	Data/Address Bit 4 of Ext. Memory
34	LCDSEG10	-	LCD Segment 10
	P0.3	I/O	Bit 3 Of Port 0
	AD3	I/O	Data/Address Bit 3 of Ext. Memory
35	LCDSEG11	-	LCD Segment 11
	P0.2	I/O	Bit 2 of Port 0
	AD2	I/O	Data/Address Bit 2 of Ext. Memory
36	LCDSEG12	-	LCD Segment 12
	P0. 1	I/O	Bit 1 of Port 0 & Data
	AD1	I/O	Address Bit 1 of Ext. Memory
37	LCDSEG13	-	LCD Segment 13
	P0.0	I/O	Bit 0 Of Port 0 & Data
	AD0	I/O	Address Bit 0 of Ext. Memory
38	VDD	-	5V supply
39	P4.2	I/O	Bit 2 of Port 4
40	T2	I	Timer 2 Clock Out
	P1.0	I/O	Bit 0 of Port 1
41	T2EX	I	Timer 2 Control
	P1.1	I/O	Bit 1 of Port 1
42	P1.2	I/O	Bit 2 of Port 1
	PWMA	O	PWM Channel A
43	P1.3	I/O	Bit 3 of Port 1
44	P1.4	I/O	Bit 4 of Port 1



DIP-40 Pin Descriptions

TABLE 3: VMX51C900 PIN DESCRIPTIONS FOR DIP40 PACKAGE

DIP - 40	Name	I/O	Function
1	T2	I	Timer 2 Clock Out
	P1.0	I/O	Bit 0 of Port 1
2	T2EX	I	Timer 2 Control
	P1.1	I/O	Bit 1 of Port 1
3	P1.2	I/O	Bit 2 of Port 1
	PWMA	O	PWM Channel A
4	P1.3	I/O	Bit 3 of Port 1
5	P1.4	I/O	Bit 4 of Port 1
6	PWMB	O	PWM Channel B
	P1.5	I/O	Bit 5 of Port 1
7	P1.6	I/O	Bit 6 of Port 1
8	P1.7	I/O	Bit 7 of Port 1
9	RES	I	Reset
10	RXD	I	Receive Data
	P3.0	I/O	Bit 0 of Port 3
11	TXD	O	Transmit Data &
	P3.1	I/O	Bit 1 of Port 3
12	#INT0	I	External Interrupt 0
	P3.2	I/O	Bit 2 of Port 3
13	#INT1	I	External Interrupt 1
	P3.3	I/O	Bit 3 of Port 3
14	ADCIN0	Ain	ADC input 0
	T0	I	Timer 0
	P3.4	I/O	Bit 4 of Port 3
15	ADCIN1	Ain	ADC input 1
	T1	I	Timer 1 & 3
	P3.5	I/O	Bit 5 of Port
16	ADCIN2	Ain	ADC input 2
	#WR	O	Ext. Memory Write
	P3.6	I/O	Bit 6 of Port 3
17	ADCIN3	Ain	ADC input 3
	#RD	O	Ext. Memory Read
	P3.7	I/O	Bit 7 of Port 3
18	XTAL2	O	Oscillator/Crystal Output
19	XTAL1	I	Oscillator/Crystal In
20	VSS	-	Ground
21	LCDCOM0	-	LCD Driver Common 0
	P2.0	I/O	Bit 0 of Port 2
	A8	O	Bit 8 of Ext. Memory Address
22	LCDCOM1	-	LCD Driver Common 1
	P2.1	I/O	Bit 1 of Port 2
	A9	O	Bit 9 of Ext. Memory Address
23	LCDCOM2	-	LCD Driver Common 2
	P2.2	I/O	Bit 2 of Port 2
	A10	O	Bit 10 of Ext. Memory Address
24	LCDCOM3	-	LCD Driver Common 3
	P2.3	I/O	Bit 3 of Port 2 &
	A11	O	Bit 11 of Ext. Memory Address
25	LCDSEG0	-	LCD Segment 0
	P2.4	I/O	Bit 4 of Port 2
	A12	O	Bit 12 of Ext. Memory Address
26	LCDSEG1	-	LCD Segment 1
	P2.5	I/O	Bit 5 of Port 2
	A13	O	Bit 13 of External Memory Address
27	LCDSEG2	-	LCD Segment 2
	P2.6	I/O	Bit 6 of Port 2
	A14	O	Bit 14 of External Memory Address
28	LCDSEG3	-	LCD Segment 3
	P2.7	I/O	Bit 7 of Port 2
	A15	O	Bit 15 of External Memory Address
29	LCDSEG4	-	LCD Segment 4
	#PSEN	O	Program Store Enable
30	LCDSEG5	-	LCD Segment 5
	ALE	O	Address Latch Enable
31	#EA	I	External Access
32	LCDSEG6	-	LCD Segment 6
	P0.7	I/O	Bit 7 Of Port 0
	AD7	I/O	Data/Address Bit 7 of Ext. Memory
33	LCDSEG7	-	LCD Segment 7
	P0.6	I/O	Bit 6 of Port 0
	AD6	I/O	Data/Address Bit 6 of Ext. Memory
34	LCDSEG8	-	LCD Segment 8
	P0.5	I/O	Bit 5 of Port 0
	AD5	I/O	Data/Address Bit 5 of Ext. Memory
35	LCDSEG9	-	LCD Segment 9
	P0.4	I/O	Bit 4 of Port 0
	AD4	I/O	Data/Address Bit 4 of Ext. Memory
36	LCDSEG10	-	LCD Segment 10
	P0.3	I/O	Bit 3 Of Port 0
	AD3	I/O	Data/Address Bit 3 of Ext. Memory
37	LCDSEG11	-	LCD Segment 11
	P0.2	I/O	Bit 2 of Port 0
	AD2	I/O	Data/Address Bit 2 of Ext. Memory
38	LCDSEG12	-	LCD Segment 12
	P0. 1	I/O	Bit 1 of Port 0 & Data
	AD1	I/O	Address Bit 1 of Ext. Memory
39	LCDSEG13	-	LCD Segment 13
	P0.0	I/O	Bit 0 Of Port 0 & Data
	AD0	I/O	Address Bit 0 of Ext. Memory
40	VDD	-	5V supply



Instruction Set

The following tables describe the instruction set of the VMX51C900. The instructions are function and binary code compatible with industry standard 8051s.

TABLE 4: LEGEND FOR INSTRUCTION SET TABLE

Symbol	Function
A	Accumulator
Rn	Register R0-R7
Direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 5: VRS570/VRS580 INSTRUCTION SET

Mnemonic	Description	Size (bytes)	Instr. Cycles	Op-Code
Arithmetic instructions				
ADD A, Rn	Add register to A	1	1	28h-2Fh
ADD A, direct	Add direct byte to A	2	1	25h
ADD A, @Ri	Add data memory to A	1	1	26h,27h
ADD A, #data	Add immediate to A	2	1	24h
ADDC A, Rn	Add register to A with carry	1	1	38h-3Fh
ADDC A, direct	Add direct byte to A with carry	2	1	35h
ADDC A, @Ri	Add data memory to A with carry	1	1	36h,37h
ADDC A, #data	Add immediate to A with carry	2	1	34h
SUBB A, Rn	Subtract register from A with borrow	1	1	98h-9Fh
SUBB A, direct	Subtract direct byte from A with borrow	2	1	95h
SUBB A, @Ri	Subtract data mem from A with borrow	1	1	96h-97h
SUBB A, #data	Subtract immediate from A with borrow	2	1	94h
INC A	Increment A	1	1	04h
INC Rn	Increment register	1	1	08h-0Fh
INC direct	Increment direct byte	2	1	05h
INC @Ri	Increment data memory	1	1	06h, 07h
DEC A	Decrement A	1	1	14h
DEC Rn	Decrement register	1	1	18h-1Fh
DEC direct	Decrement direct byte	2	1	15h
DEC @Ri	Decrement data memory	1	1	16h,17h
INC DPTR	Increment data pointer	1	2	A3h
MUL AB	Multiply A by B	1	4	A4h
DIV AB	Divide A by B	1	4	84h
DA A	Decimal adjust A	1	1	D4h
Logical Instructions				
ANL A, Rn	AND register to A	1	1	58h-5Fh
ANL A, direct	AND direct byte to A	2	1	55h
ANL A, @Ri	AND data memory to A	1	1	56-57h
ANL A, #data	AND immediate to A	2	1	54h
ANL direct, A	AND A to direct byte	2	1	52h
ANL direct, #data	AND immediate data to direct byte	3	2	53h
ORL A, Rn	OR register to A	1	1	48h-4Fh
ORL A, direct	OR direct byte to A	2	1	45h
ORL A, @Ri	OR data memory to A	1	1	46h,47h
ORL A, #data	OR immediate to A	2	1	44h
ORL direct, A	OR A to direct byte	2	1	42h
ORL direct, #data	OR immediate data to direct byte	3	2	43h
XRL A, Rn	Exclusive-OR register to A	1	1	68h-6Fh
XRL A, direct	Exclusive-OR direct byte to A	2	1	65h
XRL A, @Ri	Exclusive-OR data memory to A	1	1	66h,67h
XRL A, #data	Exclusive-OR immediate to A	2	1	64h
XRL direct, A	Exclusive-OR A to direct byte	2	1	62h
XRL direct, #data	Exclusive-OR immediate to direct byte	3	2	63h
CLR A	Clear A	1	1	E4h
CPL A	Compliment A	1	1	F4h
SWAP A	Swap nibbles of A	1	1	C4h
RL A	Rotate A left	1	1	23h
RLC A	Rotate A left through carry	1	1	33h
RR A	Rotate A right	1	1	03h
RRC A	Rotate A right through carry	1	1	13h

Mnemonic	Description	Size (bytes)	Instr. Cycles	Op Code
Boolean Instruction				
CLR C	Clear Carry bit	1	1	C3h
CLR bit	Clear bit	2	1	C2h
SETB C	Set Carry bit to 1	1	1	D3h
SETB bit	Set bit to 1	2	1	D2h
CPL C	Complement Carry bit	1	1	B3h
CPL bit	Complement bit	2	1	B2h
ANL C,bit	Logical AND between Carry and bit	2	2	82h
ANL C,#bit	Logical AND between Carry and not bit	2	2	A0h,B0h
ORL C,bit	Logical ORL between Carry and bit	2	2	72h
ORL C,#bit	Logical ORL between Carry and not bit	2	2	A0h
MOV C,bit	Copy bit value into Carry	2	1	A2h
MOV bit,C	Copy Carry value into Bit	2	2	92h
Data Transfer Instructions				
MOV A, Rn	Move register to A	1	1	E8h-Efh
MOV A, direct	Move direct byte to A	2	1	E5h
MOV A, @Ri	Move data memory to A	1	1	E6h,E7h
MOV A, #data	Move immediate to A	2	1	74h
MOV Rn, A	Move A to register	1	1	F8h-FFh
MOV Rn, direct	Move direct byte to register	2	2	A8h-AFh
MOV Rn, #data	Move immediate to register	2	1	78h-7Fh
MOV direct, A	Move A to direct byte	2	1	F5h
MOV direct, Rn	Move register to direct byte	2	2	88h-8Fh
MOV direct, direct	Move direct byte to direct byte	3	2	85h
MOV direct, @Ri	Move data memory to direct byte	2	2	86h,87h
MOV direct, #data	Move immediate to direct byte	3	2	75h
MOV @Ri, A	Move A to data memory	1	1	F6h,F7h
MOV @Ri, direct	Move direct byte to data memory	2	2	A6h,A7h
MOV @Ri, #data	Move immediate to data memory	2	1	76h-77h
MOV DPTR, #data	Move immediate to data pointer	3	2	90h
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	2	93h
MOVC A, @A+PC	Move code byte relative PC to A	1	2	83h
MOVX A, @Ri	Move external data (A8) to A	1	2	E2h,E3h
MOVX A, @DPTR	Move external data (A16) to A	1	2	E0h
MOVX @Ri, A	Move A to external data (A8)	1	2	F2h,F3h
MOVX @DPTR, A	Move A to external data (A16)	1	2	F0h
PUSH direct	Push direct byte onto stack	2	2	C0h
POP direct	Pop direct byte from stack	2	2	D0h
XCH A, Rn	Exchange A and register	1	1	C8h-CFh
XCH A, direct	Exchange A and direct byte	2	1	C5h
XCH A, @Ri	Exchange A and data memory	1	1	C6h,C7h
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6h,D7h
Branching Instructions				
ACALL addr 11	Absolute call to subroutine	2	2	11h,31h, 51h,71h, 91h,B1h, D1h,F1h
LCALL addr 16	Long call to subroutine	3	2	12h
RET	Return from subroutine	1	2	22h
RETI	Return from interrupt	1	2	32h
AJMP addr 11	Absolute jump unconditional	2	2	01h,21h, 41h,61h, 81h,A1h, C1h,E1h
LJMP addr 16	Long jump unconditional	3	2	02h
SJMP rel	Short jump (relative address)	2	2	80h
JC rel	Jump on carry = 1	2	2	40h
JNC rel	Jump on carry = 0	2	2	50h
JB bit, rel	Jump on direct bit = 1	3	2	20h
JNB bit, rel	Jump on direct bit = 0	3	2	30h
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10h
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73h
JZ rel	Jump on accumulator = 0	2	2	60h
JNZ rel	Jump on accumulator 1= 0	2	2	70h
CJNE A, direct, rel	Compare A, direct JNE relative	3	2	B5h
CJNE A, #d, rel	Compare A, immediate JNE relative	3	2	B4h
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	2	B8h-BFh
CJNE @Ri, #d, rel	Compare ind, immediate JNE relative	3	2	B6h,B7h
DJNZ Rn, rel	Decrement register, JNZ relative	2	2	D8h-DFh
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	2	D5h
Miscellaneous Instruction				
NOP	No operation	1	1	00h,A5h

Rn: Any of the register R0 to R7
@Ri: Indirect addressing using Register R0 or R1
#data: immediate Data provided with Instruction
#data16: Immediate data included with instruction
bit: address at the bit level
rel: relative address to Program counter from +127 to –128
Addr11: 11-bit address range
Addr16: 16-bit address range
#d: Immediate Data supplied with instruction

Special Function Registers (SFR)

Addresses 80h to FFh of the SFR address space can be accessed in direct addressing mode only. The following table lists the VMX51C900 special function registers.

TABLE 6: SPECIAL FUNCTION REGISTERS (SFR)

SFR Register	SFR Adrs	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset read Value
P0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111b
SP	81h	-	-	-	-	-	-	-	-	00000111b
DPL	82h	-	-	-	-	-	-	-	-	00000000b
DPH	83h	-	-	-	-	-	-	-	-	00000000b
Reserved	84h									10000100b
PCON	87h	SMOD	-	-	-	GF1	GF0	PDOWN	IDLE	00000000b
TCON	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000b
TMOD	89h	GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000b
TL0	8Ah	-	-	-	-	-	-	-	-	00000000b
TL1	8Bh	-	-	-	-	-	-	-	-	00000000b
TH0	8Ch	-	-	-	-	-	-	-	-	00000000b
TH1	8Dh	-	-	-	-	-	-	-	-	00000000b
ADCCTRL	8Eh	ADCEND	ADCCONT	ADCCLK1	ADCCLK0	ADCCH1	ADCCH0	-	-	00000000b
ADCDATA	8Fh	ADCDATA7	ADCDATA6	ADCDATA5	ADCDATA4	ADCDATA3	ADCDATA2	ADCDATA1	ADCDATA0	00000000b
P1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111b
WDTKEY	97h	WDTKEY7	WDTKEY6	WDTKEY5	WDTKEY4	WDTKEY3	WDTKEY2	WDTKEY1	WDTKEY0	10010111b
SCON	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b
SBUF	99h	-	-	-	-	-	-	-	-	10000000b
P0IOCTRL	9Ah	LCDSEG6	LCDSEG7	LCDSEG8	LCDSEG9	LCDSEG10	LCDSEG11	LCDSEG12	LCDSEG13	00000000b
P1IOCTRL	9Bh		PWMBE				PWMAE			00000000b
P2IOCTRL	9Ch	LCDSEG3	LCDSEG2	LCDSEG1	LCDSEG0	LCDCOM3	LCDCOM2	LCDCOM1	LCDCOM0	00000000b
P3IOCTRL	9Dh	ADCIEN3	ADCIEN2	ADCIEN1	ADCIEN0	-	-	-	-	00000000b
WDTCTRL	9Fh	WDTE	-	WDTCLR	-	-	WDTPS2	WDTPS1	WDTPS0	00000000b
P2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111b
PWMACTRL	A3h	-	-	-	-	-	-	PWMACK1	PWMACK0	00000000b
PWMA	A4h	PWMA.4	PWMA.3	PWMA.2	PWMA.1	PWMA.0	NPA.2	NPA.1	NPA.0	00000000b
IEN0	A8h	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00000000b
IEN1	A9h	-	-	-	-	ADCIE	-	-	-	00000000b
IF1	AAh	-	-	-	-	ADCIF	-	-	-	00000000b
PWMD4	ACh	PWMD4.4	PWMD4.3	PWMD4.2	PWMD4.1	PWMD4.0	NP4.2	NP4.1	NP4.0	10101100b
P3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111b
PWMB	B3h	PWMB.7	PWMB.6	PWMB.5	PWMB.4	PWMB.3	PWMB.2	PWMB.1	PWMB.0	00000000b
IP	B8h	-	-	PT2	PS	PT1	PX1	PT0	PX0	00000000b
IP1	B9h	-	-	-	-	ADCIP	-	-	-	00000000b
SYSCON	BFh	WDR	-	-	-	-	-	-	ALEI	00000000b
T2CON	C8h	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
RCAP2L	CAh	-	-	-	-	-	-	-	-	00000000b
RCAP2H	CBh	-	-	-	-	-	-	-	-	00000000b
TL2	CCh	-	-	-	-	-	-	-	-	00000000b
TH2	CDh									00000000b
PSW	D0h	CY	AC	F0	RS1	RS0	OV	-	P	00000001b
PWMBCTRL	D3h	-	-	-	-	-	PWMBRES	PWMBCK1	PWMBCK0	00000000b
P4	D8h	-	-	-	-	P4.3	P4.2	P4.1	P4.0	00001111b
LCDCTRL	DFh	LCDON	LCDEN	LCDPRI	-	-	LCDCLK2	LCDCLK1	LCDCLK0	00000000b
ACC	E0h	-	-	-	-	-	-	-	-	11100000b
LCDBUF0	E1h	SEG0_COM3	SEG0_COM2	SEG0_COM1	SEG0_COM0	SEG1_COM3	SEG1_COM2	SEG1_COM1	SEG1_COM0	11100001b
LCDBUF1	E2h	SEG2_COM3	SEG2_COM2	SEG2_COM1	SEG2_COM0	SEG3_COM3	SEG3_COM2	SEG3_COM1	SEG3_COM0	11100010b
LCDBUF2	E3h	SEG4_COM3	SEG4_COM2	SEG4_COM1	SEG4_COM0	SEG5_COM3	SEG5_COM2	SEG5_COM1	SEG5_COM0	11100011b
LCDBUF3	E4h	SEG6_COM3	SEG6_COM2	SEG6_COM1	SEG6_COM0	SEG7_COM3	SEG7_COM2	SEG7_COM1	SEG7_COM0	11100100b
LCDBUF4	E5h	SEG8_COM3	SEG8_COM2	SEG8_COM1	SEG8_COM0	SEG9_COM3	SEG9_COM2	SEG9_COM1	SEG9_COM0	11100101b
LCDBUF5	E6h	SEG10_COM3	SEG10_COM2	SEG10_COM1	SEG10_COM0	SEG11_COM3	SEG11_COM2	SEG11_COM1	SEG11_COM0	11100110b
LCDBUF6	E7h	SEG12_COM3	SEG12_COM2	SEG12_COM1	SEG12_COM0	SEG13_COM3	SEG13_COM2	SEG13_COM1	SEG13_COM0	1100111b
B	F0h	-	-	-	-	-	-	-	-	00000000b

VMX51C900 Program Memory

The VMX51C900 includes 8KB of on-chip Program Flash memory which can be programmed using a parallel programmer.

The System Control Register

System control is enabled by the SYSCON register. The SYSCON register is used to monitor whether the system has been reset due to overflow of the watchdog timer and to inhibit activity on the ALE pin when the VMX51C900 executes code from the internal program memory.

TABLE 7: SYSTEM CONTROL REGISTER (SYSCON) – SFR BFH

7	6	5	4	3	2	1	0
WDR	Unused						ALEI

Bit	Mnemonic	Description
7	WDR	This is the Watchdog Timer reset bit. It will be set to 1 when the reset signal generated by WDT overflows.
6:1	Unused	-
0	ALEI	ALE output inhibit bit, which is used to reduce EMI.

Reduced EMI Function

The VMX51C900 can be set up to reduce EMI (electromagnetic interference) emissions by setting bit 0 (ALEI) of the SYSCON register to 1. This function will inhibit the Fosc/6Hz clock signal output on the ALE pin.

Program Status Word Register

The PSW register is a bit addressable register that contains the status flags (CY, AC, OV, P), user flag (F0) and register bank select bits (RS1, RS0) of the 8051 processor.

TABLE 8: PROGRAM STATUS WORD REGISTER (PSW) - SFR DOH

7	6	5	4	3	2	1	0
CY	AC	F0	RS1	RS0	OV	-	P

Bit	Mnemonic	Description
7	CY	Carry Bit
6	AC	Auxiliary Carry Bit from bit 3 to 4.
5	F0	User definer flag
4	RS1	R0-R7 Registers bank select bit 0
3	RS0	R0-R7 Registers bank select bit 1
2	OV	Overflow flag
1	-	-
0	P	Parity flag

RS1	RS0	Active Bank	Address
0	0	0	00h-07h
0	1	1	08h-0Fh
1	0	2	10h-17h
1	1	3	18-1Fh

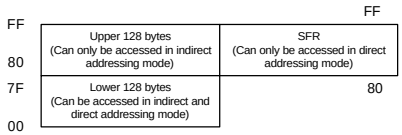
Data Pointer

The VMX51C900 has one 16-bit data pointer. The DPTR is accessed through two SFR addresses: DPL is located at address 82h and DPH is located at address 83h.

Data Memory

The VMX51C900 includes 256 bytes of RAM configured as the standard internal memory structure of a 8052.

FIGURE 1: VMX51C900 DATA MEMORY STRUCTURE



Lower 128 Bytes (00h to 7Fh, Bank 0 & Bank 1)

The lower 128 bytes of data memory (from 00h to 7Fh) is summarized as follows:

- Address range 00h to 7Fh can be accessed in direct and indirect addressing modes
- Address range 00h to 1Fh includes the R0-R7 register area
- Address range 20h to 2Fh is bit addressable
- Address range 30h to 7Fh is not bit addressable and can be used as general-purpose storage

Upper 128 Bytes (80h to FFh, Bank 2 & Bank 3)

The upper 128 bytes of the data memory (80h to FFh) can be accessed using indirect addressing or by using bank mapping in direct addressing mode.

Stack Pointer

The stack pointer (SP) register is located at SFR address 81h. The SP value corresponds to the address of the last data item written to the processor stack. When data is put on the stack, the SP value is incremented.

The SP's default value at reset is 07h. The SP can be programmed to point anywhere in the 00h to FFh RAM memory range.

Each time a function call is performed or an interrupt is serviced, the 16-bit return address (2 bytes) is stored onto the stack. Data can also be placed manually on the stack by using the PUSH and POP instructions.

Description of Power Control Register

The VMX51C900 provides two power saving modes: Idle and Power Down, which are controlled by the PDOWN and IDLE bits of the PCON register at address 87h.

TABLE 9: POWER CONTROL REGISTER (PCON) - SFR 87H

7	6:4	3	2	1	0
SMOD		GF1	GF0	PDOWN	IDLE

Bit	Mnemonic	Description
7	SMOD	1: Double the baud rate of the serial port frequency that was generated by Timer 1. 0: Normal serial port baud rate generated by Timer 1.
6		
5		
4		
3	GF1	General Purpose Flag
2	GF0	General Purpose Flag
1	PDOWN	Power Down mode control bit
0	IDLE	Idle mode control bit

The Idle mode is useful in applications that require reduced power consumption. When in Idle mode, the processor clock is stopped, but the peripherals continue running. The contents of the RAM, I/O state and SFR registers are maintained and the timer, external interrupts and UARTs are left operational. Since only the processor clock stops, normal operating power will be cut to about half. The processor will awaken if an external event triggering an interrupt occurs.

In Power Down mode, the VMX51C900 oscillator and peripherals, including the watchdog timer, are disabled. The contents of the RAM and the SFR registers, however, are maintained.

When in Power Down mode, the VMX51C900 current consumption drops to about 100uA. The only way to exit a Power Down mode is to perform a hardware reset.

The SMOD bit of the PCON register controls the oscillator divisor applied to Timer1 when used as a baud rate generator for the UART. Setting this bit to 1 doubles the frequency of the UART's baud rate generator.

Input/Output Ports

The VMX51C900 has 36 I/O lines grouped into four 8-bit and one 4-bit I/O port(s). These I/Os can be individually configured as inputs or outputs.

With the exception of the P0 I/Os, which are of the open drain type, each I/O consists of a transistor connected to ground and a dynamic pull-up resistor comprised of a combination of transistors.

Writing a 0 into a given I/O port bit register will activate the transistor connected to ground. This will bring the I/O to a logic low level.

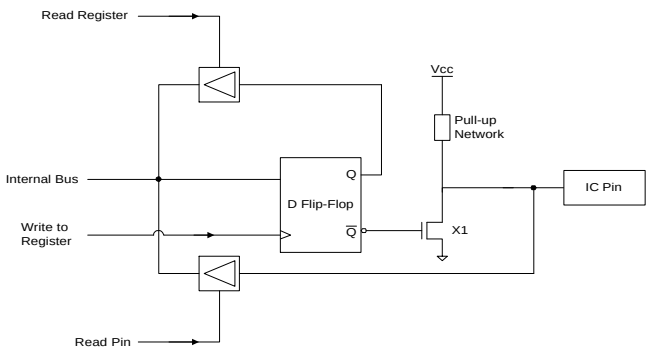
Writing a 1 into a given I/O port bit register deactivates the transistor between the pin and ground. In this case, an internal weak pull-up resistor will bring the pin to a high level (except on Port 0 which is open-drain based).

To use a given I/O as an input, a 1 must be written into its associated port register bit. By default, upon reset all the I/Os are configured as inputs. Note that the VMX51C900 I/O ports are not designed to source current.

Structure of the P1, P2, P3 and P4 Ports

The following figure describes the general structure of the P1, P2, P3 and P4 port I/Os. For these ports, the output stage consists of transistor X1 and additional transistors configured as pull-ups. Note that the figure below does not show the intermediary logic that connects the register output with the output stage because this logic varies with the auxiliary function of each port.

FIGURE 2: GENERAL STRUCTURE OF THE OUTPUT STAGE OF P1, P2, P3 AND P4



Each I/O may be used independently as a logical input or output. When configured as an input, the corresponding bit register must be high. This would correspond to #Q=0 in the above figure.

The transistor would be off (open-circuited) and the current would flow from VCC to the pin, generating a logical high at the output.

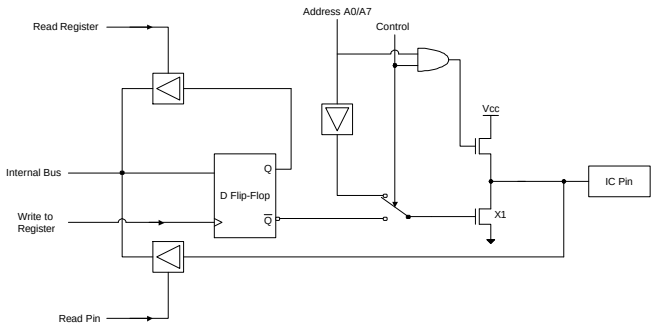
The VMX51C900 I/O ports P1, P2, P3 and P4 are considered “quasi bi-directional” because of the pull-up resistance (even though the I/O’s are configured as inputs). As such, a small current is likely to flow from the VMX51C900 I/O’s pull-up resistors to the driving circuit when the inputs are driven low.

Structure of Port 0

The internal structure of P0 is shown in the following figure. As opposed to the other ports, P0 is truly bi-directional. In other words, when used as an input, it is considered to be in a floating logical state (high impedance state). This arises from the absence of the internal pull-up resistance. The pull-up resistance is actually replaced by a transistor that is only used when the port is configured to access the external memory/data bus (EA=0).

When used as an I/O port, P0 acts as an open drain port and the use of an external pull-up resistor is likely to be required for some applications.

FIGURE 3: PORT P0’S PARTICULAR STRUCTURE



Alternately, P0 can be configured as the low byte (AD0 through AD7) of the address/data bus when the

VMX51C900 EA pin is held at 0V during reset, or when a MOVX instruction is executed.

The P0 register located at address 80h controls the individual pin direction when configured as an I/O. The P0 register is bit-addressable.

TABLE 10: PORT 0 REGISTER (P0) - SFR 80H

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Bit	Mnemonic	Description
7	P0.7	For each bit of the P0 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V.
6	P0.6	
5	P0.5	
4	P0.4	
3	P0.3	
2	P0.2	
1	P0.1	
0	P0.0	

Port 2

Port P2 is very similar to Port1 and Port3, the difference being that the alternate function of P2 is to act as the upper address bus (A8-A15) when the EA line of the VMX51C900 is held low at reset time or when a MOVX instruction is executed.

Like the P1, P2 and P3 registers, the P2 register is bit-addressable.

TABLE 11: PORT 2 REGISTER (P2) - SFR A0H

7	6	5	4	3	2	1	0
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

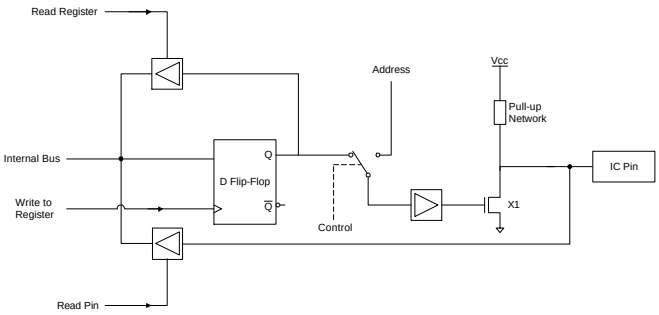
Bit	Mnemonic	Description
7	P2.7	For each bit of the P2 register correspond to an I/O line: 0: Output transistor pull the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V.
6	P2.6	
5	P2.5	
4	P2.4	
3	P2.3	
2	P2.2	
1	P2.1	
0	P2.0	

Port P0 and P2 as Address and Data Bus

The output stage may receive data from two sources:

- The outputs of register P0 or the bus address itself multiplexed with the data bus for P0
- The outputs of the P2 register or the high byte (A8 through A15) of the bus address for the P2 port

FIGURE 4: P2 PORT STRUCTURE



When the ports are used as an address or data bus, the special function registers P0 and P2 are disconnected from the output stage, the 8 bits of the P0 register are forced to 1 and the contents of the P2 register remains constant.

Port 1

The P1 register controls the direction of the Port 1 I/O pins. Writing a 1 to the corresponding bit configures the port as an output. This presents a logic 1 to the corresponding I/O pin or allows the I/O pin to be used as an input. Writing a 0 activates the output "pull-down" transistor, which will force the corresponding I/O line to a logic low.

TABLE 12: PORT 1 REGISTER (P2) - SFR 90H

7	6	5	4	3	2	1	0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Bit	Mnemonic	Description
7	P1.7	For each bit of the P1 register correspond to an I/O line: 0: Output transistor pulls the line to 0V 1: The output transistor is blocked so the pull-up brings the I/O to 5V
6	P1.6	
5	P1.5	
4	P1.4	
3	P1.3	
2	P1.2	
1	P1.1	
0	P1.0	

Auxiliary Port 1 Functions

The Port 1 I/O pins are shared with the PWMA & PWMB outputs, the Timer2 EXT and the T2 input (see following table).

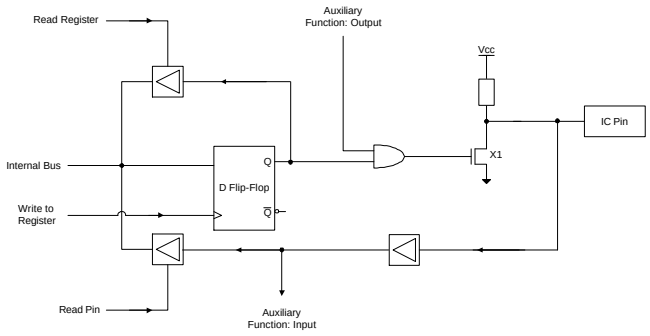
Pin	Mnemonic	Function
P1.0	T2	Timer 2 Counter input
P1.1	T2EX	Timer2 Auxiliary input
P1.2	PWMA	PWMA output
P1.3		
P1.4		
P1.5	PWMB	PWMB output
P1.6		
P1.7		

Auxiliary P3 Port Functions

The Port 3 I/O pins are shared with the UART interface, the INT0 and INT1 interrupts, the Timer0 and Timer1 inputs and the #WR and #RD lines when external memory access is performed.

To maintain the correct line functionality in auxiliary function mode, the P3 register Q output must be held stable at 1. This is achieved by setting the corresponding P3 bit to 1.

FIGURE 5: P3 PORT STRUCTURE



The P3 register controls the P3 pin operation.

TABLE 13: PORT 3 REGISTER (P3) - SFR B0H

7	6	5	4	3	2	1	0
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Bit	Mnemonic	Description
7	P3.7	Each bit of the P3 register corresponds to an I/O line: 0: Output transistor pulls the line to 0V 1: Output transistor is blocked so the pull-up brings the I/O to 5V To configure P3 pins as inputs or use alternate P3 functions, the corresponding bit must be set to 1
6	P3.6	
5	P3.5	
4	P3.4	
3	P3.3	
2	P3.2	
1	P3.1	
0	P3.0	

The following table describes the auxiliary functions of the Port 3 I/O pins.

TABLE 14: P3 AUXILIARY FUNCTION TABLE

Pin	Mnemonic	Function
P3.0	RXD	Serial Port: Receive data in asynchronous mode Input and output data in synchronous mode
P3.1	TXD	Serial Port: Transmit data in asynchronous mode Output clock value in synchronous mode
P3.2	$\overline{\text{INT0}}$	External Interrupt 0 Timer 0 Control Input
P3.3	$\overline{\text{INT1}}$	External Interrupt 1 Timer 1 Control Input
P3.4	T0	Timer 0 Counter Input
P3.5	T1	Timer 1 Counter Input
P3.6	$\overline{\text{WR}}$	Write signal for external memory
P3.7	$\overline{\text{RD}}$	Read signal for external memory

Port 4

Port 4 consists of four pins and its SFR (P4) address is 0D8H.

TABLE 15: PORT 4 (P4) - SFR D8H

7	6	5	4	3	2	1	0
Unused				P4.3	P4.2	P4.1	P4.0

Bit	Mnemonic	Description
7	Unused	-
6	Unused	-
5	Unused	-
4	Unused	-
3	P4.3	Used to output the setting to pins P4.3, P4.2, P4.1, P4.0 respectively.
2	P4.2	
1	P4.1	
0	P4.0	

Software Particulars Concerning the Ports

Some instructions allow the user to read the logic state of the output pin, while others allow the user to read the contents of the associated port register. These instructions are called *read-modify-write* instructions. A list of these instructions may be found in the table below.

Upon execution of these instructions, the contents of the port register (at least 1 bit) is modified. The other read instructions take the present state of the input into account. For example, the instruction ANL P3, #01h obtains the value in the P3 register; performs the desired logic operation with the constant 01h and recopies the result into the P3 register. When users want to take the present state of the inputs into account, they must first read these states and perform an AND operation of the value read and the constant (see following example).

```
MOV A, P3; State of the inputs in the accumulator
ANL A, #01; AND operation between P3 and 01h
```

When the port is used as an output, the register contains information on the state of the output pins. Measuring the state of an output directly on the pin is inaccurate because the electrical level depends mostly on the type of charge that is applied to it. The functions shown below take the value of the register rather than that of the pin.

TABLE 16: LIST OF INSTRUCTIONS THAT READ AND MODIFY THE PORT USING REGISTER VALUES

Instruction	Function
ANL	Logical AND ex: ANL P0, A
ORL	Logical OR ex: ORL P2, #01110000B
XRL	Exclusive OR ex: XRL P1, A
JBC	Jump if the bit of the port is set to 0
CPL	Complement one bit of the port
INC	Increment the port register by 1
DEC	Decrement the port register by 1
DJNZ	Decrement by 1 and jump if the result is not equal to 0
MOV P.,C	Copy the held bit C to the port
CLR P.x	Set the port bit to 0
SETB P.x	Set the port bit to 1

Port Operation Timing

Writing to a Port (Output)

When an operation results in a modification of the contents in a port register, the new value is placed at the output of the D flip-flop during the last machine cycle that the instruction needed to execute.

Reading a Port (Input)

In order to be sampled, the signal duration present on the I/O inputs must be longer than Fosc/12.

I/O Port Drive Capability

The maximum allowable continuous current that the device can sink on an I/O port is defined in the following table.

Maximum sink current on one given I/O	10mA
Maximum total sink current for P0	26mA
Maximum total sink current for P1, 2, 3,4	15mA
Maximum total sink current on all I/O	71mA

It is not recommended to exceed the sink current outlined in the above table. Doing so will likely result in the low-level output voltage exceeding device specifications and in turn affect device reliability.

The VMX51C900 I/O ports are not designed to source current.

Timers

The VMX51C900 includes three 16-bit timers: Timer0, Timer1 and Timer2.

The timers can operate in two modes:

- Event counting mode
- Timer mode

When operating in event counting mode, the counter is incremented each time an external event, such as a transition in the logical state of the timer input (T0, T1, T2 input), is detected. When operating in timer mode, the counter is incremented by the microcontroller's system clock (Fosc/12) or by a divided version of it.

Timer0 and Timer1

Timers0 and 1 have four modes of operation. These modes allow the user to change the size of the counting register or to authorize an automatic reload when encountering a specific value. Timer1 can also be used as a baud rate generator to generate communication frequencies for the serial interface.

Timer0 and Timer1 are configured by the TMOD and TCON registers.

TABLE 17: TIMER MODE CONTROL REGISTER (TMOD) – SFR 89H

7	6	5	4	3	2	1	0
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0

Bit	Mnemonic	Description
7	GATE1	1: Enables external gate control (pin INT1 for Counter 1). When INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T1IN input pin
6	C/T1	Selects timer or counter operation (Timer 1). 1 = A counter operation is performed 0 = The corresponding register will function as a timer
5	T1M1	Selects the operating mode of Timer/Counter 1
4	T1M0	
3	GATE0	If set, enables external gate control (pin INT0 for Counter 0). When INT0 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on the T0IN input pin
2	C/T0	Selects timer or counter operation (Timer 0). 1 = A counter operation is performed 0 = The corresponding register will function as a timer
1	T0M1	Selects the operating mode of Timer/Counter 0
0	T0M0	

The table below summarizes the four operating modes of timers 0 and 1. The timer operating mode is selected by the T1M1/T1M0 and T0M1/T0M0 bits of the TMOD register.

TABLE 18: TIMER/COUNTER MODE DESCRIPTION SUMMARY

M1	M0	Mode	Function
0	0	Mode 0	13-bit Counter
0	1	Mode 1	16-bit Counter
1	0	Mode 2	8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, the value of THx is copied to TLx.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops.

Timer0 /Timer1 Counter/Timer Functions

Timing Function

When either Timer 0 or 1 is configured to operate as a timer, its value is automatically incremented at every system cycle. In the event of an overflow, the overflow flag is set and the counter is set to zero. The overflow flags (TF0 and TF1) are located in the TCON register.

The TR0 and TR1 bits of the TCON register gate the corresponding timer operation. . In order for the timer to run, the corresponding TRx bit must be set to 1.

The IT0 and IT1 bits of the TCON register control the event that will trigger an external interrupt as follows:

IT0 = 0: The INT0, if enabled, occurs if a low level is present on P3.2

IT0 = 1: The INT0, if enabled, occurs if a high to low transition is detected on P3.2

IT1 = 0: The INT1, if enabled, occurs if a low level is present on P3.3

IT1 = 1: The INT1, if enabled, occurs if a high to low transition is detected on P3.3

The IE0 and IE1 bits of the TCON register are external flags which indicate that a transition has been detected on the INT0 and INT1 interrupt pins, respectively.

If the external interrupt is configured as edge sensitive, the corresponding IE0 and IE1 flags are automatically cleared when the corresponding interrupt is serviced.

If the external interrupt is configured as level sensitive, the corresponding flag must be cleared by the software.

TABLE 19: TIMER 0 AND 1 CONTROL REGISTER (TCON) –SFR 88H

7	6	5	4	3	2	1	0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Bit	Mnemonic	Description
7	TF1	Timer 1 Overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
6	TR1	Timer 1 Run Control Bit. Set/cleared by software to turn Timer/Counter on or off.
5	TF0	Timer 0 Overflow Flag. Set by hardware on Timer/Counter overflow. Cleared by hardware when processor vectors to interrupt routine.
4	TR0	Timer 0 Run Control Bit. Set/cleared by software to turn Timer/Counter on or off.
3	IE1	Interrupt Edge Flag. Set by hardware when external interrupt edge is detected. Cleared when interrupt processed.
2	IT1	Interrupt 1 Type Control Bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
1	IE0	Interrupt 0 Edge Flag. Set by hardware when external interrupt edge is detected. Cleared when interrupt processed.
0	IT0	Interrupt 0 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.

Counting Function

When operating as a counter, the timer register is incremented at every falling edge of the T0 and T1 signals located at the input of the timers.

When the sampling circuit detects a high immediately followed by a low in the following machine cycle, the counter is incremented. Two system cycles are required to detect and record an event. In order to be properly sampled, the counting frequency should be reduced by a factor of 24 (24 times less than the oscillator's frequency).

Timer0/Timer1 Operating Modes

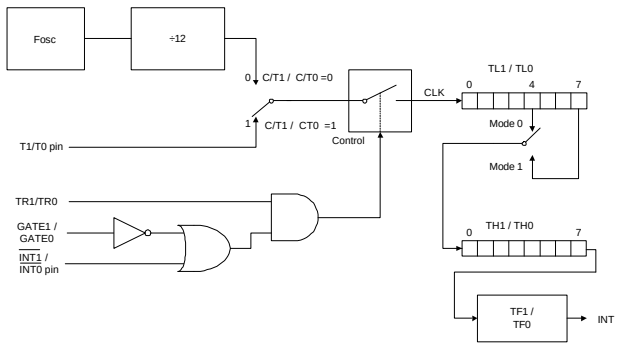
The user may change the operating mode via the M1 and M0 bits of the TMOD SFR.

Mode 0

A schematic representation of this mode of operation is presented in the figure below. In Mode 0, the Timer

operates as 13-bit counter made up of 5 LSBs from the TLx register and the 8 upper bits coming from the THx register. When an overflow causes the value of the register to roll over to 0, the TFx interrupt signal goes to 1. The count value is validated as soon as TRx goes to 1 and the GATE bit is 0, or when INTx is 1.

FIGURE 6: TIMER/COUNTER 1 MODE 0: 13-BIT COUNTER



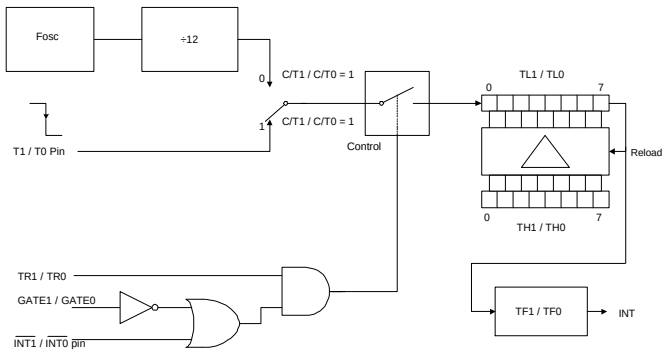
Mode 1

Mode 1 is almost identical to Mode 0, with the difference being that in Mode 1, the counter/timer uses the full 16-bits of the Timer.

Mode 2

In this Mode, the register of the Timer is configured as an 8-bit auto-re-loadable Counter/Timer. In Mode 2, the TLx is used as the counter. In the event of a counter overflow, the TFx flag is set to 1 and the value contained in THx, which is preset by software, is reloaded into the TLx counter. The value of THx remains unchanged.

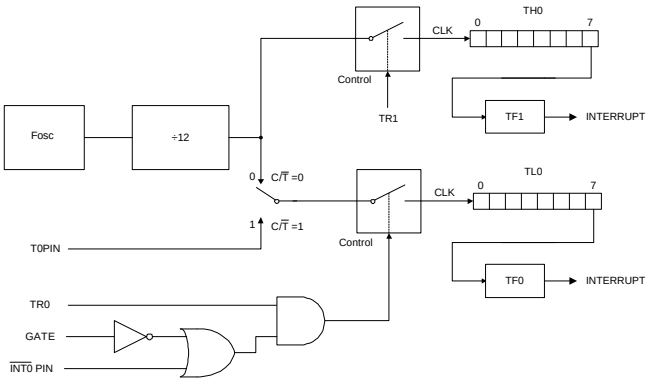
FIGURE 7: TIMER/COUNTER 1 MODE 2: 8-BIT AUTOMATIC RELOAD



Mode 3

In Mode 3, Timer 1 is blocked as if its' control bit, TR1, was set to 0. In this mode, Timer 0's registers TL0 and TH0 are configured as two separate 8-bit counters. The TL0 counter uses Timer 0's control bits (C/T, GATE, TR0, INT0, TF0), the TH0 counter is held in Timer Mode (counting machine cycles) and gains control over TR1 and TF1 from Timer 1. At this point, TH0 controls the Timer 1 interrupt.

FIGURE 8: TIMER/COUNTER 0 MODE 3



Timer 2

Timer 2 of the VMX51C900 is a 16-bit Timer/Counter and is similar to Timers 0 and 1 in that it can operate either as an event counter or as a timer. This is controlled by the C/T2 bit in the T2CON special function register. Timer 2 has three operating modes - Auto-Load, Capture and Baud Rate Generator. These modes are selected via the T2CON SFR The following table describes T2CON special function register bits.

TABLE 20: TIMER 2 CONTROL REGISTER (T2CON) –SFR C8H

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2

Bit	Mnemonic	Description
7	TF2	Timer 2 Overflow Flag: Set by an overflow of Timer 2 and must be cleared by software. TF2 will not be set when either RCLK =1 or TCLK =1.
6	EXF2	Timer 2 external flag change in state occurs when either a capture or reload is caused by a negative transition on T2EX and EXEN2=1. When Timer 2 is enabled, EXF=1 will cause the CPU to Vector to the Timer 2 interrupt routine. Note that EXF2 must be cleared by software.
5	RCLK	Serial Port Receive Clock Source. 1: Causes Serial Port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. 0: Causes Timer 1 overflow to be used for the Serial Port receive clock.
4	TCLK	Serial Port Transmit Clock. 1: Causes Serial Port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. 0: Causes Timer 1 overflow to be used for the Serial Port transmit clock.
3	EXEN2	Timer 2 External Mode Enable. 1: Allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the Serial Port. 0: Causes Timer 2 to ignore events at T2EX.
2	TR2	Start/Stop Control for Timer 2. 1: Start Timer 2 0: Stop Timer 2
1	$\overline{C/T2}$	Timer or Counter Select (Timer 2) 1: External event counter falling edge triggered. 0: Internal Timer (OSC/12)
0	$\overline{CP/RL2}$	Capture/Reload Select. 1: Capture of Timer 2 value into RCAP2H, RCAP2L is performed if EXEN2=1 and a negative transitions occurs on the T2EX pin. The capture mode requires RCLK and TCLK to be 0. 0: Auto-reload reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2=1. When either RCK =1 or TCLK =1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

The Timer 2 mode selection bits and their function are described in the following table.

TABLE 21: TIMER 2 MODE SELECTION BITS

RCLK + TCLK	$\overline{CP/RL2}$	TR2	MODE
0	0	1	16-bit Auto-Reload Mode
0	1	1	16-bit Capture Mode
1	X	1	Baud Rate Generator Mode
X	X	0	Timer 2 stops

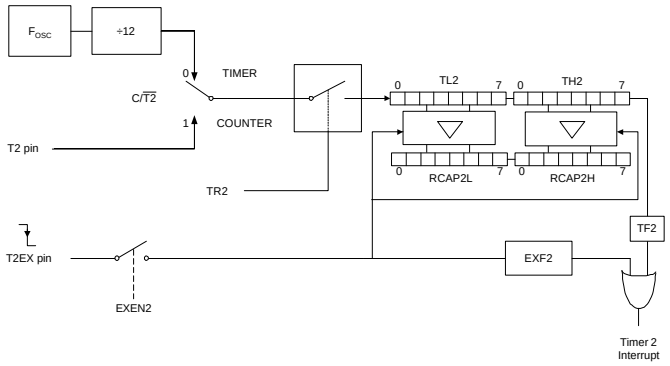
The details of each mode are described below.

Timer 2 Capture Mode

In Capture Mode, the EXEN2 bit of the T2CON register controls whether an external transition on the T2EX pin will trigger capture of the timer value.

When EXEN2 = 0, Timer 2 acts as a 16-bit timer or counter, which, upon overflowing, will set the TF2 bit (Timer 2 overflow bit). This overflow can be used to generate an interrupt

FIGURE 9: TIMER 2 IN CAPTURE MODE



When EXEN2 = 1, the above still applies, however, in addition, it is possible to allow a 1 to 0 transition at the T2EX input to cause the current value stored in the Timer 2 registers (TL2 and TH2) to be captured into the RCAP2L and RCAP2H registers. Furthermore, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2, like TF2, can generate an interrupt. Note that both EXF2 and TF2 share the same interrupt vector.

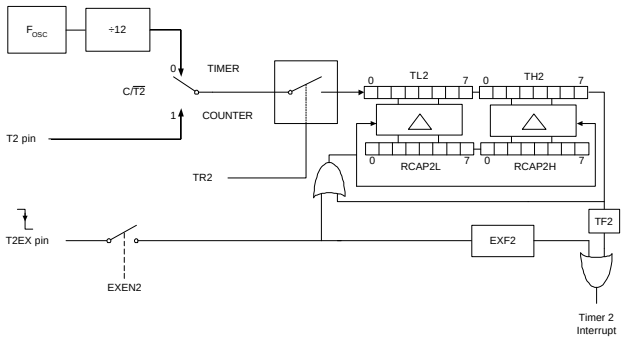
Timer 2 Auto-Reload Mode

In this mode, there are also two options controlled by the EXEN2 bit in the T2CON register.

If EXEN2 = 0, when Timer 2 rolls over, it not only sets TF2, but also causes the Timer 2 registers to be reloaded with the 16-bit value in the RCAP2L and RCAP2H registers previously initialised. In this mode, Timer 2 can be used as a baud rate generator source for the serial port.

If EXEN2=1, Timer 2 still performs the above operation, however, additionally, a 1 to 0 transition at the external T2EX input will also trigger an anticipated reload of Timer 2 with the value stored in RCAP2L, RCAP2H and set EXF2.

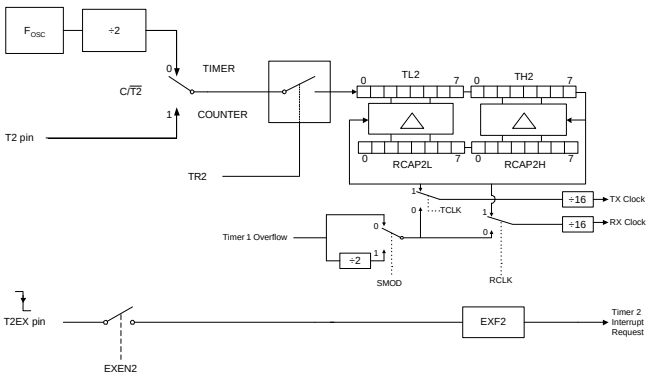
FIGURE 10: TIMER 2 IN AUTO-RELOAD MODE



Timer 2 Baud Rate Generator Mode

Timer 2 can be configured as a UART baud rate generator. This mode is activated when RCLK is set to 1 and/or TCLK is set to 1. This mode will be described in the serial port section.

FIGURE 11: TIMER 2 IN AUTOMATIC BAUD GENERATOR MODE



UART Serial Port

The serial port on the VMX51C900 can operate in full duplex; in other words, it can transmit and receive data simultaneously. Different communication speeds can be configured for transmission and reception by assigning one timer for transmission and another for reception.

The VMX51C900 serial port includes a double buffering feature, such that the serial port can begin reception of a byte even if the processor has not retrieved the last byte from the receive register. However, if the previously received byte has not been read by the time reception of the next byte is complete, the byte present in the receive buffer will be lost.

The SBUF register provides access to the transmit and receive registers of the serial port. Reading from the SBUF register will access the receive register, while a write to the SBUF loads the transmit register.

UART Control Register

The SCON (serial port control) register contains control and status information, and includes the 9th data bit for transmit/receive (TB8/RB8 if required), mode selection bits and serial port interrupt bits (TI and RI).

TABLE 22: SERIAL PORT CONTROL REGISTER (SCON) – SFR 98H

7	6	5	4	3	2	1	0
SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit	Mnemonic	Description
7	SM0	Bit to select mode of operation (see table below)
6	SM1	Bit to select mode of operation (see table below)
5	SM2	Multiprocessor communication is possible in Modes 2 and 3. In Modes 2 or 3 if SM2 is set to 1, RI will not be activated if the received 9th data bit (RB8) is 0. In Mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received.
4	REN	Serial Reception Enable Bit This bit must be set by software and cleared by software. 1: Serial reception enabled 0: Serial reception disabled
3	TB8	9th data bit transmitted in Modes 2 and 3 This bit must be set by software and cleared by software.
2	RB8	9th data bit received in Modes 2 and 3. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, this bit is not used. This bit must be cleared by software.
1	TI	Transmission Interrupt flag. Automatically set to 1 when: • The 8th bit has been sent in Mode 0. • Automatically set to 1 when the stop bit has been sent in the other modes. This bit must be cleared by software.
0	RI	Reception Interrupt flag Automatically set to 1 when: • The 8th bit has been received in Mode 0. • Automatically set to 1 when the stop bit has been sent in the other modes (see SM2 exception). This bit must be cleared by software.

TABLE 23: SERIAL PORT MODES OF OPERATION

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift Register	$F_{osc}/12$
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	$F_{osc}/64$ or $F_{osc}/32$
1	1	3	9-bit UART	Variable

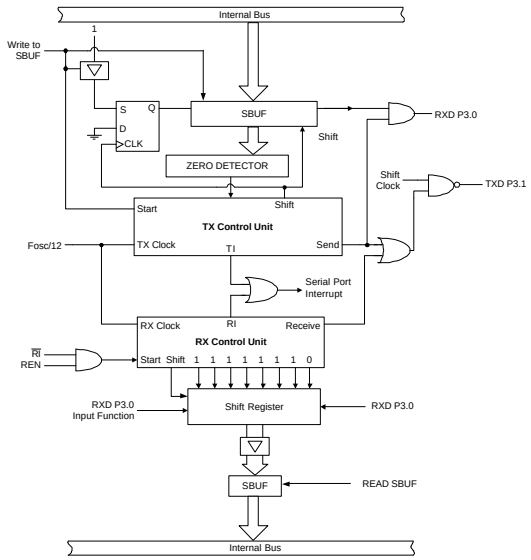
UART Operating Modes

The VMX51C900's serial port can operate in four modes. In all four modes, a transmission is initiated by an instruction that uses the SBUF register as a destination register. In Mode 0, reception is initiated by setting RI to 0 and REN to 1. An incoming Start bit initiates reception in the other modes, provided that REN is set to 1. The following section describes the four modes.

UART Operation in Mode 0

In Mode 0, serial data exits and enters through the RXD pin. TXD is used to output the shift clock. The signal is composed of 8 data bits starting with the LSB. The baud rate in this mode is 1/12 the oscillator frequency.

FIGURE 12: SERIAL PORT MODE 0 BLOCK DIAGRAM



UART Transmission in Mode 0

Any instruction that uses SBUF as a destination register may initiate a transmission. The "write to SBUF" signal also loads a 1 into the 9th position of the transmit shift register and informs the TX control block to begin a transmission. The internal timing is such that one full machine cycle will elapse between a write to SBUF instruction and the activation of SEND.

The SEND signal enables the output of the shift register to the alternate output function line of P3.0 and enables SHIFT CLOCK to the alternate output function line of P3.1.

At every machine cycle in which SEND is active, the contents of the transmit shift register are shifted to the right by one position.

Zeros come in from the left as data bits shift out to the right. The TX control block sends its final shift and de-activates SEND while setting T1 after one condition is fulfilled. When the MSB of the data byte is at the output position of the shift register; the 1 that was initially loaded into the 9th position is just to the left of the MSB; and all positions to the left of that contain zeros. Once these conditions are met, the de-activation of SEND and the setting of T1 occurs at T1 of the 10th machine cycle after the "write to SBUF" pulse.

UART Reception in Mode 0

When REN and R1 are set to 1 and 0, respectively, reception is initiated. The bits 11111110 are written to the receive shift register at the end of the next machine cycle by the RX control unit. In the following phase, the RX control unit will activate RECEIVE.

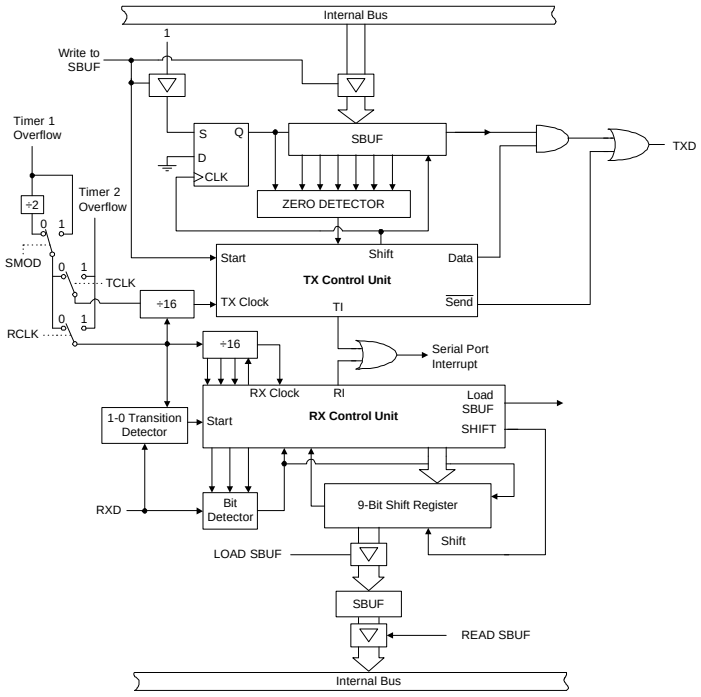
The contents of the receive shift register are shifted one position to the left at the end of every machine cycle during which RECEIVE is active. The value that comes in from the right is the value that was sampled at the P3.0 pin.

1's are shifted out to the left as data bits are shifted in from the right. The RX control block is flagged to do one last shift and load SBUF when the 0 that was initially loaded into the rightmost position arrives at the leftmost position in the shift register.

UART Operation in Mode 1

In Mode 1 operation, 10 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (Low); 8 data bits (LSB first) and one Stop bit (high). The reception is completed once the Stop bit sets the RB8 flag in the SCON register. Either Timer 1 or Timer 2 controls the baud rate in this mode.
The following diagram shows the serial port structure when configured in Mode 1.

FIGURE 13: SERIAL PORT MODE 1 AND 3 BLOCK DIAGRAM



UART Transmission in Mode 1

Transmission in this mode is initiated by any instruction that makes use of SBUF as a destination register. The 9th bit position of the transmit shift register is loaded by the "write to SBUF" signal. This event also flags/informs the TX Control Unit that a transmission has been requested.

It is after the next rollover in the divide-by-16 counter when transmission actually begins. It follows that the bit times are synchronized to the divide-by-16 counter and not to the "write to SBUF" signal.

When a transmission begins, it places the start bit at TXD. Data transmission is activated one bit time later. This activation enables the output bit of the transmit shift register to TXD. One bit time after that, the first shift pulse occurs.
In this Mode, zeros are clocked in from the left as data bits are shifted out to the right. When the most significant bit of the data byte is at the output position of the shift register, the 1 that was initially loaded into the 9th position is to the immediate left of the MSB, and all positions to the left of that contain zeros. This condition flags the TX Control Unit to shift one more time.

UART Reception in Mode 1

A one to zero transition at pin RXD will initiate reception. It is for this reason that RXD is sampled at a rate of 16 multiplied by the baud rate that has been established. When a transition is detected, 1FFh is written into the input shift register and the divide-by-16 counter is immediately reset. The divide-by-16 counter is reset in order to align its rollovers with the boundaries of the incoming bit times.
In total, there are 16 states in the counter. During the 7th, 8th and 9th counter states of each bit time; the bit detector samples the value of RXD. The accepted value is the value that was seen in at least two of the three samples. The purpose of doing this is for noise rejection. If the value accepted during the first bit time is not zero, the receive circuits are reset and the unit goes back to searching for another one to zero transition. All false start bits are rejected by doing this. If the start bit is valid, it is shifted into the input shift register, and the reception of the rest of the frame will proceed.
For a receive operation, the data bits come in from the right as 1's shift out on the left. As soon as the start bit

arrives at the leftmost position in the shift register, (9-bit register), it tells the UART's receive controller block to perform one last shift operation: to set RI and to load SBUF and RB8. The signal to load SBUF and RB8, and to set RI, will be generated if, and only if, the following conditions are met at the time the final shift pulse is generated:

- Either SM2 = 0 or the received stop bit = 1
- RI = 0

If both conditions are met, the stop bit goes into RB8, the 8 data bits go into SBUF, and RI is activated. If one of these conditions is not met, the received frame is completely lost. At this time, whether the above conditions are met or not, the unit goes back to searching for a one to zero transition in RXD.

UART Operation in Mode 2

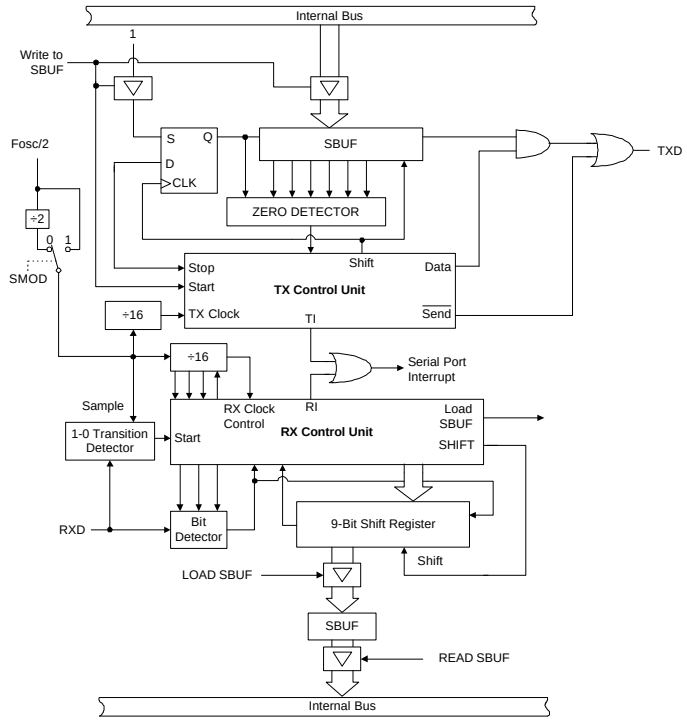
In Mode 2 a total of 11 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (Low), 8 data bits (LSB first), a programmable 9th data bit, and one Stop bit (High).

For transmission, the 9th data bit comes from the TB8 bit of SCON. For example, the parity bit P in the PSW could be moved into TB8.

In the case of receive, the 9th data bit is automatically written into RB8 of the SCON register.

In Mode 2, the baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

FIGURE 14: SERIAL PORT MODE 2 BLOCK DIAGRAM

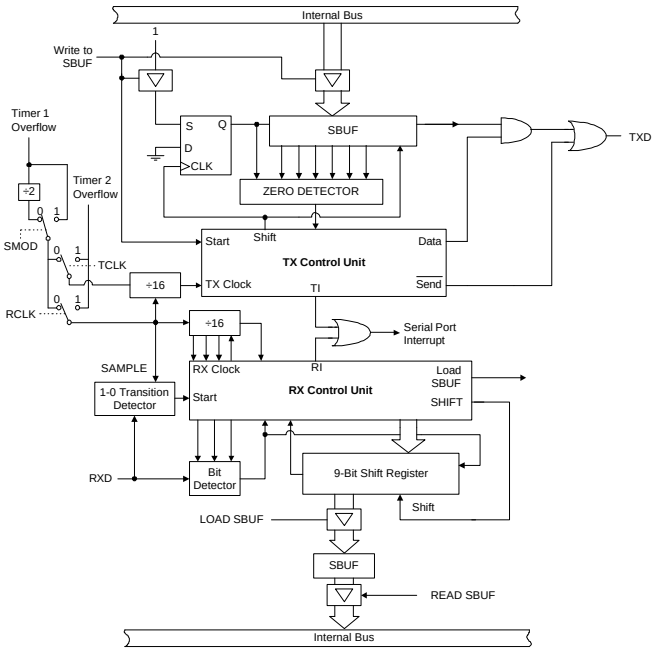


UART Operation in Mode 3

In Mode 3, 11 bits are transmitted (through TXD) or received (through RXD). The transactions are composed of: a Start bit (Low), 8 data bits (LSB first), a programmable 9th data bit, and one Stop bit (High).

Mode 3 is identical to Mode 2 in all respects but one: the baud rate. Either Timer 1 or Timer 2 generates the baud rate in Mode 3.

FIGURE 15: SERIAL PORT MODE 3 BLOCK DIAGRAM



UART in Mode 2 and 3: Additional Information

As mentioned previously, for an operation in Modes 2 and 3, 11 bits are transmitted (through TXD) or received (through RXD). The signal comprises: a logical low Start bit, 8 data bits (LSB first), a programmable 9th data bit, and one logical high Stop bit.
On transmit, (TB8 in SCON) can be assigned the value of 0 or 1. On receive; the 9th data bit goes into RB8 in SCON. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency in Mode 2. Mode 3 may have a variable baud rate generated from either Timer 1 or Timer 2 depending on the states of TCLK and RCLK.

UART Transmission in Mode 2 and Mode 3

The transmission is initiated by any instruction that makes use of SBUF as the destination register. The 9th bit position of the transmit shift register is loaded by the "write to SBUF" signal. This event also informs the UART transmission control unit that a transmission has been requested. After the next rollover in the divide-by-16 counter, a transmission actually starts at the beginning of the machine cycle. It follows that the bit times are synchronized to the divide-by-16 counter and not to the "write to SBUF" signal, as in the previous mode.

Transmissions begin when the SEND signal is activated, which places the Start bit on TXD pin. Data is activated one bit time later. This activation enables the output bit of the transmit shift register to the TXD pin. The first shift pulse occurs one bit time after that.

The first shift clocks a Stop bit (1) into the 9th bit position of the shift register on TXD. Thereafter, only zeros are clocked in. Thus, as data bits shift out to the right, zeros are clocked in from the left. When TB8 is at the output position of the shift register, the stop bit is just to the left of TB8, and all positions to the left of that contain zeros. This condition signals to the TX control unit to shift one more time and set TI, while deactivating SEND. This occurs at the 11th divide-by-16 rollover after "write to SBUF".

UART Reception in Mode 2 and Mode 3

One to zero transitions on the RXD pin initiate reception. It is for this reason that RXD is sampled at a rate of 16 multiplied by the baud rate that has been established.
When a transition is detected, the 1FFh is written into the input shift register and the divide-by-16 counter is immediately reset.

During the 7^{th}, 8^{th} and 9^{th} counter states of each bit time; the bit detector samples the value of RXD. The accepted value is the value that was seen in at least two of the three samples. If the value accepted during the first bit time is not zero, the receive circuits are reset and the unit goes back to searching for another one to zero transition. If the start bit is valid, it is shifted into the input shift register, and the reception of the rest of the frame will proceed.

For a receive operation, the data bits come in from the right as 1's shift out on the left. As soon as the start bit arrives at the leftmost position in the shift register (9-bit register), it tells the RX control block to do one more shift, to set RI, and to load SBUF and RB8. The signal to set RI and to load SBUF and RB8 will be generated if, and only if, the following conditions are satisfied at the instance when the final shift pulse is generated:

- Either SM2 = 0 or the received 9^{th} bit equal 1
- RI = 0

If both conditions are met, the 9^{th} data bit received goes into RB8, and the first 8 data bits go into SBUF. If one of these conditions is not met, the received frame is completely lost. One bit time later, whether the above conditions are met or not, the unit goes back to searching for a one to zero transition at the RXD input.
Please note that the value of the received stop bit is unrelated to SBUF, RB8 or RI.

UART Baud Rates

In Mode 0, the baud rate is fixed and is represented by the following formula:

$$\text{Mode 0 Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

In Mode 2, the baud rate depends on the value of the SMOD bit in the PCON SFR. From the formula below, we can see that if SMOD = 0 (which is the value on reset), the baud rate is 1/32 the oscillator frequency.

$$\text{Mode 2 Baud Rate} = \frac{2^{SMOD} \times (\text{Oscillator Frequency})}{64}$$

The Timer 1 and/or Timer 2 overflow rate determines the baud rates in modes 1 and 3.

Generating UART Baud Rate with Timer 1

When Timer 1 functions as a baud rate generator, the baud rate in modes 1 and 3 are determined by the Timer 1 overflow rate.

$$\text{Mode 1,3 Baud Rate} = \frac{2^{SMOD} \times \text{Timer 1 Overflow Rate}}{32}$$

Timer 1 must be configured as an 8-bit timer (TL1) with auto-reload with TH1 value when an overflow occurs (Mode 2). In this application, the Timer 1 interrupt should be disabled.

The following two formulas can be used to calculate the baud rate and the reload value to be written into the TH1 register.

$$\text{Mode 1,3 Baud Rate} = \frac{2^{SMOD} \times Fosc}{32 \times 12(256 - TH1)}$$

The value to write into the TH1 register is defined by the following formula:

$$TH1 = 256 - \frac{2^{SMOD} \times Fosc}{32 \times 12 \times (Baud\ Rate)}$$

Generating UART Baud Rates with Timer 2

Timer 2 is often preferred to generate the baud rate, as it can be easily configured to operate as a 16-bit timer with auto-reload. This enables much better resolution than using Timer 1 in 8-bit auto-reload mode.

The baud rate using Timer 2 is defined as:

$$Mode\ 1,3\ Baud\ Rate = \frac{Timer\ 2\ Overflow\ Rate}{16}$$

The timer can be configured as either a timer or a counter in any of its three running modes. In typical applications, it is configured as a timer (C/T2 is set to 0).

To make the Timer 2 operate as a baud rate generator, the TCLK and RCLK bits of the T2CON register must be set to 1.

The baud rate generator mode is similar to the auto-reload mode in that an overflow in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software. However, when Timer 2 is configured as a baud rate generator, its clock source is Osc/2.

The following formula can be used to calculate the baud rate in modes 1 and 3 using Timer2:

$$Modes\ 1,\ 3\ Baud\ Rate = \frac{Oscillator\ Frequency}{32 \times [65536 - (RCAP2H, RCAP2L)]}$$

The formula below is used to define the reload value to write into the RCAP2h, RCAP2L registers to achieve a given baud rate.

$$(RCAP2H, RCAP2L) = 65536 - \frac{Fosc}{32 \times [Baud\ Rate]}$$

In the above formula, RCAP2H and RCAP2L are the content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

Note that a rollover in TH2 does not set TF2 and will not generate an interrupt. Therefore, the Timer 2 interrupt does not have to be disabled when Timer 2 is configured in baud rate generator mode. Furthermore, when Timer 2 is operating as a UART baud rate generator (TR2 is set to 1), the user should not try to perform read or write operations to the TH2 or TL2 and RCAP2H, RCAP2L registers.

Timer 1 Reload Value in Modes 1 & 3 for UART Baud Rate

The following table provides examples of the Timer 1, 8-bit reload value when used as a UART baud rate generator and the SMOD bit of the PCON register is set to 1.

	22.184MHz	16.000MHz	14.745MHz	12.000MHz	11.059MHz	8.000MHz	3.57MHz
115200bps	FFh	-	-	-	-	-	-
57600bps	Feh	-	-	-	FFh	-	-
38400bps	FDh	-	FEh	-	-	-	-
31250bps	-	-	-	FEh	-	-	-
19200bps	FAh	-	FCh	-	FDh	-	-
9600bps	F4h	-	F8h	-	FAh	-	-
2400bps	D0h	DDh	E0h	E6h	E8h	-	-
1200bps	A0h	BBh	C0h	CCh	D0h	DDh	-
300bps	-	-	00h	30h	40h	75h	C2h

Timer 2 Reload Value in Modes 1 & 3 for UART Baud Rate

The following table contains examples of [RCAP2H, RCAP2L] reload values for Timer 2 when T2 is configured as baud rate generator for the VMX51C900 UART.

	22.184MHz	16.000MHz	14.745MHz	12.000MHz	11.059MHz	8.000MHz	3.57MHz
230400bps	FFFDh	-	FFFEh	-	-	-	-
115200bps	FFFAh	-	FFFCh	-	FFFDh	-	-
57600bps	FFF4h	-	FFF8h	-	FFFAh	-	-
38400bps	FFEEh	FFF3h	FFF4h	-	FFF7h	-	-
31250bps	FFEAh	FFF0h	FFF1h	FFF4h	FFF5h	FFF8h	-
19200bps	FFDCh	FFE6h	FFE8h	-	FFEEh	FFF3h	
9600bps	FFB8h	FFCCh	FFD0h	FFD9h	FFDCh	FFE6h	-
2400bps	FEE0h	FF30h	FF40h	FF64h	FF70h	FF98h	FFD1h
1200bps	FDC0h	FE5Fh	FE80h	FEC7h	FEE0h	FF30h	FFA3h
300bps	F700h	F97Dh	FA00h	FB1Eh	FB80h	FCBEh	FE8Bh

UART initialization in Mode 3 using Timer 1

```
;*** INTIALIZE THE UART @ 9600BPS, Fosc=11.0592MHz

INISER0T1I: MOV   A,T2CON           ;RETRIEVE CURRENT VALUE OF T2CON
            ANL   A,#11001111B      ;RCLK & TCLK BIT = 0 -> TO USE TIMER1
            MOV   T2CON,A           ;BAUD RATE GENERATOR SOURCE FOR UART
            MOV   PCON,#80H         ;SET THE SMOD BIT TO 1
            MOV   TL1,#0FAH         ;CONFIG TIMER1 AT 8BIT WITH AUTO-RELOAD
            MOV   TH1,#0FAH         ;CALCULATE THE TIMER 1 RELOAD VALUE
                                    ;TH1 = [(2^SMOD) * Fosc] / (32 * 12 * Fcomm)
                                    ;TH1 FOR 9600BPS @ 11.059MHz = FAh
            MOV   SCON,#05Ah        ;CONFIG SCON_0 MODE_1
            MOV  TMOD,#00100000B ;CONFIG TIMER 1 IN MODE 2, 8BIT
                                    ; + AUTO RELOAD
            MOV   TCON,#01000000B  ;START TIMER1


            CLR   SCON.0            ;CLEAR UART RX, TX FLAGS
            CLR   SCON.1

            MOV   SBUF,#DATA        ;SEND ONE BYTE ON THE SERIAL PORT
```

UART initialization in Mode 3, using Timer 2

```
;*** INTIALIZE THE UART @57600BPS, Fosc=11.0592MHz

INISER0T2I: MOV   SCON,#05Ah        ;CONFIG SCON_0 MODE_1,
                                    ;CALCULATE RELOAD VALUE WITH T2
                                    ;RCAP2H,RCAP2L = 65536 - [ Fosc / (32*Fcomm)]

            MOV   RCAP2H,#0FFh      ;RELOAD VALUE 57600bps, 11.059MHz  =FFFAh
            MOV   RCAP2L,#0DCh      ;

            MOV  T2CON,#034h        ;SERIAL PORT0, TIMER2 RELOAD START


            CLR   SCON.0            ;CLEAR UART RX, TX FLAGS
            CLR   SCON.1

            MOV   SBUF,#DATA        ;SEND ONE BYTE ON THE SERIAL PORT
```

PWM outputs

The VMX51C900 includes 2 PWM outputs, PWMA and PWMB.

PWM Registers - Port1 Configuration Register

The VMX51C900 PWM outputs are shared with Port1's I/Os. To activate the PWM output, the corresponding bit in the P1IOCTRL register must be set.

TABLE 24: PORT1 I/O CONTROL REGISTER (P1IOCTRL, 9BH)

7	6	5	4
-	PWMBE	-	-

3	2	1	0
-	PWMAE	-	-

Bit	Mnemonic	Description
7		
6	PWMBE	PWMB output enabled when set to 1
5:3	-	
2	PWMAE	PWMA output enabled when set to 1
1:0	-	-

Description of PWMA Function

The PWMA channel is controlled by two SFR registers; one for the PWM data and the other to control the PWMA input clock, PWMACK.

PWMA Data Register

The PWMA data register is composed of two parts: the upper 5 bits, which control the duty cycle of the PWM output and the remaining 3 bits, which control the narrow pulse generator (NPA), The NPA generates narrow pulses among the PWMA 8-cycle frames. The number of pulses generated in the frame cycle corresponds to the values defined in the NPA bits. The insertion of narrow pulses in the PWM frame cycles enables a PWM resolution equivalent to 8 bits.

The following table describes the PWMA data register. The PWMA.x bits determine the duty cycle of the PWMA output waveform. The NPAx bits will generate narrow pulses in the 8-cycle PWM frame.

TABLE 25: PWMA DATA REGISTER (PWMA) – SFR A4H

7	6	5	4
PWMA.4	PWMA.3	PWMA.2	PWMA.1

3	2	1	0
PWMA.0	NPA.2	NPA.1	NPA.0

Bit	Mnemonic	Description
7:4	PWMA[4:0]	Contents of PWM Data
3:0	NPA[3:0]	Inserts Narrow Pulses in a 8-PWM-Cycle Frame

The table below displays the number of narrow pulses generated in an 8-cycle frame versus the NPA number.

NPA[2:0]	Number of Narrow Pulses inserted in an 8-cycle frame
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

PWMA Control Register

The table below describes the PWMA control register which is used to control the frequency at which the PWMA operates.

TABLE 26: PWM CONTROL REGISTER (PWMACTRL) – SFR A3H

7	6	5	4	3	2	1	0
Unused						PWMACK1	PWMACK0

Bit	Mnemonic	Description
7:2	Unused	-
1	PWMACK1	Input Clock Frequency Divider Bit 1
0	PWMACK0	Input Clock Frequency Divider Bit 0

The following table shows the relationship between the values of PWMACK1/PWMACK0 and the value of the divider. Numerical values of the corresponding frequencies are also provided.

PWMACK1	PWMACK0	Divider	PWM clock, Fosc=20MHz
0	0	2	10MHz
0	1	4	5MHz
1	0	8	2.5MHz
1	1	16	1.25MHz

The following formulas can be used to calculate the PWMA output frequency and the PWMA frame rate.

$$\text{PWMA Clock} = \frac{F_{osc}}{2^{(\text{PWMACTRL [1:0] +1})}}$$

$$\text{PWMA Frame} = \frac{F_{osc}}{32 \times 2^{(\text{PWMACTRL [1:0] +1})}}$$

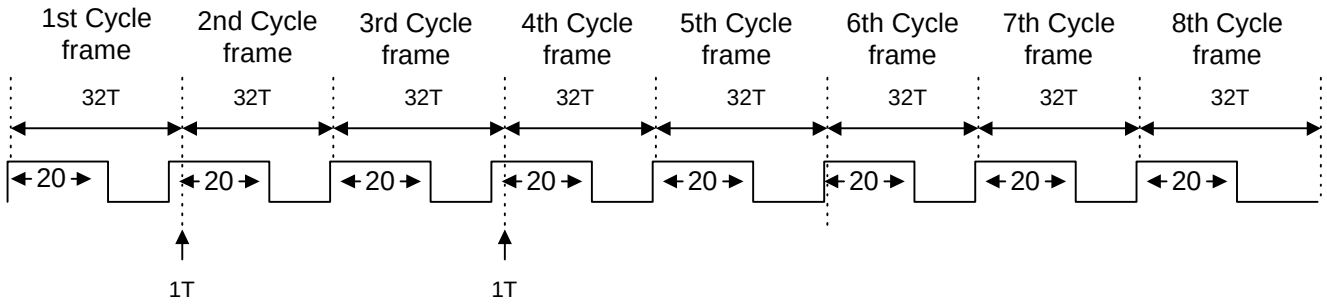
Example of PWM Timing Diagram

The following provides an example the PWMA configuration.

If Fosc = 20MHz, PWMACTRL = #02H, then PWMA clock = 20MHz/2^(2+1) = 20MHz/8 = 2.5MHz. PWMA output cycle frame frequency = (20MHz/2^(2+1))/32 = 78.1 kHz

```
MOV PWMACTRL,#02H     ; PWMA Clock = Fosc/8
MOV PWMA #82H         ; PWMA[4:0]=10h (=20T high, 12T low), NPA[2:0] = 2
MOV P1IOCTRL, #04H    ; Enable P1.2 as PWMA output pin
```

FIGURE 16: PWMA TIMING DIAGRAM



(Narrow pulse inserted by NPA[2:0]=2)

PWMA clock= 1/T= Fosc / 2^(PWMACK+1)
The PWMA output cycle frame frequency = PWMA clock/32 = [Fosc/2^(PWMACK+1)]/32

.

PWMB Function Description

The VMX51C900 PWMB can operate as an 8-bit PWM or as a 5-bit PWM. Unlike the PWMA, when the PWMB is configured to operate in 5-bit resolution, there are no narrow pulses generated in the PWM frame cycle.

The PWMB channel is controlled by two SFR registers PWMB Data & PWMB Control). These registers are used to control the resolution and input clock division factor.

PWMB Data Register

The following table describes the PWMB data register which is used to control the duty cycle of the PWM output waveform.

When the PWMB is configured to operate in 5-bit resolution (see below) only the 5 LSBs of the PWMB register are used.

TABLE 27: PWMB DATA REGISTER (PWMB) – SFR B3HH

7	6	5	4
PWMB.7	PWMB.6	PWMB.5	PWMB.4

3	2	1	0
PWMB.3	PWMB.2	PWMB.1	PWMB.0

Bit	Mnemonic	Description
7:0	PWMB[7:0]	PWM duty cycle control

PWMB Control Register

The following table describes the PWMB control register.

TABLE 28: PWMB CONTROL REGISTER (PWMBCTRL) – SFR D3H

7	6	5	4	3	2	1	0
					PWMBRES	PWMBCK1	PWMBCK0

Bit	Mnemonic	Description
[7:3]	Unused	-
2	PWMBRES	0: Set PWMB resolution to 8-bit 1: Set PWMB resolution to 5-bit
1	PWMBCK1	Input Clock Frequency Divider Bit 1
0	PWMBCK0	Input Clock Frequency Divider Bit 0

The following formula is used to calculate the PWMB output frequency:

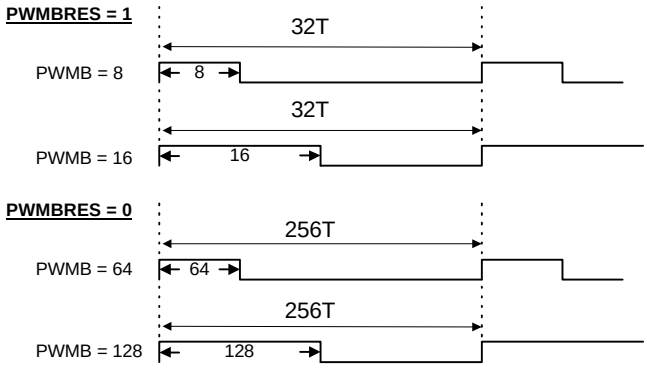
$$\text{PWMB Clock} = \frac{F_{osc}}{2^{(\text{PWMBCK [1:0] +4})}}$$

The following table provides examples of PWMBCK[1:0] bit values versus output frequency when a 20MHz oscillator is used:

PWMBK1	PWMBCK0	Divider	PWMB clock, Fosc=20MHz
0	0	16	1.25MHz
0	1	32	625 KHz
1	0	64	312.5KHz
1	1	128	156.2KHz

The following figure describes the relationship between the PWMB duty cycle vs. the PWMB data register contents and the PWMBRES bit value.

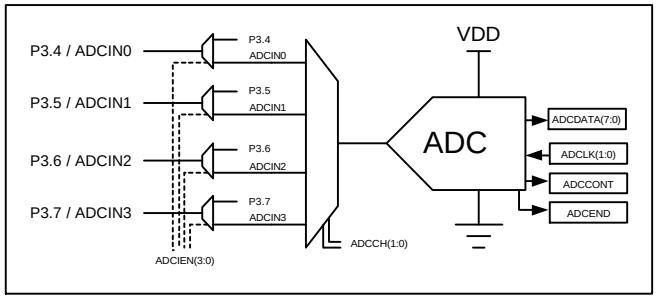
FIGURE 17: PWMB TIMING DIAGRAM EXAMPLES



Analog-to-Digital Converter (ADC)

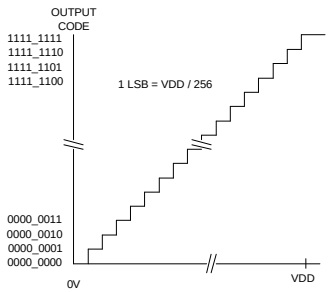
The VMX51C900 includes a 4-channel, 8-bit A/D converter. ADC inputs are shared with I/O ports P3.4 to P3.7. The ADC derives its reference from the supply voltage.

FIGURE 18: ADC SRUCTURE



The ADC binary output represents the ratio of the analog voltage at its input vs. the VMX51C900 supply as shown in the following figure:

FIGURE 19: ADC OUTPUT VS. ANALOG VOLTAGE PRESENT AT ITS INPUTS



The following formula is used to calculate the ADC conversion result based on input and supply voltages.

$$ADCresult = \frac{Vin}{Vsupply} * 256$$

When the ADC input voltage exceeds the supply voltage, the ADC conversion result will saturate at 0FFh. When the voltage is lower than the VMX51C900's ground reference, the ADC conversion result will remain at 00h.

Configuring the VMX51C900 ADC

The configuration and use of the VMX51C900 A/D Converter involves the following steps:

- Activate the ADC Input
- Set the ADC Control Register
- Set the ADC Interrupts (if required)
- Collect the ADC Data

The VMX51C900 ADC shares its inputs with the upper nibble of Port 3. Writing a 1 into a given ADCIENx bit of the P3IOCTRL register configures the corresponding I/O pins as ADC inputs. When the ADCIENx bit remains at 0, the P3 pins can be used as general purpose I/Os.

When the Port 3 pins are configured as ADC inputs, writing to the corresponding P3 register bits will not affect device operation, while reading these port pins will return the port register values.

TABLE 29: PORT3 CONFIGURATION REGISTER (P3IOCTRL, 9DH)

7	6	5	4
ADCIEN3	ADCIEN2	ADCIEN1	ADCIEN0

3	2	1	0
-	-	-	-

Bit	Mnemonic	Description
7	ADCIEN3	ADC Input 3 Enable 0 = P3.7 I/O 1 = ADC input 3
6	ADCIEN2	ADC Input 2 Enable 0 = P3.6 I/O 1 = ADC input 2
5	ADCIEN1	ADC Input 1 Enable 0 = P3.5 I/O 1 = ADC input 1
4	ADCIEN0	ADC Input 0 Enable 0 = P3.4 I/O 1 = ADC input 0
3:0	-	Unused

The ADCCLTR register sets the ADC clock speed value, selects the analog channel which the conversion is to be performed on and defines whether the ADC will perform a single or continuous conversion of the selected channel.

TABLE 30: ADC CONTROL REGISTER ADCCTRL (8EH)

7	6	5	4
ADCEND	ADCCONT	ADCCLK[1:0]	

3	2	1	0
ADCCH[1:0]		-	-

Bit	Mnemonic	Description
7	ADCEND	ADC End of conversion bit Get set to 1 when the ADC conversion completes. It is cleared when the ADCCTRL is written and when the ADCDATA Register is read.
6	ADCCONT	ADC Continuous conversion Bit 1 = ADC run in continuous and the ADCDATA is refreshed after each conversion is performed on the selected channel. 0 = ADC conversion is performed once
5:4	ADCCLK[1:0]	ADC Clock prescaler (see Table below)
3:2	ADCCH[1:0]	ADC Channel select (See table below)
1:0	-	-

The ADCEND bit is used to monitor the status of the ADC conversion process. At the end of a conversion, the ADCEND flag is set. Writing to the ADCCTRL register or reading the ADCDATA register automatically clears the ADCEND bit.

When set to 1, the ADCCONT bit of the ADCCTRL register configures the ADC to perform continuous conversions on the selected ADC input channel and refreshes the ADCDATA register when the conversion is complete.

In order for the ADC to operate properly, a 500KHz to 2.5MHz clock must be fed into the VMX51C900 ADC. The ADC clock is derived from the VMX51C900's oscillator and the division factor is controlled by the ADCCLK1 and ADCCLK0 bits of the ADCCTRL register (see following table).

ADCCLK1	ADCCLK0	ADC_CLK
0	0	Fosc / 8*
0	1	Fosc / 16
1	0	Fosc / 32
1	1	Fosc / 64

*Use this Fosc division factor below 20MHz

Operating the ADC with a clock outside of the 500KHz to 2.5MHz frequency range may lead to an ADC malfunction.

Bits 3 and 2 of the ADCCTRL register control the ADC input on which the conversion will be performed.

ADCCH1	ADCCH0	ADC input channel
0	0	ADCIN0
0	1	ADCIN1
1	0	ADCIN2
1	1	ADCIN3

The ADCDATA register is a read-only register which receives the ADC conversion result.

TABLE 31: ADC DATA REGISTER ADCDATA (8FH)

7	6	5	4	3	2	1	0
ADCDATA[7:0]							

Bit	Mnemonic	Description
7:0	ADCDATA	ADC data register

ADC Conversion Time

ADC conversion requires 20 ADC clock cycles. The conversion rate can be calculated as follows:

$$\textbf{ADC Conv Rate} = \frac{\text{Fadc clock}}{20}$$

$$\textbf{ADC Conv Rate} = \frac{\text{Fosc}}{20*2^{(\text{ADCCLK[1:0]} + 3)}}$$

VMX51C900 ADC Initialization and Use

The following is an example of how to configure the VMX51C900 and use the ADC to read channel 0 in continuous mode using the ADC interrupt to retrieve the conversion result.

```
(...)
            ;*** INITIALIZE THE A/D CONVERTER
            MOV   P3CON,#10000000B          ;CONFIG P3.7 -> ADCIN3

            MOV   ADCCTRL,#0001110B         ;CONFIG ADCCTRL
                                            ;7  ADCEND  = 0
                                            ;6  ADCCONT = SINGLE CONV.
                                            ;5:4 ADCCLK =  Fosc/16
                                            ;3:2 ADCCH =   ADCIN3
                                            ;1:0 UNUSED
                                            ; Fosc = 11.059MHz CONV=34.5KHz
WAITADC:    MOV   A,ADCCTRL                 ;WAIT FOR ADC CONVERSION TO
            ANL   A,#80H                    ;COMPLETE
            JZ    WAITADC

            MOV   BINL,ADCDATA              ;RETRIEVE ADC DATA
(...)
```

Integrated LCD Driver

The VMX51C900 features an on-chip LCD driver designed to drive custom LCD panels in consumer, medical and industrial systems.

The LCD driver is set up to drive a 14-segment x 4 common LCD panel, without the need for external components.

Once configured, the LCD driver operates independently of the processor and generates the appropriate signals to display the data saved in the LCD buffer (LCDBUFx) registers, which are accessible via the SFR registers.

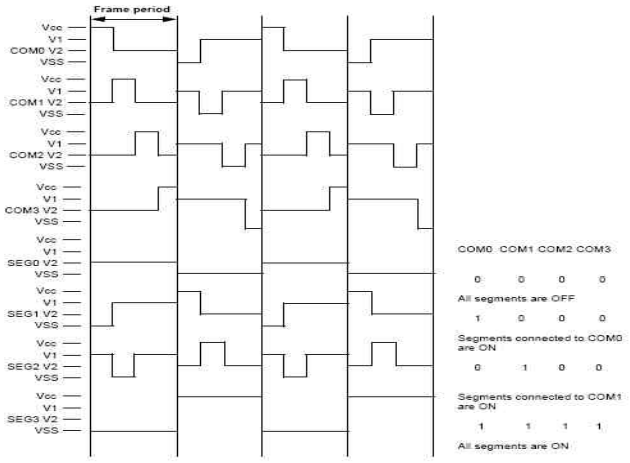
The VMX51C900 LCD driver works on 1/4 duty and 1/3 bias. When activated, LCD driver power consumption is about 0.88mA (1.2uA when de-activated).

Timing Chart of LCD Driver Output

The 14-segment and the 4-common drivers are 4-level outputs that switch between VDD, V1, V2 and VSS LCD driver voltage levels.

The LCD segment/common states are stored into six SFRs called LCDBUFx registers. Each LCDBUFx register controls the state of two LCD segments for each time-slot activated by the LCDCOMx lines. The following diagram shows a typical LCD driver output timing diagram:.

FIGURE 20: LCD DRIVER OUTPUT TIMING DIAGRAM



Configuring the LCD Driver

The initialization of the LCD driver is performed using the LCDCTRL, P0IOCTRL, P2IOCTRL and LCDBUF[6:0] registers.

The LCD driver outputs are multiplexed with regular VMX51C900 I/Os. For this reason, the I/Os required for LCD operation must be configured for the LCD driver mode. This is done by setting the corresponding bits of the P0IOCTRL and P2IOCTRL registers to 1 and, if required, setting the LCDPRI bit of the LCDCTRL register.

TABLE 32: PORT 0 I/O CONTROL REGISTER (P0IOCTRL, 9AH)

7	6	5	4
LCDSEG6	LCDSEG7	LCDSEG8	LCDSEG9

3	2	1	0
LCDSEG10	LCDSEG11	LCDSEG12	LCDSEG13

Bit	Mnemonic	Description
7	LCDSEG6	1= Assign P0.7 to LCD Seg. 6 driver
6	LCDSEG7	1= Assign P0.6 to LCD Seg. 7 driver
5	LCDSEG8	1= Assign P0.5 to LCD Seg. 8 driver
4	LCDSEG9	1= Assign P0.4 to LCD Seg. 9 driver
3	LCDSEG10	1= Assign P0.3 to LCD Seg. 10 driver
2	LCDSEG11	1= Assign P0.2 to LCD Seg. 11 driver
1	LCDSEG12	1= Assign P0.1 to LCD Seg. 12 driver
0	LCDSEG13	1= Assign P0.0 to LCD Seg. 13 driver

TABLE 33: PORT 2 I/O CONTROL REGISTER (P2IOCTRL, 9CH)

7	6	5	4
LCDSEG3	LCDSEG2	LCDSEG1	LCDSEG0-

3	2	1	0
LCDCOM3	LCDCOM2	LCDCOM1	LCDCOM0

Bit	Mnemonic	Description
7	LCDSEG3	1= Assign P2.7 to LCD Seg. 3 driver
6	LCDSEG2	1= Assign P2.6 to LCD Seg. 2 driver
5	LCDSEG1	1= Assign P2.6 to LCD Seg. 1 driver
4	LCDSEG0	1= Assign P2.6 to LCD Seg. 0 driver
3	LCDCOM3	1= Assign P2.6 to LCD Com. 3 driver
2	LCDCOM2	1= Assign P2.6 to LCD Com. 2 driver
1	LCDCOM1	1= Assign P2.6 to LCD Com. 1 driver
0	LCDCOM0	1= Assign P2.6 to LCD Com. 0 driver

The LCD is activated by setting the LCDEN bit of the LCDCTRL register.

The LCDON bit of the LCDCTRL serves to turn the display ON so that the contents in the LCDBUFx registers are sent to the display.

When the LCDPRI bit is set to 1, the VMX51C900 PSEN and ALE pins are assigned as the LCDSEG4 and LCDSEG5 lines, respectively.

TABLE 34: LCD CONTROL REGISTER (LCDCTRL, DFH)

7	6	5	4
LCDON	LCDEN	LCDPRI	-

3	2	1	0
-	LCDCLK2	LCDCLK1	LCDCLK0

Bit	Mnemonic	Description
7	LCDON	1 = LCD Display is ON 0 = LCD Display is OFF
6	LCDEN	1 = LCD is enabled 0 = LCD is disabled
5	LCDPRI	1 = Give priority of LCD operation on #PSEN/LCDSEG4 and ALE/LCDSEG5 pins
4:3	-	Unused
2:0	LCDCLK[2:0]	LCD prescaler select

The LCD driver clock can be adjusted to meet the driving speed requirements of the LCD display. The LCDCLK[2:0] bits of the LCDCTRL register are used to define the LCD driver clock prescaler value as follows:

LCDCLK[2:0]	LCD Clock prescaler value
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The LCD clock speed can be calculated using the following formula.

$$F_{CLK\_LCD} = \frac{F_{osc}}{2 * 32 * LCDCLK[2:0]}$$

The LCD frame frequency is defined as follows:

$$F_{LCD\_Frame} = F_{CLKLCD} / 256$$

The typical range of F_{Frame} is:

1026HZ ~ 8HZ at 16MHz (Fosc = 8MHz)

The six LCDBUFx registers contain the mapping of the LCDSEGxx/LCDCOMx segment state. To activate a given segment (ON) during one of the four time-slots in each frame, the bit corresponding to the segment/common must be set to 1.

For example, to activate the LCDSEG 0 during the second time-slot (controlled by LCDCOM2), bit 6 of the LCDBUF0 must be set to 1. If the LCDSEG 0 also needs to be active during the LCDCOM1 time-slot, then both bits 5 and 6 of the LCDBUF0 register must be set.

The following tables describe the LCD segment/common combinations controlled by the LCDBUFx registers..

TABLE 35: LCD BUFFER REGISTER 0 (LCDBUF0, E1H)

7	6	5	4
SEG0_COM3	SEG0_COM2	SEG0_COM1	SEG0_COM0

3	2	1	0
SEG1_COM3	SEG1_COM2	SEG1_COM1	SEG1_COM0

Bit	Mnemonic	Description
7	SEG0_COM3	If set to 1, the LCDSEG0 will be ON during LCDCOM3 time slot
6	SEG0_COM2	If set to 1, the LCDSEG0 will be ON during LCDCOM2 time slot
5	SEG0_COM1	If set to 1, the LCDSEG0 will be ON during LCDCOM1 time slot
4	SEG0_COM0	If set to 1, the LCDSEG0 will be ON during LCDCOM0 time slot
3	SEG1_COM3	If set to 1, the LCDSEG1 will be ON during LCDCOM3 time slot
2	SEG1_COM2	If set to 1, the LCDSEG1 will be ON during LCDCOM2 time slot
1	SEG1_COM1	If set to 1, the LCDSEG1 will be ON during LCDCOM1 time slot
0	SEG1_COM0	If set to 1, the LCDSEG1 will be ON during LCDCOM0 time slot

TABLE 36: LCD BUFFER REGISTER 1 (LCDBUF1, E2H)

7	6	5	4
SEG2_COM3	SEG2_COM2	SEG2_COM1	SEG2_COM0

3	2	1	0
SEG3_COM3	SEG3_COM2	SEG3_COM1	SEG3_COM0

Bit	Mnemonic	Description
7	SEG2_COM3	If set to 1, the LCDSEG2 will be ON during LCDCOM3 time slot
6	SEG2_COM2	If set to 1, the LCDSEG2 will be ON during LCDCOM2 time slot
5	SEG2_COM1	If set to 1, the LCDSEG2 will be ON during LCDCOM1 time slot
4	SEG2_COM0	If set to 1, the LCDSEG2 will be ON during LCDCOM0 time slot
3	SEG3_COM3	If set to 1, the LCDSEG3 will be ON during LCDCOM3 time slot
2	SEG3_COM2	If set to 1, the LCDSEG3 will be ON during LCDCOM2 time slot
1	SEG3_COM1	If set to 1, the LCDSEG3 will be ON during LCDCOM1 time slot
0	SEG3_COM0	If set to 1, the LCDSEG3 will be ON during LCDCOM0 time slot

TABLE 37: LCD BUFFER REGISTER 2 (LCDBUF2, E3H)

7	6	5	4
SEG4_COM3	SEG4_COM2	SEG4_COM1	SEG4_COM0

3	2	1	0
SEG5_COM3	SEG5_COM2	SEG5_COM1	SEG5_COM0

Bit	Mnemonic	Description
7	SEG4_COM3	If set to 1, the LCDSEG4 will be ON during LCDCOM3 time slot
6	SEG4_COM2	If set to 1, the LCDSEG4 will be ON during LCDCOM2 time slot
5	SEG4_COM1	If set to 1, the LCDSEG4 will be ON during LCDCOM1 time slot
4	SEG4_COM0	If set to 1, the LCDSEG4 will be ON during LCDCOM0 time slot
3	SEG5_COM3	If set to 1, the LCDSEG5 will be ON during LCDCOM3 time slot
2	SEG5_COM2	If set to 1, the LCDSEG5 will be ON during LCDCOM2 time slot
1	SEG5_COM1	If set to 1, the LCDSEG5 will be ON during LCDCOM1 time slot
0	SEG5_COM0	If set to 1, the LCDSEG5 will be ON during LCDCOM0 time slot

TABLE 38: LCD BUFFER REGISTER 3 (LCDBUF3, E4H)

7	6	5	4
SEG6_COM3	SEG6_COM2	SEG6_COM1	SEG6_COM0

3	2	1	0
SEG7_COM3	SEG7_COM2	SEG7_COM1	SEG7_COM0

Bit	Mnemonic	Description
7	SEG6_COM3	If set to 1, the LCDSEG6 will be ON during LCDCOM3 time slot
6	SEG6_COM2	If set to 1, the LCDSEG6 will be ON during LCDCOM2 time slot
5	SEG6_COM1	If set to 1, the LCDSEG6 will be ON during LCDCOM1 time slot
4	SEG6_COM0	If set to 1, the LCDSEG6 will be ON during LCDCOM0 time slot
3	SEG7_COM3	If set to 1, the LCDSEG7 will be ON during LCDCOM3 time slot
2	SEG7_COM2	If set to 1, the LCDSEG7 will be ON during LCDCOM2 time slot
1	SEG7_COM1	If set to 1, the LCDSEG7 will be ON during LCDCOM1 time slot
0	SEG7_COM0	If set to 1, the LCDSEG7 will be ON during LCDCOM0 time slot

TABLE 39: LCD BUFFER REGISTER 4 (LCDBUF4, E5H)

7	6	5	4
SEG8_COM3	SEG8_COM2	SEG8_COM1	SEG8_COM0

3	2	1	0
SEG9_COM3	SEG9_COM2	SEG9_COM1	SEG9_COM0

Bit	Mnemonic	Description
7	SEG8_COM3	If set to 1, the LCDSEG8 will be ON during LCDCOM3 time slot
6	SEG8_COM2	If set to 1, the LCDSEG8 will be ON during LCDCOM2 time slot
5	SEG8_COM1	If set to 1, the LCDSEG8 will be ON during LCDCOM1 time slot
4	SEG8_COM0	If set to 1, the LCDSEG8 will be ON during LCDCOM0 time slot
3	SEG9_COM3	If set to 1, the LCDSEG9 will be ON during LCDCOM3 time slot
2	SEG9_COM2	If set to 1, the LCDSEG9 will be ON during LCDCOM2 time slot
1	SEG9_COM1	If set to 1, the LCDSEG9 will be ON during LCDCOM1 time slot
0	SEG9_COM0	If set to 1, the LCDSEG9 will be ON during LCDCOM0 time slot

TABLE 40: LCD BUFFER REGISTER 5 (LCDBUF5, E6H)

7	6	5	4
SEG10_COM3	SEG10_COM2	SEG10_COM1	SEG10_COM0

3	2	1	0
SEG11_COM3	SEG11_COM2	SEG11_COM1	SEG11_COM0

Bit	Mnemonic	Description
7	SEG10_COM3	If set to 1, the LCDSEG10 will be ON during LCDCOM3 time slot
6	SEG10_COM2	If set to 1, the LCDSEG10 will be ON during LCDCOM2 time slot
5	SEG10_COM1	If set to 1, the LCDSEG10 will be ON during LCDCOM1 time slot
4	SEG10_COM0	If set to 1, the LCDSEG10 will be ON during LCDCOM0 time slot
3	SEG11_COM3	If set to 1, the LCDSEG11 will be ON during LCDCOM3 time slot
2	SEG11_COM2	If set to 1, the LCDSEG11 will be ON during LCDCOM2 time slot
1	SEG11_COM1	If set to 1, the LCDSEG11 will be ON during LCDCOM1 time slot
0	SEG11_COM0	If set to 1, the LCDSEG11 will be ON during LCDCOM0 time slot

Table 41: LCD Buffer Register 6 **(LCDBUF6, E7h)**

7	6	5	4
SEG12_COM3	SEG12_COM2	SEG12_COM1	SEG12_COM0

3	2	1	0
SEG13_COM3	SEG13_COM2	SEG13_COM1	SEG13_COM0

Bit	Mnemonic	Description
7	SEG12_COM3	If set to 1, the LCDSEG12 will be ON during LCDCOM3 time slot
6	SEG12_COM2	If set to 1, the LCDSEG12 will be ON during LCDCOM2 time slot
5	SEG12_COM1	If set to 1, the LCDSEG12 will be ON during LCDCOM1 time slot
4	SEG12_COM0	If set to 1, the LCDSEG12 will be ON during LCDCOM0 time slot
3	SEG13_COM3	If set to 1, the LCDSEG13 will be ON during LCDCOM3 time slot
2	SEG13_COM2	If set to 1, the LCDSEG13 will be ON during LCDCOM2 time slot
1	SEG13_COM1	If set to 1, the LCDSEG13 will be ON during LCDCOM1 time slot
0	SEG13_COM0	If set to 1, the LCDSEG13ill be ON during LCDCOM0 time slot

VMX51C900 LCD Driver Example Program

The following program example show the basic steps required to initialize and use the VMX51C900 LCD driver.

```
;** LCD DRIVER INITIALISATION

        MOV   P0IOCTRL,#0FFH        ;Assign I/O pin to LCD driver
        MOV   P2IOCTRL,#0FFH

        MOV  LCDCON,#11100110B      ;LCD_ON=1
                                    ;LCD_EN =1 -> ENABLE
                                    ;SEG = 1
                                    ;BIT3, BIT4 = UNUSED
                                    ;LS[2:0] = 110 -> PRESCALER = 64

;**LCD SEGMENTS CONFIGURATION
        MOV  LCDBUF0,#00010010B     ;LCDSEG0 is ON during COM0
                                    ;& LCDSEG1 is ON during
                                    ;LCDCOM1 period
        MOV  LCDBUF1,#01000000B     ;LCDSEG2 is ON during LCDCOM2
                                    ;period
        MOV  LCDBUF2,#11111111B     ;LCDSEG4 & LCDSEG5 are always
                                    ;ON (…)
        MOV  LCDBUF6,#00000010B     ;LCDSEG13 is ON during LCDCOM1
```

The following table provides a condensed view of the LCD Segment/LCD Common control vs. LCDBUFx registers.

		LCDCOM3	**LCDCOM2**	**LCDCOM1**	**LCDCOM0**	**LCDCOM3**	**LCDCOM2**	**LCDCOM1**	**LCDCOM0**
Mnemonic	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCDBUF0	E1H	LCDSEG0	LCDSEG0	LCDSEG0	LCDSEG0	LCDSEG1	LCDSEG1	LCDSEG1	LCDSEG1
LCDBUF1	E2H	LCDSEG2	LCDSEG2	LCDSEG2	LCDSEG2	LCDSEG3	LCDSEG3	LCDSEG3	LCDSEG3
LCDBUF2	E3H	LCDSEG4	LCDSEG4	LCDSEG4	LCDSEG4	LCDSEG5	LCDSEG5	LCDSEG5	LCDSEG5
LCDBUF3	E4H	LCDSEG6	LCDSEG6	LCDSEG6	LCDSEG6	LCDSEG7	LCDSEG7	LCDSEG7	LCDSEG7
LCDBUF4	E5H	LCDSEG8	LCDSEG8	LCDSEG8	LCDSEG8	LCDSEG9	LCDSEG9	LCDSEG9	LCDSEG9
LCDBUF5	E6H	LCDSEG10	LCDSEG10	LCDSEG10	LCDSEG10	LCDSEG11	LCDSEG11	LCDSEG11	LCDSEG11
LCDBUF6	E7H	LCDSEG12	LCDSEG12	LCDSEG12	LCDSEG12	LCDSEG13	LCDSEG13	LCDSEG13	LCDSEG13

Interrupts

The VMX51C900 has nine interrupts (10 if the WDT is included) and eight interrupt vectors (including reset) used for handling. The interrupts are enabled via the IE register (see following table).

TABLE 42: IEN0 INTERRUPT ENABLE REGISTER –SFR A8H

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit	**Mnemonic**	**Description**
7	EA	Disables All Interrupts 0: no interrupt acknowledgment 1: Each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
6	-	Reserved
5	ET2	Timer 2 Interrupt Enable Bit
4	ES	Serial Port Interrupt Enable Bit
3	ET1	Timer 1 Interrupt Enable Bit
2	EX1	External Interrupt 1 Enable Bit
1	ET0	Timer 0 Interrupt Enable Bit
0	EX0	External Interrupt 0 Enable Bit

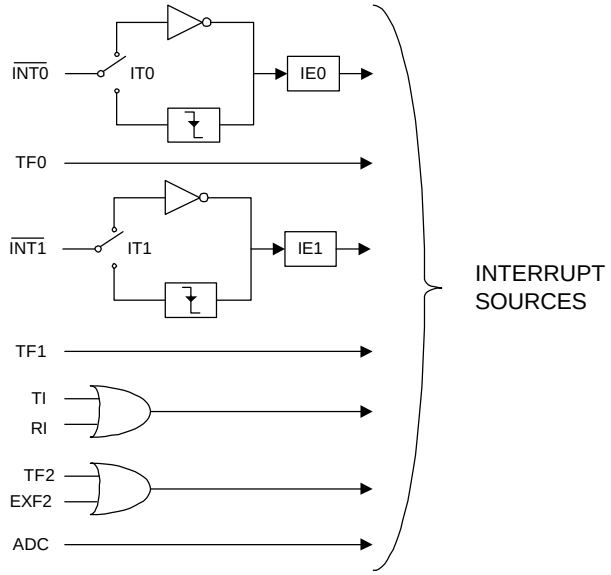
TABLE 43: IEN1 INTERRUPT ENABLE REGISTER 1–SFR A9H

7	6	5	4	3	2	1	0
-	-	-	-	ADCIE	-	-	-

Bit	**Mnemonic**	**Description**
7:4	-	-
3	ADCIE	ADC Interru[pt Enable
2:0	-	-

The following figure provides a pictorial description of the various interrupts on the VMX51C900:

FIGURE 21: INTERRUPT SOURCES



Interrupt Vectors

The following table specifies each interrupt source, its flag and its vector address.

TABLE 44: INTERRUPT VECTOR ADDRESS

Interrupt Source	**Flag**	**Vector Address**
RESET (+ WDT)	WDR	0000h*
INT0	IE0	0003h
Timer 0	TF0	000Bh
INT1	IE1	0013h
Timer 1	TF1	001Bh
Serial Port	RI+TI	0023h
Timer 2	TF2+EXF2	002Bh
ADC Interrupt	ADCIF	004Bh

Execution of an Interrupt

When the processor receives an interrupt request, an automatic jump to the desired subroutine occurs. This jump is similar to executing a branch to a subroutine instruction: the processor automatically saves the address of the next instruction on the stack. An internal flag is set to indicate that an interrupt is taking place, and then the jump instruction is executed. An interrupt subroutine must always end with the RETI instruction. This instruction allows the processor to retrieve the return address placed on the stack and update the internal flags of the interrupt controller.

Interrupt Enable and Interrupt Priority

When the VMX51C900 is reset, the IEN0 and IEN1 registers are cleared, disabling all the interrupts. The corresponding bits in the IEN0 and IEN1 registers must be set to enable the interrupts.

The IEN0 register is part of the bit addressable internal RAM. Therefore, each bit can be individually modified in one instruction without having to modify the other bits of the register. The IEN1 register that controls the ADC interrupt is not bit addressable. In order to enable the ADC interrupt, a direct write must be performed in the IEN1 register to set the ADCIE bit to 1.

All interrupts can be inhibited by clearing the EA bit of the IEN0 register.

The priority in which the interrupts are serviced is displayed in the following table:

TABLE 45: INTERRUPT PRIORITY

Interrupt Source
RESET + WDT (Highest Priority)
IE0
TF0
IE1
TF1
RI+TI
TF2+EXF2
ADCIP (Lowest Priority)

Modifying the Order of Priority

The VMX51C900 allows the user to modify the natural priority of the interrupts by programming the corresponding bits in the IP (interrupt priority) register. When any bit in this register is set to 1, it gives the corresponding source priority over interrupts from sources that do not have their corresponding IP or IP1 bit set to 1.

The IP and IP1 register structures are represented in the following tables:

TABLE 46: IP INTERRUPT PRIORITY REGISTER –SFR B8H

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit	Mnemonic	Description
7	-	
6	-	
5	PT2	Gives Timer 2 Interrupt Higher Priority
4	PS	Gives Serial Port Interrupt Higher Priority
3	PT1	Gives Timer 1 Interrupt Higher Priority
2	PX1	Gives INT1 Interrupt Higher Priority
1	PT0	Gives Timer 0 Interrupt Higher Priority
0	PX0	Gives INT0 Interrupt Higher Priority

TABLE 47: IP1 INTERRUPT PRIORITY REGISTER 1 –SFR B9H

7	6	5	4	3	2	1	0
-	-	-	-	ADCIP	-	-	-

Bit	Mnemonic	Description
7:4	-	
3	ADCIP	Gives ADC Interrupt Higher Priority
2:0	-	

External Interrupts

The VMX51C900 has two external interrupt inputs (INT0 and INT1). These interrupt lines are shared with P3.2 and P3.3.

The IE0 and IE1 bits of the TCON register are external flags that detect a low level or high-to-low transition on the INT0, INT1 interrupt pins respectively. These flags are automatically cleared when the corresponding interrupt is serviced.

Bits IT0 and IT1 of the TCON register determine whether the external interrupts are level or edge sensitive.

IT0 = 0: The INT0, if enabled, occurs if a low level is present on P3.2

IT0 = 1: The INT0, if enabled, occurs if a high-to-low transition is detected on P3.2

IT1 = 0: The INT1, if enabled, occurs if a low level is present on P3.3

IT1 = 1: The INT1, if enabled, occurs if a high-to-low transition is detected on P3.3

The state of the external interrupt, when enabled, can be monitored using flags IE0 and IE1 of the TCON register that are set when the interrupt condition occurs.

In cases where the interrupt is configured as edge triggered, the associated flag is automatically cleared when the interrupt is serviced. If the interrupt is configured as level sensitive, the interrupt flag must be cleared by the software.

Timer0 and Timer1 Interrupts

Both Timer0 and Timer1 can be configured to generate an interrupt when a rollover of the timer/counter occurs (exception is Timer 0 in Mode 3).

The TF0 and TF1 flags serve to monitor timer overflow occurring intimers 0 and 1. These interrupt flags are automatically cleared when the interrupt is serviced.

Timer 2 interrupt

A Timer 2 interrupt can occur if the TF2 and/or EXF2 flags are set to 1 and if the Timer 2 interrupt is enabled. The TF2 flag is set when a rollover of the Timer 2 counter/timer occurs. The EXF2 flag can be set by a 1 to 0 transition on the T2EX pin by the software.

Note that neither flag is cleared by the hardware upon execution of the interrupt service routine. The service routine may have to determine whether it was TF2 or EXF2 that generated the interrupt. These flag bits will have to be cleared by the software.

Every bit that generates interrupts can either be cleared or set by the software, yielding the same result as when the operation is done by the hardware. In other words, pending interrupts can be cancelled and interrupts can be generated by the software.

Serial Port Interrupt

The serial port can generate an interrupt upon byte reception or when byte transmission is completed. Both conditions share the same interrupt vector and it is up to the user-developed interrupt service routine software to determine what caused the interrupt by examining the serial interrupt flags RI and TI.

Note that neither of these flags are cleared by the hardware upon execution of the interrupt service routine. The flags must be cleared by the software.

ADC Interrupt

Like other peripherals on the VMX51C900, the A/D converter can generate an interrupt to the processor once the conversion is completed. The interrupt vector associated with the A/D converter is 04Bh.

The IP1, IEN1 and IFI special function registers control the ADC interrupt.

To activate the ADC interrupt, the ADCIE bit of the IEN1 register must be set, as well as the general interrupt bit, EA bit 7 of the IEN0 register.

TABLE 48: INTERRUPT ENABLE REGISTER (IEN1, A9H)

7	6	5	4
-	-	-	-

3	2	1	0
ADCIE	-	-	-

Bit	Mnemonic	Description
7:4	-	Unused
3	ADCIE	ADC Interrupt Enable 0 = ADC interrupt Disabled 1 = ADC interrupt Enabled
2:0	-	Unused

By default, the ADC interrupt is set to low priority. However, setting the ADCIP bit of the IP1 register will give the ADC higher priority.

TABLE 49: INTERRUPT PRIORITY REGISTER (IP1, B9H)

7	6	5	4
-	-	-	-

3	2	1	0
ADCIP	-	-	-

Bit	Mnemonic	Description
7:4	-	Unused
3	ADCIP	ADC Interrupt Priority 0 = ADC interrupt is Low Priority 1 = ADC interrupt is High Priority
2:0	-	Unused

When the ADC interrupt is authorized and a conversion is completed, the ACDIF flag of the IF1 register will be set to 1. Once the ADC interrupt routine is executed, the ADCIF will be automatically cleared.

TABLE 50: INTERRUPT FLAG REGISTER (IF1, AAH)

7	6	5	4
-	-	-	-

3	2	1	0
ADCIF	-	-	-

Bit	Mnemonic	Description
7:4	-	Unused
3	ADCIF	ADC Interrupt Flag Will be set to 1 if ADC interrupt occurred. Cleared automatically when the interrupt is serviced.
2:0	-	Unused

ADC Initialization & Use (by Interrupt)

The following code example demonstrates the basic steps for configuring the VMX51C900 A/D converter and use the ADC interrupt to retrieve conversion results. The ADCEND bit of the ADCCTRL register can be used to monitor when the A/D conversion process is terminated.

```
;*** RESET VECTOR
ORG   0000H
            LJMP   START

;*** ADC INTERRUPT JUMP VECTOR ***
ORG   04BH
            LJMP   IRQADC            ;JUMP TO ADC INTERRUPT ROUTINE

;*** MAIN PROGRAM START ***
ORG   0100H

START:      MOV    SP,#0C0H          ;INITIALISE STACK POINTER

;*** INITIALIZE THE A/D CONVERTER

            MOV    P3IOCTRL,#01000000B      ;CONFIG P3.6 -> ADCIN2
ADCGO:      MOV    ADCCTRL,#01001000B       ;CONFIG ADCCTRL
                                            ;7   ADCEND  = 0
                                            ;6   ADCCONT = CONT CONV.
                                            ;5:4 ADCCLK =  Fosc/8
                                            ;3:2 ADCCH =   ADCI2
                                            ;1:0 UNUSED
                                            ;WITH Fosc = 11.059MHz
                                            ;CONV RATE 69.1KHz
            MOV    ADCVALUE,#00H
            MOV    IEN1,#00001000B          ;ENABLE ADC INTERRUPT
            SETB   EA                       ;ENABLE  GENERAL  INTERRUPTS

            (...)

;****************************
;* ADC INTERRUPT
;****************************
IRQADC:     MOV    ADCVALUE,ADCDATA         ;RETRIEVE ADCDATA
            RETI
```

The Watchdog Timer

The VMX51C900 watchdog timer (WDT) is a 16-bit free-running counter operating from an independent 250KHz internal RC oscillator. An overflow of the WDT counter will reset the processor.

The WDT is a useful safety measure for systems that are susceptible to noise, power glitches and other conditions that could cause the software to go into infinite dead loops or runaways. The WDT provides the user software with a recovery mechanism from abnormal software conditions.

Watchdog Timer Registers

The configuration and use of the VMX51C900 watchdog timer is handled by three registers: WDTKEY, WDTCTRL and SYSCON.

The WDTKEY register ensures that the watchdog timer is not inadvertently reset in case of program malfunction.

The WDTCTRL register is by default configured as a read-only register. To modify its contents, two consecutive write operations to the WDTKEY register must be performed as follows:

```
MOV   WDTKEY,#01Eh
MOV   WDTKEY,#0E1h
```

Once the configuration or WDT reset operation is complete, the WDTCTRL register can be restored to read-only by writing the following sequence into the WDTKEY register:

```
MOV   WDTKEY,#0E1h
MOV   WDTKEY,#01Eh
```

TABLE 51: WATCH DOG TIMER KEY REGISTER: WDTKEY – SFR 97H

7	6	5	4	3	2	1	0
WDTKEY7:0							

Bit	Mnemonic	Description
7:0	WDTKEY	Watchdog Key

Once the WDT is enabled, the user software must clear it periodically. If the WDT is not cleared, its overflow will trigger a reset of the VMX51C900.

TABLE 52: WATCH DOG TIMER REGISTERS: WDTCTRL – SFR 9FH

7	6	5	4	3	2	1	0
WDTE	Unused	WDT CLR	Unused		WDT PS2	WDT PS1	WDT PS0

Bit	Mnemonic	Description
7	WDTE	Watchdog Timer Enable Bit
6	Unused	-
5	WDTCLR	Watchdog Timer Counter Clear Bit
[4:3]	Unused	-
2	WDTPS2	Clock Source Divider Bit 2
1	WDTPS1	Clock Source Divider Bit 1
0	WDTPS0	Clock Source Divider Bit 0

The WDT timeout delay can be adjusted by configuring the clock divider input for the WDT time base source clock. To select the divider value, the [WDTPS2~WDTPS0] bits of the watchdog timer control register should be set accordingly.

The following table indicates the approximate timeout periods for different values of the WDTPSx bits of the watchdog timer register.

TABLE 53: TIMEOUT PERIOD AT

WDTPS [2:0]	WDT Period
000	2.048ms
001	4.096ms
010	8.192ms
011	16.384ms
100	32.768ms
101	65.536ms
110	131.072ms
111	262.144ms

To enable the WDT, bit 7 (WDTE) of the WDTCTRL register must be set to 1. The 16-bit counter will then begin counting from the 250KHz oscillator divided, according to the value of the WDTPS2~WDTPS0 bits.

The WDT is cleared by setting the WDTCLR bit of the WDTCTRL to 1. This will clear the contents of the 16-bit counter and force it to restart.

If the WDT overflows, the processor will be reset, the WDR bit (7) of the SYSCON register will be set to 1 and the WDTE bit will be cleared to 0. The user should check the WDR bit if an unexpected reset has taken place.

TABLE 54: WATCH DOG TIMER REGISTER-SYSTEM CONTROL REGISTER (SYSCON)–SFR BFH

7	6	5	4	3	2	1	0
WDR	Unused						ALEI

Bit	Mnemonic	Description
7	WDR	Watch Dog Timer Reset Bit
[6:1]	Unused	-
0	ALEI	1: Enable Electromagnetic Interference Reducer 0: Disable Electromagnetic Interference Reducer

WDT initialization Example

The following program example shows the WDT initialization sequence and the routine to periodically clear it.

```
;*** VARIABLE DEFINITION ***

CPTR        EQU         020H
PORTVAL     EQU         00H

;*** PROGRAM START HERE ****
ORG   0000h
            LJMP    START

;*** MAIN PROGRAM START ***
ORG   0100h

;*** CHECK IF RESET WAS CAUSED BY THE WATCHDOG TIMER
START:      MOV   A,SYSCON
            ANL   A,#80H
            JNZ   WDTRESET          ;WDT BIT SET -> WE GOT A WDT RESET

INITWDT:    MOV   WDTKEY,#01EH  ;UNLOCK THE WDTCTRL REG ACCESS IN
            MOV   WDTKEY,#0E1H  ;WRITING MODE

            MOV   WDTCTRL,#10000010B  ;CONFIG THE WATCHDOG TIMER
                                      ;BIT 7  - WDTEN=1 WATCHDOG TIMER ENABLE
                                      ;BIT 6   - UNUSED
                                      ;BIT 5   - WDTCLR=1 WATCHDOG CLEAR
                                      ;BIT 4:3 - UNUSED
                                      ;BIT 2:0 - WDTCLK=010 - WDT TIMEOUT = 8mS

            MOV   WDTKEY,#0E1H  ;LOCK THE WDTCTRL ACCESS IN WRITING
            MOV   WDTKEY,#01EH
            MOV   PORTVAL,#00H  ;INIT PORT VALUE TO 00H

WDTRESET:   NOP                 ;IF THE WDT CAUSE THE RESET INIT PORTVAL
            MOV   A,PORTVAL     ;TOGGLE P1 VALUE
            CPL   A
            MOV   PORTVAL,A
            MOV   P1,A

;*** SEQUENCE TO CLEAR THE WATCHDOG TIMER (SAME AS CONFIG)
LOOP:       ;MOV   WDTKEY,#01EH  ;UNLOCK THE WDTCTRL REG ACCESS IN
                                 ;WRITING MODE
            ;MOV   WDTKEY,#0E1H
            ;MOV   WDTCTRL,#10100010B      ;CONFIG THE WDT TIMER
                                           ;BIT 7 - WDTEN=1 WDT ENABLE
                                           ;BIT 6   - UNUSED
                                           ;BIT 5   - WDTCLR=1 WDT CLEAR
                                           ;BIT 4:3 - UNUSED
                                           ;BIT 2:0 - WDTCLK=010 - WDT TIMEOUT = 8mS

            ;MOV   WDTKEY,#0E1H  ;LOCK THE WDTCTRL ACCESS IN WRITING
            ;MOV   WDTKEY,#01EH

            (...)

            LJMP   LOOP
```

Crystal Configuration

The crystal connected to the VMX51C900 oscillator input should be of a parallel type, operating in fundamental mode.

The following table shows the recommended value of the capacitors and feedback resistors used at different operating frequencies.

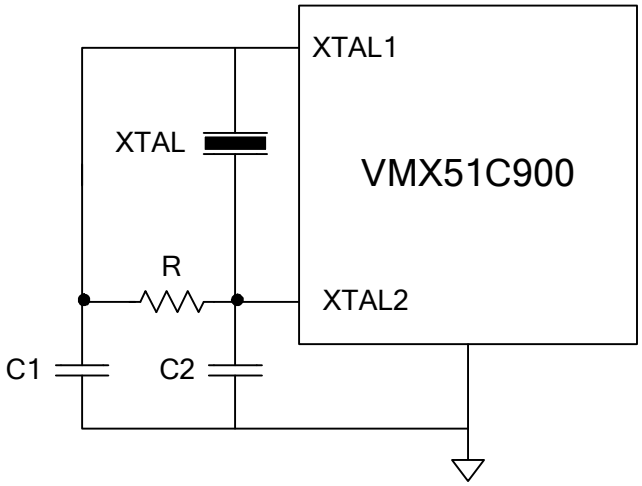
VMX51C900 Crystal configuration			
XTAL	3MHz	6MHz	12MHz
C1	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF
R	open	open	open

XTAL	16MHz	20MHz	25MHz
C1	30 pF	22 pF	15 pF
C2	30 pF	22 pF	15 pF
R	open	open	62KO

Note: Oscillator circuits may differ with various crystals or ceramic resonators of higher oscillation frequency.

Crystals or ceramic resonator characteristics vary from one manufacturer to the other. The user should review the technical literature provided with any crystal or ceramic resonator or contact the manufacturer to select the appropriate values for external components.

FIGURE 22: CRYSTAL CONFIGURATION



Operating Conditions

TABLE 55: OPERATING CONDITIONS

Symbol	Description	Min.	Typ.	Max.	Unit	Remarks
TA	Operating temperature	-40	25	+85	ºC	Ambient temperature under bias
TS	Storage temperature	-55	25	155	ºC	
VCC5	Supply voltage	4.5	5.0	5.5	V	
Fosc	Oscillator Frequency	3.0	-	25	MHz	

DC Characteristics

TABLE 56: DC CHARACTERISTICS

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	Port 0,1,2,3,4,#EA	-0.5	1.0	V	VCC=5V
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	VCC=5V
VIH1	Input High Voltage	Port 0,1,2,3,4,#EA	2.0	VCC+0.5	V	VCC=5V
VI H2	Input High Voltage	RES, XTAL1	70% VCC	VCC+0.5	V	VCC=5V
VOL1	Output Low Voltage	Port 0, ALE, #PSEN		0.4	V	IOL=3.2mA
VOL2	Output Low Voltage	Port 1,2,3,4		0.4	V	IOL=1.6mA
VOH1	Output High Voltage	Port 0	2.4		V	IOH=-800uA
			90%VCC		V	IOH=-80uA
VOH2	Output High Voltage	Port 1,2,3,4,ALE,#PSEN	2.4		V	IOH=-60uA
			90% VCC		V	IOH=-10uA
IIL	Logical 0 Input Current	Port 1,2,4, P3.0-P3.3		-50	uA	Vin=0.45V
ITL	Logical Transition Current	Port 1,2,3,4,P3.0-P3.3		-650	uA	Vin=2.0V
ILI	Input Leakage Current	Port 0, #EA		10	uA	0.45V<Vin< 5V
R RES	Reset Pull-down Resistance	RES	18	90	Kohm	
C˙10	Pin Capacitance			10	pF	Fre=1 MHz, Ta=25˚C
ICC	Power Supply Current	VDD		20	mA	Active mode, 16MHz
				10	mA	Idle mode, 16MHz
				100	uA	Power down mode

FIGURE 23: ICC ACTIVE MODE TEST CIRCUIT

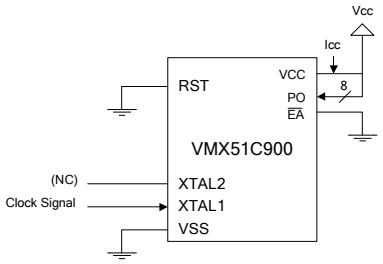
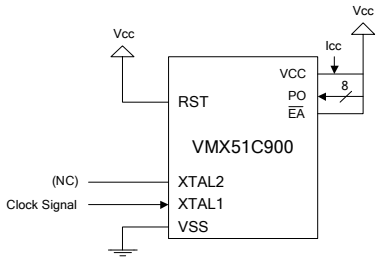


FIGURE 24: ICC IDLE MODE TEST CIRCUIT



AC Characteristics

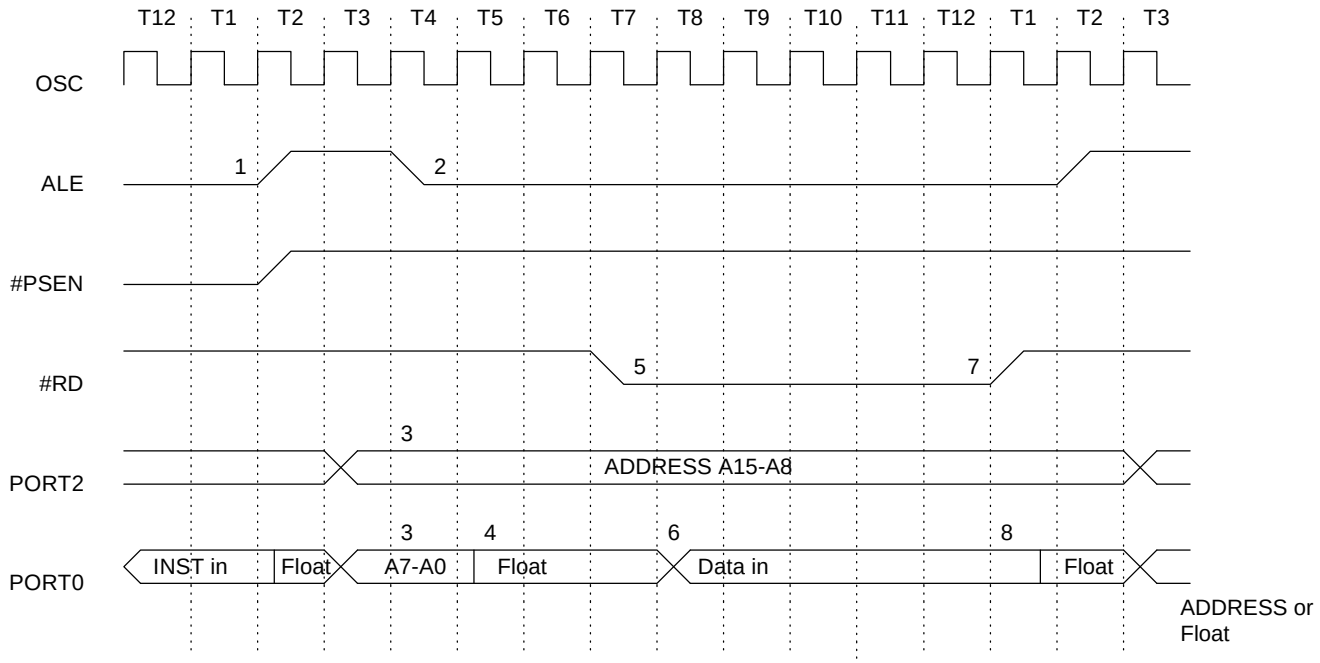
TABLE 57: AC CHARACTERISTICS

Symbol	Parameter	Valid Cycle	Fosc 16			Variable Fosc			Unit
			Min.	Type	Max.	Min.	Type	Max.	
T LHLL	ALE Pulse Width	RD/WRT	115			2xT - 10			nS
T AVLL	Address Valid to ALE Low	RD/WRT	43			T - 20			nS
T LLAX	Address Hold after ALE Low	RD/WRT	53			T - 10			nS
T LLIV	ALE Low to Valid Instruction In	RD			240			4xT - 10	nS
T LLPL	ALE Low to #PSEN low	RD	53			T - 10			nS
T PLPH	#PSEN Pulse Width	RD	173			3xT - 15			nS
T PLIV	#PSEN Low to Valid Instruction In	RD			177			3xT -10	nS
T PXIX	Instruction Hold after #PSEN	RD	0			0			nS
T PXIZ	Instruction Float after #PSEN	RD			87			T + 25	nS
T AVIV	Address to Valid Instruction In	RD			292			5xT - 20	nS
T PLAZ	#PSEN Low to Address Float	RD			10			10	nS
T RLRH	#RD Pulse Width	RD	365			6xT - 10			nS
T WLWH	#WR Pulse Width	WRT	365			6xT - 10			nS
T RLDV	#RD Low to Valid Data In	RD			302			5xT - 10	nS
T RHDX	Data Hold after #RD	RD	0			0			nS
T RHDZ	Data Float after #RD	RD			145			2xT + 20	nS
T LLDV	ALE Low to Valid Data In	RD			590			8xT - 10	nS
T AVDV	Address to Valid Data In	RD			542			9xT - 20	nS
T LLYL	ALE low to #WR High or #RD Low	RD/WRT	178		197	3xT - 10		3xT + 10	nS
T AVYL	Address Valid to #WR or #RD Low	RD/WRT	230			4xT - 20			nS
T QVWH	Data Valid to #WR High	WRT	403			7xT - 35			nS
T QVWX	Data Valid to #WR Transition	WRT	38			T - 25			nS
T WHQX	Data Hold after #WR	WRT	73			T + 10			nS
T RLAZ	#RD Low to Address Float	RD						5	nS
T YALH	#W R or #RD High to ALE High	RD/WRT	53		72	T -10		T+10	nS
T CHCL	Clock Fall Time								nS
T CLCX	Clock Low Time								nS
T CLCH	Clock Rise Time								nS
T CHCX	Clock High Time								nS
T, TCLCL	Clock Period		63				1/fosc		nS

Data Memory Read Cycle Timing

The following timing diagram shows the signal timing of Data Memory Read Cycle.

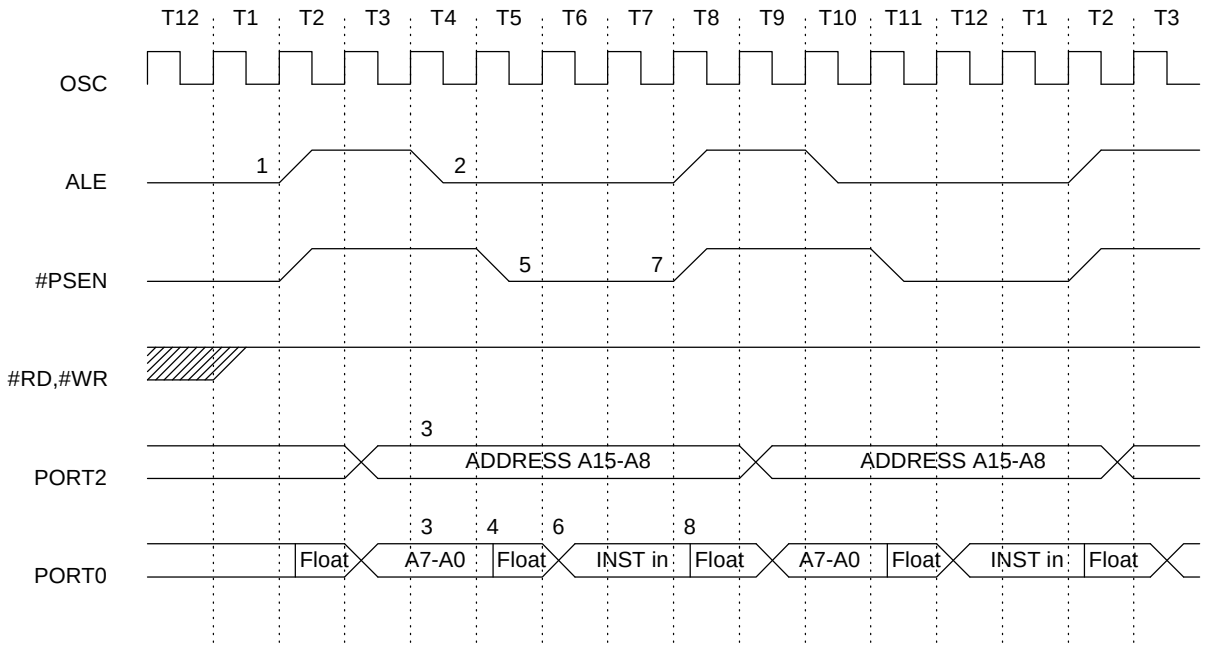
FIGURE 25: DATA MEMORY READ CYCLE TIMING



Program Memory Read Cycle Timing

The following timing diagram shows the signal timing during Program Memory Read Cycle.

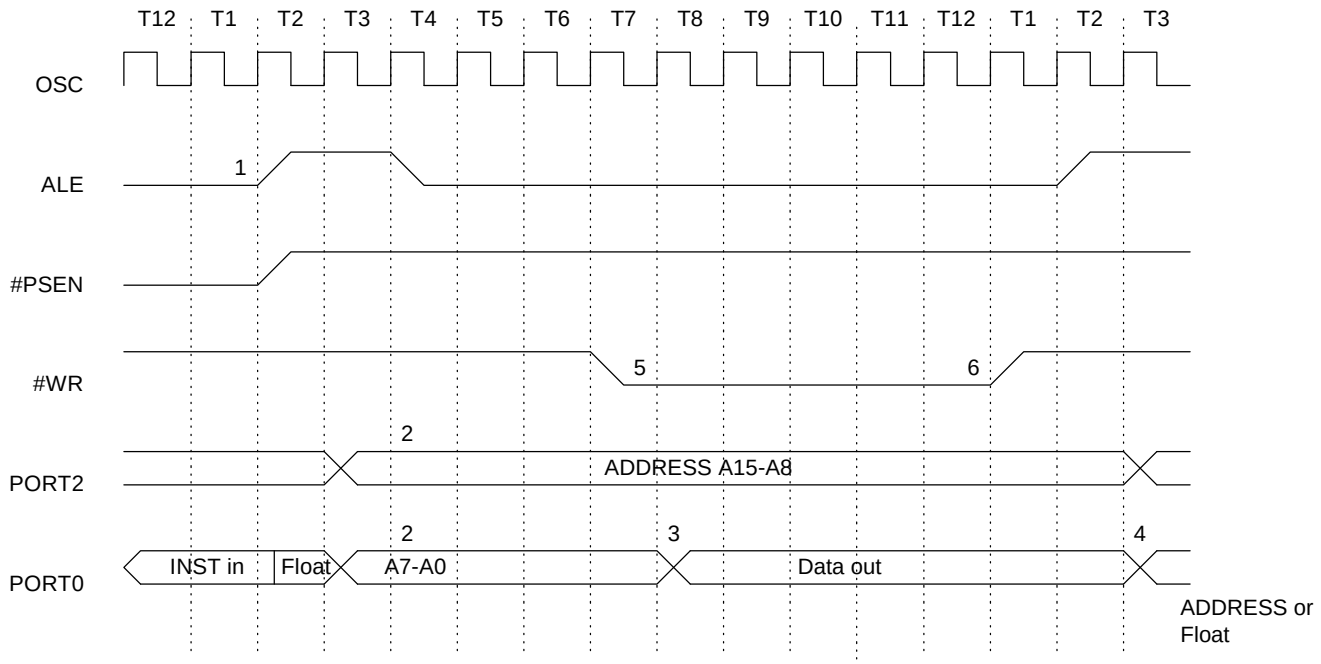
FIGURE 26: PROGRAM MEMORY READ CYCLE



Data Memory Write Cycle Timing

The following timing diagram shows the signal timing during Data Memory Write Cycle.

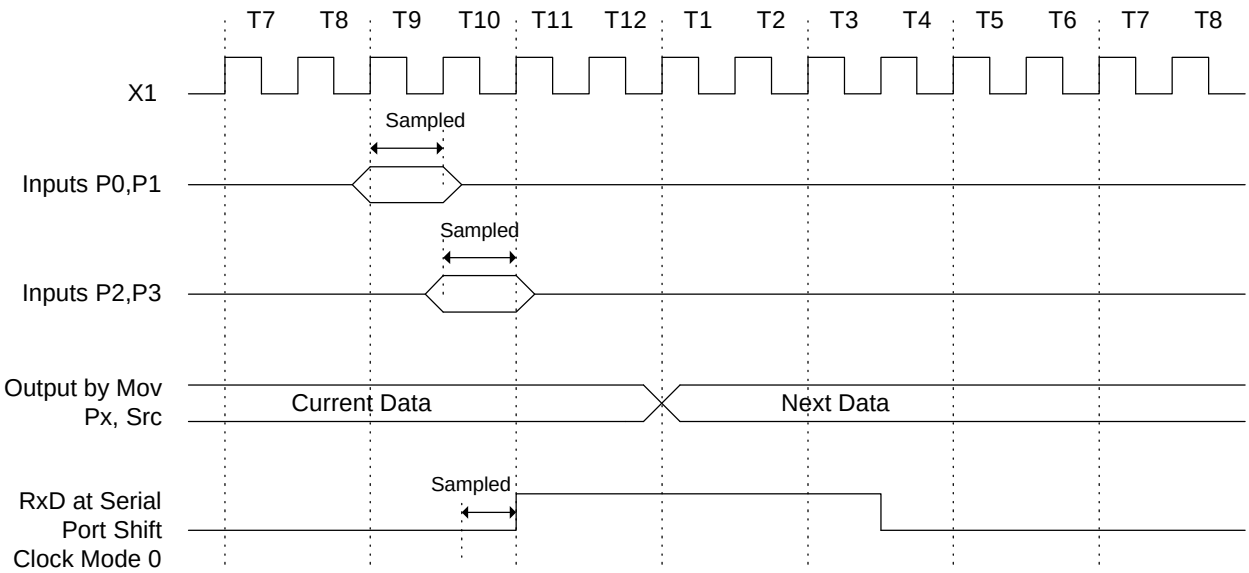
FIGURE 27: DATA MEMORY WRITE CYCLE TIMING



I/O Ports Timing

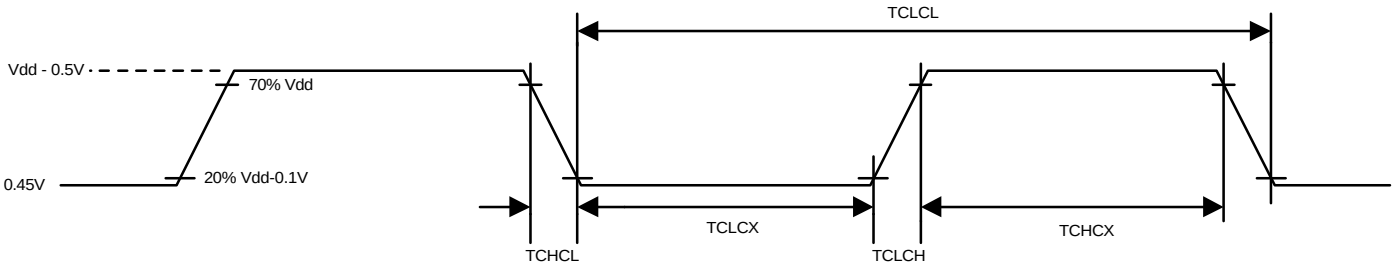
The following timing diagram shows I/O Port Timing.

FIGURE 28: I/O PORTS TIMING



Timing Requirement of the External Clock (VSS = 0v is assumed)

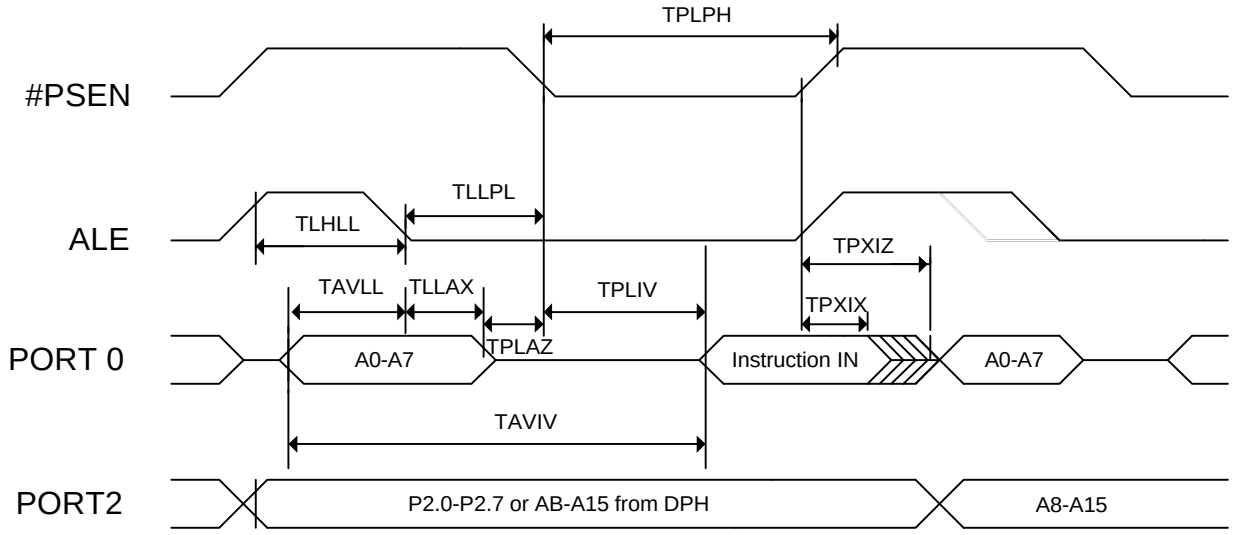
FIGURE 29: TIMING REQUIREMENT OF EXTERNAL CLOCK (VSS= 0.0V IS ASSUMED)



External Program Memory Read Cycle

The following timing diagram shows the signal timing during an External Program Memory Read Cycle.

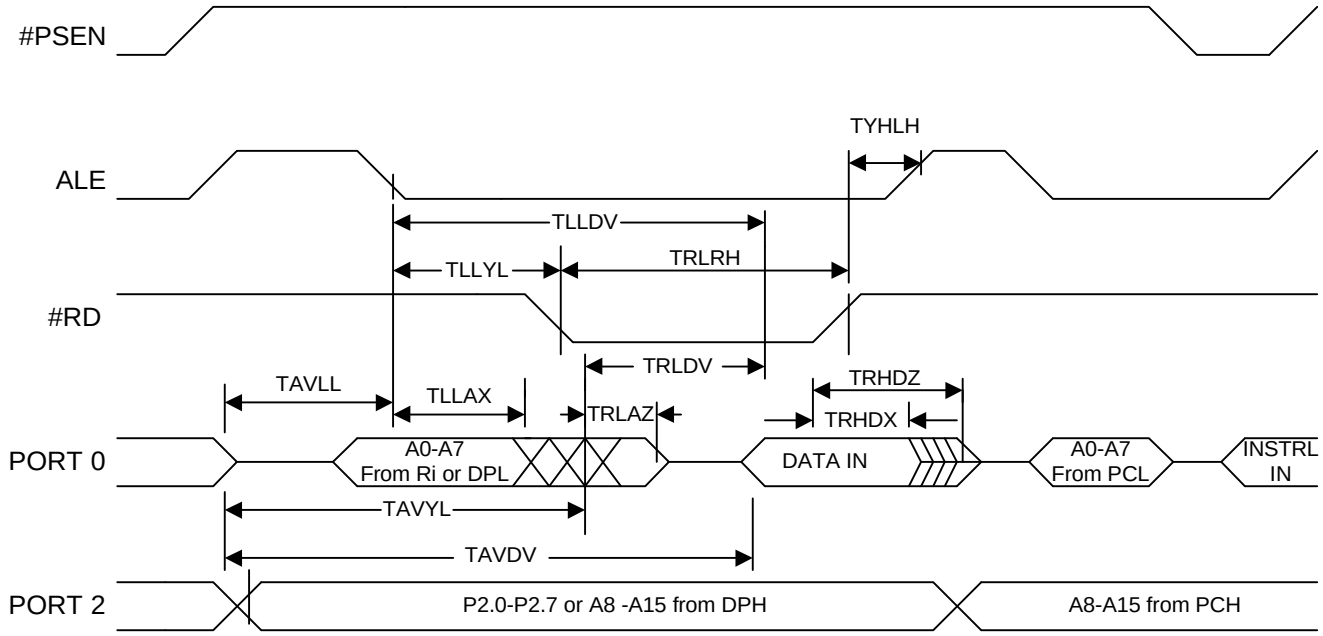
FIGURE 30: EXTERNAL PROGRAM MEMORY READ CYCLE



External Data Memory Read Cycle

The following timing diagram shows the signal timing during an External Data Memory Read Cycle.

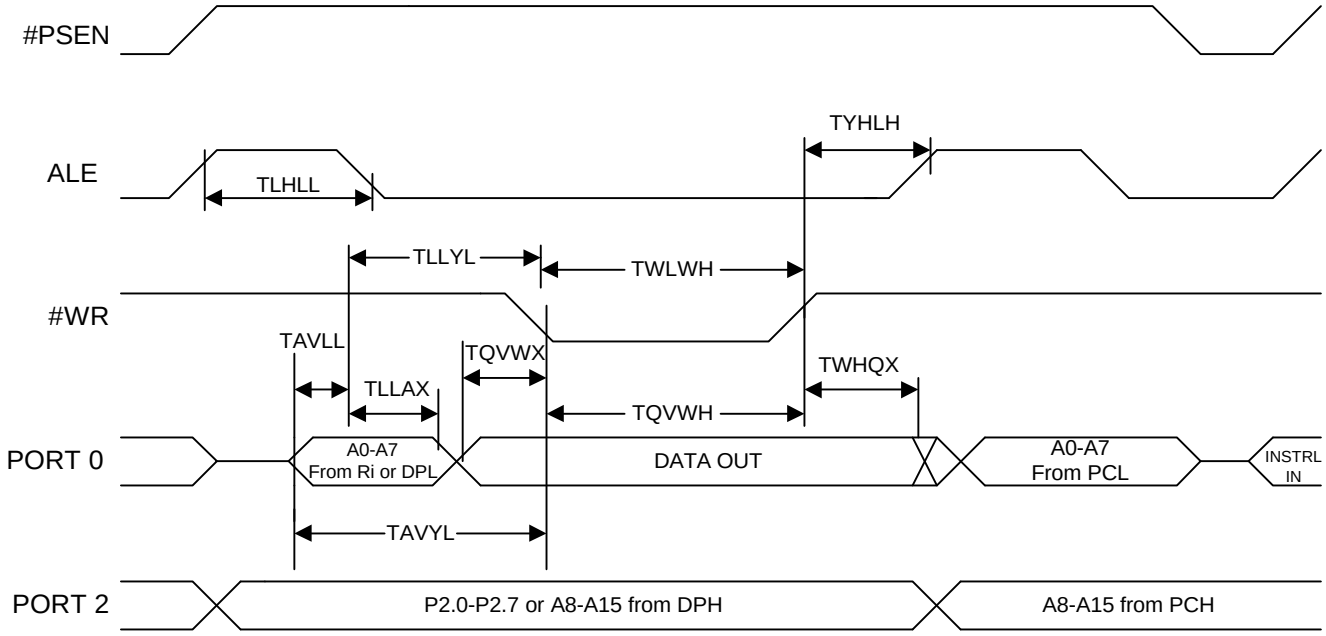
FIGURE 31: EXTERNAL DATA MEMORY READ CYCLE



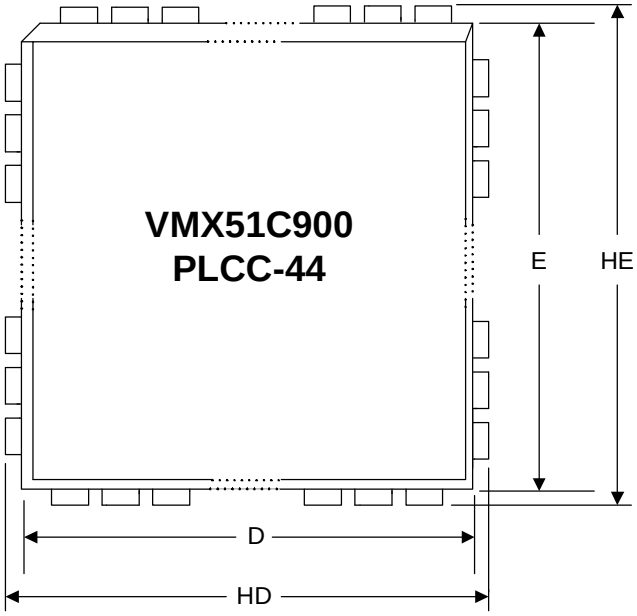
External Data Memory Write Cycle

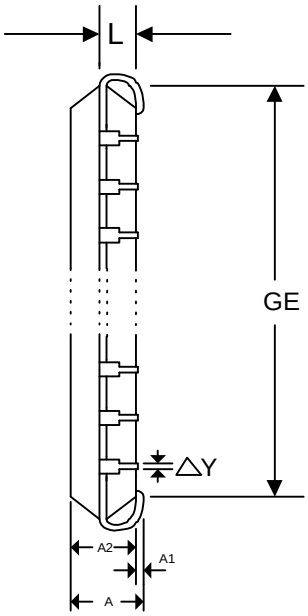
The following timing diagram shows the signal timing during an External Data Memory Write Cycle.

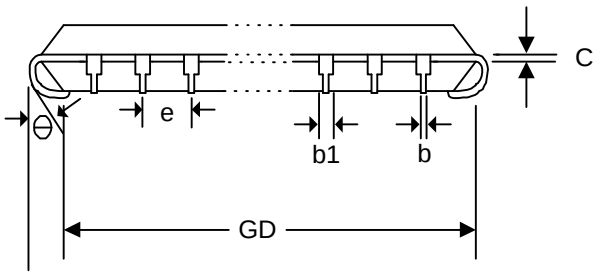
FIGURE 32: EXTERNAL DATA MEMORY WRITE CYCLE



Plastic Chip Carrier (PLCC-44)





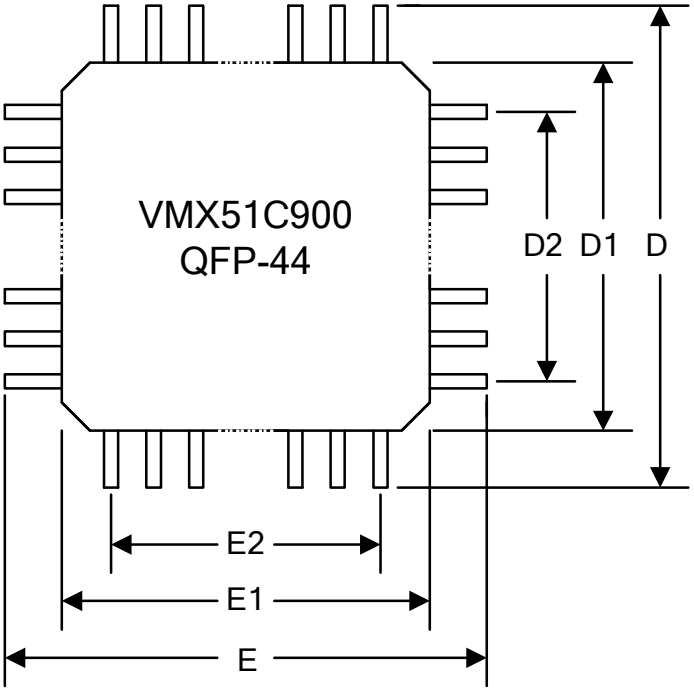


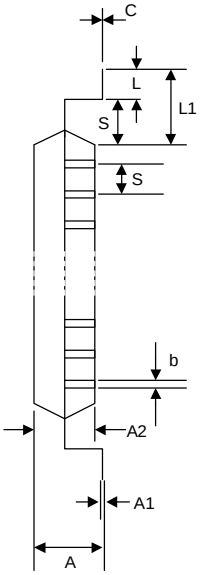
Note:
1. Dimensions D & E do not include interlead Flash.
2. Dimension B1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inch
4. General appearance spec should be based on final visual inspection spec.

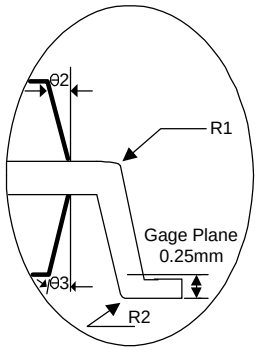
TABLE 58: DIMENSIONS OF PLCC-44 CHIP CARRIER

Symbol	Dimension in inch	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.185	-/4.70
Al	0.020/-	0.51/
A2	0.145/0.155	3.68/3.94
bl	0.026/0.032	0.66/0.81
b	0.016/0.022	0.41/0.56
C	0.008/0.014	0.20/0.36
D	0.648/0.658	16.46/16.71
E	0.648/0.658	16.46/16.71
e	0.050 BSC	1.27 BSC
GD	0.590/0.630	14.99/16.00
GE	0.590/0.630	14.99/16.00
HD	0.680/0.700	17.27/17.78
HE	0.680/0.700	17.27/17.78
L	0.090/0.110	2.29/2.79
?	-/0.004	-/0.10
?y	/	/

Plastic Quad Flat Package (QFP-44)







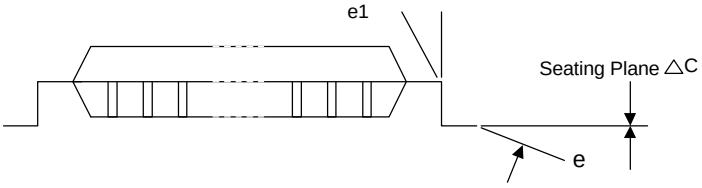


TABLE 59: DIMENSIONS OF QFP-44 CHIP CARRIER

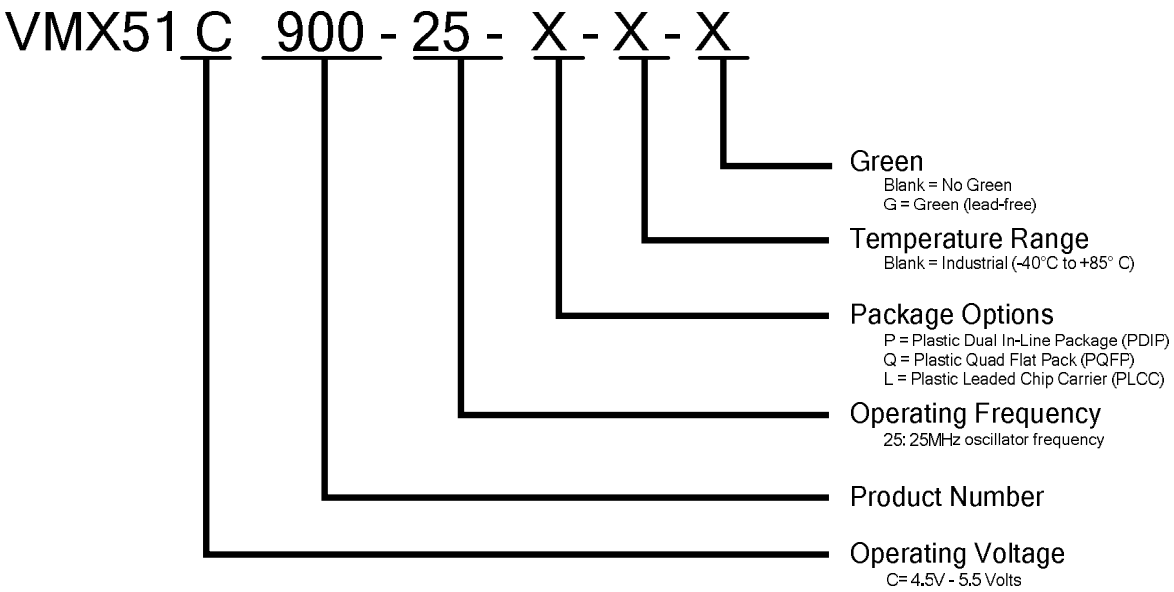
Symbol	Dimension in in.	Dimension in mm
	Minimal/Maximal	Minimal/Maximal
A	-/0.100	-/2.55
Al	0.006/0.014	0.15/0.35
A2	0.071 / 0.087	1.80/2.20
b	0.012/0.018	0.30/0.45
c	0.004 / 0.009	0.09/0.20
D	0.520 BSC	13.20 BSC
D1	0.394 BSC	10.00 BSC
D2	0.315	8.00
E	0.520 BSC	13.20 BSC
E1	0.394 BSC	10.00 BSC
E2	0.315	8.00
e	0.031 BSC	0.80 BSC
L	0.029 / 0.041	0.73/1.03
L1	0.063	1.60
R1	0.005/-	0.13/-
R2	0.005/0.012	0.13/0.30
S	0.008/-	0.20/-
0	0°/7°	as left
? 1	0°/ -	as left
? 2	10° REF	as left
? 3	7° REF	as left
?C	0.004	0.10

Note:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Allowance protrusion is 0.25mm per side.
3. Dimensions D1 and E1 do not include mold mismatch and are determined datum plane.
4. Dimension b does not include dambar protrusion.
5. Allowance dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the lead foot.

Ordering Information

Device Number Structure



VMX51C900 Ordering Options

Device Number	Flash Size	RAM Size	Package Option	Voltage	Temperature	Frequency
VMX51C900-25-L	8KB	256B	PLCC-44	4.5V to 5.5V	-40°C to +85°C	25MHz
VMX51C900-25-Q	8KB	256B	QFP-44	4.5V to 5.5V	-40°C to +85°C	25MHz
VMX51C900-25-P	8KB	256B	DIP-40	4.5V to 5.5V	-40°C to +85°C	25MHz
VMX51C900-25-LG	8KB	256B	PLCC-44	4.5V to 5.5V	-40°C to +85°C	25MHz
VMX51C900-25-QG	8KB	256B	QFP-44	4.5V to 5.5V	-40°C to +85°C	25MHz
VMX51C900-25-PG	8KB	256B	DIP-40	4.5V to 5.5V	-40°C to +85°C	25MHz

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