VND600PEP-E

DOUBLE CHANNEL HIGH SIDE DRIVER

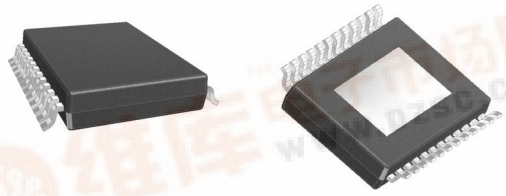
Table 1. General Features

TYPE	$R_{DS(on)}$	I_{lim}	V_{CC}
VND600PEP-E	30mΩ (*)	25A	36V

(*) Per each channel

- DC SHORT CIRCUIT CURRENT: 25A
- CMOS COMPATIBLE INPUTS
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST: LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (**)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



PowerSSO-24

DESCRIPTION

The VND600PEP-E is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device has two channels in high side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current. Built-in thermal shut-down and outputs current limitation protect the chip from over temperature and short circuit. Device turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-24	VND600PEP-E	VND600PEPTR-E

Note: (**) See application schematic at page 9

Figure 2. Block Diagram

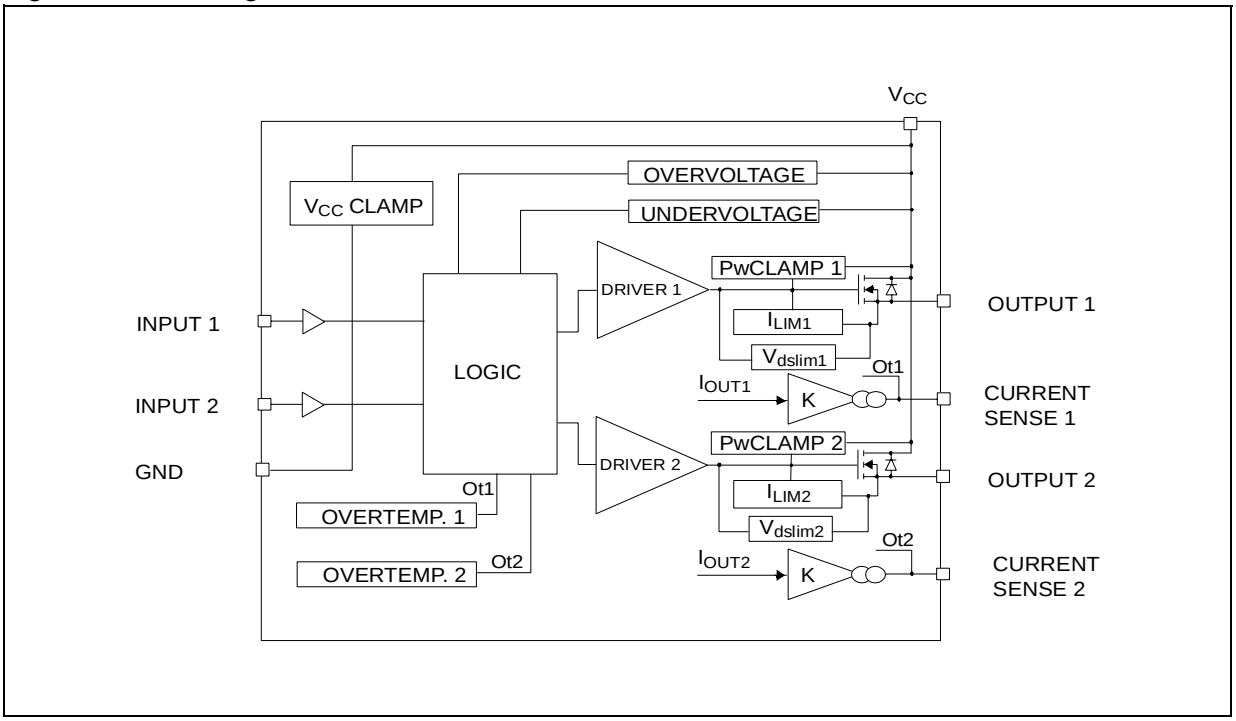
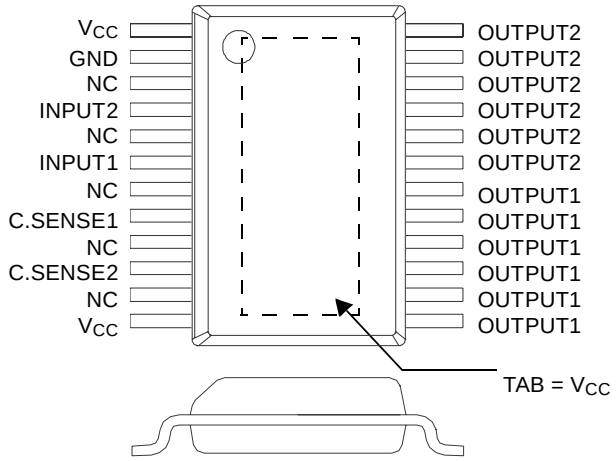


Table 3. Absolute Maximum Ratings

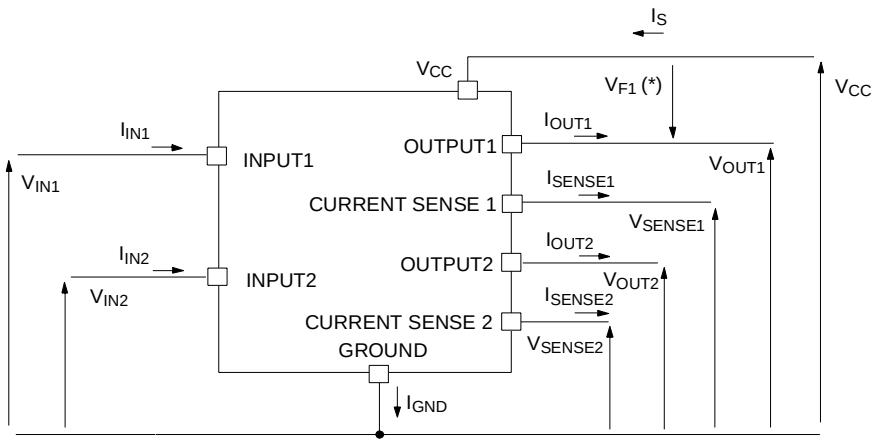
Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
$- I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current	-21	A
I_{IN}	Input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum Switching Energy (L=0.13mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=40A)	146	mJ
P_{tot}	Power dissipation at T_c=25°C	96	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins



Connection / Pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To Ground	Through 1KΩ resistor	X		Through 10KΩ resistor

Figure 4. Current and Voltage Conventions



(*) $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition

Table 4. Thermal Data

Symbol	Parameter		Value		Unit
$R_{thj\text{-}case}$ (1)	Thermal resistance junction-case	(MAX)	1.8		°C/W
$R_{thj\text{-}case}$ (2)	Thermal resistance junction-case	(MAX)	1.3		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	(MAX)	54 (*)	39 (**)	°C/W

Note: (*) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick).
Note: (**) When mounted on a standard single-sided FR-4 board with 8cm^2 of Cu (at least 35µm thick).
Note: (1) one channel ON - (2) two channels ON

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)
(Per each channel)

Table 5. Power

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC} (**)	Operating supply voltage		5.5	13	36	V
V_{USD} (**)	Undervoltage shutdown		3	4	5.5	V
V_{OV} (**)	Overvoltage shutdown		36			V
R_{ON}	On state resistance	I_{OUT}=5A; T_j=25°C I_{OUT}=5A; T_j=150°C I_{OUT}=3A; V_{CC}=6V			30 60 100	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (see note 1)	41	48	55	V
I_S (**)	Supply current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C On state; V_{IN}=5V; V_{CC}=13V; I_{OUT}=0A; R_{SENSE}=3.9kΩ		12 12	40 25 6	µA µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V	0		50	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=V_{SENSE}=0V; V_{CC}=13V; T_j =25°C			3	µA

Note: 1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Note: (**) Per device.

Table 6. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L=2.6Ω (see Figure 5)		30		µs
$t_{d(off)}$	Turn-on delay time	R_L=2.6Ω (see Figure 5)		30		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=2.6Ω (see Figure 5)		See relative diagram		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=2.6Ω (see Figure 5)		See relative diagram		V/µs

Table 7. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_F	Forward on Voltage	-I_{OUT}=2.6A; T_j=150°C			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

Table 8. Logic Input (Channels 1,2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN}=1.25V	20	65		µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

Table 9. Current Sense (9V≤V_{CC}≤16V) (see Figure 8)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=0.5A; V_{SENSE}=0.5V; other channels open; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=0.5A; V_{SENSE}=0.5V; other channels open; T_j= -40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=5A; V_{SENSE}=4V; other channels open; T_j=-40°C T_j=25°C...150°C	3800 3950	4400 4400	5400 5200	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=5A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT1} or I_{OUT2}=15A; V_{SENSE}=4V; other channels open; T_j=-40°C T_j=25°C...150°C	3800 3950	4400 4400	4900 4700	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT1} or I_{OUT2}=15A; V_{SENSE}=4V; other channels open; T_j=-40°C...150°C	-6		+6	%
$V_{SENSE1,2}$	Max analog sense output voltage	V_{CC}=5.5V; $I_{OUT1,2}$=2.5A; R_{SENSE}=10kΩ V_{CC}>8V, $I_{OUT1,2}$=5A; R_{SENSE}=10kΩ	2 4			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=3.9kΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	V_{CC}=13V; T_j>T_{TSD}; All Channels Open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 2)			500	µs

Note: 2. Current sense signal delay after positive input slope

ELECTRICAL CHARACTERISTICS (continued)

Table 10. Protections (See note 3)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	DC short circuit current	V_{CC}=13V 5.5V<V_{CC}<36V	25	40	70 70	A A
T_{TSD}	Thermal shut-down temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{demag}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=0.5A; T_j= -40°C...+150°C		50		mV

Note: 3. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Figure 5. Switching Characteristics (Resistive load R_L=2.6Ω)

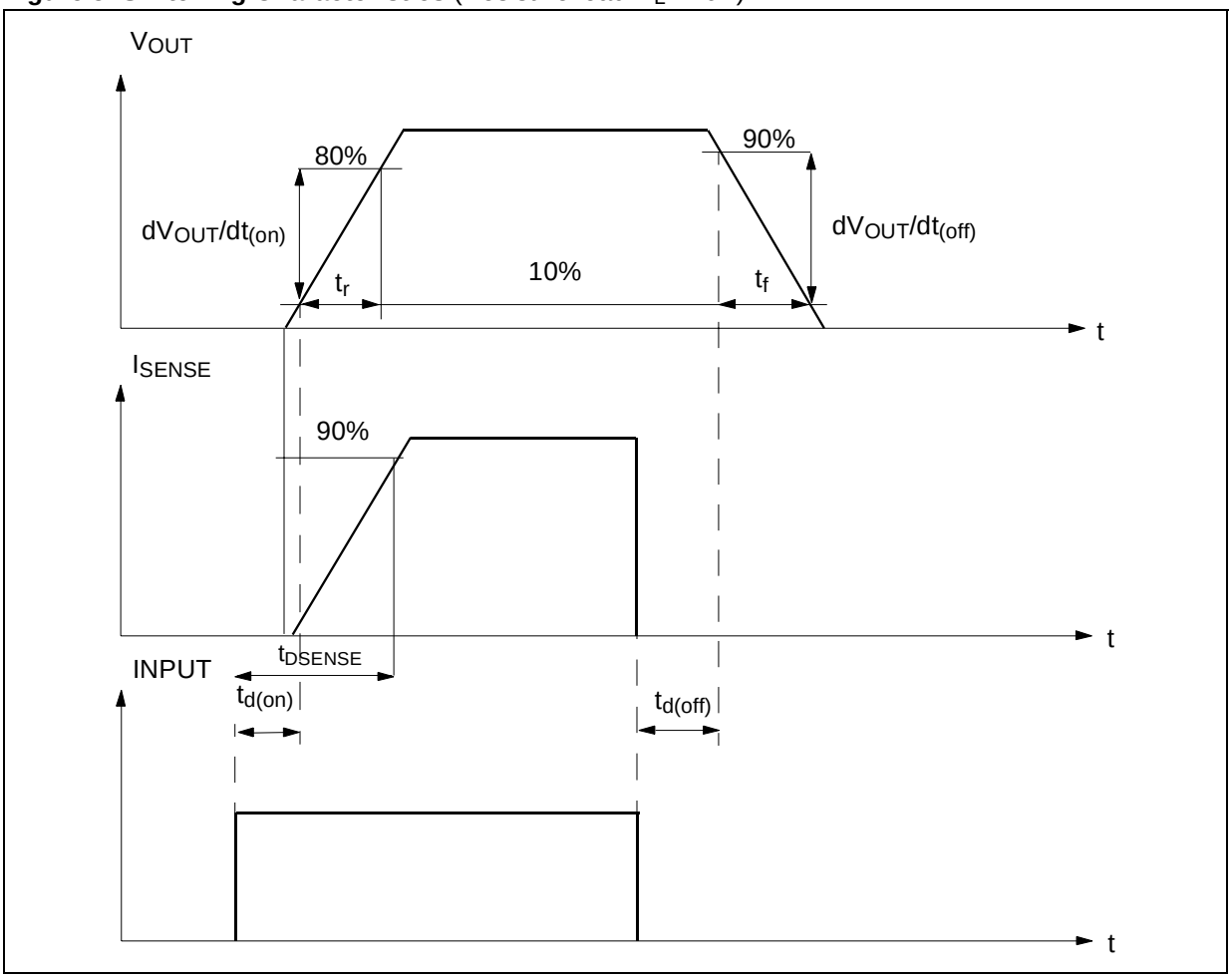


Table 11. Truth Table (per channel)

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms

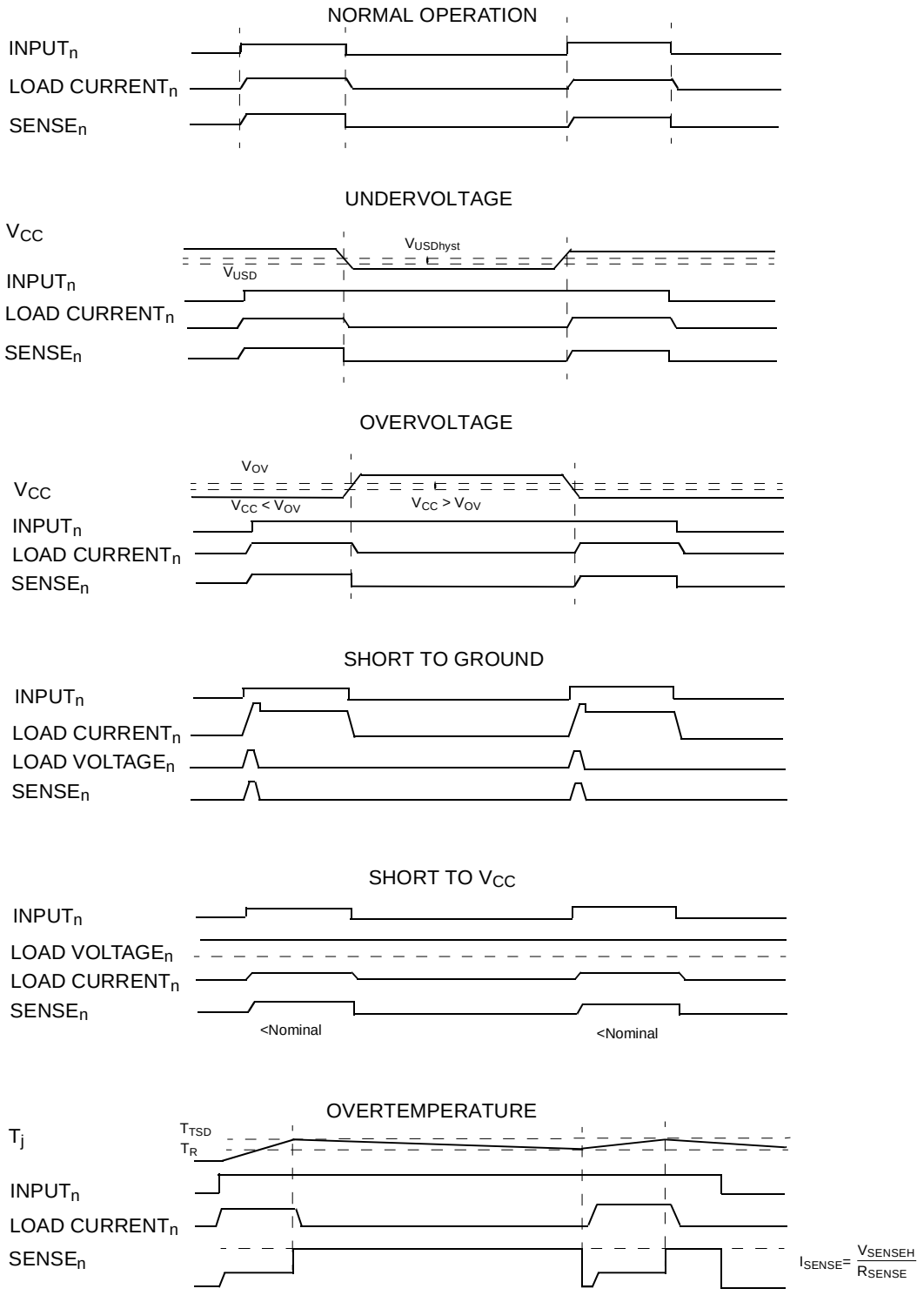
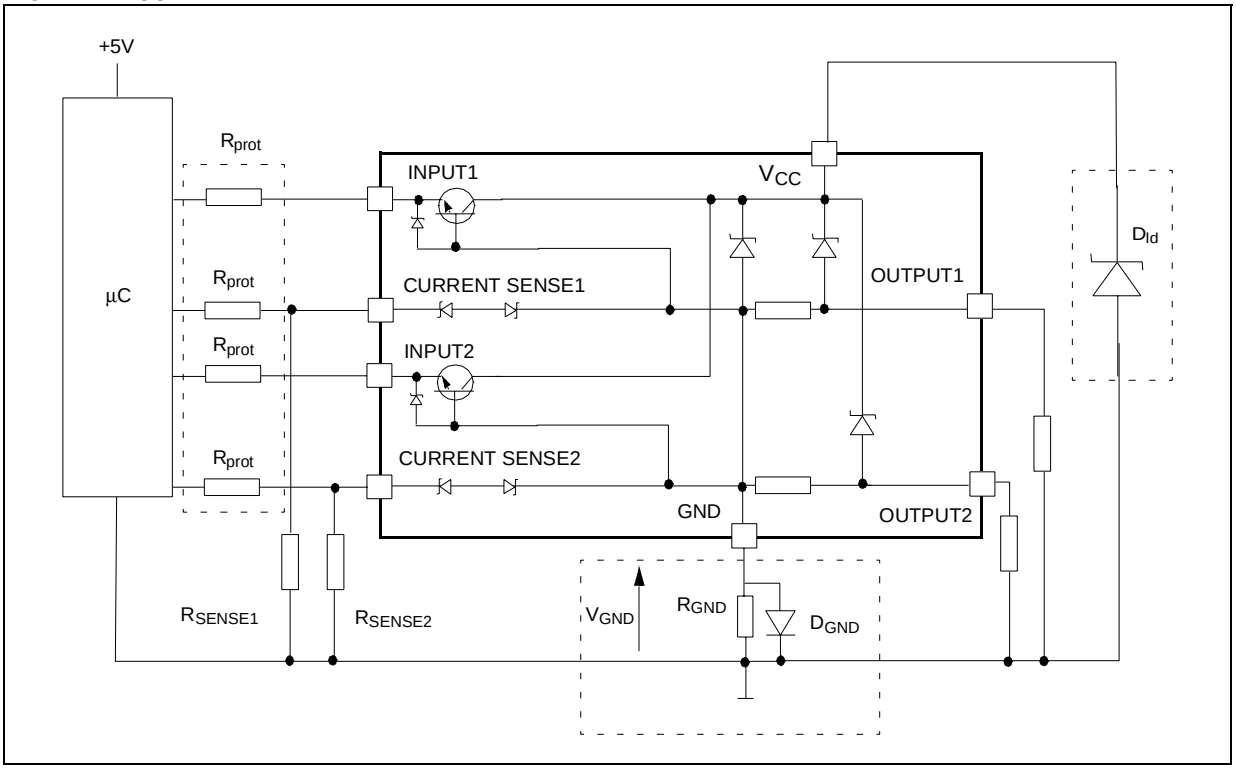


Figure 7. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.
2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (≃600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

LOAD DUMP PROTECTION

D_{Id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

5kΩ ≤ R_{prot} ≤ 65kΩ.

Recommended R_{prot} value is 10kΩ.

Figure 8. I_{OUT}/I_{SENSE} versus I_{OUT}

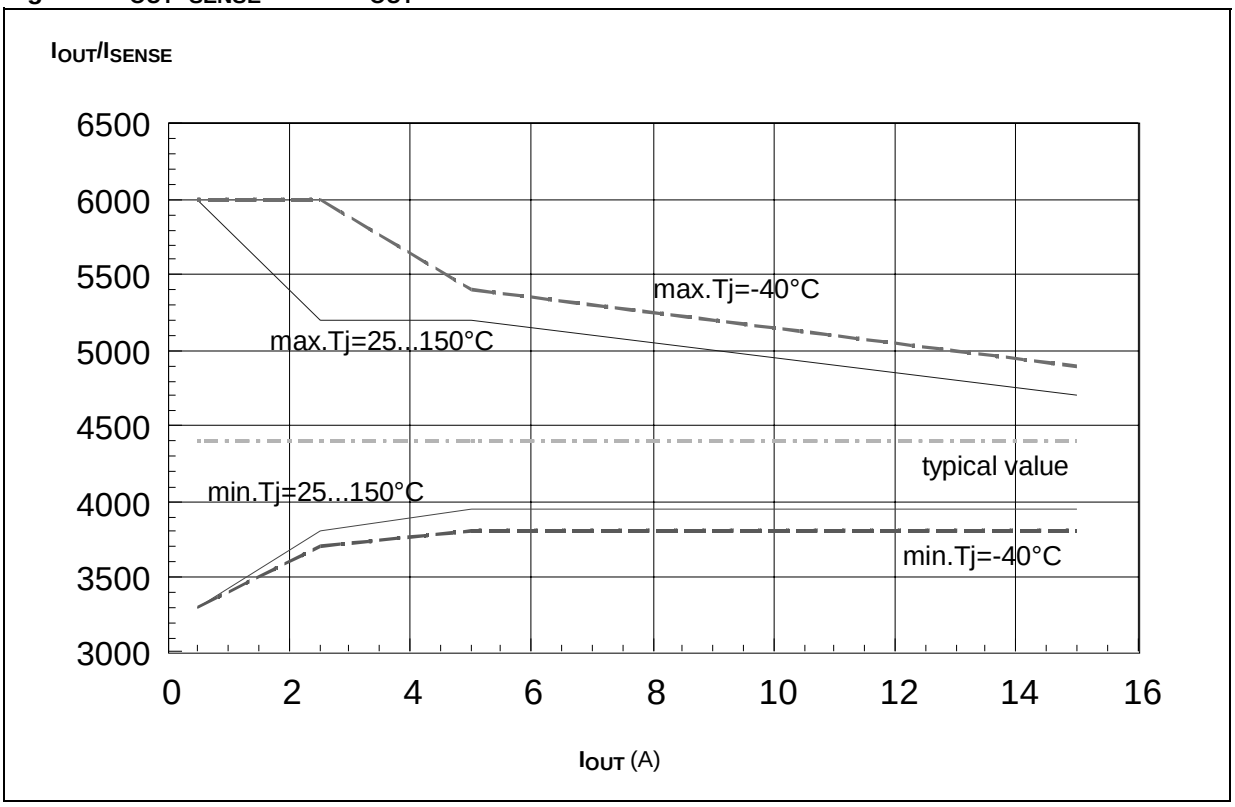


Figure 9. Off State Output Current

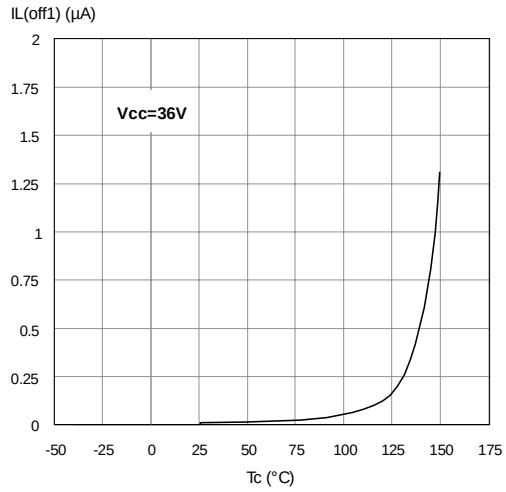


Figure 10. High Level Input Current

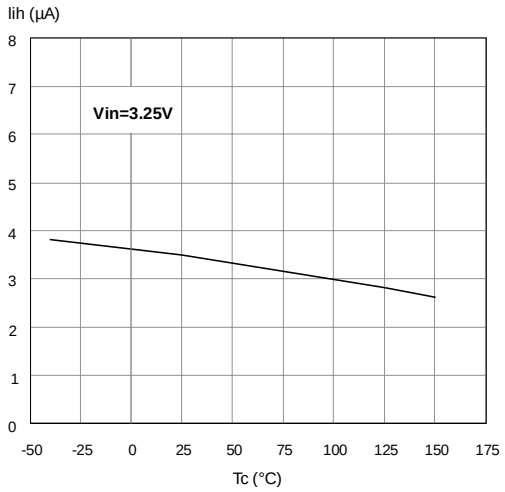


Figure 11. Input Clamp Voltage

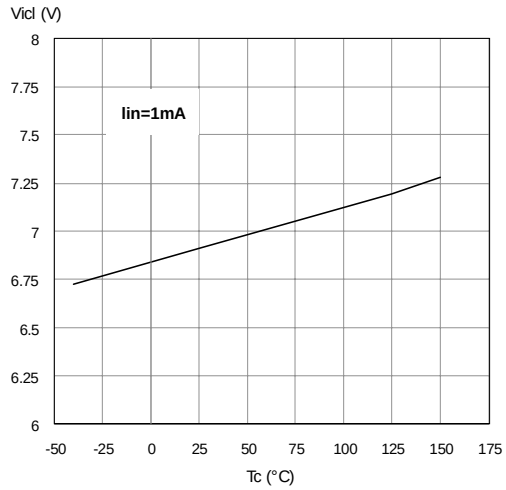


Figure 13. Input High Level

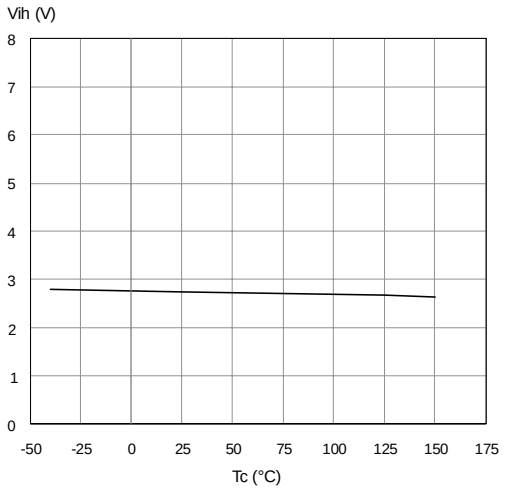


Figure 12. Input Low Level

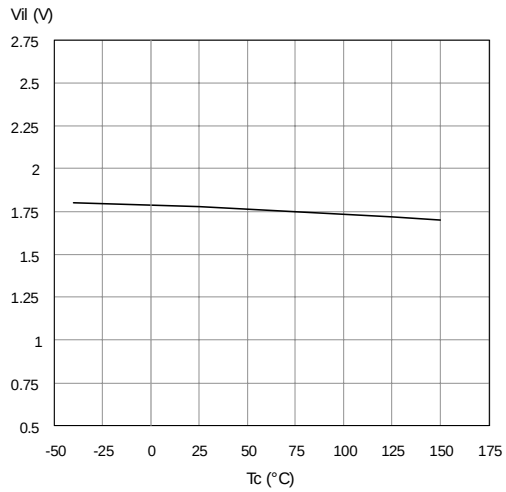


Figure 14. Input Hysteresis Voltage

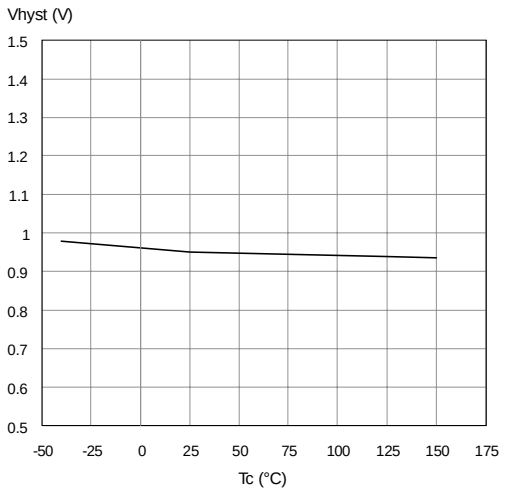


Figure 15. Overvoltage Shutdown

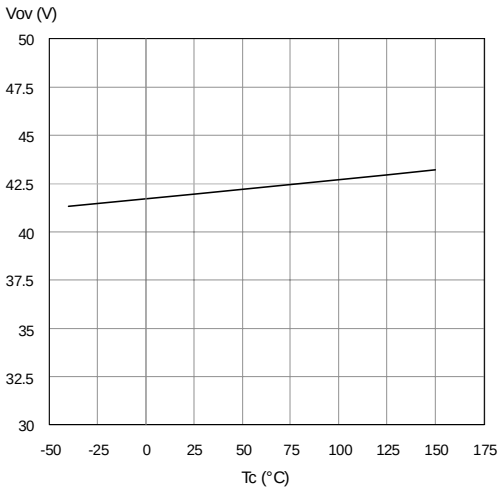


Figure 16. Turn-on Voltage Slope

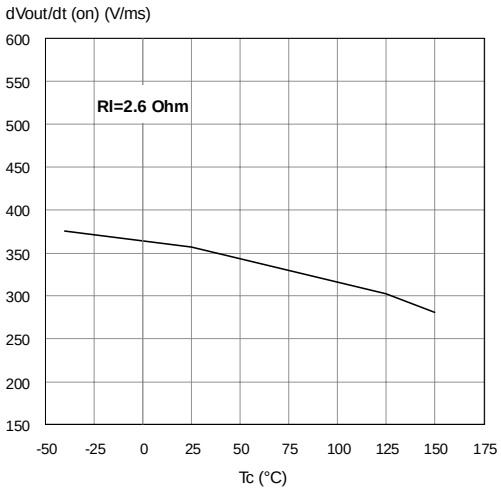


Figure 17. On State Resistance Vs T_{case}

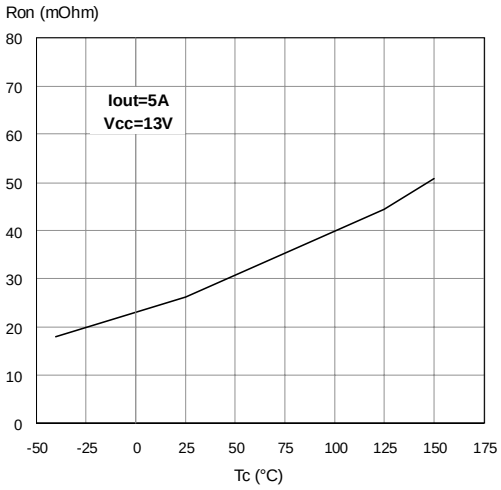


Figure 18. I_{LIM} Vs T_{case}

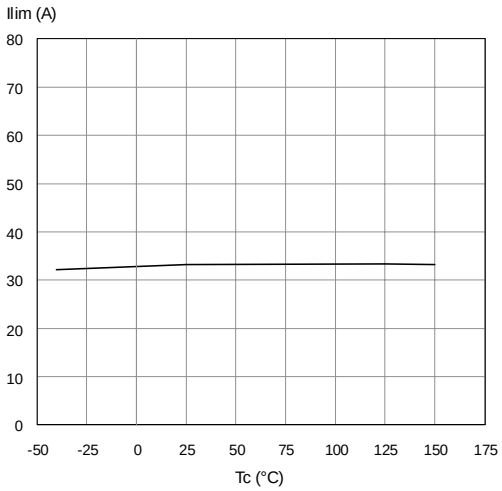


Figure 19. Turn-off Voltage Slope

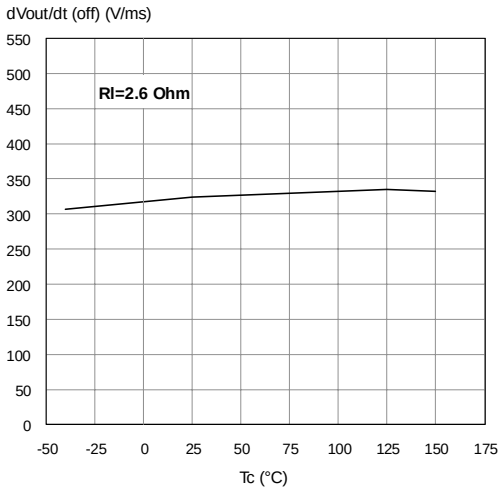
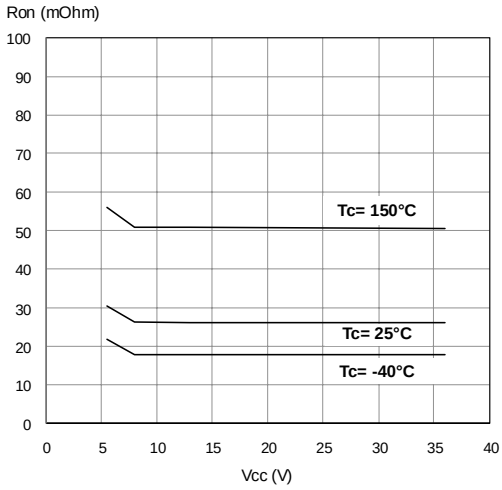
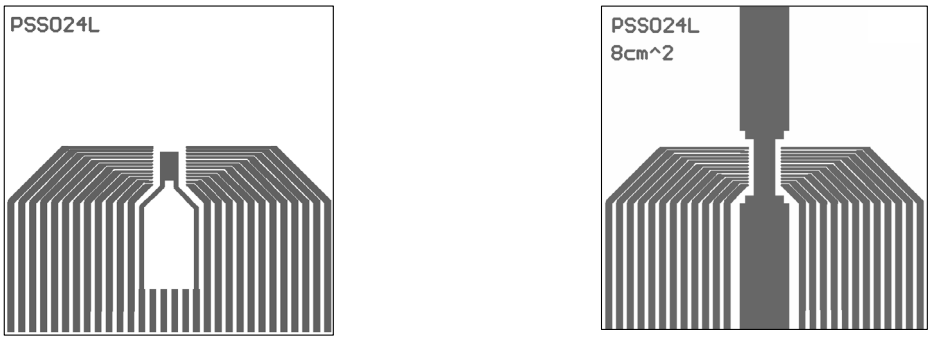


Figure 20. On State Resistance Vs V_{CC}



PowerSSO-24 Thermal Data

Figure 21. PowerSSO-24 PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 78mm x 78mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 8cm^2).

Figure 22. $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

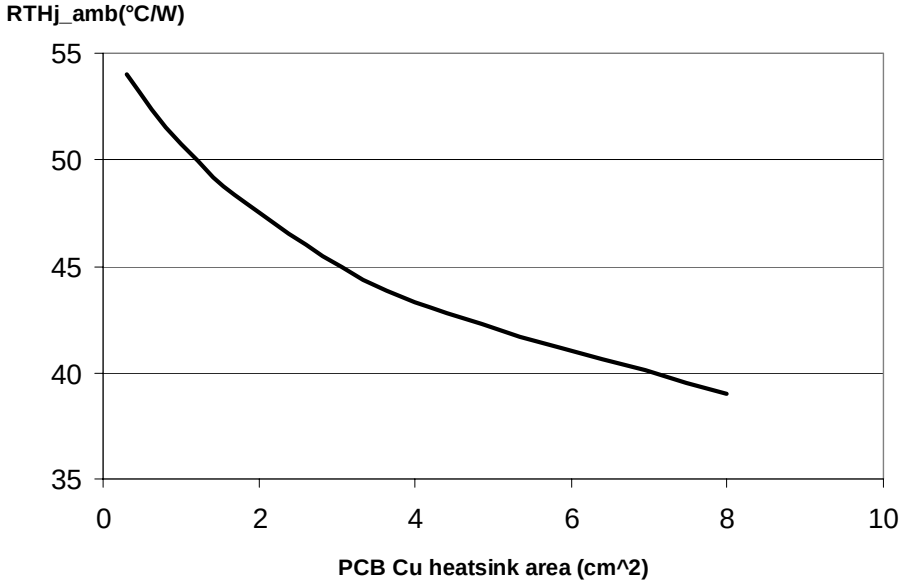
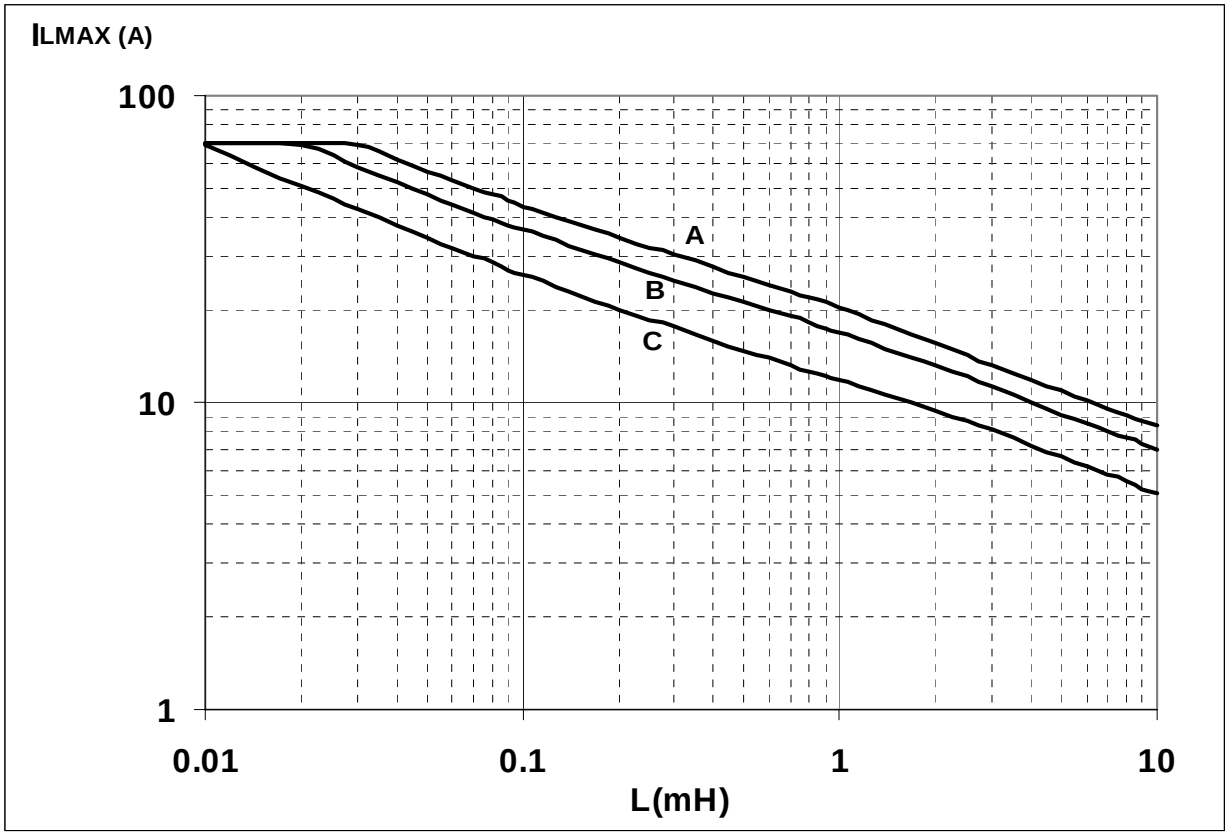


Figure 23. Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

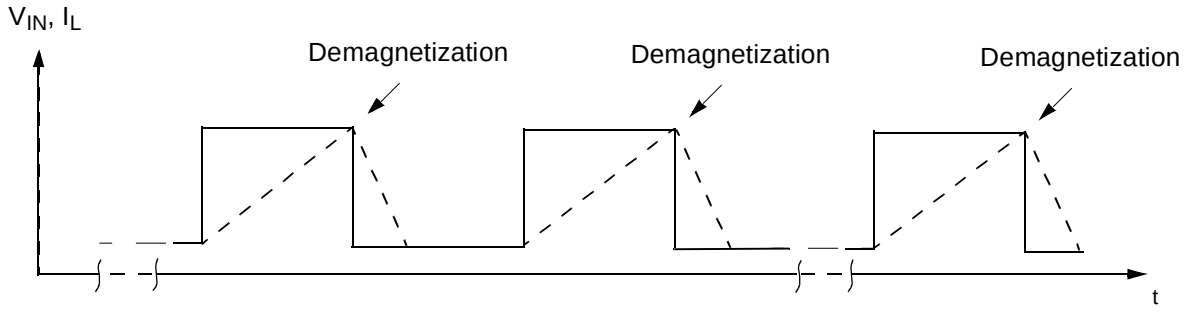


Figure 24. PowerSSO-24 Thermal Impedance Junction Ambient Single Pulse

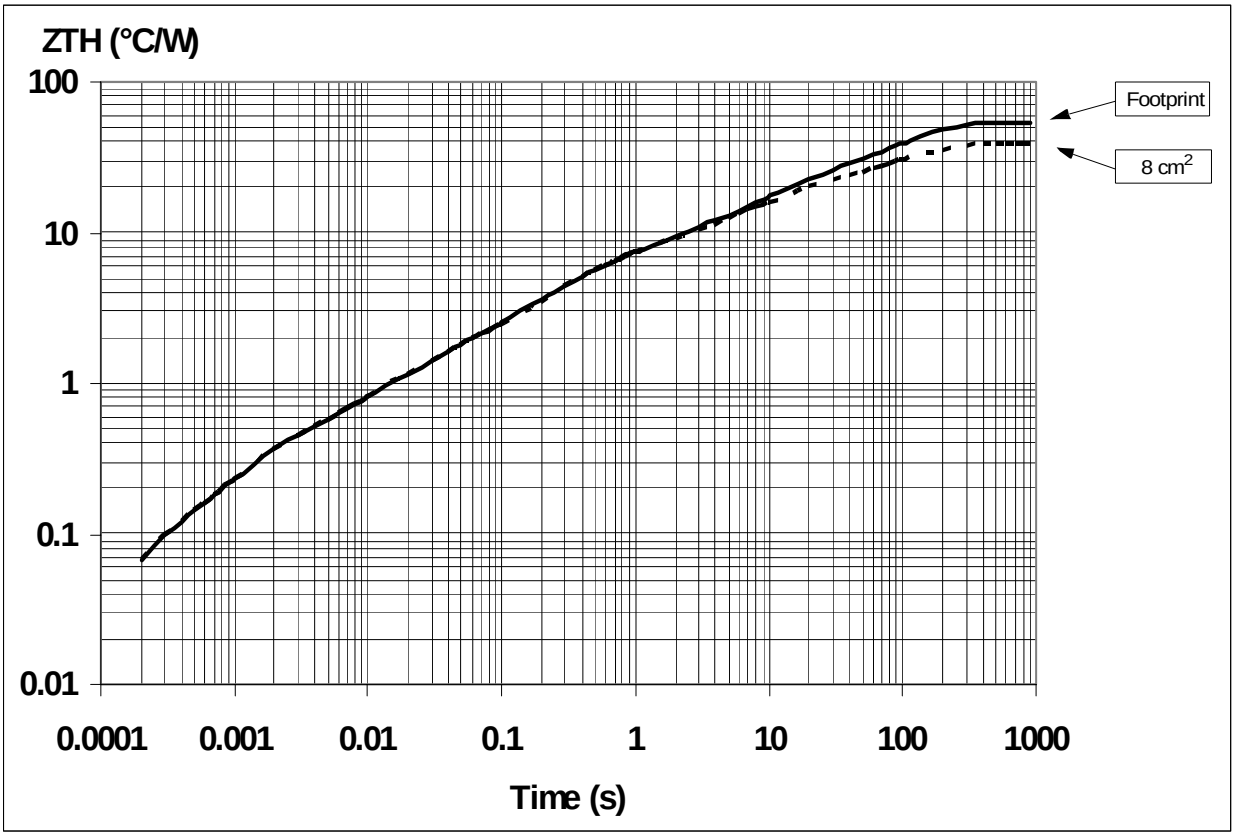
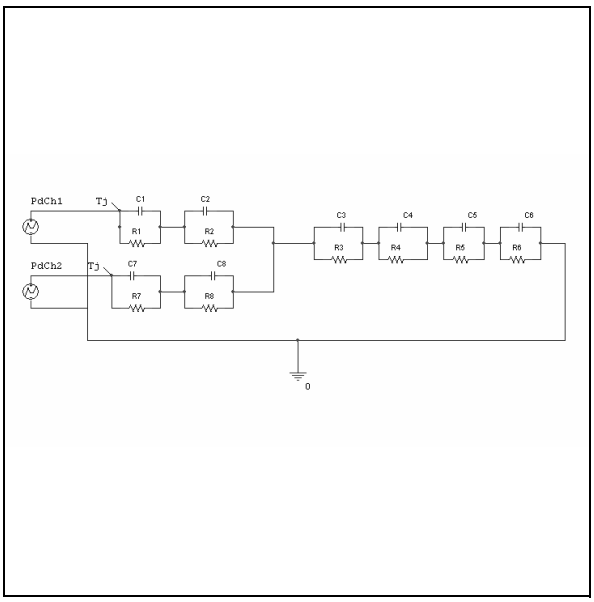


Figure 25. Thermal Fitting Model of a Double Channel HSD in PowerSSO-24



Pulse Calculation Formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 13. Thermal Parameter

Area/island (cm^2)	Footprint	8
R1=R7 (°C/W)	0.05	
R2=R8 (°C/W)	0.3	
R3 (°C/W)	0.9	
R4 (°C/W)	5	
R5 (°C/W)	13.5	
R6 (°C/W)	37	22
C1=C7 (W.s/°C)	0.001	
C2=C8 (W.s/°C)	0.005	
C3 (W.s/°C)	0.025	
C4 (W.s/°C)	0.08	
C5 (W.s/°C)	0.7	
C6 (W.s/°C)	3	5

PACKAGE MECHANICAL

Table 14. PowerSSO-24™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 26. PowerSSO-24™ Package Dimensions

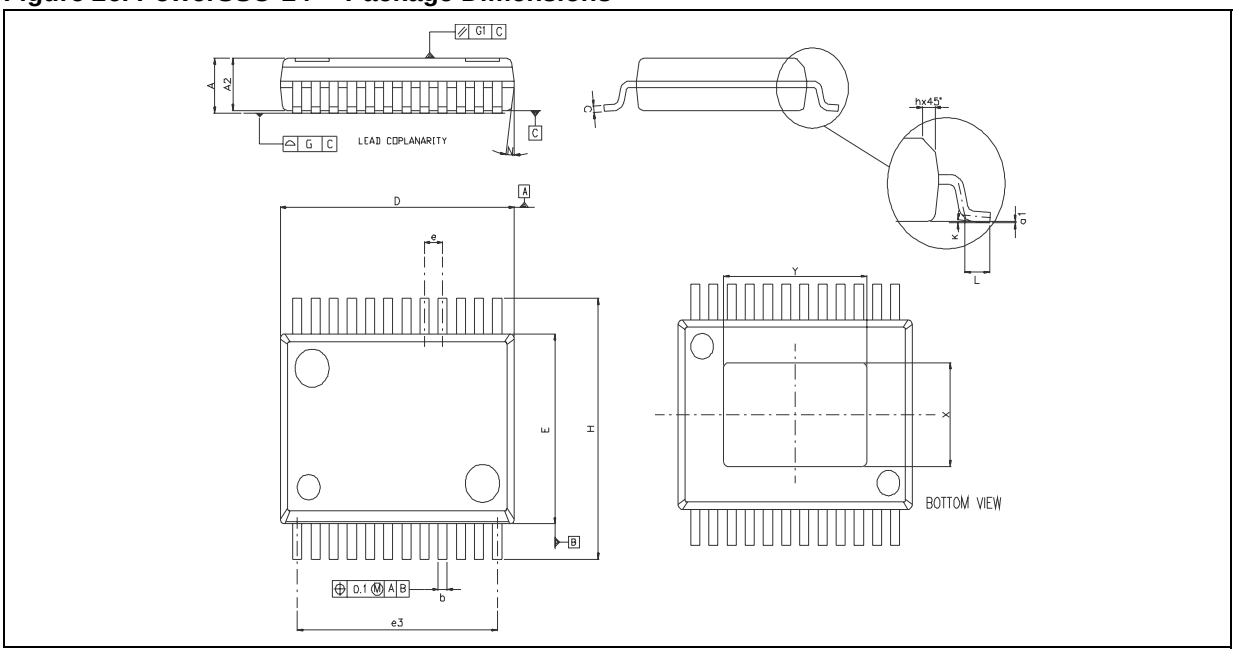
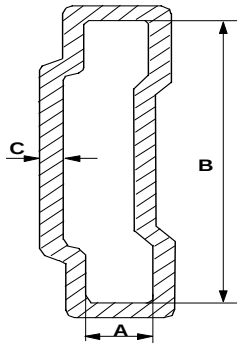


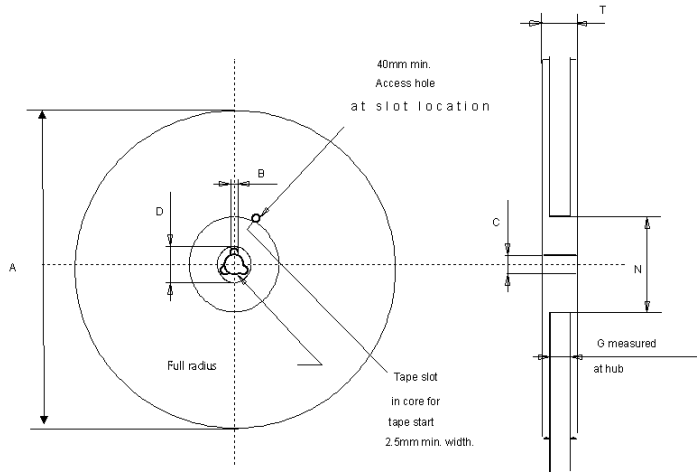
Figure 27. PowerSSO-24 Tube Shipment (No Suffix)



Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 28. Tape And Reel Shipment (Suffix "TR")



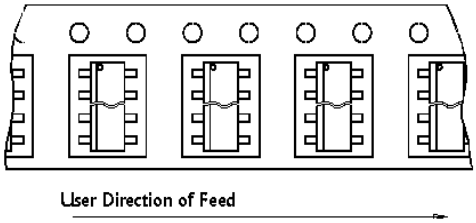
REEL DIMENSIONS

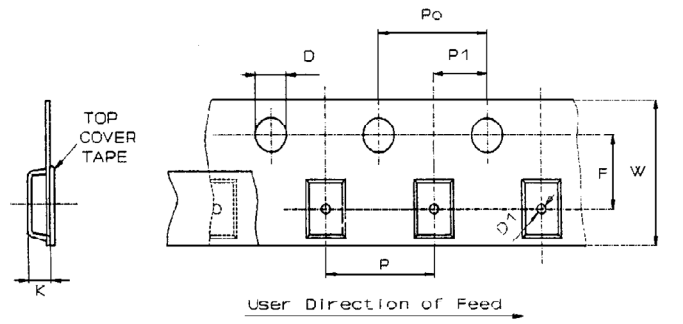
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

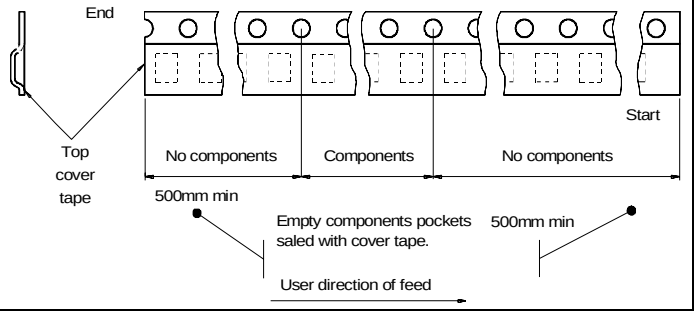
TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2







REVISION HISTORY

Table 15. Revision History

Date	Revision	Description of Changes
Nov. 2004	1	- First Issue.
Dec. 2004	2	- $I_{L(off2)}$ removal.
Mar. 2005	3	- Maximum Switching Energy insertion; - Thermal data insertion; - Maximum turn off current versus load inductance; - Thermal Impedance Junction Ambient Single Pulse curve insertion.
Apr. 2005	4	- Configuration diagram modification - Shipment data insertion
May 2005	5	- Minor changes