



VNW50N04A

"OMNIFET": FULLY AUTOPROTECTED POWER MOSFET

Table 1. General Features

Type	V _{clamp}	R _{DS(on)}	I _{lim}
VNW50N04A	42 V	0.012 Ω	50 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET
- STANDARD TO-247 PACKAGE

DESCRIPTION

The VNW50N04A, is a monolithic device made using STMicroelectronics VIPower™ M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Figure 1. Package

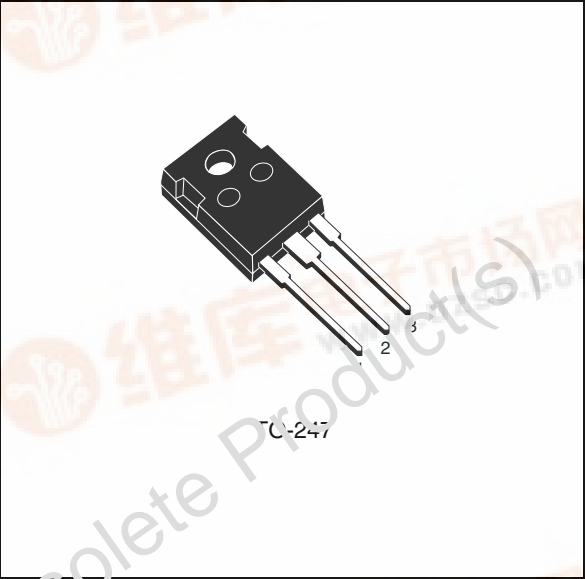


Table 2. Order Codes

Package	Tube	Tape and Reel
TO-247	VNW50N04A	—

Figure 2. Block Diagram

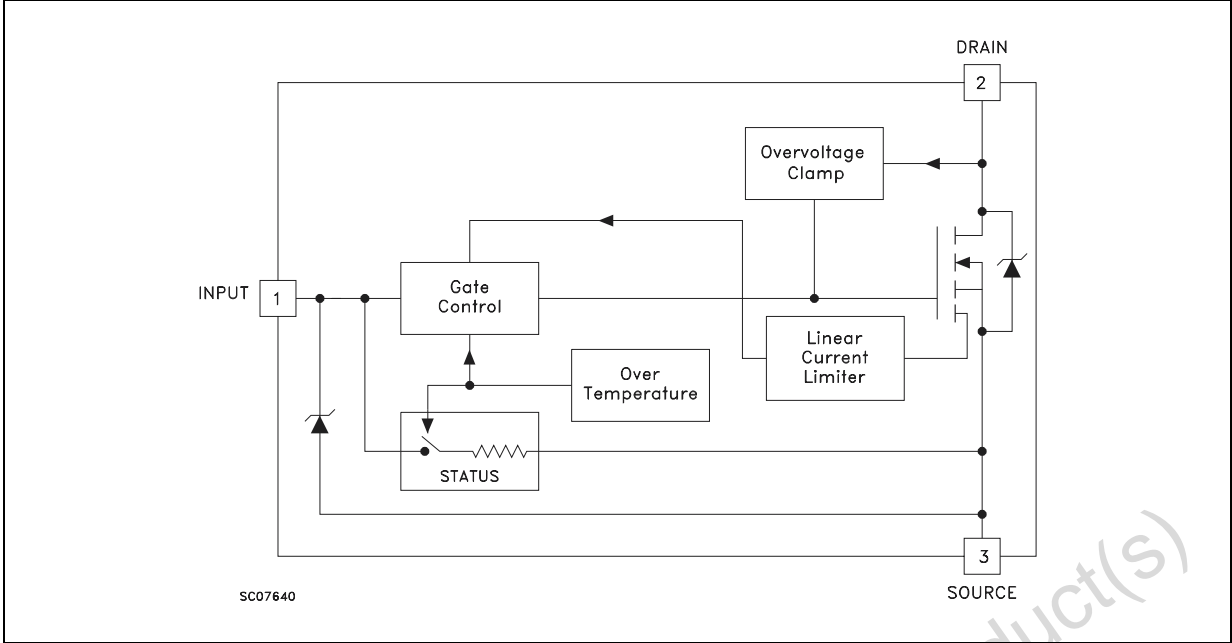


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage ($V_{in} = 0$)	Internally Clamped	V
V_{in}	Input Voltage	18	V
I_D	Drain Current	Internally Limited	A
I_R	Reverse DC Output Current	-100	A
V_{esd}	Electrostatic Discharge ($C = 100$ pF, $R = 1.5$ K Ω)	2000	V
P_{tot}	Total Dissipation at $T_c = 25$ °C	208	W
T_j	Operating Junction Temperature	Internally Limited	°C
T_c	Case Operating Temperature	Internally Limited	°C
T_{stg}	Storage Temperature	-55 to 150	°C

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	0.6	°C/W
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	30	°C/W

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}\text{C}$ unless otherwise specified)**Table 5. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$I_D = 18\text{ A}$; $V_{in} = 0$	36	42	48	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$I_D = 2\text{ mA}$; $V_{in} = 0$	35			V
V_{INCL}	Input-Source Reverse Clamp Voltage	$I_{in} = -1\text{ mA}$	-1		-0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{in} = 0$)	$V_{DS} = 13\text{ V}$; $V_{in} = 0$ $V_{DS} = 25\text{ V}$; $V_{in} = 0$			50 200	μA μA
I_{ISS}	Supply Current from Input Pin	$V_{DS} = 0\text{ V}$; $V_{in} = 10\text{ V}$		250	500	μA

Table 6. On ⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IN(th)}$	Input Threshold Voltage	$V_{DS} = V_{in}$; $I_D + I_{in} = 1\text{ mA}$	0.8		3	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{in} = 10\text{ V}$; $I_D = 25\text{ A}$ $V_{in} = 5\text{ V}$; $I_D = 25\text{ A}$			0.012 0.015	Ω Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%**Table 7. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(2)}$	Forward Transconductance	$V_{DS} = 13\text{ V}$; $I_D = 25\text{ A}$	35	50		S
C_{oss}	Output Capacitance	$V_{DS} = 13\text{ V}$; $f = 1\text{ MHz}$; $V_{in} = 0$		2000	3000	pF

Note: 2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.**Table 8. Switching ⁽³⁾**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$; $I_d = 25\text{ A}$;		100	200	ns
t_r	Rise Time	$V_{gen} = 10\text{ V}$; $R_{gen} = 10\ \Omega$		400	700	ns
$t_{d(off)}$	Turn-off Delay Time	(see Figure 27)		800	1500	ns
t_f	Fall Time			500	900	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$; $I_d = 25\text{ A}$;		1.8	3	μs
t_r	Rise Time	$V_{gen} = 10\text{ V}$; $R_{gen} = 1000\ \Omega$		3	5	μs
$t_{d(off)}$	Turn-off Delay Time	(see Figure 27)		18	25	μs
t_f	Fall Time			10	15	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 15\text{ V}$; $I_D = 25\text{ A}$ $V_{in} = 10\text{ V}$; $R_{gen} = 10\ \Omega$		55		A/ μs
Q_i	Total Input Charge	$V_{DD} = 15\text{ V}$; $I_D = 25\text{ A}$; $V_{in} = 10\text{ V}$		190		nC

Note: 3. Parameters guaranteed by design/characterization.

ELECTRICAL CHARACTERISTICS (cont'd)
Table 9. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(4)}$	Forward On Voltage	$I_{SD} = 25\text{ A}$; $V_{in} = 0$			1.6	V
$t_{rr}^{(5)}$	Reverse Recovery Time	$I_{SD} = 25\text{ A}$; $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$ (see test circuit, Figure 29)		800		ns
$Q_{rr}^{(5)}$	Reverse Recovery Charge			5		μC
$I_{RRM}^{(5)}$	Reverse Recovery Current			15		A

Note: 4. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

5. Parameters guaranteed by design/characterization.

Table 10. Protection

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	$V_{in} = 10\text{ V}$; $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$; $V_{DS} = 13\text{ V}$	35 35	50 50	65 65	A A
$t_{dlim}^{(6)}$	Step Response Current Limit	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		50 130	80 200	μs μs
$T_{jsh}^{(6)}$	Overtemperature Shutdown		150			$^\circ\text{C}$
$T_{jrs}^{(6)}$	Overtemperature Reset		135			$^\circ\text{C}$
$I_{gf}^{(6)}$	Fault Sink Current	$V_{in} = 10\text{ V}$; $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$; $V_{DS} = 13\text{ V}$		50 20		mA mA
$E_{as}^{(6)}$	Single Pulse Avalanche Energy	starting $T_j = 25\text{ }^\circ\text{C}$; $V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V}$; $R_{gen} = 1\text{ K}\Omega$; $L = 10\text{ mH}$	4			J

Note: 6. Parameters guaranteed by design/characterization.

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{iss}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 170 $^\circ\text{C}$. The device is automatically restarted when the chip temperature falls below 155 $^\circ\text{C}$.
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Figure 3. Thermal Impedance

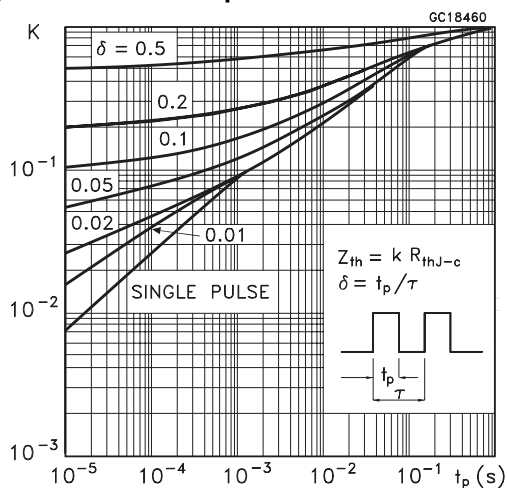


Figure 4. Derating Curve

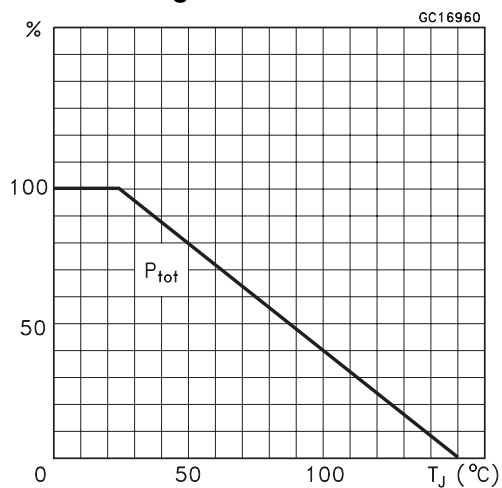


Figure 5. Output Characteristics

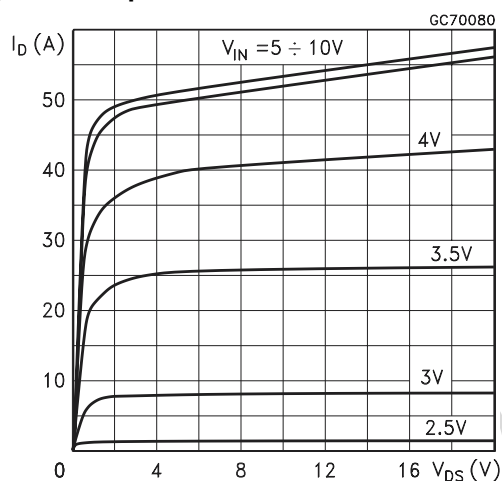


Figure 6. Transconductance

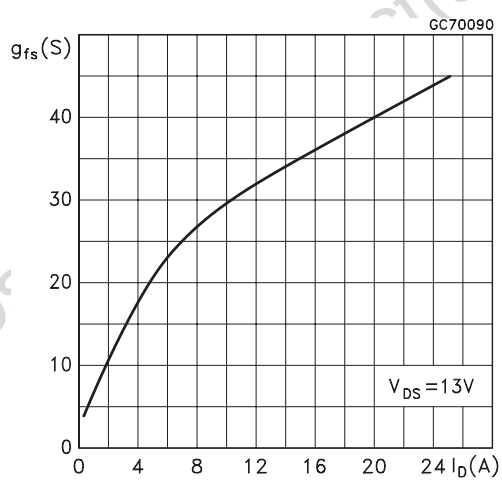


Figure 7. Static Drain-Source On Resistance vs Input Voltage

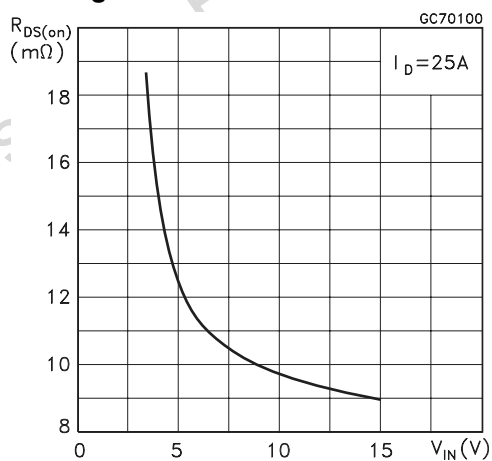


Figure 8. Static Drain-Source On Resistance

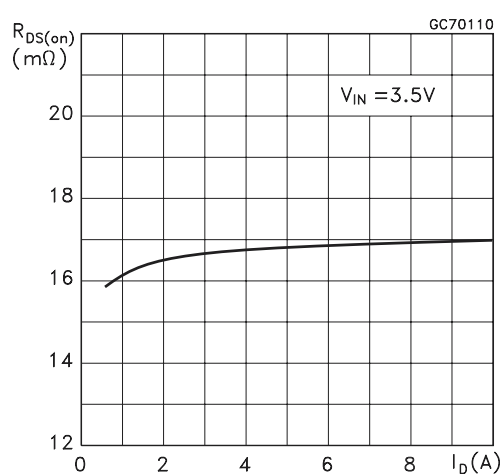


Figure 9. Static Drain-Source On Resistance

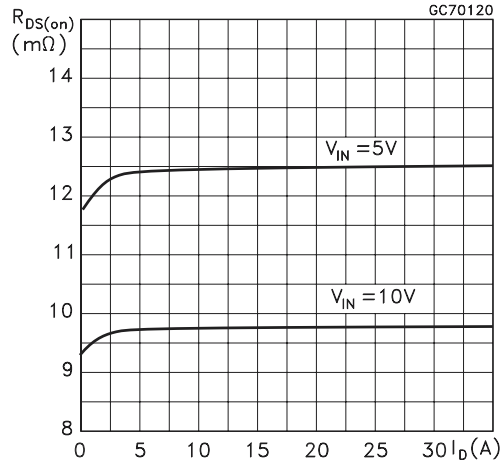


Figure 10. Input Charge vs Input Voltage

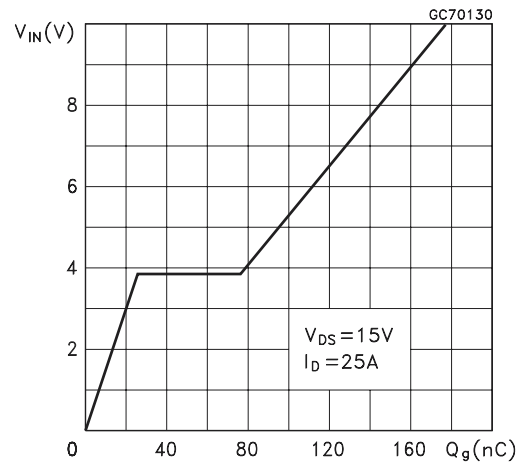


Figure 11. Capacitance Variations

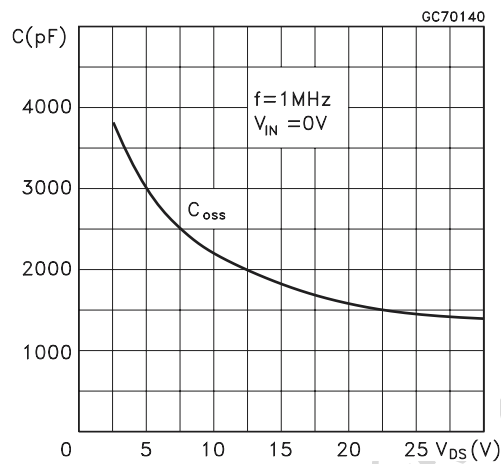


Figure 12. Normalized Input Threshold Voltage vs Temperature

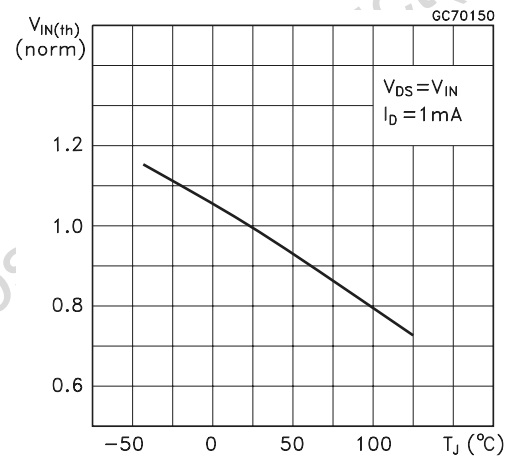


Figure 13. Normalized On Resistance vs Temperature

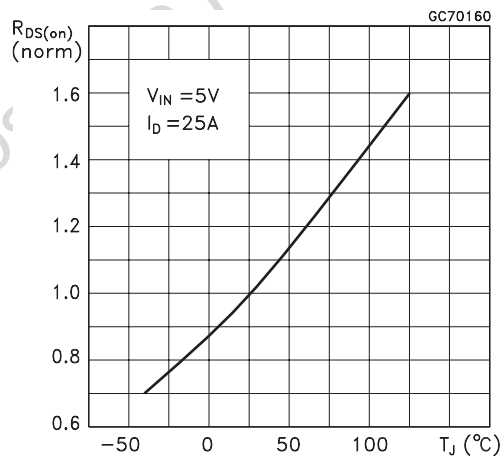


Figure 14. Normalized On Resistance vs Temperature

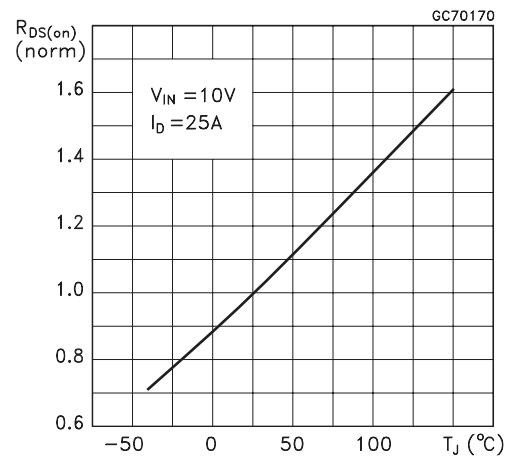


Figure 15. Turn-on Current Slope

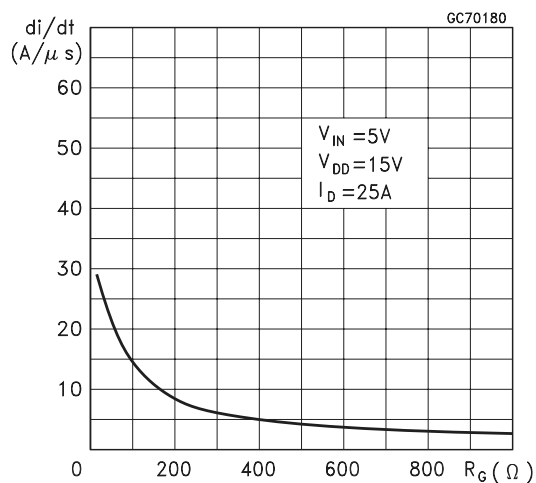


Figure 16. Turn-on Current Slope

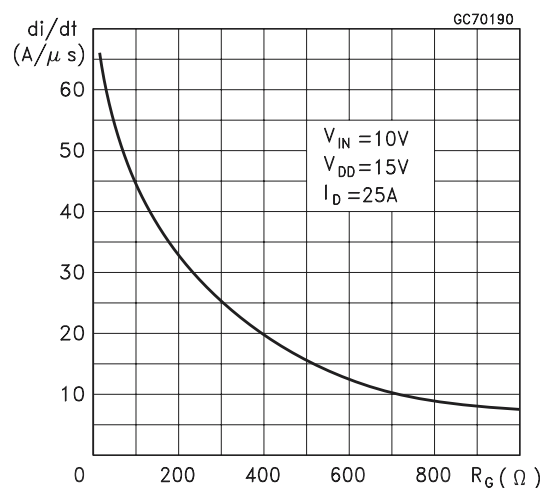


Figure 17. Turn-off Drain-Source Voltage Slope

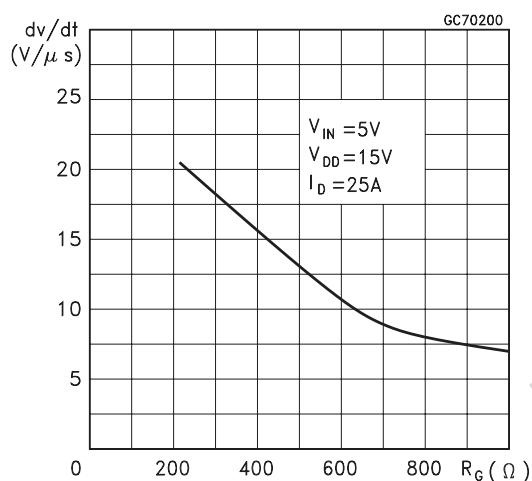


Figure 18. Turn-off Drain-Source Voltage Slope

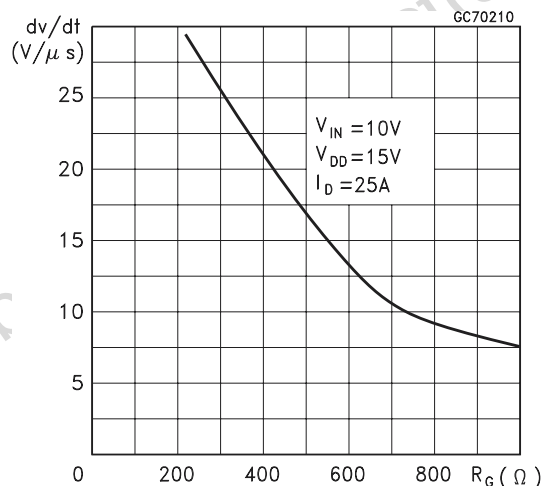


Figure 19. Switching Time Resistive Load

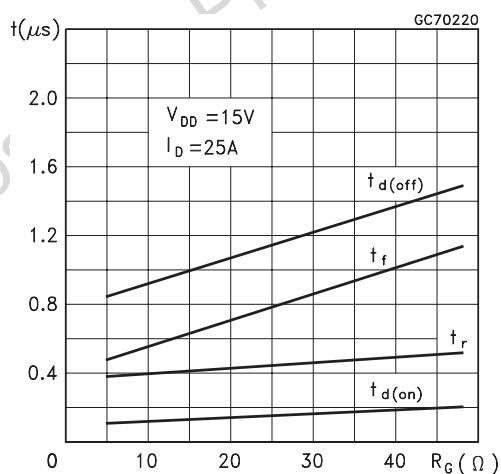


Figure 20. Switching Time Resistive Load

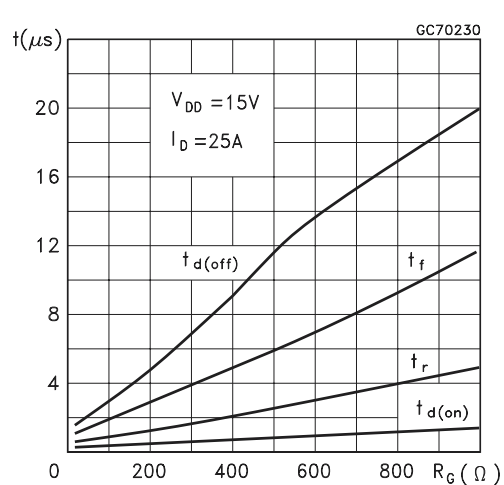


Figure 21. Switching Time Resistive Load

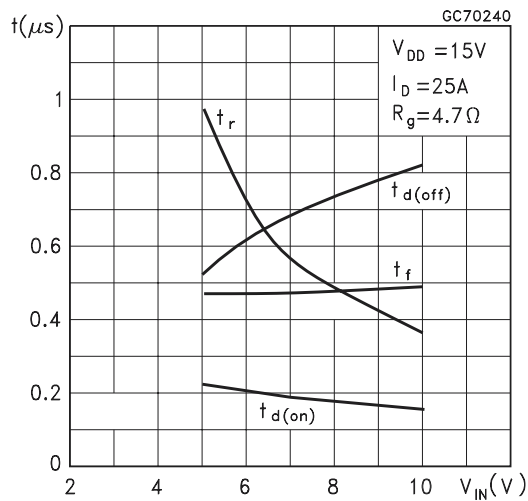


Figure 22. Current Limit vs Junction Temperature

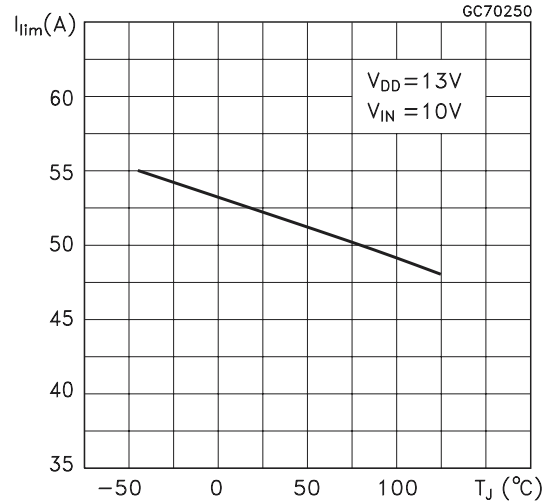


Figure 23. Step Response Current Limit

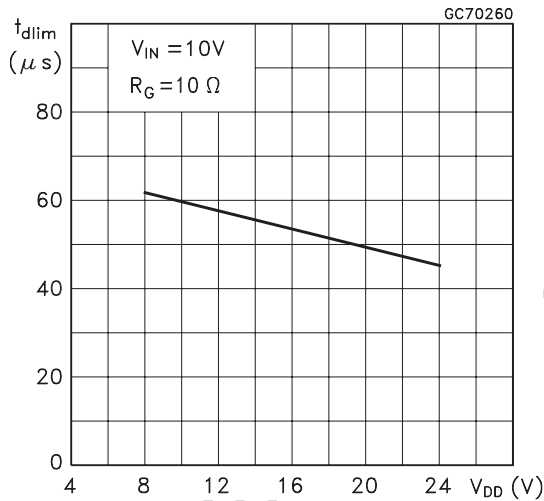


Figure 24. Source Drain Diode Forward Characteristics

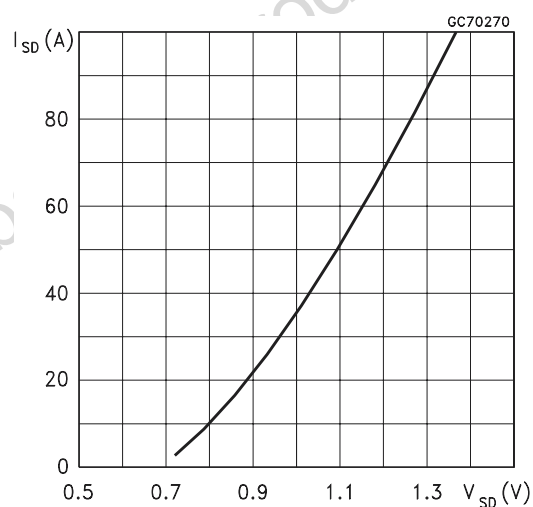


Figure 25. Unclamped Inductive Load Test Circuits

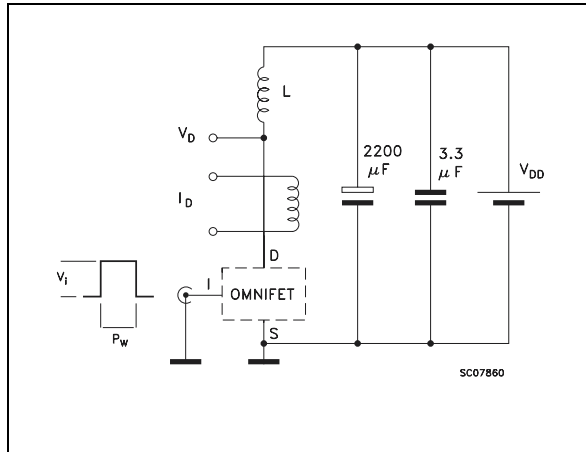


Figure 26. Unclamped Inductive Waveforms

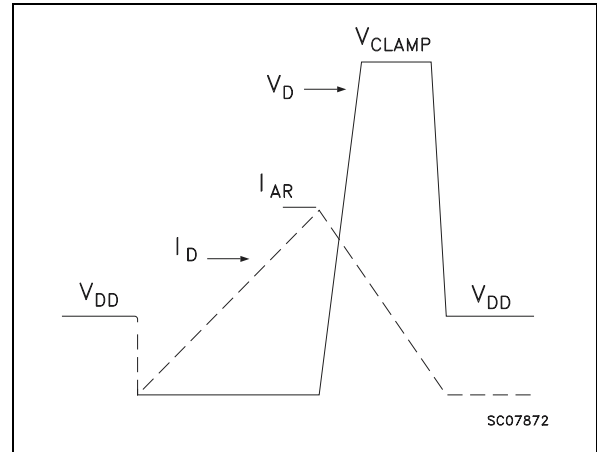


Figure 27. Switching Times Test Circuits For Resistive Load

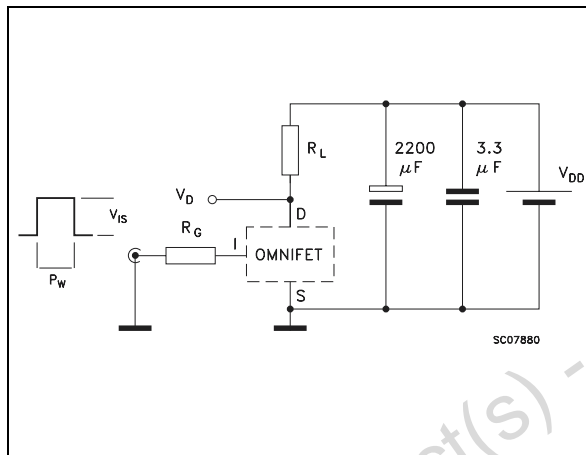


Figure 28. Input Charge Test Circuit

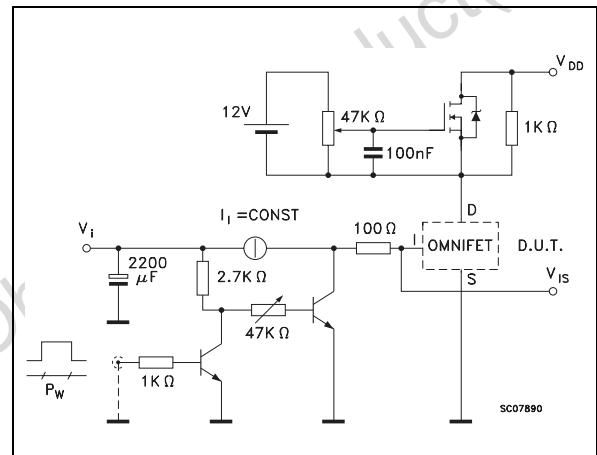


Figure 29. Test Circuit For Inductive Load Switching And Diode Recovery Times

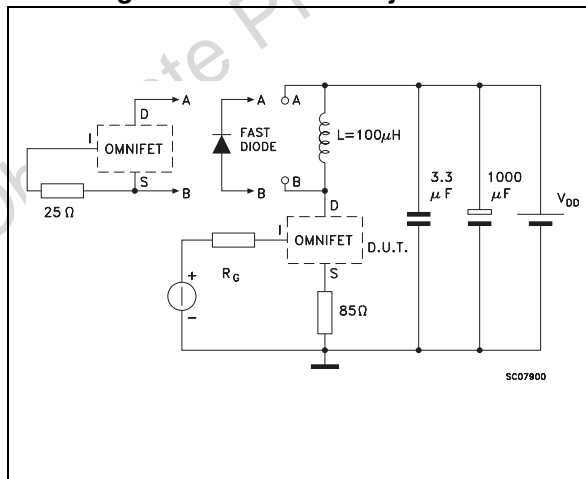
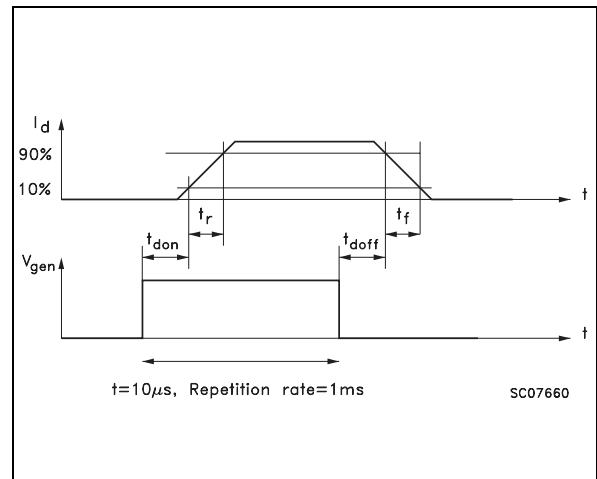


Figure 30. Waveforms

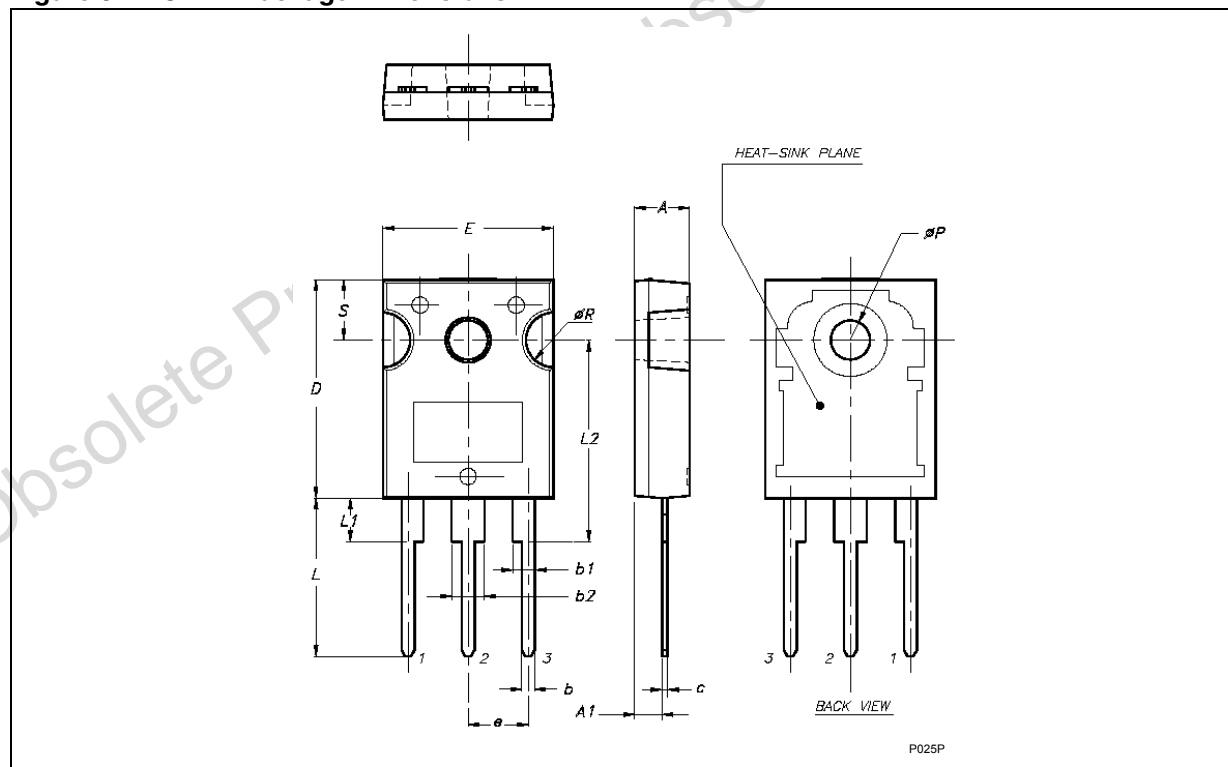


PACKAGE MECHANICAL

Table 11. TO-247 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	
Package Weight	Gr. 4.43		

Figure 31. TO-247 Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY**Table 12. Revision History**

Date	Revision	Description of Changes
February-1998	1	First Issue
18-June-2004	2	Stylesheet update. No content change.

Obsolete Product(s) - Obsolete Product(s)

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