



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	V <sub>GS(th)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package
				TO-92
350V	15Ω	1.8V	0.15A	VN3515L
400V	12Ω	1.8V	0.15A	VN4012L

### Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

### Applications

- Motor controls
- Converters
- Amplifiers
- Telecom Switching
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

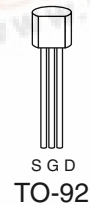
\*Distance of 1.6 mm from case for 10 seconds.

### Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Option



Note: See Package Outline section for dimensions.



## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jc}$ $^\circ\text{C/W}$	$\theta_{ja}$ $^\circ\text{C/W}$	$I_{DR}^*$	$I_{DRM}$
VN3515L (TO-92)	150mA	600mA	1W	125	170	150mA	600mA
VN4012L (TO-92)	160mA	650mA	1W	125	170	160mA	650mA

\*  $I_D$  (continuous) is limited by max rated  $T_j$ .

## Electrical Characteristics (@ $25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	VN3515 350			V	$V_{GS} = 0V, I_D = 100\mu\text{A}$
		VN4012 400				
$V_{GS(th)}$	Gate Threshold Voltage	0.6		1.8	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$I_{GSS}$	Gate Body Leakage			10	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero Gate Voltage Drain Current			1	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = 0.8$ Max Rating
				100		$V_{GS} = 0V, V_{DS} = 0.8$ Max Rating $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	0.15	0.3		A	$V_{DS} = 10V, V_{GS} = 4.5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN3515	9.5	15	$\Omega$	$V_{GS} = 4.5V, I_D = 100\text{mA}$
			17	35		$V_{GS} = 4.5V, I_D = 100\text{mA}, T_A = 125^\circ\text{C}$
		VN4012	9.5	12		$V_{GS} = 4.5V, I_D = 100\text{mA}$
			17	30		$V_{GS} = 4.5V, I_D = 100\text{mA}, T_A = 125^\circ\text{C}$
$G_{FS}$	Forward Transconductance	125	350		$\text{m}\Omega$	$V_{DS} = 15V, I_D = 100\text{mA}$
$C_{ISS}$	Input Capacitance			110	$\text{pF}$	$V_{DS} = 25V, V_{GS} = 0V$ $f = 1\text{MHz}$
$C_{OSS}$	Common Source Output Capacitance			30		
$C_{RSS}$	Reverse Transfer Capacitance			10		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	$V_{DD} = 25V$ $I_D = 100\text{mA}$ $R_{GEN} = 25\Omega$
$t_r$	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			65		
$t_f$	Fall Time			65		
$V_{SD}$	Diode Forward Voltage Drop			1.2	V	$V_{GS} = 0V, I_{SD} = 160\text{mA}$

### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.
- See TN2540 data sheet for characteristic curves.

## Switching Waveforms and Test Circuit

