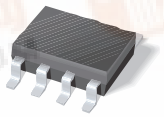


3.3-V CAN TRANSCEIVERS

FEATURES

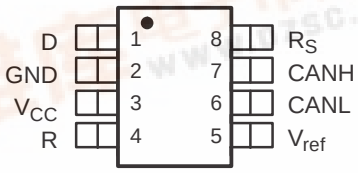
- Operates With a 3.3-V Supply
- Low Power Replacement for the PCA82C250 Footprint
- Bus/Pin ESD Protection Exceeds 16 kV HBM
- High Input Impedance Allows for 120 Nodes on a Bus
- Controlled Driver Output Transition Times for Improved Signal Quality on the SN65HVD230 and SN65HVD231
- Unpowered Node Does Not Disturb the Bus
- Compatible With the Requirements of the ISO 11898 Standard
- Low-Current SN65HVD230 Standby Mode 370 μA Typical
- Low-Current SN65HVD231 Sleep Mode 40 nA Typical
- Designed for Signaling Rates(1) up to 1 Megabit/Second (Mbps)
- Thermal Shutdown Protection
- Open-Circuit Fail-Safe Design
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

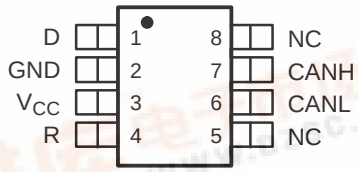
APPLICATIONS

- Motor Control
- Industrial Automation
- Basestation Control and Status
- Robotics
- Automotive
- UPS Control

SN65HVD230D (Marked as VP230)
SN65HVD231D (Marked as VP231)
(TOP VIEW)



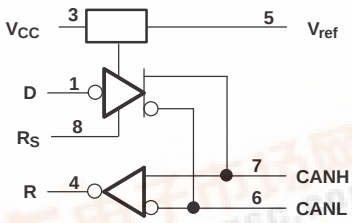
SN65HVD232D (Marked as VP232)
(TOP VIEW)



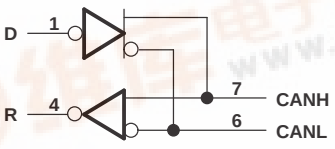
NC – No internal connection

LOGIC DIAGRAM (POSITIVE LOGIC)

SN65HVD230, SN65HVD231
Logic Diagram (Positive Logic)



SN65HVD232
Logic Diagram (Positive Logic)



TMS320Lx240x is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The SN65HVD230, SN65HVD231, and SN65HVD232 controller area network (CAN) transceivers are designed for use with the Texas Instruments TMS320Lx240x™; 3.3-V DSPs with CAN controllers, or with equivalent devices. They are intended for use in applications employing the CAN serial communication physical layer in accordance with the ISO 11898 standard. Each CAN transceiver is designed to provide differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 Mbps.

Designed for operation in especially-harsh environments, these devices feature cross-wire protection, loss-of-ground and overvoltage protection, overtemperature protection, as well as wide common-mode range.

The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications. It operates over a -2-V to 7-V common-mode range on the bus, and it can withstand common-mode transients of ±25 V.

On the SN65HVD230 and SN65HVD231, pin 8 provides three different modes of operation: high-speed, slope control, and low-power modes. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch on and off as fast as possible with no limitation on the rise and fall slopes. The rise and fall slopes can be adjusted by connecting a resistor to ground at pin 8, since the slope is proportional to the pin's output current. This slope control is implemented with external resistor values of 10 kΩ, to achieve a 15-V/µs slew rate, to 100 kΩ, to achieve a 2-V/µs slew rate. See the *Application Information* section of this data sheet.

The circuit of the SN65HVD230 enters a low-current standby mode during which the driver is switched off and the receiver remains active if a high logic level is applied to pin 8. The DSP controller reverses this low-current standby mode when a dominant state (bus differential voltage > 900 mV typical) occurs on the bus.

The unique difference between the SN65HVD230 and the SN65HVD231 is that both the driver and the receiver are switched off in the SN65HVD231 when a high logic level is applied to pin 8 and remain in this sleep mode until the circuit is reactivated by a low logic level on pin 8.

The V_{ref} pin 5 on the SN65HVD230 and SN65HVD231 is available as a $V_{CC}/2$ voltage reference.

The SN65HVD232 is a basic CAN transceiver with no added options; pins 5 and 8 are NC, no connection.

AVAILABLE OPTIONS(1)

PART NUMBER	LOW POWER MODE	INTEGRATED SLOPE CONTROL	V_{ref} PIN	T_A	MARKED AS:
SN65HVD230	Standby mode	Yes	Yes	40°C to 85°C	VP230
SN65HVD231	Sleep mode	Yes	Yes		VP231
SN65HVD232	No standby or sleep mode	No	No		VP232

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

FUNCTION TABLES

DRIVER (SN65HVD230, SN65HVD231)(1)				
INPUT D	R_S	OUTPUTS		BUS STATE
		CANH	CANL	
L	$V_{(Rs)}$ < 1.2 V	H	L	Dominant
H		Z	Z	Recessive
Open	X	Z	Z	Recessive
X	$V_{(Rs)}$ > 0.75 V_{CC}	Z	Z	Recessive

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

DRIVER (SN65HVD232)(1)			
INPUT D	OUTPUTS		BUS STATE
	CANH	CANL	
L	H	L	Dominant
H	Z	Z	Recessive
Open	Z	Z	Recessive

(1) H = high level; L = low level; Z = high impedance

RECEIVER (SN65HVD230)(1)		
DIFFERENTIAL INPUTS	R_S	OUTPUT R
$V_{ID} \geq 0.9$ V	X	L
0.5 V < V_{ID} < 0.9 V	X	?
$V_{ID} \leq 0.5$ V	X	H
Open	X	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

RECEIVER (SN65HVD231)(1)		
DIFFERENTIAL INPUTS	R_S	OUTPUT R
$V_{ID} \geq 0.9$ V	$V_{(Rs)} < 1.2$ V	L
0.5 V < V_{ID} < 0.9 V		?
$V_{ID} \leq 0.5$ V		H
X	$V_{(Rs)} > 0.75\ V_{CC}$	H
X	1.2 V < $V_{(Rs)}$ < 0.75 V_{CC}	?
Open	X	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

RECEIVER (SN65HVD232)(1)	
DIFFERENTIAL INPUTS	OUTPUT R
$V_{ID} \geq 0.9$ V	L
0.5 V < V_{ID} < 0.9 V	?
$V_{ID} \leq 0.5$ V	H
Open	H

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate

TRANSCEIVER MODES (SN65HVD230, SN65HVD231)	
$V_{(Rs)}$	OPERATING MODE
$V_{(Rs)} > 0.75\ V_{CC}$	Standby
10 kΩ to 100 kΩ to ground	Slope control
$V_{(Rs)} < 1$ V	High speed (no slope control)

TERMINAL FUNCTIONS

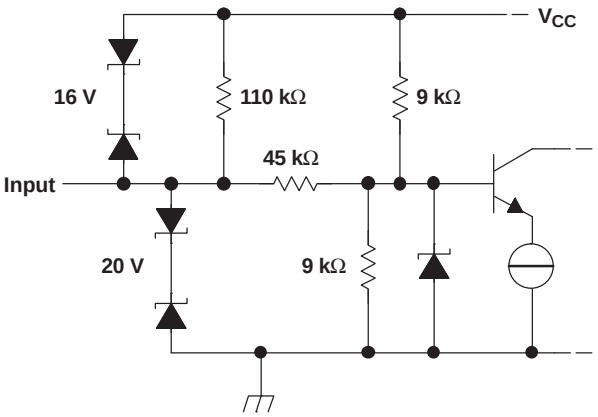
TERMINAL		DESCRIPTION
NAME	NO.	
SN65HVD230, SN65HVD231		
CANL	6	Low bus output
CANH	7	High bus output
D	1	Driver input
GND	2	Ground
R	4	Receiver output

TERMINAL FUNCTIONS (continued)

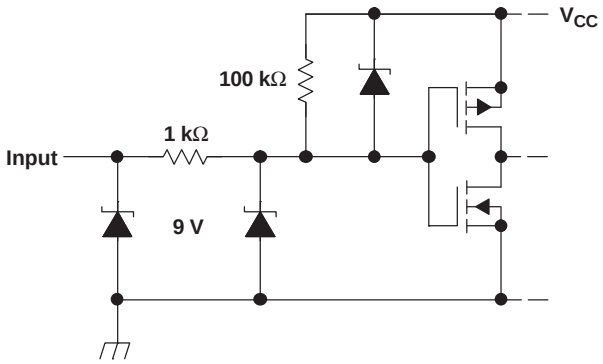
TERMINAL		DESCRIPTION
NAME	NO.	
R_S	8	Standby/slope control
V_{CC}	3	Supply voltage
V_{ref}	5	Reference output
SN65HVD232		
CANL	6	Low bus output
CANH	7	High bus output
D	1	Driver input
GND	2	Ground
NC	5, 8	No connection
R	4	Receiver output
V_{CC}	3	Supply voltage

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

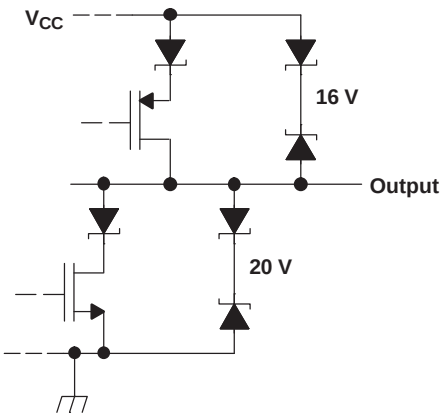
CANH and CANL Inputs



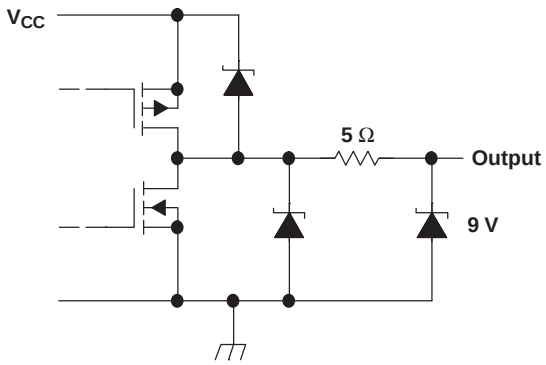
D Input



CANH and CANL Outputs



R Output



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

			UNIT
Supply voltage range, V_{CC}			-0.3 V to 6 V
Voltage range at any bus terminal (CANH or CANL)			-4 V to 16 V
Voltage input range, transient pulse, CANH and CANL, through 100 Ω (see Figure 7)			-25 V to 25 V
Input voltage range, V_I (D or R)			-0.5 V to V_{CC} + 0.5 V
Receiver output current, I_O			±11 mA
Electrostatic discharge	Human body model(3)	CANH, CANL and GND	16 kV
		All Pins	4 kV
	Charged-device model(4)	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods amy affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		3.6	V
Voltage at any bus terminal (common mode) V_{IC}		-2(1)		7	V
Voltage at any bus terminal (separately) V_I		-2.5		7.5	V
High-level input voltage, V_{IH}	D, R	2			V
Low-level input voltage, V_{IL}	D, R			0.8	V
Differential input voltage, V_{ID} (see Figure 5)		-6		6	V
Input voltage, $V_{(Rs)}$		0		V_{CC}	V
Input voltage for standby or sleep, $V_{(Rs)}$		0.75 V_{CC}		V_{CC}	V
Wave-shaping resistance, Rs		0		100	kΩ
High-level output current, I_{OH}	Driver	-40			mA
	Receiver	-8			
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Operating free-air temperature, T_A		-40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER				TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	Bus output voltage	Dominant		V_I = 0 V, See Figure 1 and Figure 3	CANH	2.45		V_{CC}	V
					CANL	0.5		1.25	
V_{OL}		Recessive		V_I = 3 V, See Figure 1 and Figure 3	CANH		2.3		
					CANL		2.3		
$V_{OD(D)}$	Differential output voltage	Dominant		V_I = 0 V, See Figure 1		1.5	2	3	V
				V_I = 0 V, See Figure 2		1.2	2	3	
$V_{OD(R)}$		Recessive		V_I = 3 V, See Figure 1		-120	0	12	mV
				V_I = 3 V, No load		-0.5	-0.2	0.05	V
I_{IH}	High-level input current			V_I = 2 V		-30			µA
I_{IL}	Low-level input current			V_I = 0.8 V		-30			µA
I_{OS}	Short-circuit output current			V_{CANH} = -2 V		-250		250	mA
				V_{CANL} = 7 V		-250		250	
C_o	Output capacitance			See receiver					
I_{CC}	Supply current	Standby	SN65HVD230	$V_{(Rs)}$ = V_{CC}			370	600	µA
		Sleep	SN65HVD231	$V_{(Rs)}$ = V_{CC}, D at V_{CC}			0.04	1	
		All devices	Dominant	V_I = 0 V, No load	Dominant		10	17	mA
			Recessive	V_I = V_{CC}, No load	Recessive		10	17	

(1) All typical values are at 25°C and with a 3.3-V supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SN65HVD230 AND SN65HVD231							
t_{PLH}	Propagation delay time, low-to-high-level output	$V_{(Rs)}$ = 0 V	C_L = 50 pF, See Figure 4		35	85	ns
		R_S with 10 kΩ to ground			70	125	
		R_S with 100 kΩ to ground			500	870	
t_{PHL}	Propagation delay time, high-to-low-level output	$V_{(Rs)}$ = 0 V			70	120	ns
		R_S with 10 kΩ to ground			130	180	
		R_S with 100 kΩ to ground			870	1200	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	$V_{(Rs)}$ = 0 V			35		ns
		R_S with 10 kΩ to ground			60		
		R_S with 100 kΩ to ground			370		
t_r	Differential output signal rise time	$V_{(Rs)}$ = 0 V		25	50	100	ns
t_f	Differential output signal fall time			40	55	80	ns
t_r	Differential output signal rise time	R_S with 10 kΩ to ground		80	120	160	ns
t_f	Differential output signal fall time			80	125	150	ns
t_r	Differential output signal rise time	R_S with 100 kΩ to ground		600	800	1200	ns
t_f	Differential output signal fall time			600	825	1000	ns
SN65HVD232							
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 50 pF, See Figure 4		35	85	ns
t_{PHL}	Propagation delay time, high-to-low-level output				70	120	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				35		
t_r	Differential output signal rise time			25	50	100	
t_f	Differential output signal fall time			40	55	80	

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Table 1			750	900	mV
V_{IT-}	Negative-going input threshold voltage			500	650		mV
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				100		
V_{OH}	High-level output voltage	-6 V ≤ V_{ID} ≤ 500 mV, I_O = -8 mA, See Figure 5		2.4			V
V_{OL}	Low-level output voltage	900 mV ≤ V_{ID} ≤ 6 V, I_O = 8 mA, See Figure 5				0.4	
I_I	Bus input current	V_{IH} = 7 V	Other input at 0 V, D = 3 V	100		250	µA
		V_{IH} = 7 V, V_{CC} = 0 V		100		350	
		V_{IH} = -2 V		-200		-30	µA
		V_{IH} = -2 V, V_{CC} = 0 V		-100		-20	
C_i	CANH, CANL input capacitance	Pin-to-ground, V_I = 0.4 sin(4E6πt) + 0.5 V	$V_{(D)}$ = 3 V,		32		pF
C_{diff}	Differential input capacitance	Pin-to-pin, V_I = 0.4 sin(4E6πt) + 0.5 V	$V_{(D)}$ = 3 V,		16		pF
R_{diff}	Differential input resistance	Pin-to-pin, $V_{(D)}$ = 3 V		40	70	100	kΩ
R_I	CANH, CANL input resistance			20	35	50	kΩ
I_{CC}	Supply current	See driver					

(1) All typical values are at 25°C and with a 3.3-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6		35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				10	ns
t_r	Output signal rise time	See Figure 6		1.5		ns
t_f	Output signal fall time			1.5		ns

DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(LOOP1)}$	Total loop delay, driver input to receiver output, recessive to dominant	$V_{(Rs)}$ = 0 V,	See Figure 9		70	115	ns
		R_S with 10 kΩ to ground,	See Figure 9		105	175	
		R_S with 100 kΩ to ground,	See Figure 9		535	920	
$t_{(LOOP2)}$	Total loop delay, driver input to receiver output, dominant to recessive	$V_{(Rs)}$ = 0 V,	See Figure 9		100	135	ns
		R_S with 10 kΩ to ground,	See Figure 9		155	185	
		R_S with 100 kΩ to ground,	See Figure 9		830	990	

DEVICE CONTROL-PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{(WAKE)}$	SN65HVD230 wake-up time from standby mode with R_S	See Figure 8		0.55	1.5	µs
	SN65HVD231 wake-up time from sleep mode with R_S			3	5	µs

(1) All typical values are at 25°C and with a 3.3-V supply.

DEVICE CONTROL-PIN CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{ref}	Reference output voltage	-5 µA < $I_{(Vref)}$ < 5 µA	0.45 V_{CC}		0.55 V_{CC}	V
		-50 µA < $I_{(Vref)}$ < 50 µA	0.4 V_{CC}		0.6 V_{CC}	
$I_{(Rs)}$	Input current for high-speed	$V_{(Rs)}$ < 1 V	-450		0	µA

PARAMETER MEASUREMENT INFORMATION

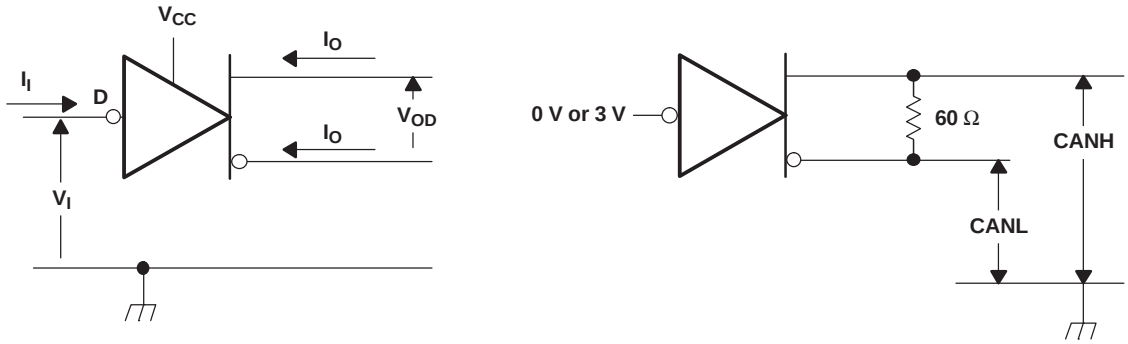


Figure 1. Driver Voltage and Current Definitions

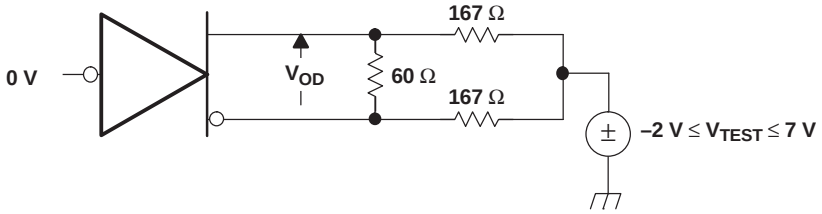


Figure 2. Driver V_{OD}

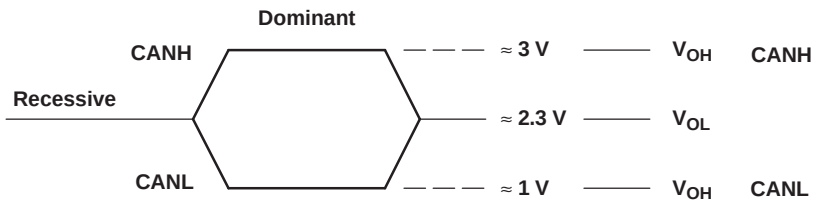
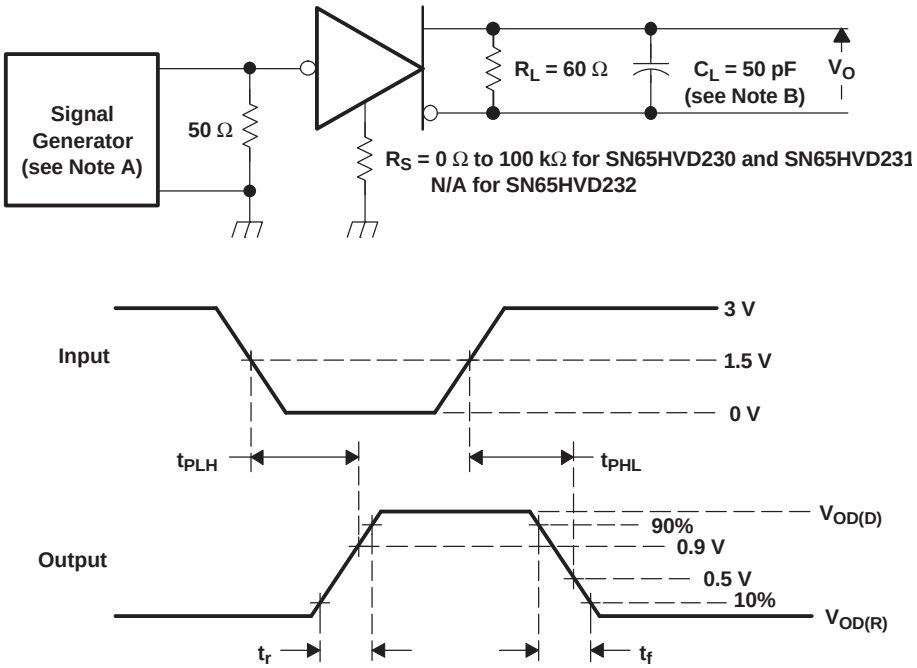


Figure 3. Driver Output Voltage Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_o = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

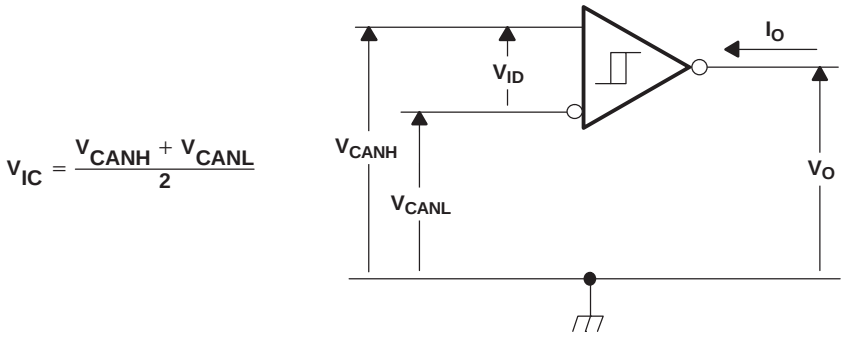
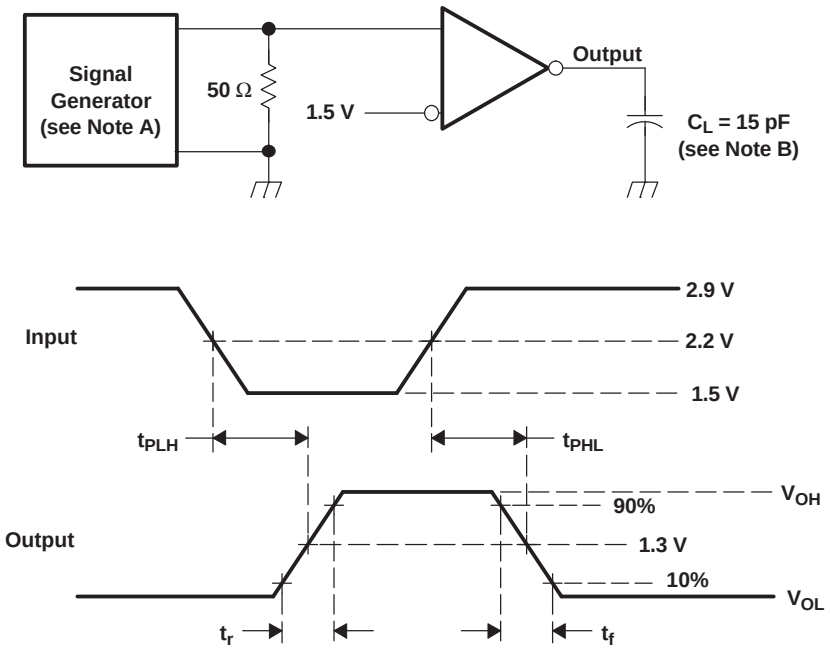


Figure 5. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 500 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_o = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

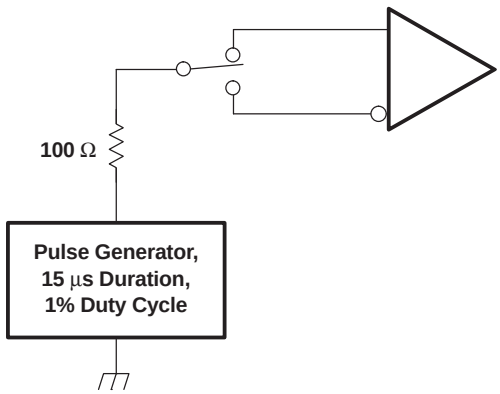


Figure 7. Overvoltage Protection

PARAMETER MEASUREMENT INFORMATION (continued)

Table 1. Receiver Characteristics Over Common Mode With $V_{(Rs)}$ = 1.2 V

V_{IC}	V_{ID}	V_{CANH}	V_{CANL}	R OUTPUT	
-2 V	900 mV	-1.55 V	-2.45 V	L	V_{OL}
7 V	900 mV	8.45 V	6.55 V	L	
1 V	6 V	4 V	-2 V	L	
4 V	6 V	7 V	1 V	L	
-2 V	500 mV	-1.75 V	-2.25 V	H	V_{OH}
7 V	500 mV	7.25 V	6.75 V	H	
1 V	-6 V	-2 V	4 V	H	
4 V	-6 V	1 V	7 V	H	
X	X	Open	Open	H	

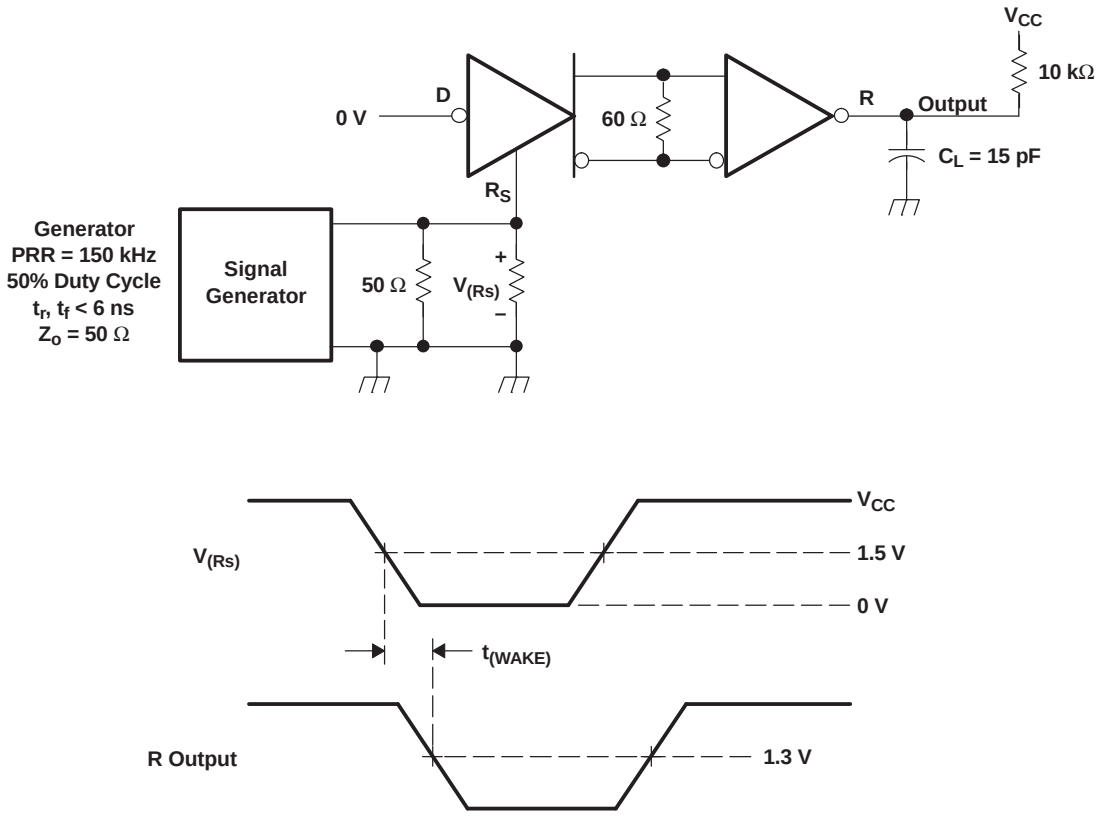
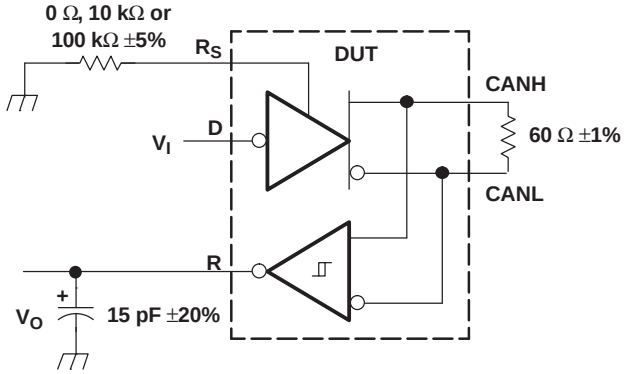
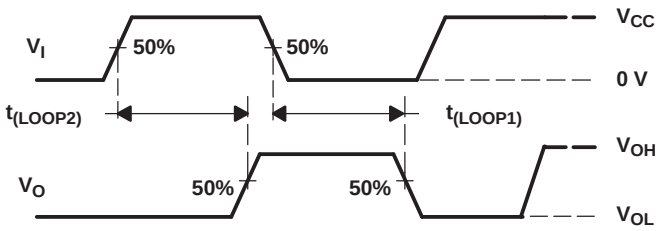


Figure 8. $t_{(WAKE)}$ Test Circuit and Voltage Waveforms





A. All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ ns, Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Figure 9. $t_{(LOOP)}$ Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

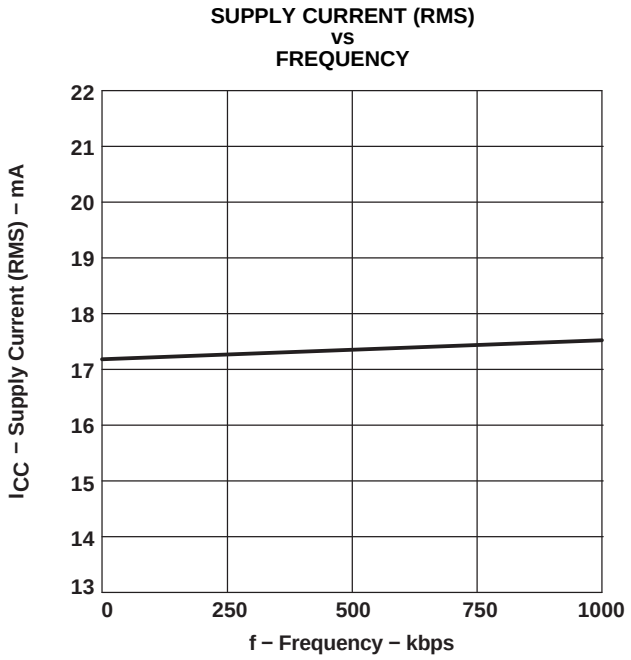


Figure 10.

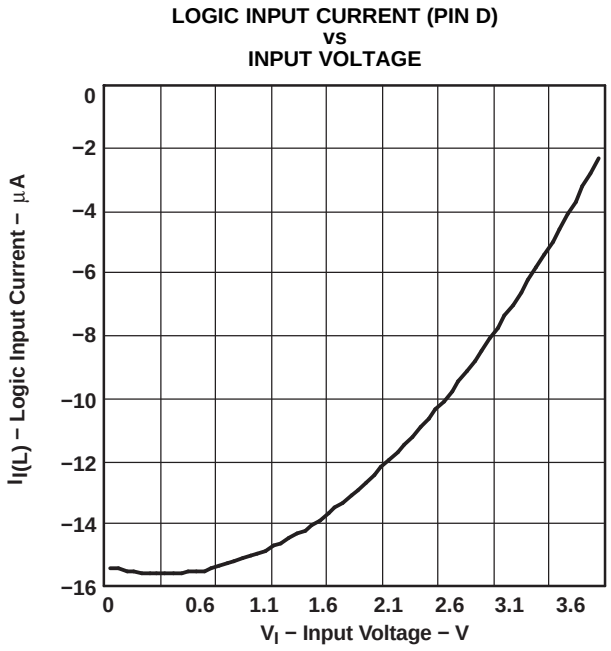


Figure 11.

TYPICAL CHARACTERISTICS (continued)

BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

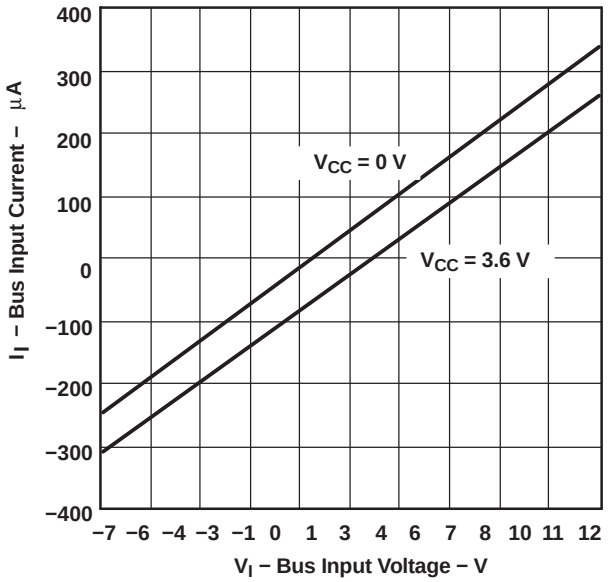


Figure 12.

DRIVER LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

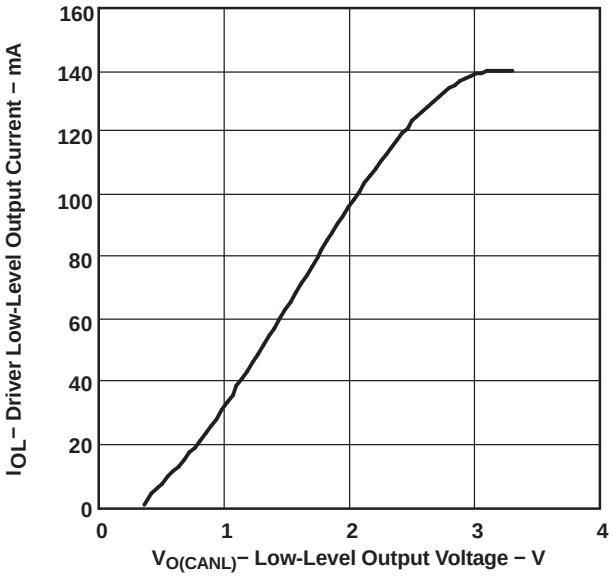


Figure 13.

DRIVER HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

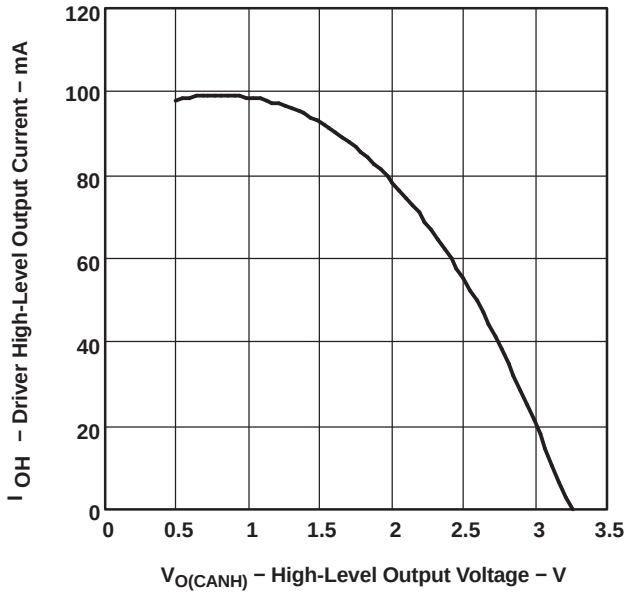


Figure 14.

DOMINANT VOLTAGE (V_{OD})
vs
FREE-AIR TEMPERATURE

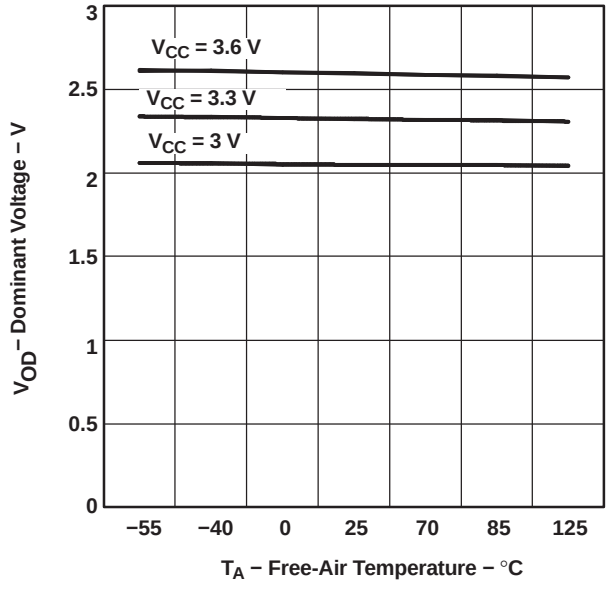


Figure 15.

TYPICAL CHARACTERISTICS (continued)

RECEIVER LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

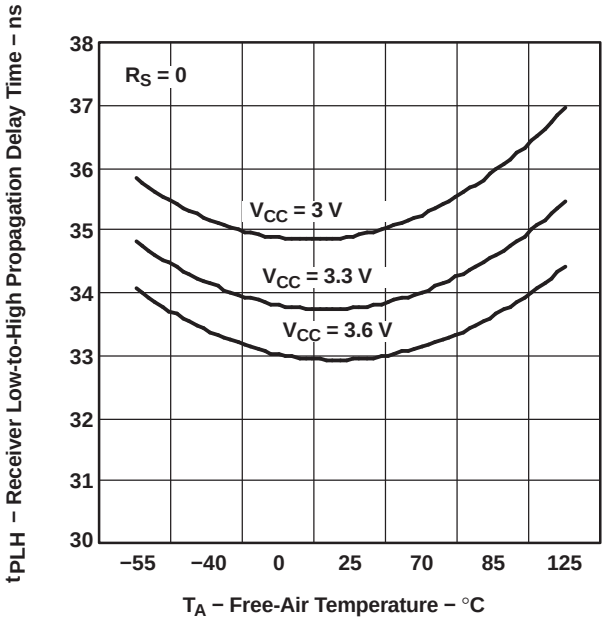


Figure 16.

RECEIVER HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

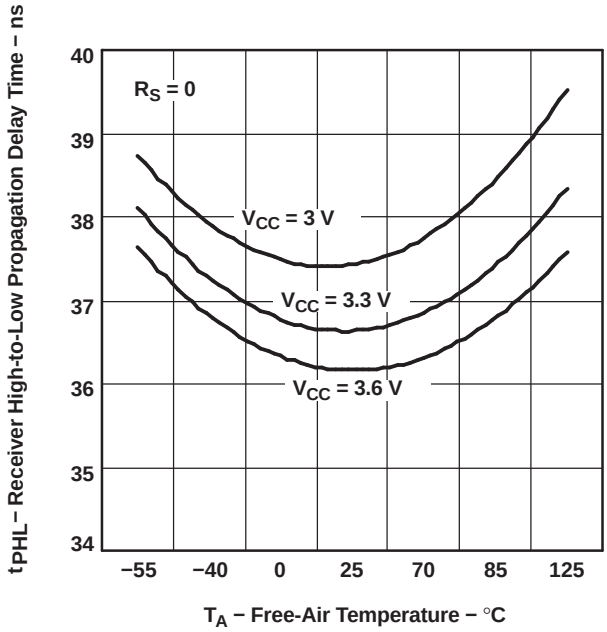


Figure 17.

DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

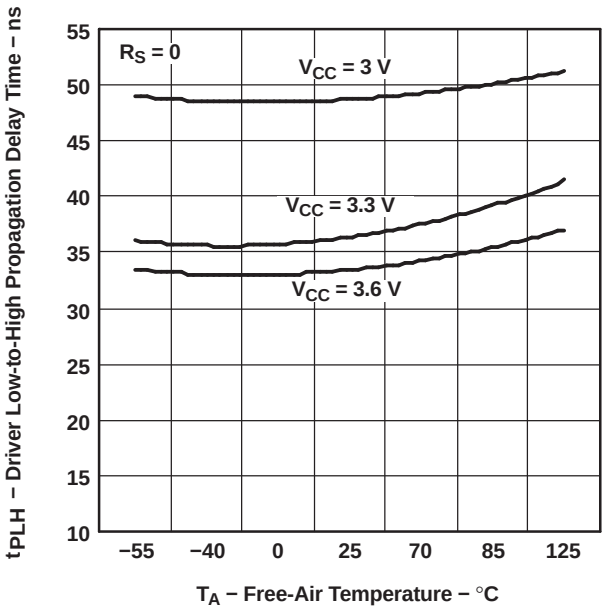


Figure 18.

DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

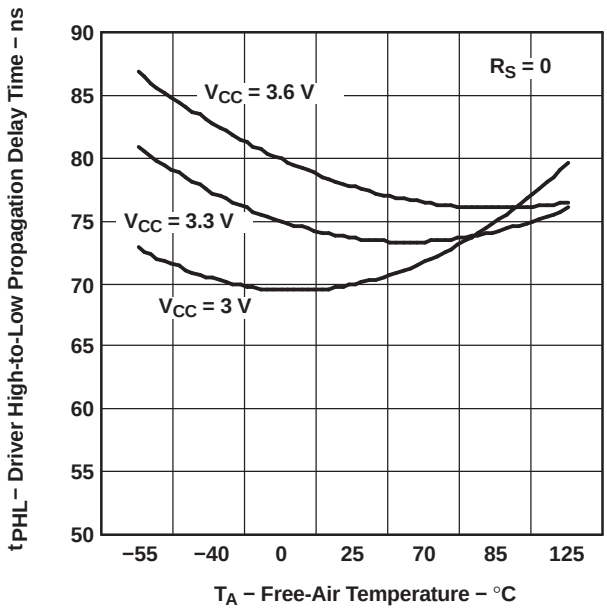


Figure 19.

TYPICAL CHARACTERISTICS (continued)

DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

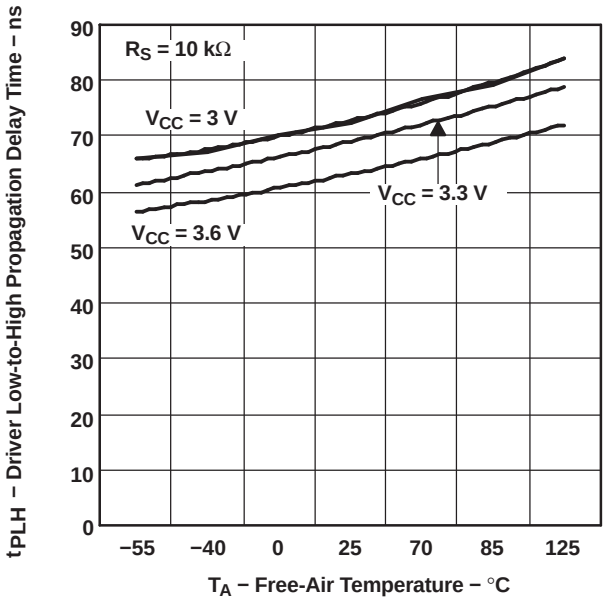


Figure 20.

DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

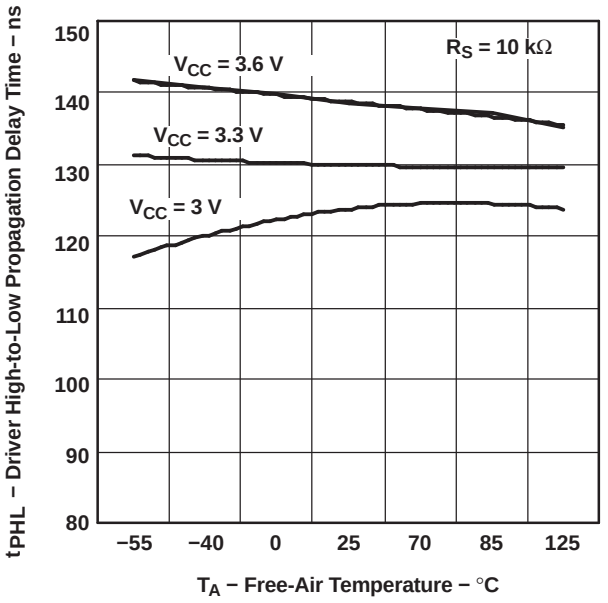


Figure 21.

DRIVER LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

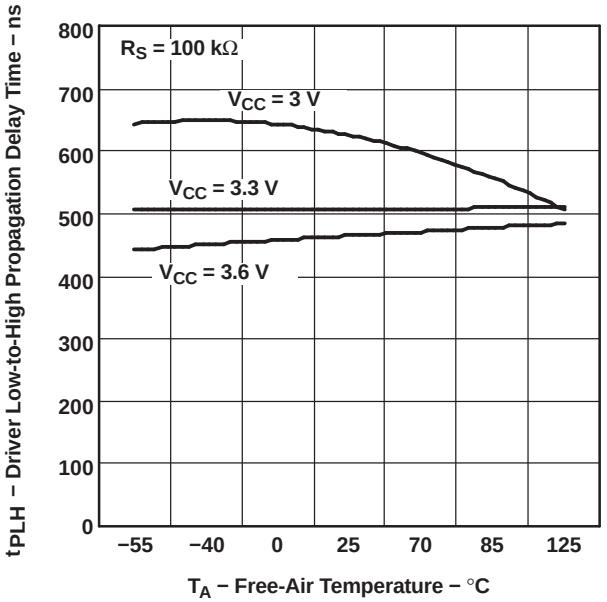


Figure 22.

DRIVER HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

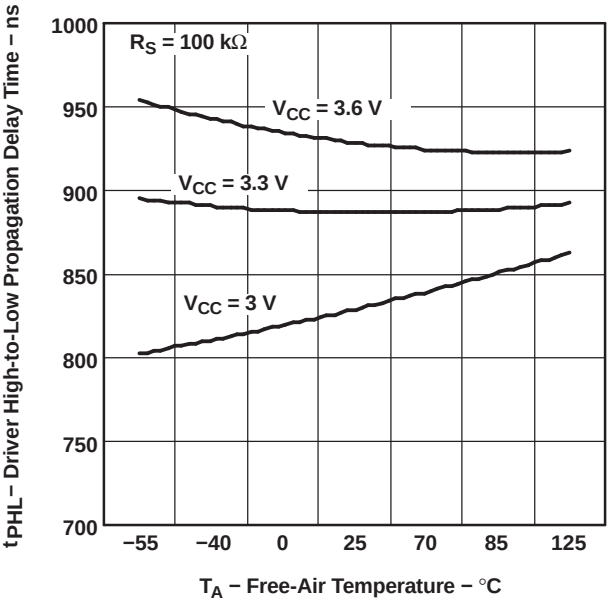


Figure 23.

TYPICAL CHARACTERISTICS (continued)

DRIVER OUTPUT CURRENT
vs
SUPPLY VOLTAGE

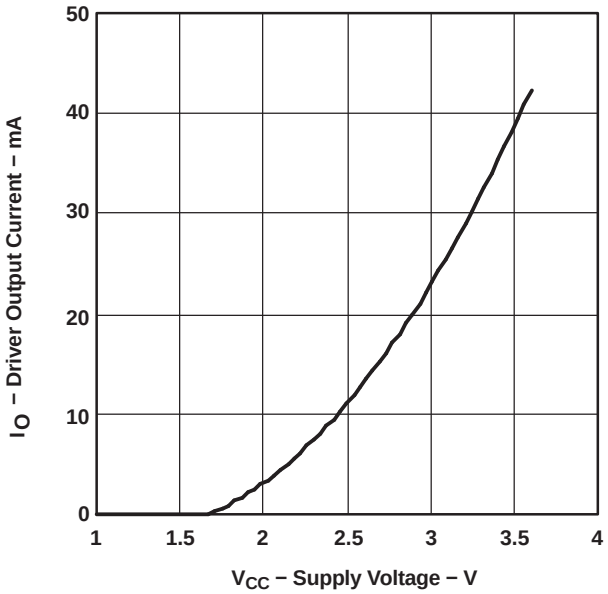


Figure 24.

DIFFERENTIAL DRIVER OUTPUT FALL TIME
vs
SOURCE RESISTANCE (R_s)

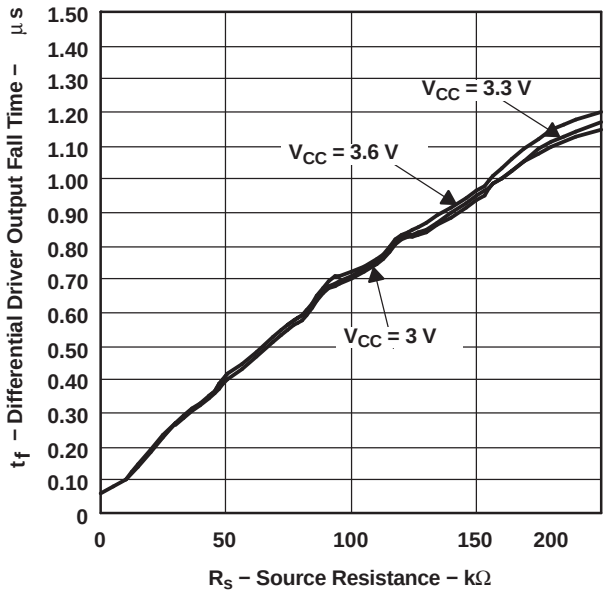


Figure 25.

REFERENCE VOLTAGE
vs
REFERENCE CURRENT

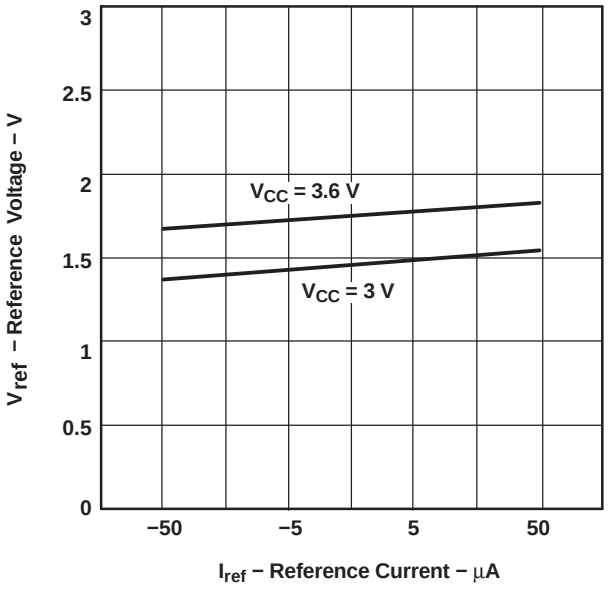


Figure 26.

HVD230, HVD231 LOW-TO-HIGH PROPAGATION DELAY TIME
vs
COMMON-MODE INPUT VOLTAGE

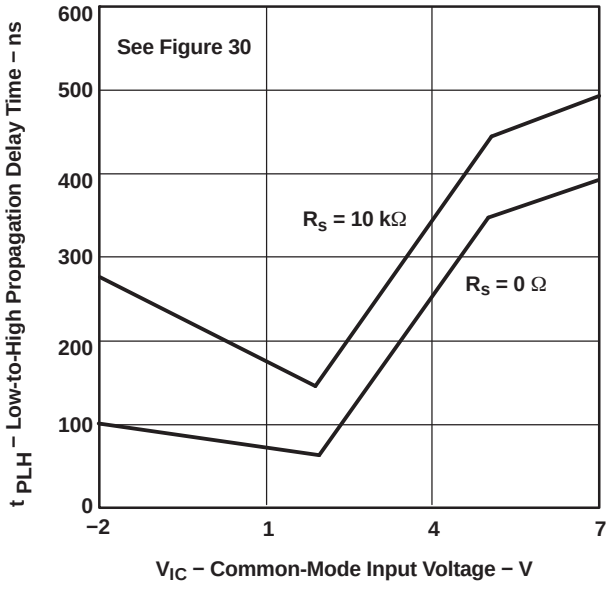


Figure 27.

TYPICAL CHARACTERISTICS (continued)

HVD230, HVD231 LOW-TO-HIGH PROPAGATION DELAY TIME
vs
COMMON-MODE INPUT VOLTAGE

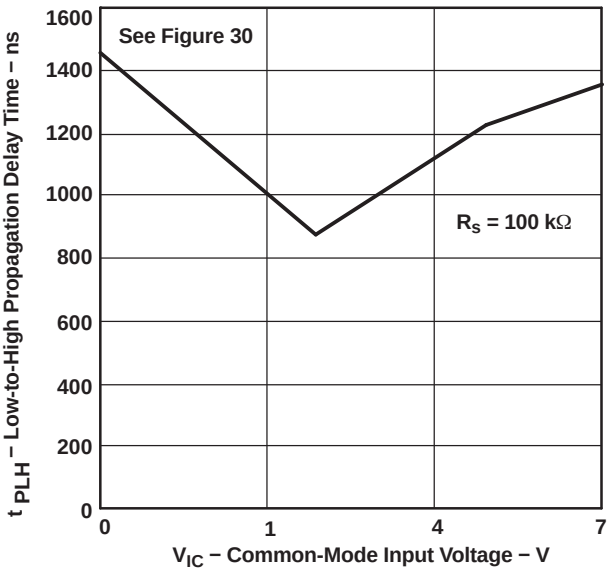


Figure 28.

HVD232 LOW-TO-HIGH PROPAGATION DELAY TIME
vs
COMMON-MODE INPUT VOLTAGE

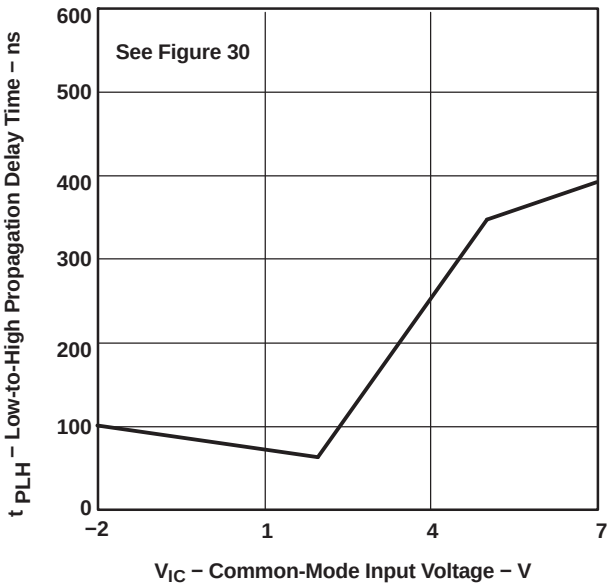


Figure 29.

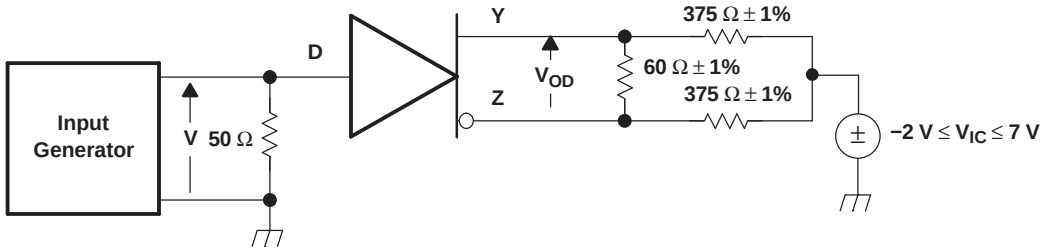


Figure 30. Driver Schematic

APPLICATION INFORMATION

This application provides information concerning the implementation of the physical medium attachment layer in a CAN network according to the ISO 11898 standard. It presents a typical application circuit and test results, as well as discussions on slope control, total loop delay, and interoperability in 5-V systems.

INTRODUCTION

ISO 11898 is the international standard for high-speed serial communication using the controller area network (CAN) bus protocol. It supports multimaster operation, real-time control, programmable data rates up to 1 Mbps, and powerful redundant error checking procedures that provide reliable data transmission. It is suited for networking *intelligent* devices as well as sensors and actuators within the rugged electrical environment of a machine chassis or factory floor. The SN65HVD230 family of 3.3-V CAN transceivers implement the lowest layers of the ISO/OSI reference model. This is the interface with the physical signaling output of the CAN controller of the Texas Instruments TMS320Lx240x 3.3-V DSPs, as illustrated in Figure 31.

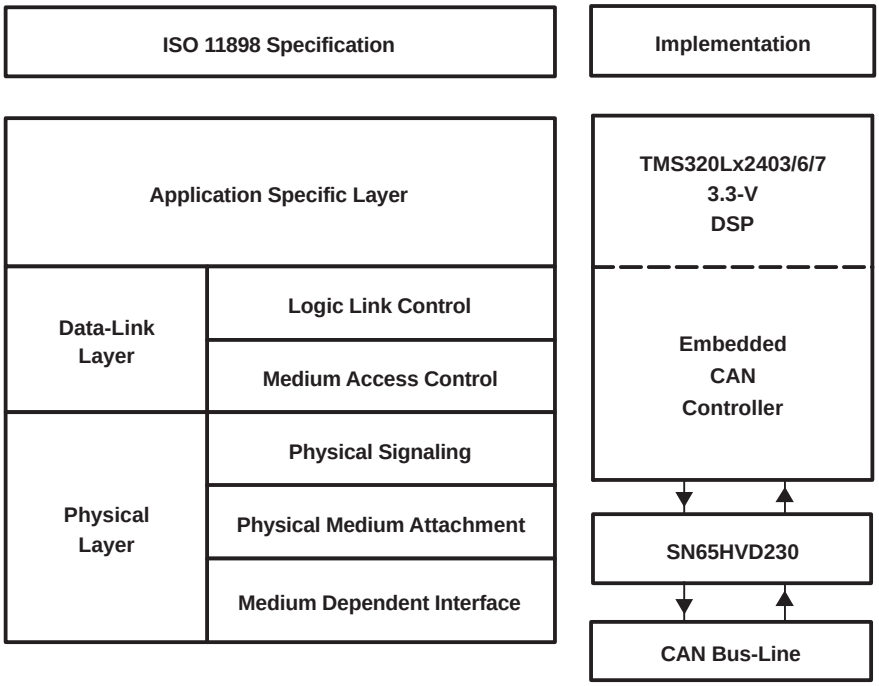


Figure 31. The Layered ISO 11898 Standard Architecture

The SN65HVD230 family of CAN transceivers are compatible with the ISO 11898 standard; this ensures interoperability with other standard-compliant products.

APPLICATION OF THE SN65HVD230

Figure 32 illustrates a typical application of the SN65HVD230 family. The output of a DSP's CAN controller is connected to the serial driver input, pin D, and receiver serial output, pin R, of the transceiver. The transceiver is then attached to the differential bus lines at pins CANH and CANL. Typically, the bus is a twisted pair of wires with a characteristic impedance of 120 Ω, in the standard half-duplex multipoint topology of Figure 33. Each end of the bus is terminated with 120-Ω resistors in compliance with the standard to minimize signal reflections on the bus.

APPLICATION INFORMATION (continued)

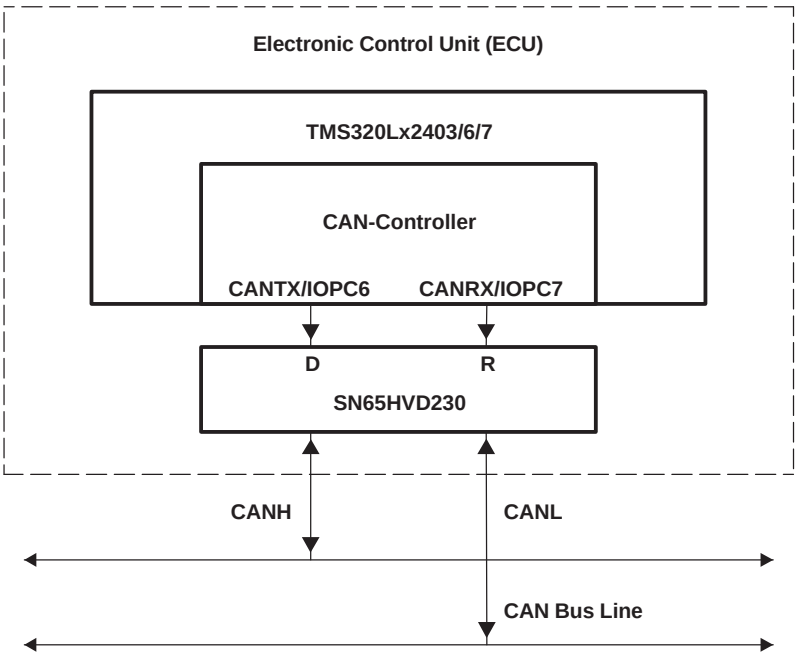


Figure 32. Details of a Typical CAN Node

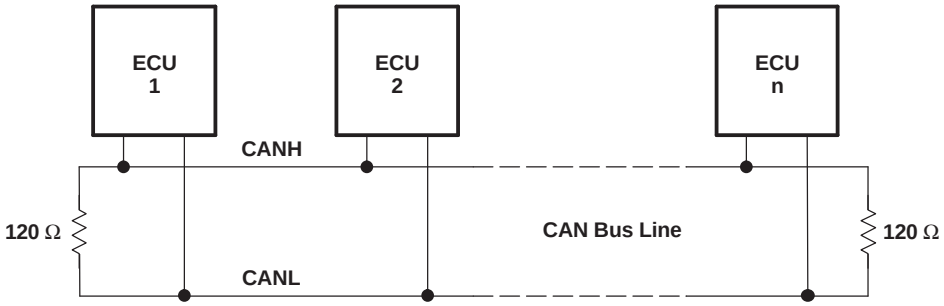


Figure 33. Typical CAN Network

The SN65HVD230/231/232 3.3-V CAN transceivers provide the interface between the 3.3-V TMS320Lx2403/6/7 CAN DSPs and the differential bus line, and are designed to transmit data at signaling rates up to 1 Mbps as defined by the ISO 11898 standard.

FEATURES of the SN65HVD230, SN65HVD231, and SN65HVD232

The SN65HVD230/231/232 are pin-compatible (but not functionally identical) with one another and, depending upon the application, may be used with identical circuit boards.

These transceivers feature 3.3-V operation and standard compatibility with signaling rates up to 1 Mbps, and also offer 16-kV HBM ESD protection on the bus pins, thermal shutdown protection, bus fault protection, and open-circuit receiver failsafe. The fail-safe design of the receiver assures a logic high at the receiver output if the bus wires become open circuited. If a high ambient operating environment temperature or excessive output current result in thermal shutdown, the bus pins become high impedance, while the D and R pins default to a logic high.

APPLICATION INFORMATION (continued)

The bus pins are also maintained in a high-impedance state during low V_{CC} conditions to ensure glitch-free power-up and power-down bus protection for hot-plugging applications. This high-impedance condition also means that an unpowered node does not disturb the bus. Transceivers without this feature usually have a very low output impedance. This results in a high current demand when the transceiver is unpowered, a condition that could affect the entire bus.

OPERATING MODES

R_S (pin 8) of the SN65HVD230 and SN65HVD231 provides for three different modes of operation: high-speed mode, slope-control mode, and low-power mode.

High-Speed

The high-speed mode can be selected by applying a logic low to R_S (pin 8). The high-speed mode of operation is commonly employed in industrial applications. High-speed allows the output to switch as fast as possible with no internal limitation on the output rise and fall slopes. The only limitations of the high-speed operation are cable length and radiated emission concerns, each of which is addressed by the slope control mode of operation.

If the low-power standby mode is to be employed in the circuit, direct connection to a DSP output pin can be used to switch between a logic-low level (< 1 V) for high speed operation, and the logic-high level (> 0.75 V_{CC}) for standby. Figure 34 shows a typical DSP connection, and Figure 35 shows the HVD230 driver output signal in high-speed mode on the CAN bus.

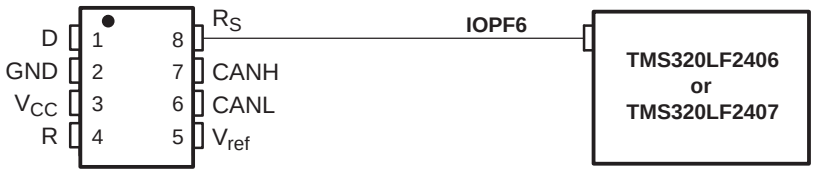


Figure 34. R_S (Pin 8) Connection to a TMS320LF2406/07 for High Speed/Standby Operation

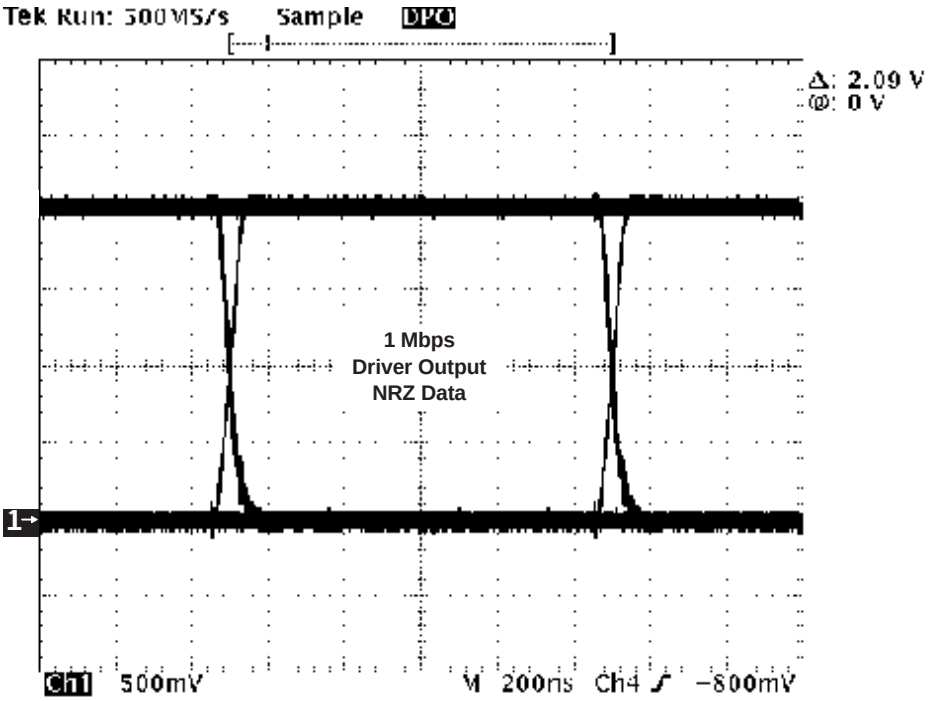


Figure 35. Typical High Speed SN65HVD230 Output Waveform Into a 60-Ω Load

APPLICATION INFORMATION (continued)

Slope Control

Electromagnetic compatibility is essential in many applications using unshielded bus cable to reduce system cost. To reduce the electromagnetic interference generated by fast rise times and resulting harmonics, the rise and fall slopes of the SN65HVD230 and SN65HVD231 driver outputs can be adjusted by connecting a resistor from R_S (pin 8) to ground or to a logic low voltage, as shown in Figure 36. The slope of the driver output signal is proportional to the pin's output current. This slope control is implemented with an external resistor value of 10 kΩ to achieve a ≈ 15 V/µs slew rate, and up to 100 kΩ to achieve a ≈ 2.0 V/µs slew rate as displayed in Figure 37. Typical driver output waveforms from a pulse input signal with and without slope control are displayed in Figure 38. A pulse input is used rather than NRZ data to clearly display the actual slew rate.

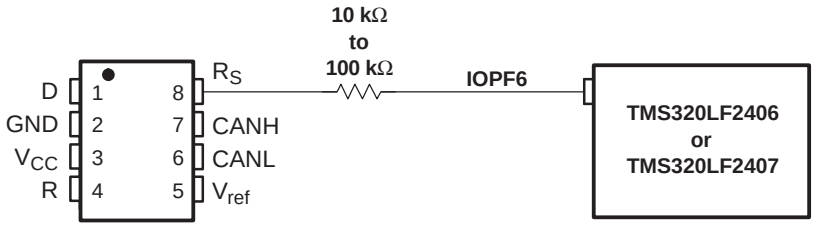


Figure 36. Slope Control/Standby Connection to a DSP

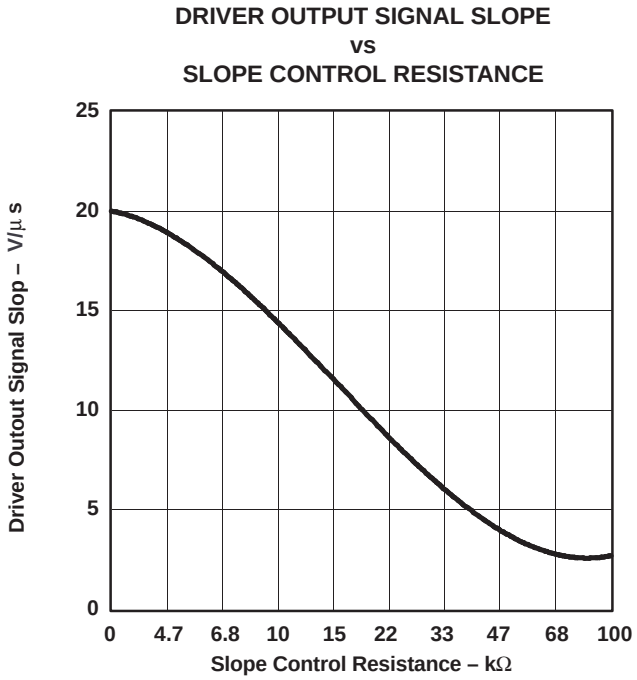


Figure 37. HVD230 Driver Output Signal Slope vs Slope Control Resistance Value

APPLICATION INFORMATION (continued)

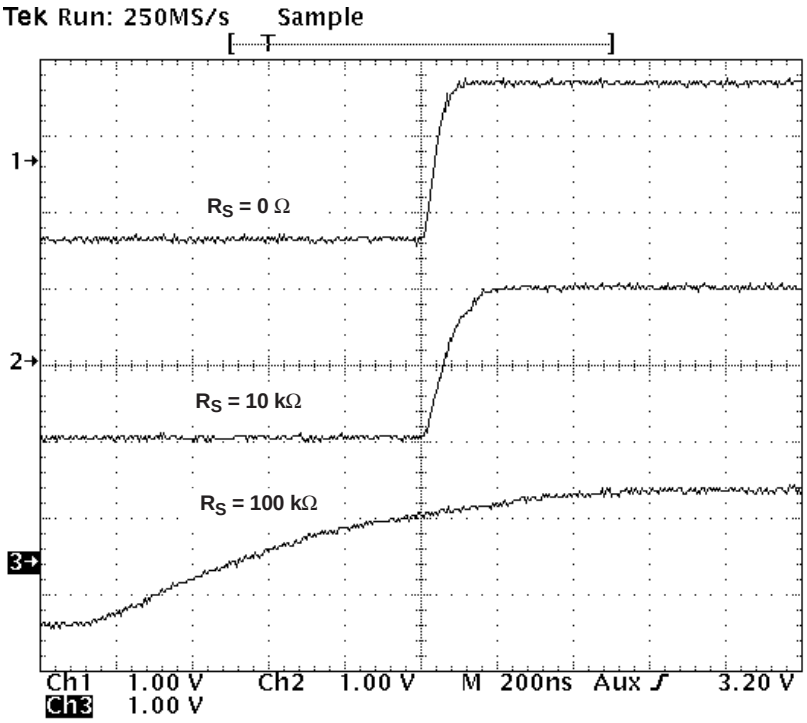


Figure 38. Typical SN65HVD230 250-kbps Output Pulse Waveforms With Slope Control

Standby Mode (Listen Only Mode) of the HVD230

If a logic high (> 0.75 V_{CC}) is applied to R_S (pin 8) in Figure 34 and Figure 36, the circuit of the SN65HVD230 enters a low-current, *listen only* standby mode, during which the driver is switched off and the receiver remains active. In this *listen only* state, the transceiver is completely passive to the bus. It makes no difference if a slope control resistor is in place as shown in Figure 36. The DSP can reverse this low-power standby mode when the rising edge of a dominant state (bus differential voltage > 900 mV typical) occurs on the bus. The DSP, sensing bus activity, reactivates the driver circuit by placing a logic low (< 1.2 V) on R_S (pin 8).

The Babbling Idiot Protection of the HVD230

Occasionally, a runaway CAN controller unintentionally sends messages that completely tie up the bus (what is referred to in CAN jargon as a babbling idiot). When this occurs, the DSP can engage the *listen-only* standby mode to disengage the driver and release the bus, even when access to the CAN controller has been lost. When the driver circuit is deactivated, its outputs default to a high-impedance state.

Sleep Mode of the HVD231

The unique difference between the SN65HVD230 and the SN65HVD231 is that both driver and receiver are switched off in the SN65HVD231 when a logic high is applied to R_S (pin 8). The device remains in a very low power-sleep mode until the circuit is reactivated with a logic low applied to R_S (pin 8). While in this sleep mode, the bus-pins are in a high-impedance state, while the D and R pins default to a logic high.

LOOP PROPAGATION DELAY

Transceiver loop delay is a measure of the overall device propagation delay, consisting of the delay from the driver input to the differential outputs, plus the delay from the receiver inputs to its output.

The loop delay of the transceiver displayed in Figure 39 increases accordingly when slope control is being used. This increased loop delay means that the total bus length must be reduced to meet the CAN bit-timing requirements of the overall system. The loop delay becomes ≈ 100 ns when employing slope control with a

APPLICATION INFORMATION (continued)

10-kΩ resistor, and ≈ 500 ns with a 100-kΩ resistor. Therefore, considering that the rule-of-thumb propagation delay of typical bus cable is 5 ns/m, slope control with the 100-kΩ resistor decreases the allowable bus length by the difference between the 500-ns max loop delay and the loop delay with no slope control, 70.7 ns. This equates to (500-70.7 ns)/5 ns, or approximately 86 m less bus length. This slew-rate/bus length trade-off to reduce electromagnetic interference to adjoining circuits from the bus can also be solved with a quality shielded bus cable.

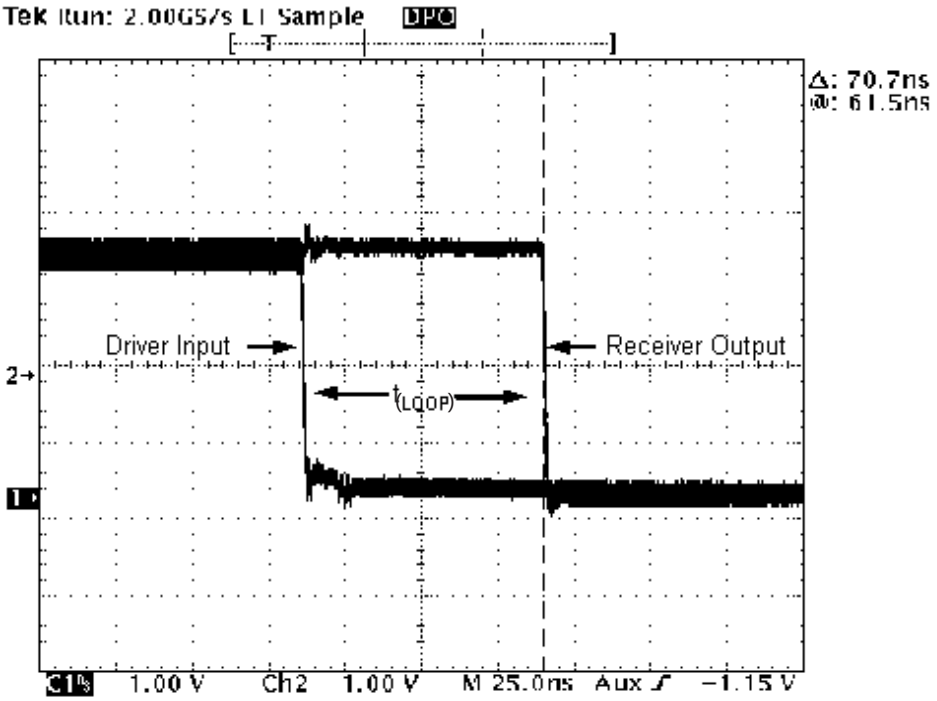


Figure 39. 70.7-ns Loop Delay Through the HVD230 With R_S = 0

INTEROPERABILITY WITH 5-V CAN SYSTEMS

It is essential that the 3.3-V HVD230 family performs seamlessly with 5-V transceivers because of the large number of 5-V devices installed. Figure 40 displays a test bus of a 3.3-V node with the HVD230, and three 5-V nodes: one for each of TI's SN65LBC031 and UC5350 transceivers, and one using a competitor X250 transceiver.

APPLICATION INFORMATION (continued)

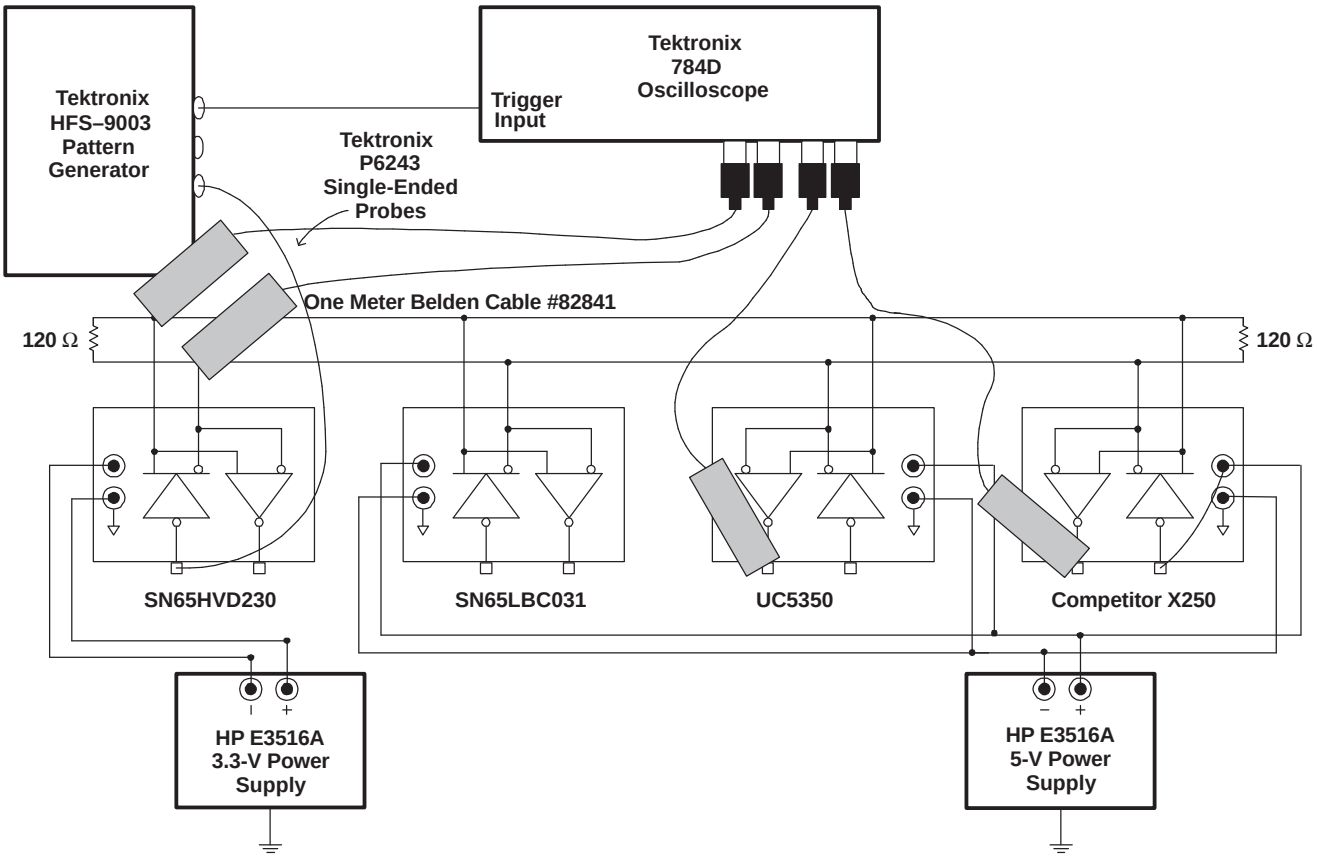


Figure 40. 3.3-V/5-V CAN Transceiver Test Bed

APPLICATION INFORMATION (continued)

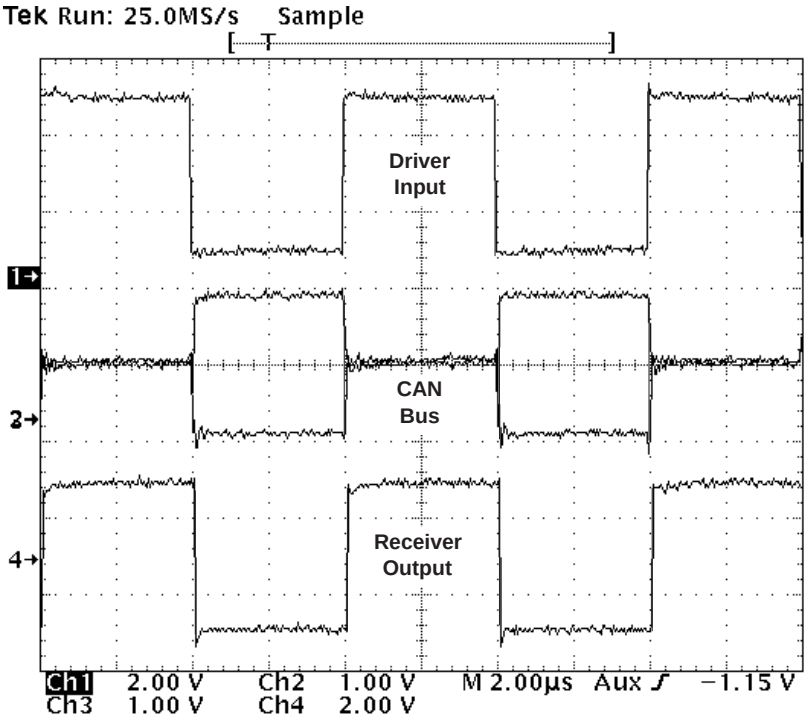


Figure 41. The HVD230's Input, CAN Bus, and X250's RXD Output Waveforms

Figure 41 displays the HVD230's input signal, the CAN bus, and the competitor X250's receiver output waveforms. The input waveform from the Tektronix HFS-9003 Pattern Generator in Figure 40 to the HVD230 is a 250-kbps pulse for this test. The circuit is monitored with Tektronix P6243, 1-GHz single-ended probes in order to display the CAN dominant and recessive bus states.

Figure 41 displays the 250-kbps pulse input waveform to the HVD230 on channel 1. Channels 2 and 3 display CANH and CANL respectively, with their recessive bus states overlaying each other to clearly display the dominant and recessive CAN bus states. Channel 4 is the receiver output waveform of the competitor X250.

PACKAGE OPTION ADDENDUM

29-Sep-2006

PACKAGING INFORMATION

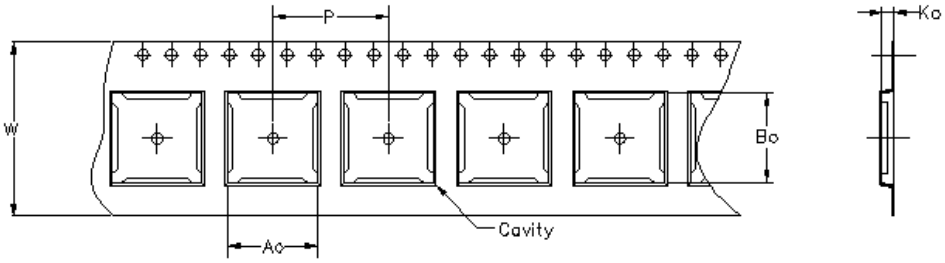
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN65HVD230D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD230DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD230DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD230DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD231D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD231DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD231DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD231DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD232D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD232DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD232DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD232DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

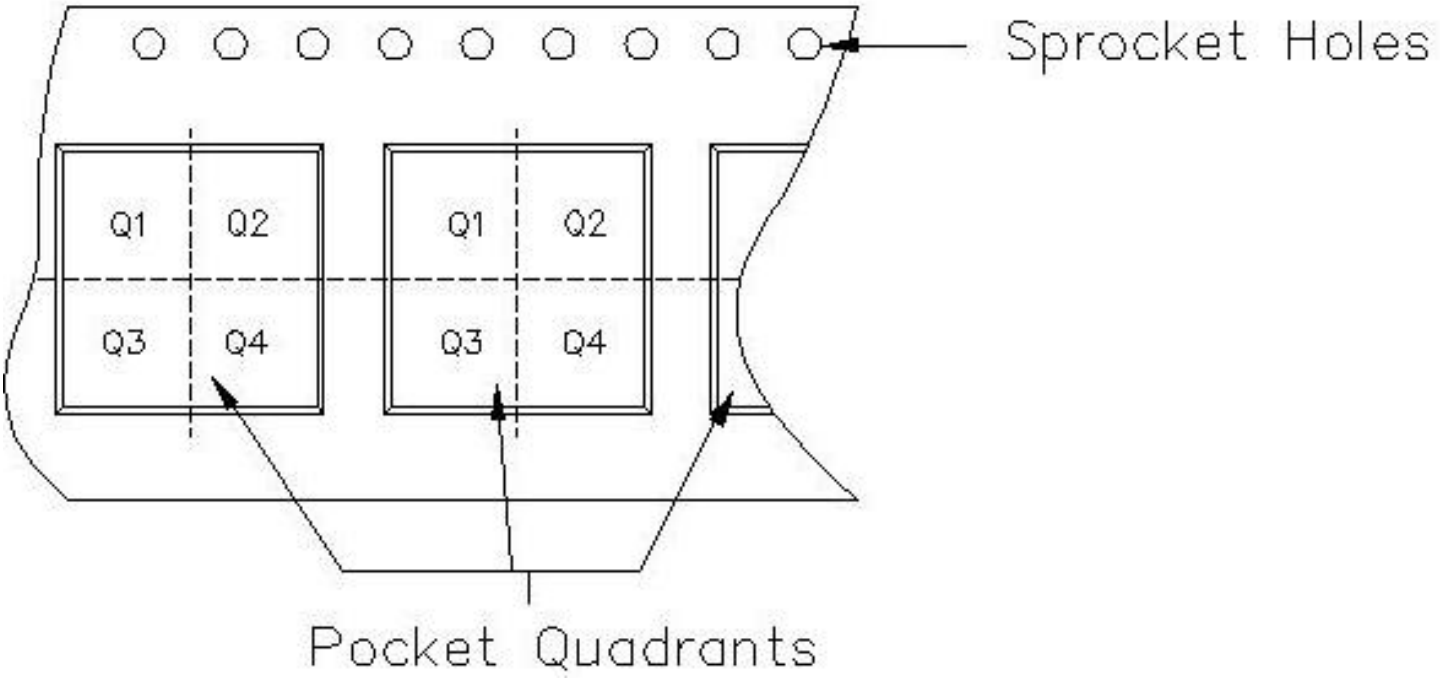
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



Carrier tape design is defined largely by the component lentgh, width, and thickness.

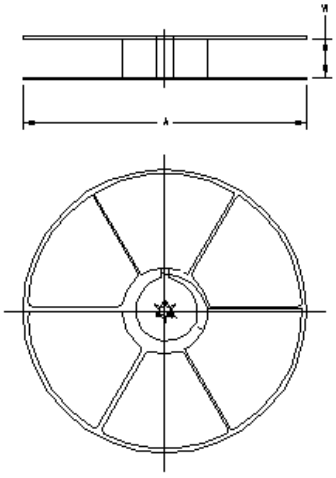
Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



TAPE AND REEL INFORMATION

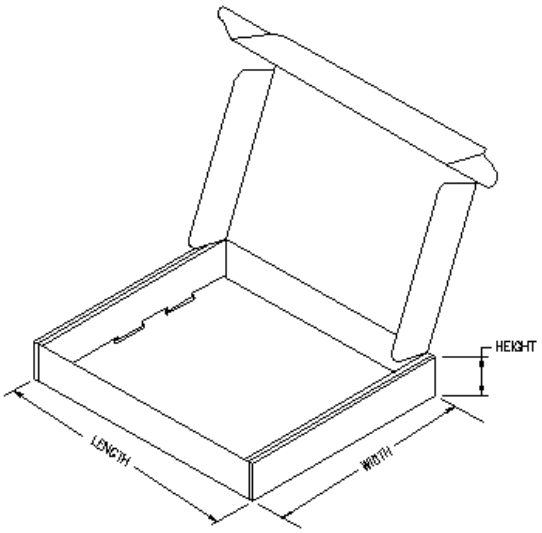
PACKAGE MATERIALS INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD230DR	D	8	FMX	330	0	6.4	5.2	2.1	8	12	Q1
SN65HVD231DR	D	8	FMX	330	0	6.4	5.2	2.1	8	12	Q1
SN65HVD232DR	D	8	FMX	330	0	6.4	5.2	2.1	8	12	Q1

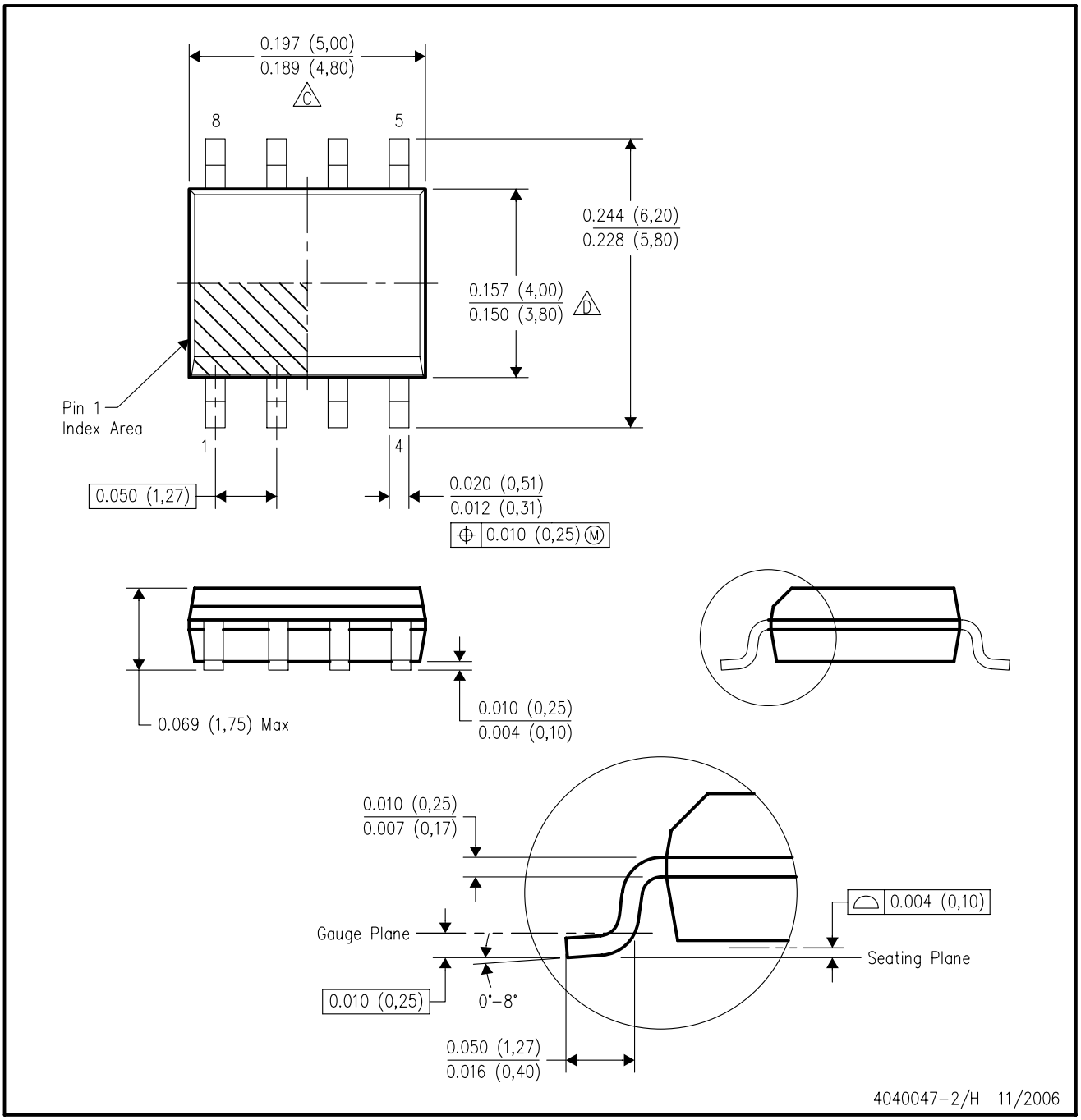


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65HVD230DR	D	8	FMX	342.9	336.6	20.64
SN65HVD231DR	D	8	FMX	342.9	336.6	20.64
SN65HVD232DR	D	8	FMX	342.9	336.6	20.64


HEIGHT
LENGTH
WIDTH

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265