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Design Guide
VT6202

PCI USB2
4-Port Host Controller

USB 2.0 UHCI and EHCI Host Controller for the PCI Bus

Revision 1.2
August 28, 2002

VIA TECHNOLOGIES, INC.

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REVISION HISTORY

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1.01	1/11/02	Updated application schematics	DH
1.02	1/21/02	Updated application schematics	DH
1.1	6/4/02	Removed "Preliminary" from document revision Changed the address of USA office and telephone and fax numbers of Taipei office Fixed error in pin 110 (GND changed to VCC33) Updated VT6202 reference design schematics and design bill of materials Changed the table content of pull-down resistors	DO
1.2	8/28/02	Added pull-high pins Changed BOM list Updated application schematics	DO

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DESIGN GUIDE

PCI USB 2.0
Four-Port
Host Controller

CHAPTER 1. INTRODUCTION

This document provides design guidelines for PCI interface card manufacturers for developing a 4 port USB 2.0 PCI card or for motherboard manufacturers designing the VT6202 on the motherboard.

1-1. About the Design Guide

A brief description chapter of each chapter is given below.

Chapter 1 - Introduction

An overview and features of the VT6202 PCI 4-port USB 2.0 host controller.

Chapter 2 - General Design Guidelines

Recommendations related to PCB power and ground.

Chapter 3 - PCI Bus and USB Layout and Routing Guidelines

Detailed layout and routing for the PCI interface, USB differential signals and power.

Chapter 4 - Design Checklist

Design checklist provided to the designer for reviewing the layout.

Appendices - VT6202 Reference Design

Bill of Materials (BOM) and Reference Schematics

1-2. VT6202 PCI 4-Port USB2 Host Controller Overview

The VT6202 PCI 4-Port USB2 Host Controller is compliant with Universal Serial Bus Specification Revision 2.0. The chip uses a Universal Host Controller Interface (UHCI) for Low / Full speed data rates (1.5/12 Mbps) and an Enhanced Host Controller Interface (EHCI) Specification Revision 0.95 for high speed data rate (480Mbps) transfers.

Features

- **Universal Serial Bus (USB) Specification Revision 2.0 compliant (Supporting 1.5, 12, and 480 Mbps data rates)**
- **Integrated multi-PCI functions in a single chip including two UHCI host controllers for low / full speed data transactions and one EHCI host controller for high-speed data transactions**
- **Four downstream ports, each port providing full support for low / full / high speed data rates**
- **USB device wake-up function support**
- **Legacy function support**
- **PCI Specification Revision 2.2 compliant**
- **PCI Bus Power Management Interface Revision 1.1 compliant**
- **3.3V / 2.5V multi-power supply and 3.3V suspend power for wake-up function**

CHAPTER 2. GENERAL DESIGN GUIDELINES

General recommendations and design guidelines for printed circuit board design**,** placement and power.

2-1. Pinout Assignment

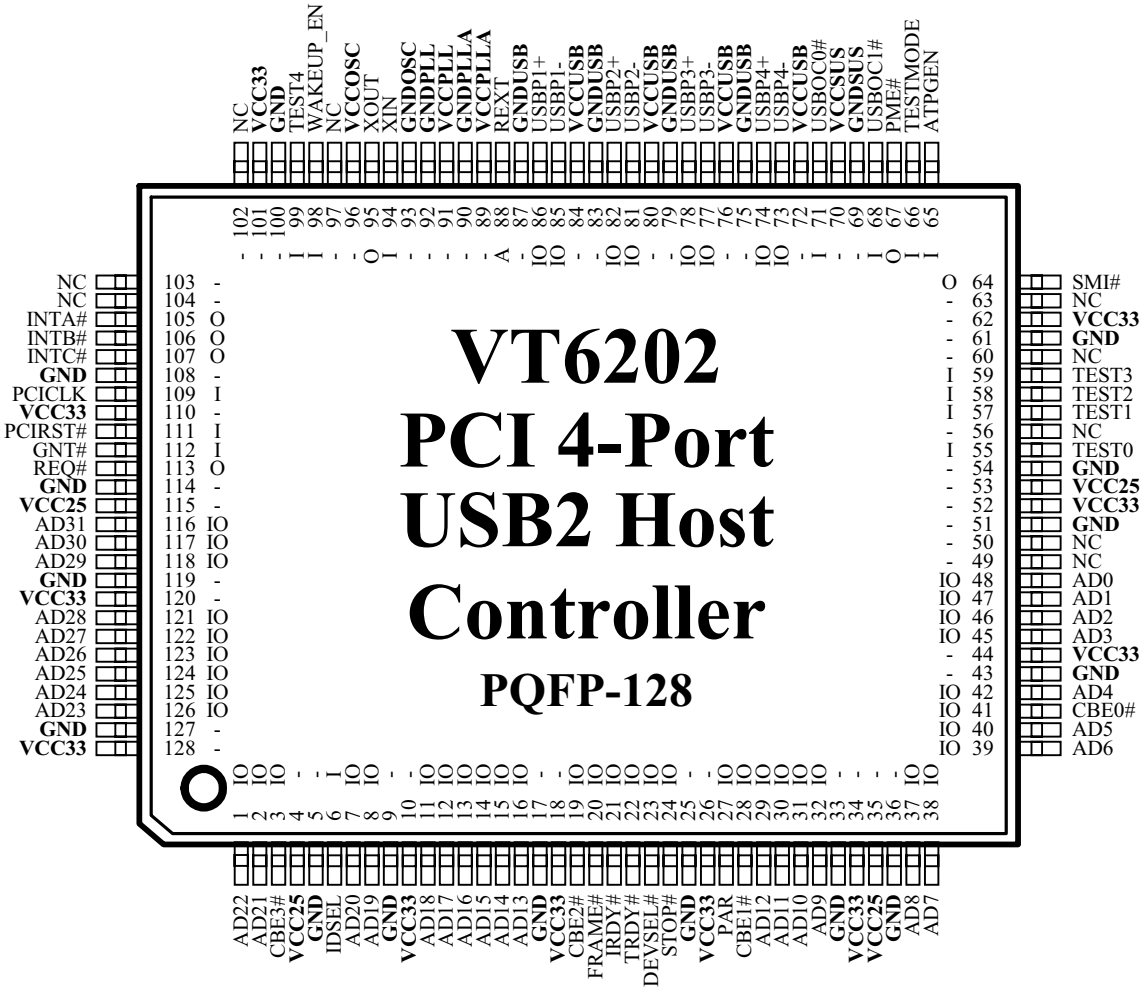


Figure 1. The VT6202 Pinout

2-2. VT6202 PCI Add-In Card General Design Guidelines

For VT6202 USB 2.0 PCI card design, it is necessary to follow PCB, Power and Ground guidelines for implementing 480 Mbps data rate.

Printed Circuit Board Requirements

The PCB (Printed Circuit Board) for the VT6202 USB 2.0 card is a 4-layer design including two signal layers, one power layer and one ground layer.

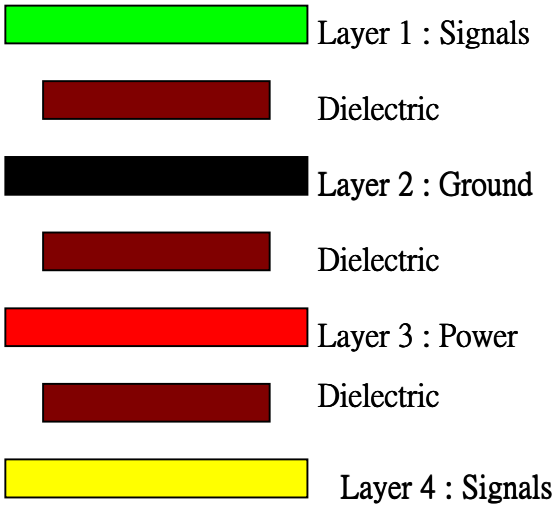


Figure 2. Four-Layer Stack-Up Description

To ensure signal quality compatible with USB 2.0 specification requirements when the VT6202 is running in high-speed mode, the recommended impedance of the PCB is regulated as 45Ω (tolerance ±15%) on a PCI add-in card or 50Ω (tolerance ±15%) on the motherboard. Table 1 provides detailed information about the PCB recommendations.

Layer(number)	Layout Partition	Copper	Thickness
Component (1)	PCI, USB Differential Signals	0.5 oz.	2.4 ~2.5 mils
Ground (2) Power (3)	Ground and Power	1 oz.	50~55 mils (Note2)
Solder (4)	PCI and Other Signal Traces	0.5 oz.	2.4 ~2.5 mils
Dielectric Layer (Note1)			5~5.5 mils

Table 1. PCB Layout Recommendations

Note1: The Dielectric layer is between the Component and Ground layers and between the Solder and Power layers
Note2: The thickness is included the dielectric layer that is between the Power layer and the Ground layer.
Note3: This table primarily applies to VT6202 PCI add-in cards, but can also be used for motherboards
Note4: Total board thickness is 63 ~65 mils

PCI Add-In Card Component Placement

Component placement includes one VT6202 chip, four USB single pin-type A receptacles, one 24MHz crystal to generate the clock to the VT6202, and other components. The component reference position, which has 4 outward ports, is shown in Figure 3. The placement including three outward ports and one inside port is shown in Figure 4. The VT6202 is placed near the PCI BUS. The USB power switch is optional and could be removed in a low-cost card without the USB wake-up function.

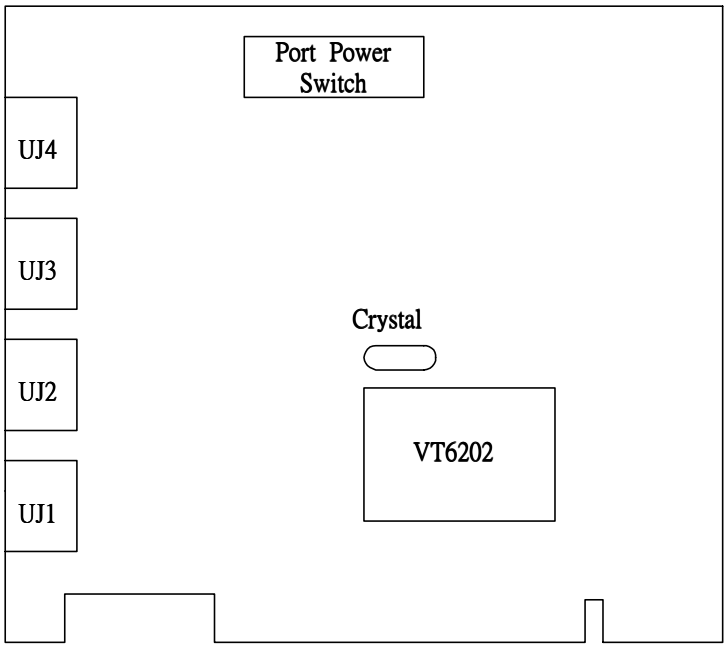


Figure 3. VT6202 PCI USB Add-in Card Component Placement

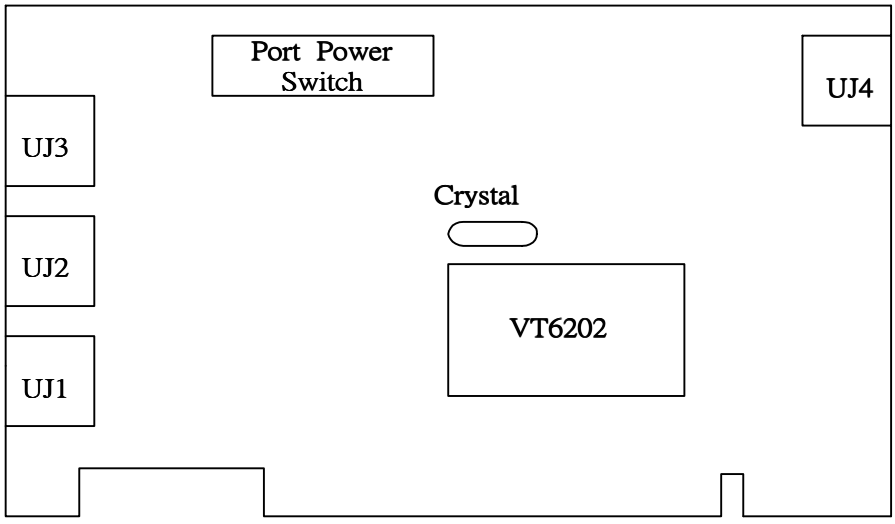


Figure 4. VT6202 PCI USB Add-in Card with One Inside Port

VT6202 Motherboard Placement

When designing the VT6202 onto the motherboard, use one Dual Pin-Type series "A" receptacle and one 2*5 Header for the USB 2.0 port. Figure 5 shows the VT6202 reference placement on an ATX motherboard.

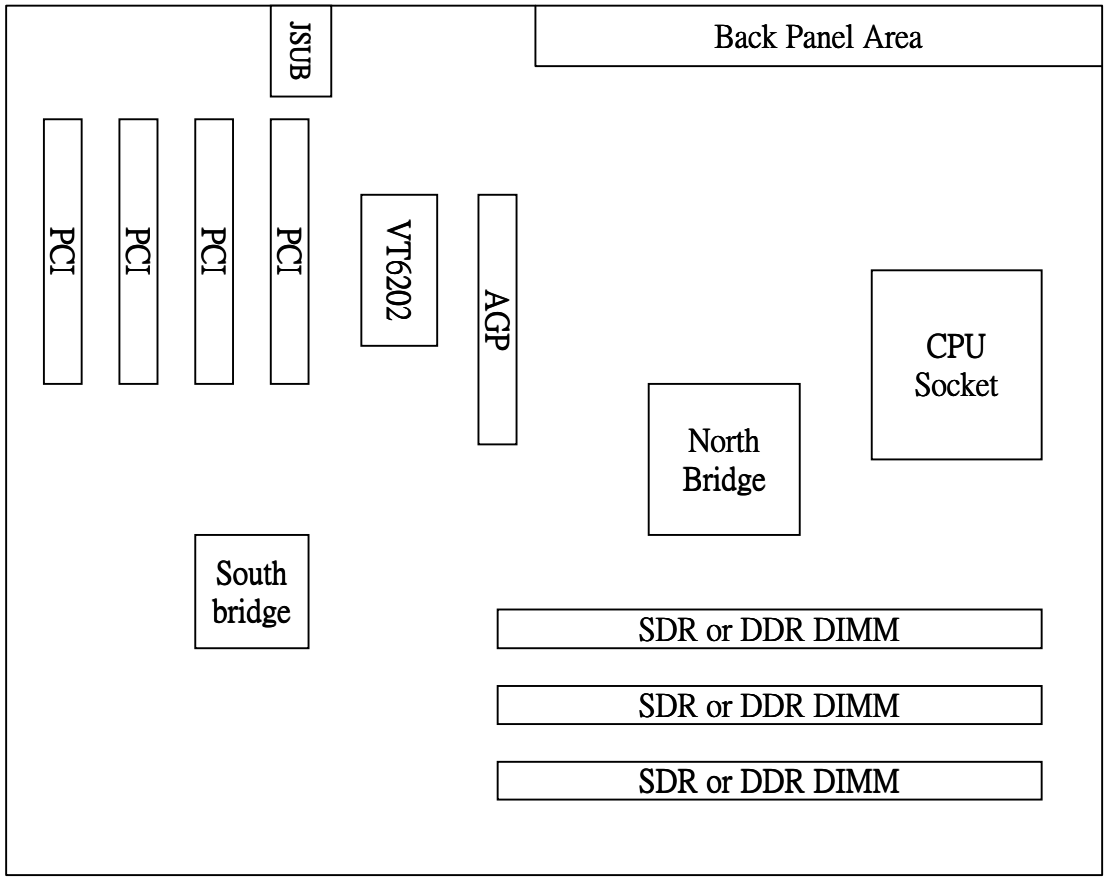


Figure 5. VT6202 ATX Mother Board Reference Placement

2-3. Power and Ground Description

Power and ground of the VT6202 PCI USB 2.0 add-in card are split up into 2 parts, digital and analog. Stable power sources guarantee the VT6202 running normally and good ground partitions are important to signal quality.

Power Partitions and Layout Recommendations

There are four voltage sources (VCC2_5, AVCC2_5, VCC3, AVCC3) supporting the VT6202 and one (AVCC5) supporting the USB receptacles (USB Root Port). Table 2 summarizes the voltage sources, functions powered by each voltage, voltage requirements, and recommended trace widths. VCC2_5, AVCC2_5 and AVCC3 traces are laid out to be compatible with the USB suspend power specification. The Suspend 3.3V to 5V converter circuit has the capability of supplying 2mA (each port is supplied 0.5mA in suspend or power-down modes). The USB port power switch is a power changeable circuit. USB port power is supplied from AVCC5 in the power-down condition or from suspend-5V in power–down or Suspend to RAM (Disk) conditions and reports the USB Over-Current signal to the VT6202. AVCC5 and VCC3 are arranged on the power plane (Power Layer).

Voltage Source	Function	Voltage Tolerance	Trace Width
VCC2_5	VT6202 core power	2.5V±5%	>10 mils
AVCC2_5	VCCPLLA VCCOSC VCCPLLA	2.5V±5%	>10 mils
VCC3	PCI interface	3.3±100mV	(See Note1)
AVCC3 (Suspend) (See Note2)	USB Port Power and USB Port Suspend Power	3.3V±5%	>40 mils (>10 mils each trace to pins)
VCC (5V)	Supply to AVCC5	5V±5%	>80 mils (See Note3)
AVCC5	USB Root port	Refer to USB Specification 2.0	(See Note1)

Table 2. Power Layout Recommendations

Note1. VCC3 and AVCC5 are arranged on the power plane layer

Note2. The voltage source of AVCC3 may be VCC3 if the USB wake-up function is not supported.

Note3. AVCC5 is supplied from VCC. Supply current capability on each USB root port is 500mA. So the current supply capacity should be at least 2A and the trace width should be wider than 80 mils.

The AVCC5 power plane should be included in the space under the USB differential signal pins as shown in Figure 6. This is to avoid having high-speed USB differential signals cross another different power plane.

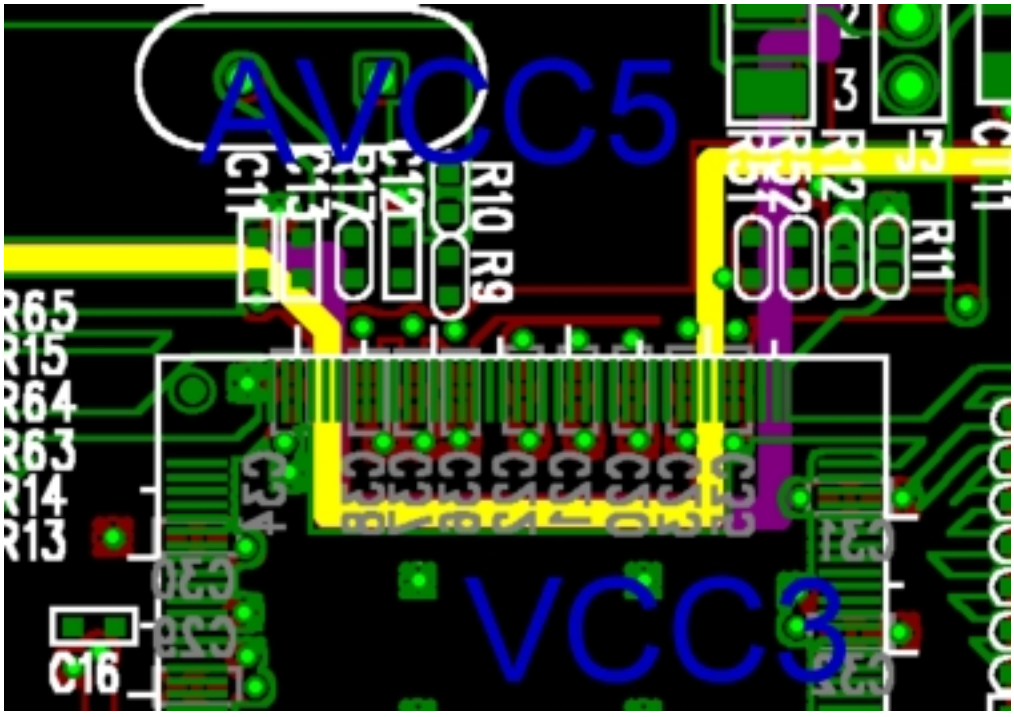


Figure 6. Reference Power Plane Partitions under the VT6202

All power pins on the VT6202 should have decoupling capacitors located as close as possible. VIA recommends that the decoupling capacitors be placed on the solder side and under the power and ground pins. Two different value capacitors (0603 size 0.1µF and 0.01µF) should be placed by each pin. The reference placement is shown in Figure 7.

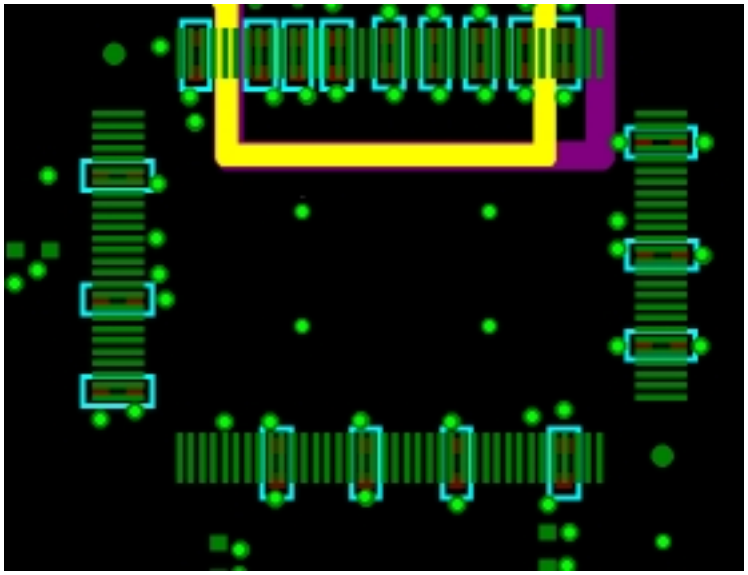


Figure 7. Decoupling Capacitor Placement

Ground Partition Recommendations

There are two ground partitions, Analog Ground (AGND) and Digital Ground (GND). The USB port power switch circuit and the Suspend 3.3V-to-5V converter circuit are arranged on the AGND plane. Table 3 lists the groups of VT6202 ground pins.

Ground Plane	Pin Name	Pin Numbers
GND	GND	5,9,17,25,33,36,43,51,54,61,100,108,114,119,127
AGND	AGND	69
	GNDUSB	87,83,79,75
	GNDOSC	93
	GNDPLLA	90
	GNDPLL	92

Table 3. Ground Pin Groups

Figure 8 shows the reference ground partitions under the VT6202. The AGND plane should be included in the space under the VT6202 USB differential signal pins and analog ground pins.

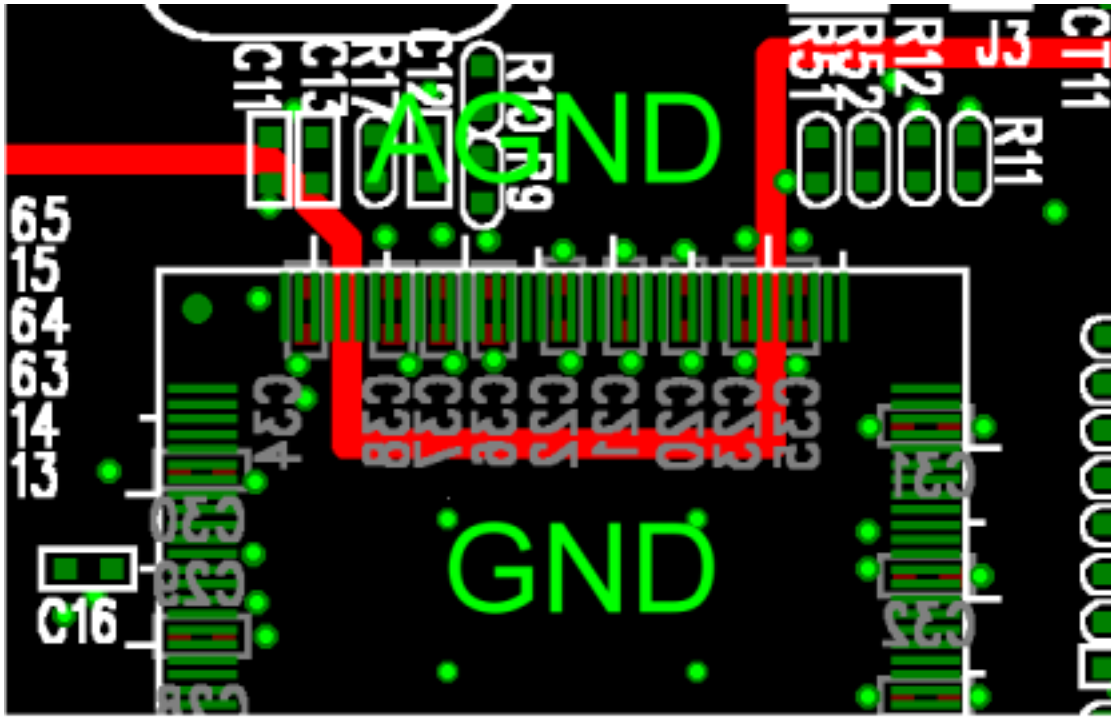


Figure 8. Reference Ground Partitions under the VT6202

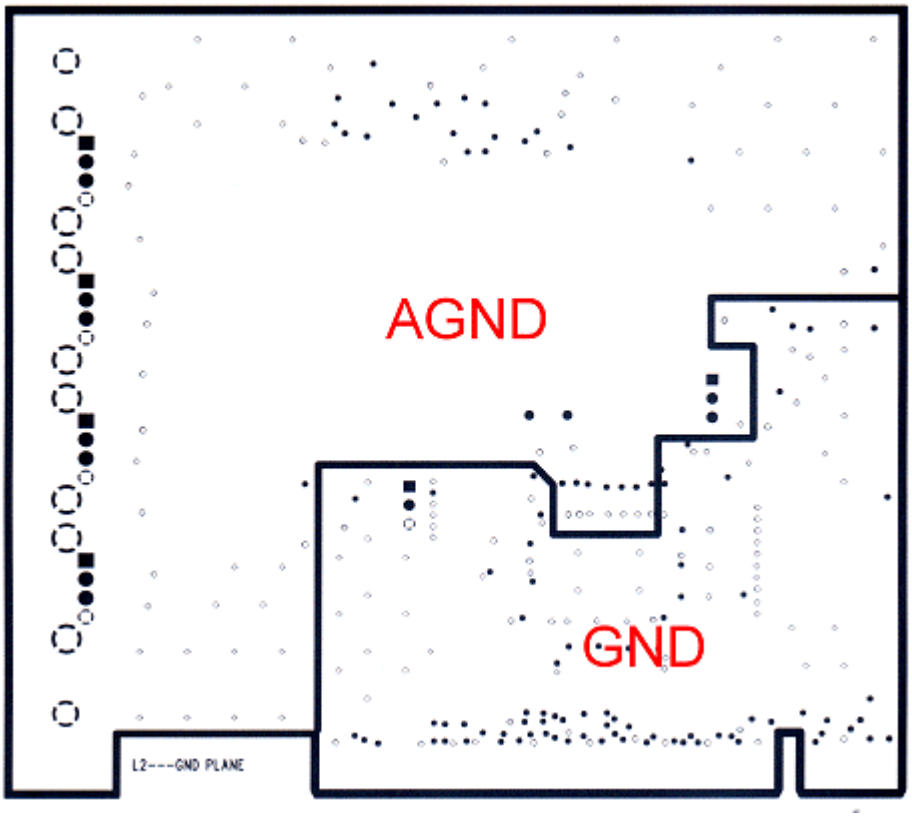


Figure 9. VT6202 PCI 4-Port USB2 Card Reference Ground Partitions

Power and Ground Recommendations for Motherboard Design

For motherboard designs, the suspend 3.3V-to-5V circuit is not necessary because the suspend 5V is supplied from the ATX power supply. The recommended 5V_SB current supply should be at least 1.2A when the system supports the VT6202 USB wake-up function. For ease of design all analog power and ground pins are connected to the digital power or ground plane except pins 89, 90, 91, 92, 93, and 96 which are isolated from digital power or ground by connecting to analog power or ground. Use Ferrite Beads to connect the digital and analog power (ground) planes.

2-4. USB Port Overcurrent Detection

The Micrel MIC2012 supervises the current that each port is sinking. Per USB specification it should not exceed 500mA. Each MIC2012 can supervise up to two USB ports. When the limit is exceeded for more than 5ms, one of the FAULTn# signal will go off. The external logic based on the 74HC132D that can be seen in Appendix B, the VT6202 Reference Schematics is then fed to either USBOC0# or USBOC1# inputs of the VT6202. For more detail on the operation of the MIC2012, please refer to its databook that can be found at www.micrel.com.

CHAPTER 3. PCI BUS AND USB LAYOUT AND ROUTING GUIDELINES

This chapter provides recommendations for VT6202 PCI bus layout and routing. This chapter also specifies how to achieve conditions that satisfy USB 2.0 high-speed layout guidelines.

3-1. Layout and Routing Guidelines for PCI Bus Interface

Table 4 lists the layout recommendations for PCI traces on a VT6202 PCI USB 2.0 add-in card.

Signal type	Trace width range(mil)	Maximum Trace (inch)
PCI Bus	5~8	2
PCI CLK	15~20	2.5 (Fixed)

Table 4. PCI Trace Recommendations

Figure 10 shows the PCI reference layout. All traces for the PCI bus are on the component layer.

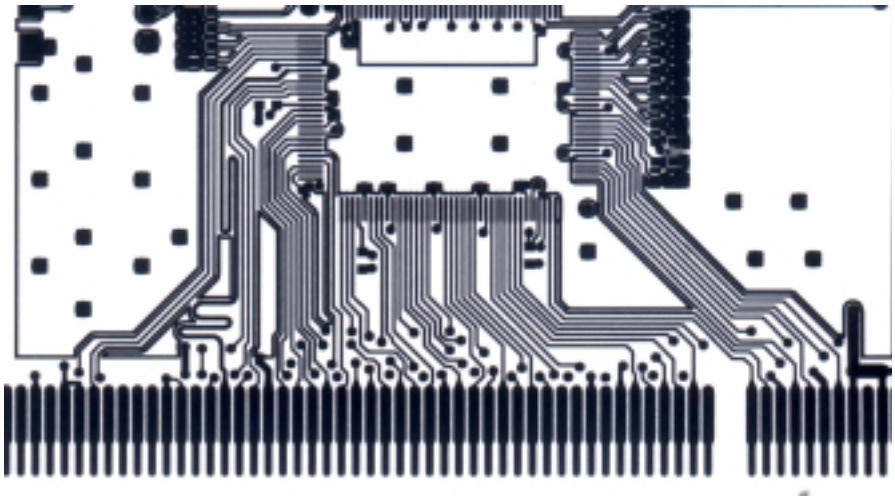


Figure 10. PCI Reference Layout

3-2. Layout and Routing Guidelines for High-Speed USB Differential Signals

It is desired to achieve 90Ω ±10% differential impedance for high-speed data transactions. First, the impedance of the Printed Circuit Board should be regulated at 45Ω ±15% (see Chapter 2). Second, it is strongly recommended that high–speed USB differential signals layout guidelines be followed.

Figure 11 shows the trace width and spacing between the plus (DP) and minus (DM) signals of one pair of USB differential signals. This layout rule should be maintained from the VT6202 to the USB receptacle to reduce the change of impedance. The allowed length range is from 4 to 18 inches.

Figure 11. USB Differential Signal Routing

USB differential signal traces should be referenced to the ground layer. Avoid laying USB signal traces near or under capacitors, inductors (ferrite beads), or power / crystal traces. Reduce the number of vias as much as possible. Keep a clear space for USB signals without copper from the VT6202 to the USB receptacle. In PCI add-in card designs, maintain traces of USB signals on a single power or ground plane, the preferred ground (power) plane is AGND (AVCC5), and avoid crossing different ground (power) planes. The minimum space between two pairs of USB signals is 20 mils. The minimum space is also 20 mils from other low speed signals or power traces to USB differential signals. The minimum space from other high speed signals or clock signals is 50 mils. Route the plus and minus signals the same length as close as possible. The length difference between plus and minus signals should be shorter than 150 mils.

Figure 12 shows placement and layout recommendations for the USB 15kΩ pull-down resistors. Place the resistors near the USB receptacle and directly on the USB signal traces. Avoid routing branching traces on the plus or minus USB differential signals.

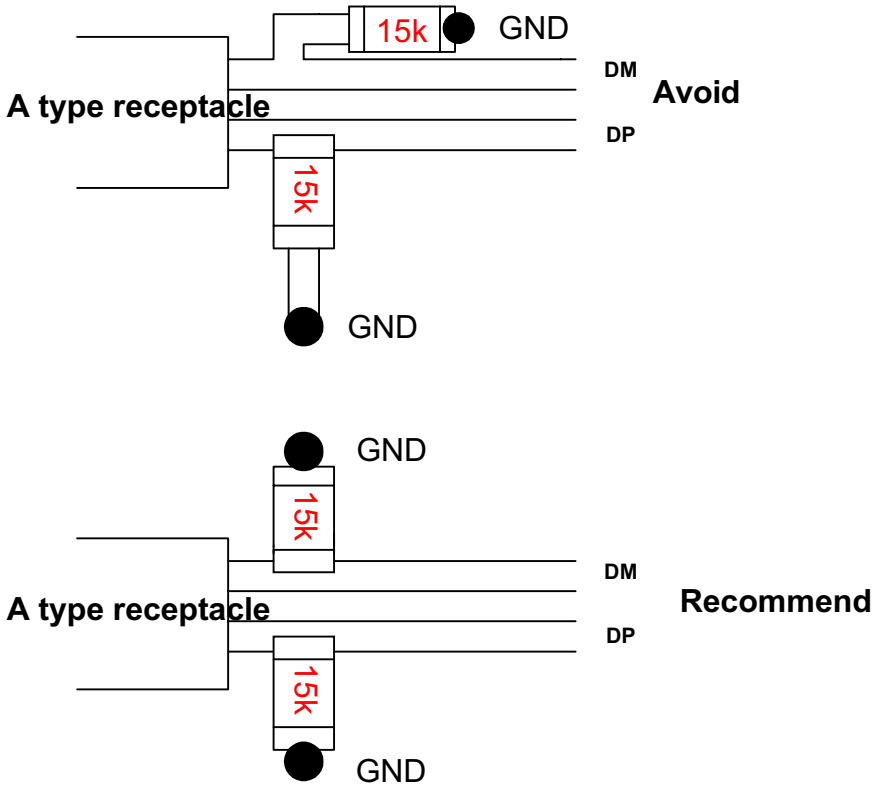


Figure 12. Pull-Down Resistor Placement and Layout Recommendations

Figure 13 shows general USB differential signal layout and routing recommendations. Maintain plus (DP) and minus (DM) signal traces a fixed distance apart (same distance apart as the width of the trace) from the VT6202 to the USB receptacle. Use two 45° corners or an arc to instead of one 90° corner

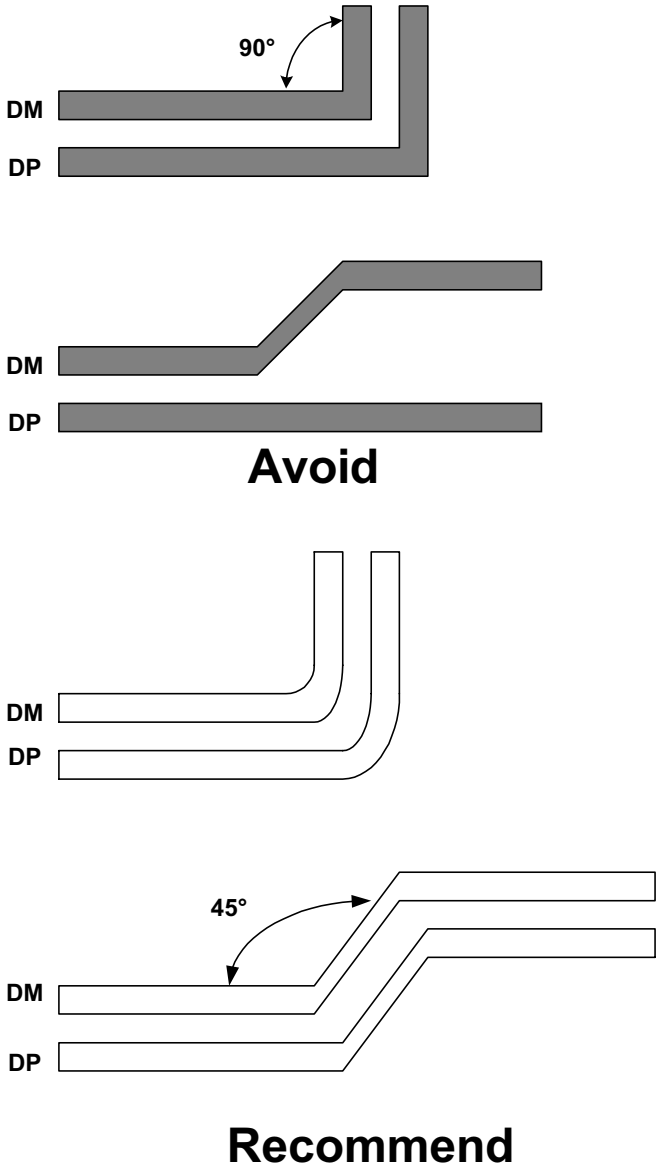


Figure 13. USB Differential Signal Layout and Routing Guidelines

3-3. Layout and Routing Guidelines for Crystal

The VT6202 needs a crystal to provide a 24.000MHz clock. The recommended crystal is TXC 24MHz±20ppm. Table 5 lists the trace recommendations for XI and XO.

Trace Width	Trace Length	Length Difference
10~20 mils	400~650 mils	0~130 mils

Table 5. Trace Recommendations for XI & XO

3-3. Layout and Routing Guidelines for Other Pins

External Resistor

Two series resistors (5.1kΩ 1% and 1.02kΩ 1% for a total of 6.12KkΩ 1%) should be placed between REXT (Pin 88) and GNDUSB (Pin 87) to generate a reference current. The reference layout is shown in Figure 14.

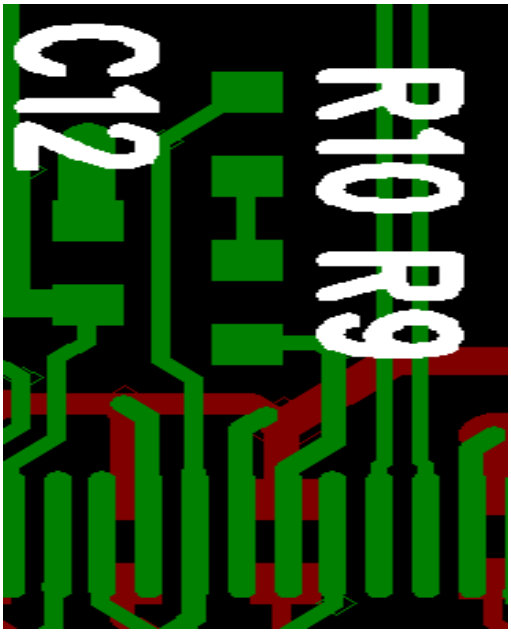


Figure 14. REXT Pin Reference Placement

Pull-Down and Pull-High Pins

Table 6 and Table 7 below list the pins that should be pulled down to the ground and pulled high with resistors respectively.

Resistor Value	Pin Number
4.7kΩ	55, 57, 58, 59, 65, 66, 99

Table 6. Pull-Down Resistors

Resistor Value	Pin Number
4.7kΩ	60, 63, 97, 102, 103, 104

Table 7. Pull-High Resistors

USB Wake-Up Function Enable / Disable Jumpers

Pin 98 is the strap pin for enable/disable of the USB Wake-Up function. Figure 15 shows the Jumper setting.

1-2: Enable Wake-up function

1-3: Disable Wake-up function

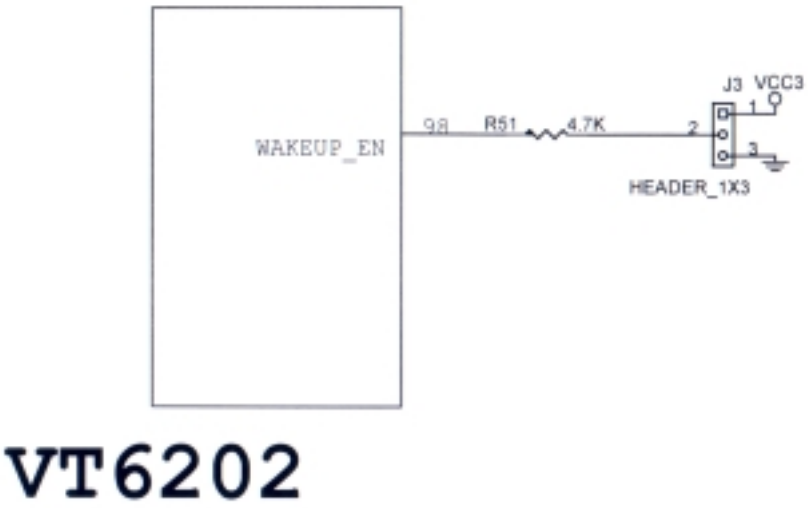


Figure 15. WAKEUP_EN Jumper

AVCC3 Voltage Selection Jumpers

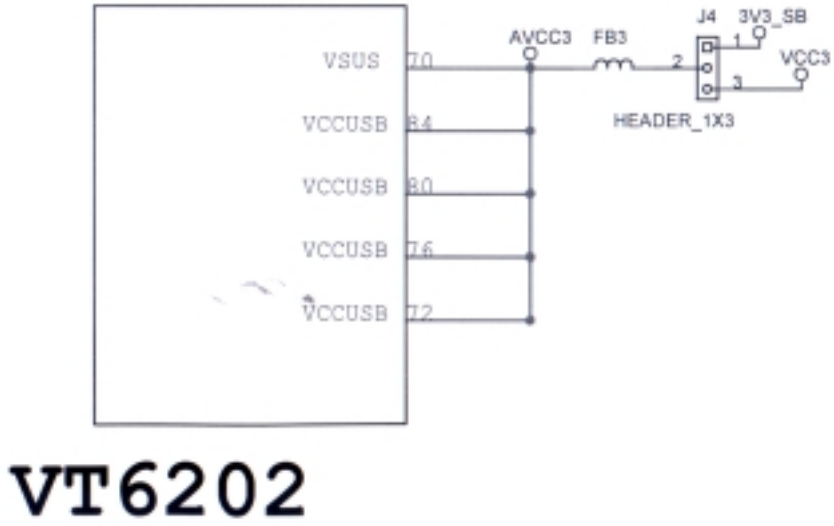


Figure 16. AVCC3 Jumper

To support enable / disable of the wake-up function, a 1x3 jumper may be used to switch the source of AVCC3. Figure 16 shows the power switch setting for AVCC3. Setting 1-2 means AVCC3 is supplied from suspend 3.3V for support of the USB wake-up function; setting 2-3 means AVCC3 is supplied from VCC3 that doesn't support the wake-up function.

System Management Interrupt

The SMI# (System Management Interrupt) pin is for legacy function support. In the PCI USB 2.0 add-in card case, the function is not supported because there is no SMI# signal from the PCI slot. So SMI# interrupts are supported only when the PCI USB 2.0 chip is used on the motherboard. The SMI# pin is connected to the SMI# signal of the CPU. The system BIOS must contain support for this function for it to work properly.

CHAPTER 4. DESIGN CHECKLIST

4-1. PCI

Pin Name	Check Items	Range
AD32~AD0	Trace length Trace width	≤ 2 inches 5~8 mil
CBE3#~CBE0#	Trace length Trace width	≤ 2 inches 5~8 mil
INTA#~INTB#	Trace length Trace width	≤ 2 inches 5~8 mil
IRDY#,TRDY#	Trace length Trace width	≤ 2 inches 5~8 mil
SMI#,PME#	Trace length Trace width	≤ 2 inches 5~8 mil
PCIRST#	Trace length Trace width	≤ 2 inches 5~8 mil
IDSEL#,DEVSEL#	Trace length Trace width	≤ 2 inches 5~8 mil
STOP#	Trace length Trace width	≤ 2 inches 5~8 mil
PAR#	Trace length Trace width	≤ 2 inches 5~8 mil
REQ#,GNT#	Trace length Trace width	≤ 2 inches 5~8 mil
PCICLK#	Trace length Trace width	Fixed 2.5 inches 15~20 mils

4-2. Power and Ground

Item	Description
Power Plane	Is the power plane partition separated into VCC3 and AVCC3?
Ground Plane	Is the ground plane partition separated into GND and AGND?
USB Port Power Supply	Does it have the ability to supply 500mA to each port and 0.5mA in power-down, STR, and STD conditions?
AVCC3	Is the total trace width ≥ 25 mils?
AVCC3	Is the power source suspending power that supports the USB wake-up function?
AVCC2_5	Is the total trace width ≥ 10 mils?
VCC2_5	Is the total trace width ≥ 10 mils?

4-3. High Speed USB Differential Signals

Is the impedance of the PCB regulated at 45Ω ±15%?
Is the differential impedance regulated at 90Ω ±15%?
Are the USB differential signal traces near or under capacitors, inductors (ferrite beads), or power or crystal traces?
Is there a clear space for USB signals without copper from the VT6202 to the USB receptacle?
Are the traces of the USB differential signals referenced to the ground layer?
Are the traces of the USB differential signals referenced to a single power or ground plane?
Is the length difference between USB plus and minus differential signals shorter than 150 mils?
Are the plus and minus signals of each USB differential signal pair maintained a fixed distance apart from the VT6202 to the USB receptacle?
Are the plus and minus signals of each USB differential signal pair routed using 45° corners or arcs instead of 90° corners?
Have the USB differential signal traces been routed with the minimum number of vias?

APPENDIX A - VT6202 REFERENCE DESIGN BILL OF MATERIALS

Bill of Materials (BOM) for VT5642D

Component Side SMD

Qty	Reference	Description
2	C12, C13	SMD-CAP 20pF (0603)
1	C41	SMD-CAP 39pF (0603)
5	C15, C17, C25, C31, C33	SMD-CAP 103pF (0.01u) (0603)
12	C9, C10, C11, C14, C16, C26, C32, C39, C40, C43, C44, C45	SMD-CAP 104pF (0.1u) (0603)
5	CT1, CT2, CT11, CT14, CT15	SMD-CAP 106pF (10u) (1206)
2	CT12, CT13	SMD-CAP 226pF (22u) (1210)
4	R28, R29, R30, R46	SMD-R 470 (0603)
1	R71	SMD-R 510 (0603)
1	R72	SMD-R 820 (0603)
1	R50	SMD-R 1.5K (0603)
1	R27	SMD-R 3K (0603)
13	R11, R12, R13, R14, R15, R63, R65, R73, R74, R75, R76, R77, R78	SMD-R 4.7K (0603)
8	R34, R35, R36, R37, R38, R39, R40, R41	SMD-R 15K (0603)
1	R68	SMD-R 150K (0603)
1	R67	SMD-R 200K (0603)
1	R66	SMD-R 499 (0603) 1%
1	R10	SMD-R 1.02K (0603) 1%
1	R9	SMD-R 5.1K (0603) 1%
1	R69	SMD-R 49.9K (0603) 1%
8	FB14, FB15, FB16, FB17, FB18, FB19, FB20, FB21	SMD-FB 60Ω (0805)
8	FB1, FB2, FB4, FB5, FB7, FB12, FB13, FB23	SMD-FB 52Ω (1206)
1	D1	SMD RB160L-40
1	U12	SMD AMS1117 (SOT223)
1	U2	SMD AMS1117-2V5 (SOT223)
1	U5	SMD-TTL 74HC132D (SOIC14)
4	CT5, CT6, CT7, CT8	SMD-ECAP 100uF/10V
2	U4, U6	SMD MIC2012 (SOIC8)
1	L1	SMD 6.8uH (0805)
4	L2, L3, L4, L5	SMD DLW21SN900SQ2
1	U9	SMD LM2621 (mini-so8)
1	U1	SMD VT6202 (PQFP128)

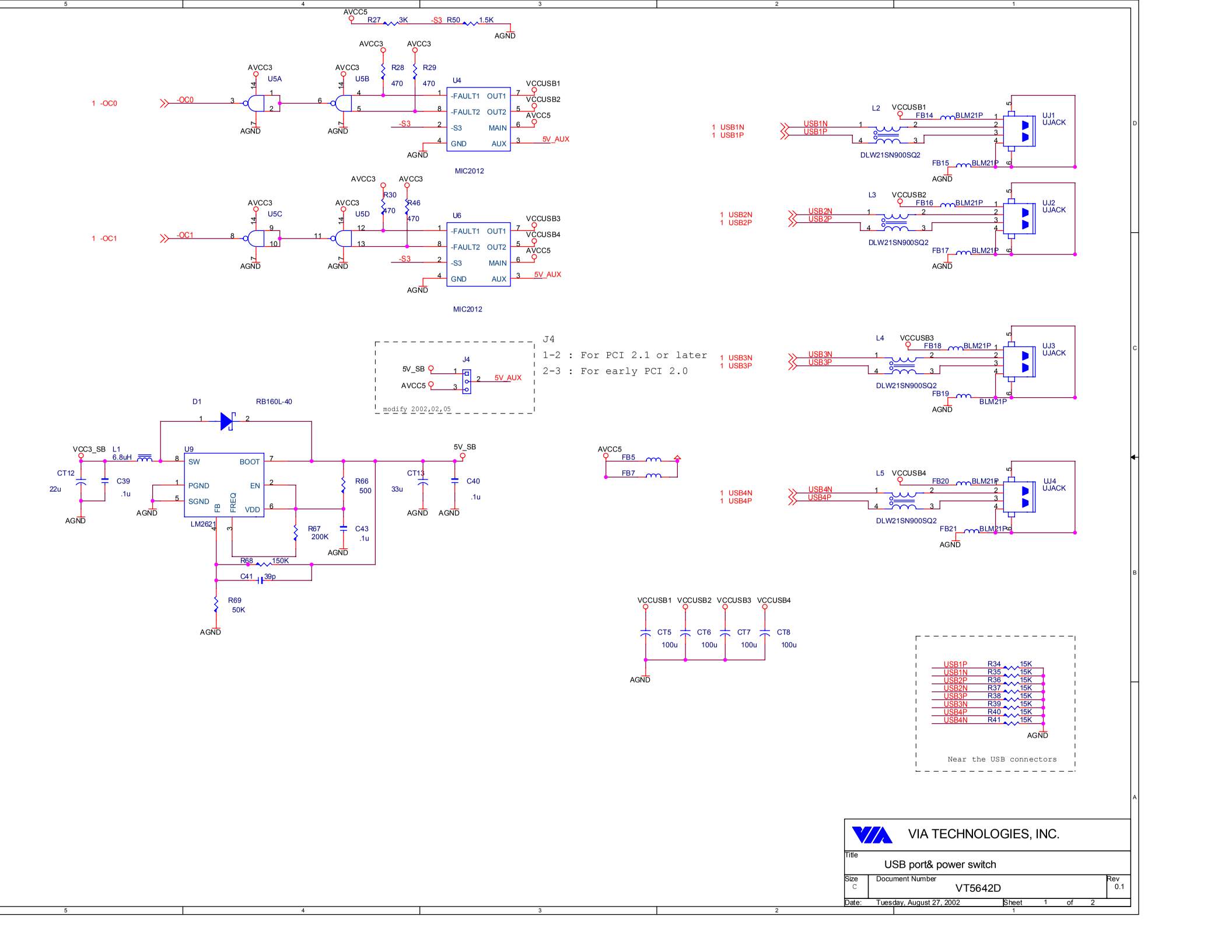
Solder Side SMD

Qty	Reference	Description
1	C29	SMD-CAP 103pF (0.01u) (0603)
10	C20, C21, C22, C23, C28, C34, C35, C36, C37, C38	SMD-CAP 104pF (0.1u) (0603)

DIP

Qty	Reference	Description
1	XTAL1	XTAL 24MHZ (TXC)
4	J2, J3, J4, J5	Header 1x3P
4	UJ1, UJ2, UJ3, UJ4	CONN USB JACK 4P

APPENDIX B - VT6202 REFERENCE DESIGN SCHEMATICS



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Title	USB port& power switch	
Size C	Document Number VT5642D	Rev 0.1
Date: Tuesday, August 27, 2002	Sheet 1 of 2	

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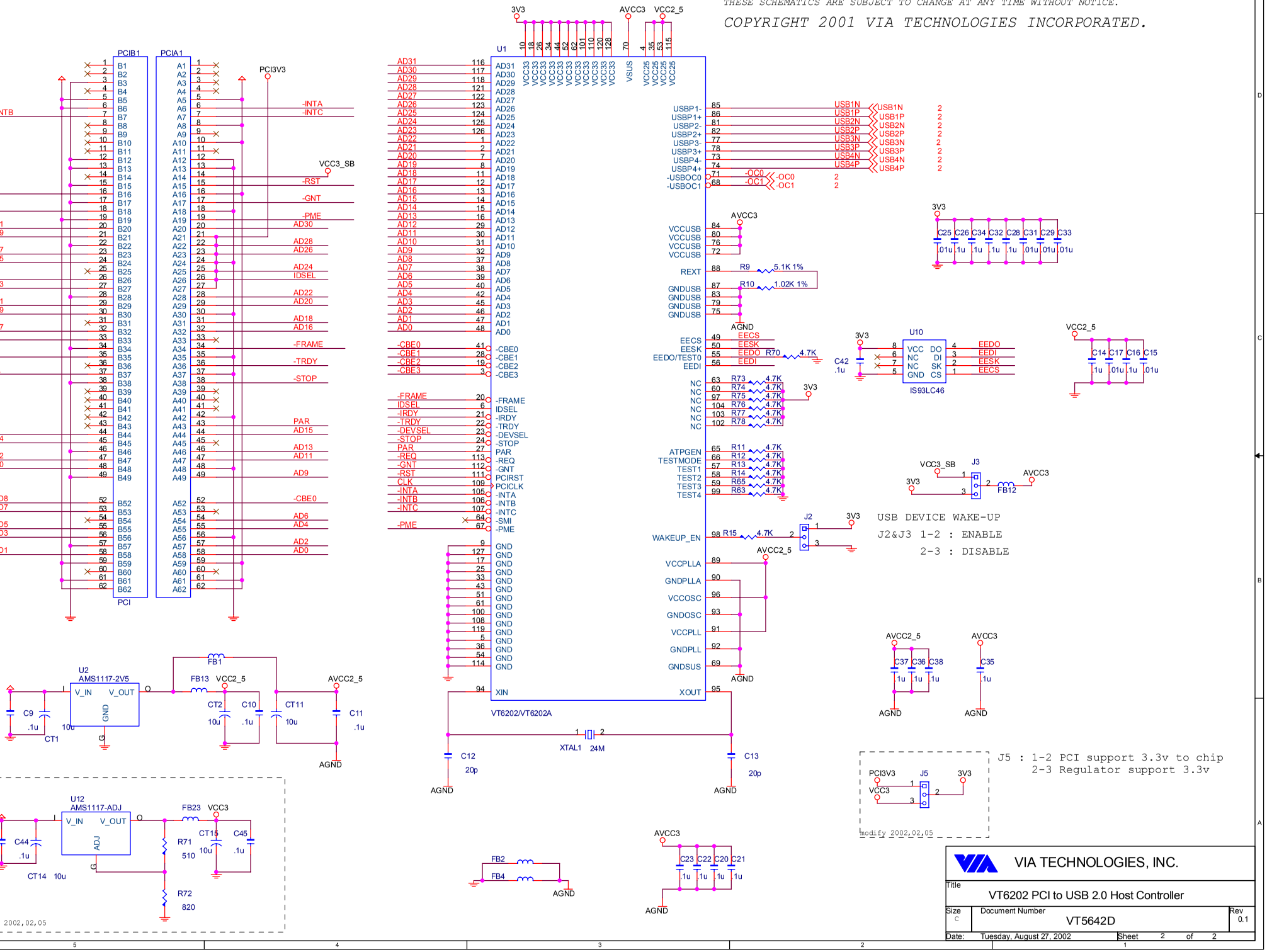

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Title	VT6202 PCI to USB 2.0 Host Controller
Size: C	Document Number: VT5642D
Rev: 0.1	
Date: Tuesday, August 27, 2002	Sheet 2 of 2