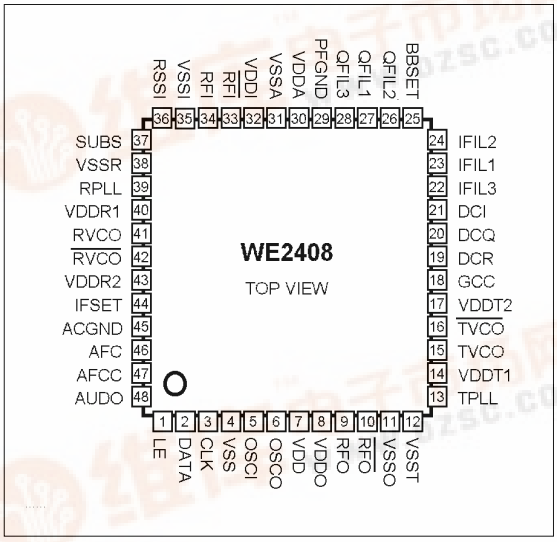
WiNEDGE & WiRELESS

Winceiver WE2408

2.4GHz Single Chip FM Transceiver

FEATURES

- 2.4GHz Operating Frequency
- 2.7 - 3.3V Operation
- -2 dBm Tx Output Power
- -99 dBm Rx Sensitivity
- Full Duplex
- Dual VCO
- FM/FSK Modulator
- No Tuning "Tankless" FM Demodulator
- Direct-Conversion, Zero-IF Architecture
- Low External Component Count
- Serial Programming Interface
- Low Standby Current
- Thin-Quad Flat Package (TQFP-48)



DESCRIPTION

WE2408 are single-chip FM/FSK transceiver ICs operate in 2.4GHz ISM band. Utilizing a unique direct-conversion, zero-intermediate frequency (zero-IF) receiver architecture, WE2408 provides radio designers a high performance RF transceiver solution with low external component count and small PCB footprint.

The receiver section of the WE2408 provides all of the required receiver functions including local oscillator synthesis (VCO), down-conversion, filtering, automatic gain control (AGC), automatic frequency control (AFC), FM/FSK demodulator and RSSI functions.

The transmitter section contains a directly modulated VCO and RF power amplifier (PA).

Internal, dual, high-performance phase locked loop (PLL) synthesizers/VCOs allow full duplex or half-duplex operation over the entire RF tuning range. Tuning, power management, and gain control (manual) functions are accomplished via serial interface.

APPLICATIONS

- 2.4G Wireless Voice/Data Products
- 2.4GHz Cordless Phones
- AMR/Telemetry/Data Radios

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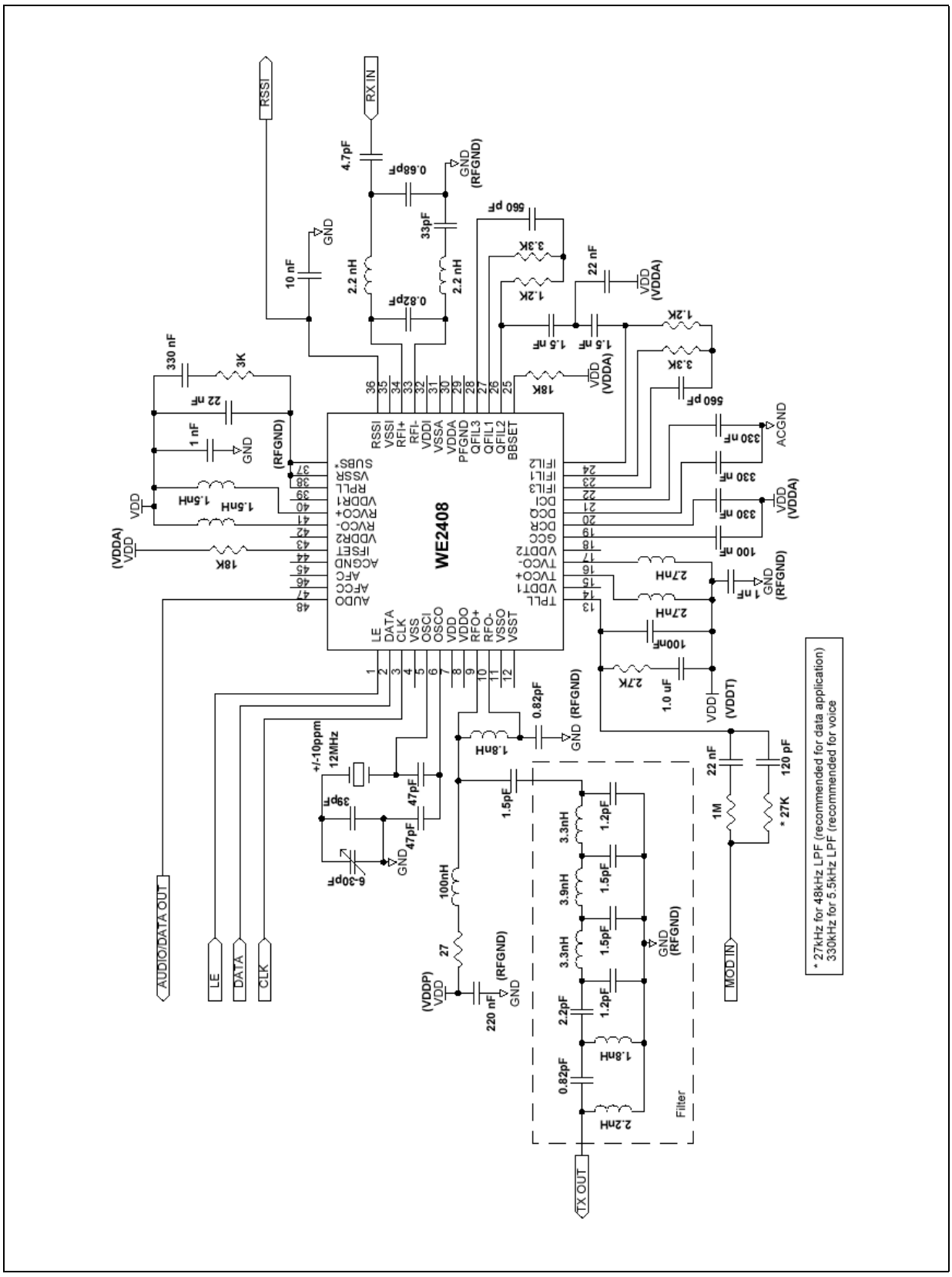
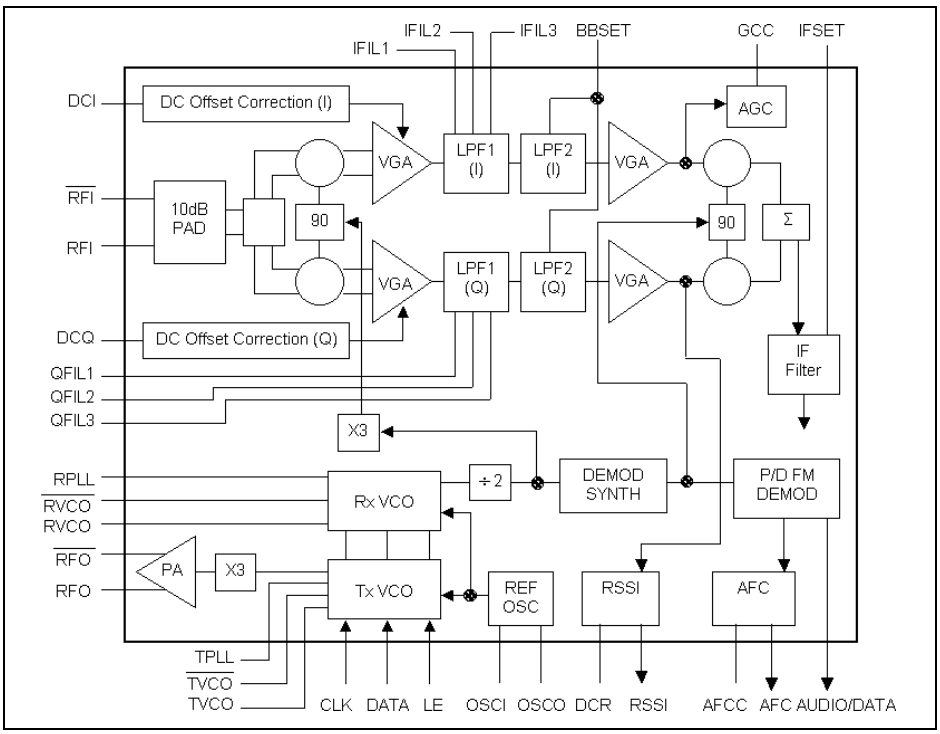
TABLE OF CONTENT

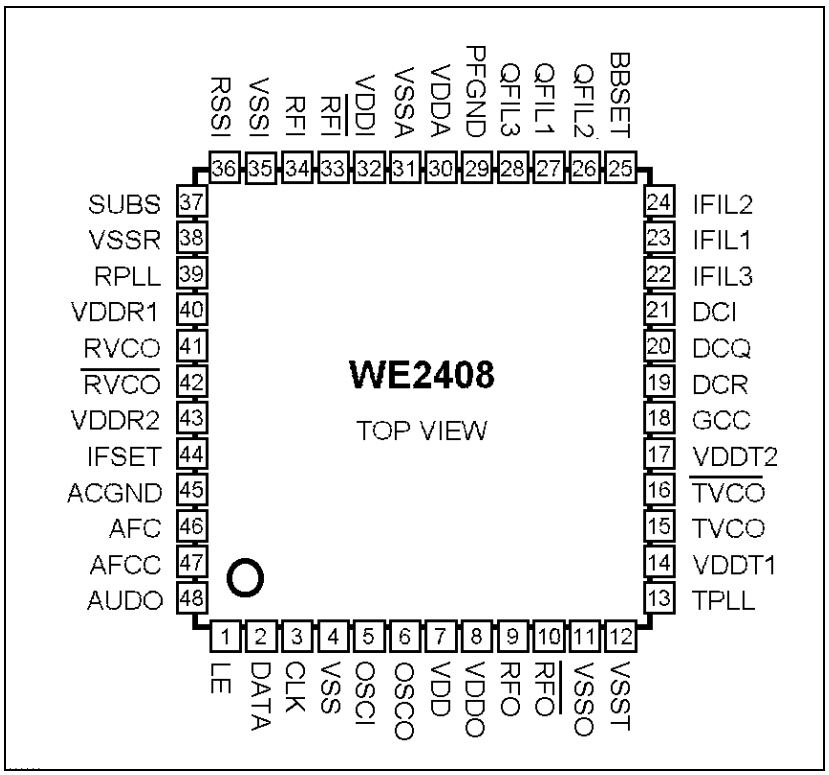
SIMPIFIED 2.4GHZ APPLICATION CIRCUIT



BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTIONS

Name	Pin	Description
LE	1	Load Enable. Active high CMOS logic compatible input
DATA	2	Serial Data. CMOS logic compatible serial data input
CLK	3	Serial Clock: CMOS logic compatible, positive edge trigger input
VSS	4	Digital ground. Ground pin for the internal CMOS digital circuitry
OSCI	5	Reference Oscillator Input. Signal level should be within the range of 200-400mV peak
OSCO	6	Reference Oscillator Output. Used in conjunction with OSCI to form a Colpitts oscillator using a crystal unit
VDD	7	Power supply for the internal CMOS digital circuitry
VDDO	8	Power supply for Tx output section (PA)
$\overline{\text{RFO}}$ RFO	9 10	Differential Tx Outputs
VSSO	11	Ground for Tx output section
VSST	12	Ground for Tx VCO
TPLL	13	Tx PLL control voltage. Connection point for PLL loop filter.
VDDT1,2	14, 17	Tx power supply pins for the internal Tx VCO
$\overline{\text{TVCO}}$ TVCO	15 16	Tx VCO Tank; establishes the natural oscillation frequency of the Tx VCO with external balanced inductors
GCC	18	Gain control decoupling capacitor
DCR	19	DC Offset for RSSI
DCI, DCQ	21	DC Offset for I and Q sections of the baseband circuit
IFIL1,2,3	23, 24, 22	Baseband In-phase (I) Filter
BBSET	25	Baseband low pass filter frequency set resistor
QFIL1,2,3	27, 26, 28	Baseband Quadrature (Q) Filter
PFGND	29	Internal Pre-Filter ground reference
VDDA	30	Power supply for Baseband and IF filters
VSSA	31	Ground for Baseband and IF filters
VDDI	32	Power supply for Rx Input section
$\overline{\text{RFI}}$ RFI	34 33	Differential Rx Inputs
VSSI	35	Ground for Rx Input section
RSSI	36	Receive Signal Strength Indicator output
SUBS	37	Ground to silicon substrate
VSSR	38	Ground for Rx VCO
RPLL	39	Rx PLL control voltage. Connection point for PLL loop filter.
VDDR1,2	40, 43	Power supply for Rx VCO
$\overline{\text{RVCO}}$ RVCO	41 42	Rx VCO Tank:: establishes the natural oscillation frequency of the Rx VCO with external balanced inductors.
IFSET	44	IF low pass filter frequency set resistor
ACGND	45	Internal AC ground reference for the baseband and IF filters
AFC	46	Automatic Frequency Control Voltage Output
AFCC	47	Automatic Frequency Control Capacitor
AUDO	48	Rx Audio/ Digital Output

FUNCTIONAL DESCRIPTION

The receive section consists of several major function blocks, including a switchable RF input attenuator (PAD), quadrature down-conversion mixer, differential-to-single-ended conversion, variable gain amplifiers (VGAs), PLL synthesizer/ voltage controlled oscillator (VCO), I/Q low-pass filters, DC offset correction circuitry, quadrature up-conversion mixer, IF filter, P/D FM demodulator.

The transmit section consists of a PLL synthesizer, direct frequency modulated voltage controlled oscillator (VCO), and a RF power amplifier (PA).

Additionally, the device contains a reference crystal oscillator, an automatic frequency control (AFC) circuitry and associated reference frequency synthesizer.

A functional block diagram of the IC is shown in page 4. The following sections give details of each functional block.

ZERO IF RECEIVER

The receiver section of the WE2408 utilizes a quadrature mixer in a direct-conversion, zero-intermediate frequency (zero-IF) approach. After quadrature down-conversion and baseband filtering, a quadrature mixer up-converts the complex baseband signal to an intermediate frequency (IF) for demodulation.

Direct conversion to zero-IF has several advantages over super-heterodyne approaches. First, the image frequency is eliminated because the IF is zero. Second, the use of active, low pass, filters provide a high level of integration, while eliminating the need for external IF filters and IF transformers.

A description of each major receive function block follows:

RF Input Attenuator Pad

A switchable 0/-10dB attenuator pad allows high signal level capability at the RF Input of the receiver. This pad is located prior to the quadrature mixer (down-conversion) and can be either manually controlled via the 3-wire interface, or automatically controlled via the AGC section of the device.

Down-Conversion Quadrature Mixer

The main advantage of the quadrature mixer is its ability to translate the RF frequency directly to a zero-IF, thereby eliminating the image frequency. Consequently, the image filter before the RF input to the WE2408 can be eliminated. The design requirements for the duplexer and RF band pass filter may also be relaxed. In addition, the quadrature mixer achieves a lower overall noise figure by virtue of image frequency elimination.

The balanced mixers in the quadrature mixer are designed to closely track each other in both amplitude and phase response. The quadrature LO signal is generated by direct division of the receive VCO, thereby eliminating external phase shifting networks. Furthermore, for improved noise immunity, all internal RF signal paths are fully differential, thereby providing common mode noise rejection. The gain of the mixer can be adjusted via the 3-wire interface programming or automatically controlled by AGC.

Receive PLL Synthesizer and VCO

The receive PLL synthesizer with voltage controlled oscillator (VCO), is designed to provide a low phase noise local oscillator. The Rx VCO operates in a balanced mode at 1.5x the Rx local oscillator frequency. The VCO frequency is immediately divided by a factor of 2 and then multiplied by 3 to provide the local oscillator for the quadrature down-conversion mixer. The synthesizer is 17 bits in total (excluding the proceeding divide by 2). These 17 bits are split into 14 bits to provide the input to the PLL phase detector to be compared with the reference frequency, with an additional 3 bits providing fractional-n capability, to allow channel frequency definition in steps of 1/8 of the PLL reference frequency.

This LO signal also drives the receive synthesizer and demodulator synthesizer.

The Rx VCO center frequency is determined by an external tank circuit comprised of an external, center-tapped, inductor. The tank circuit is connected to pin 41 and 42.

An external PLL loop filter network, connected to the RPLL pin (pin 39), filters the VCO control voltage. This control voltage is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair. The receive frequency for the WE2408 is programmed via serial interface (Data, Clock, and Load Enable).

Demodulator synthesizer

This synthesizer consists of programmable and fixed dividers which determine the IF frequency and the demodulator bandwidth of the digital FM demodulator. The demodulator synthesizer is controlled by 3 PDR bits of the reference frequency register, programmable via serial interface. The demodulator bandwidth is programmable between 150kHz and 25kHz.

Variable Gain Amplifiers

The gain of the receiver can be dynamically adjusted via the serial interface to maintain signal linearity before the demodulator. This enables the achievement of high values of SINAD for an analog FM link. An Automatic Gain Control (AGC) function is also available on-chip. The gain can be adjusted in 3 locations along the receive path:

- A 10dB RF pad before the down-conversion quadrature mixer
- Four step baseband attenuators in the down-conversion quadrature mixer load circuits
- Three-step baseband Variable Gain Amplifiers after the baseband I and Q low pass filters

In addition, each VGA provides differential to single-ended conversion and amplification of the baseband signal, prior to the I/Q low-pass filters. These gain stages are referenced to pre-filter ground (PFGND), an internally generated virtual ground.

LPF1 (I/Q)

This first stage of the I/Q baseband low pass filter (LPF) section consists of active, Sallen-key type filters. These filters provide a combination of low noise figure and gain along with a wide dynamic input range. The purpose of these filters is to provide preliminary rejection of the out-of-band interferences. The reduction of out-of-band interferer levels, reduce the dynamic range requirements for the following filter stages in LPF2. The –3dB corner frequency of these LPFs are set via external RC values.

LPF2 (I/Q)

This second stage of the I/Q baseband low pass filter (LPF) section consists of active, transconductance (gm) type filters. Combined with LPF1, these filters provide the required channel selectivity by passing the entire desired frequency spectrum, while attenuating noise and adjacent channel interference outside of the desired signal's bandwidth.

DC Offset Correction

A proprietary DC offset correction circuit is used to control DC offset voltages. The use of DC offset correction improves dynamic range, minimizes LO feed-through in the up-conversion mixer, and reduces signal distortion. The correction circuit operates automatically and in a continuous mode.

Up-Conversion Quadrature Mixer

The zero-IF, complex, filtered baseband signal is translated by the quadrature up-conversion mixer to an intermediate frequency (IF). The resultant up-converted IF signal is low enough in frequency to provide adequate SNR at the output of the period-to-digital FM demodulator, yet high enough to satisfy signal sampling criterion.

IF BPF

The band pass filter, after the quadrature up-conversion mixer, passes the IF signal and rejects the harmonic components of the up-conversion mixer's local oscillator. The IF band pass filter is comprised of cascaded, active, transconductance filters with Butterworth response characteristics. The lower corner frequency of the IF BPF is fix at 8kHz. The higher corner frequency of the filter is determined by an external resistor connected to IFSET pin.

RSSI

The receive signal strength indication (RSSI) circuitry incorporates a log amplifier and detector for the purpose of measuring the received RF carrier power level.

Period-to-Digital FM Demodulator

The Period-to-Digital (P/D) FM demodulator digitize the half-cycle period of the IF signal and convert that information into the demodulated FM audio signal via a digital to analog converter.

The digitizing clock signal for the P/D is derived from the Rx VCO oscillator and the P/D divide ratio (PDR). The PDR is programmable via serial interface.

TRANSMITTER

The transmitter section of the WE2408 is comprised of a modulation input circuit, a PLL synthesizer / VCO, and a RF power amplifier (PA) capable of providing -4.0 dBm into a 50Ω load. A description of each major function block follows:

Transmit PLL Synthesizer and VCO

The transmit (Tx) on-chip PLL synthesizer is identical to the receive PLL synthesizer except that it contains only a 3 x multiplier after its VCO. The transmit VCO frequency is therefore 1/3 the transmitter local oscillator.

The transmit PLL accepts modulation audio to provide a frequency modulated (FM) RF carrier. Utilizing a direct modulation approach, the modulation voltage is directly applied to the PLL loop filter.

The VCO center frequency is determined by an external tank circuit comprised of two inductors connected to the TVCO pins 15 and 16. An external PLL loop filter network, connected to TPLL, pin 13, filters the VCO control voltage. This control voltage (K_{VCO} 23 MHz/V for 800MHz) is used to tune the tank frequency of the VCO via an internal, common-anode, varactor pair.

The transmit frequency for the WE2408 is programmed via serial interface (Data, Clock, and Load Enable).

PA

The on-chip RF power amplifier is a differential gain stage capable of transmitting RF output power up to -4dBm.

The differential output impedance is ~ -19Ω//1pF at 2.4GHz. In the simplified application circuit shown in page 3, a discrete LC network is used to match the output impedance to 50Ω at 2.4GHz ISM band. The 27Ω resistor set the output power to ~ -4dBm.

REFERENCE OSCILLATOR

Crystal Oscillator and Reference Synthesizer

The reference synthesizer is comprised of an 11 bit counter which provides the PLL reference frequency for both the receiver and transmitter synthesizers. A crystal oscillator circuit normally provides the input to the reference synthesizer; however, external frequency source can be used as a reference for the synthesizer. All 11 bits of the synthesizer are fully programmable, to allow a large degree of flexibility in the choice of either the reference crystal or external reference frequency.

This reference oscillator can be kept active when both Tx and RX are off, by programming the Mode Register, hence, reduce turn-on time for Tx or Rx.

AFC

Automatic Frequency Control (AFC) of the receive local oscillator (LO) frequency is used to improve receiver performance. Without AFC, frequency offset (between receive signal and LO) causes a reduction in SINAD due to filter distortion and beat tone. The AFC minimized the offset by tuning the reference crystal oscillator. As a result, both transmit frequency and the receive LO are corrected at the same time.

The AFC correction signal is available as a DC current at the AFC output (pin 46). A varactor, connecting to the AFC output and the reference crystal, provides the required tuning action.

See section on AFC for more details.

OPERATION LIMITS

PARAMETER	MIN	MAX	UNITS
Power Supply Voltage	2.7	3.3	Vdc
Operating Temperature	-10	60	C
Frequency of Operation	2400	2485	MHz
Reference Frequency	5	20	MHz

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the specifications refer to performance of the typical 2400-2483.5MHz application circuit shown in page 3, with the following conditions:

Supply voltages	= 3.0V	Temperature	= 25°C
Reference Oscillator	= 12MHz	Reference Frequency	= 100kHz
Channel Bandwidth	= 150kHz (PDR=9)	Channel Spacing	= 300kHz
Modulation Frequency	= 1kHz	FM deviation	= 40kHz

PARAMETER	MIN	TYP	MAX	UNITS
DC				
Supply Current (Receive Only)		46	48	mA
Supply Current (Transmit Only)		37	40	mA
Supply Current, Total (Rx + Tx)	75	83	87	mA
Standby Current			5	uA
Receiver				
Input Sensitivity (12dB SINAD) [1]	-97	-99	-101	dBm
Input Sensitivity (57.6kbps, 10^{-3} BER) [2]	-81	-83	-85	dBm
Input Impedance (across RFI pins)		26Ω series with 0.9nHF		
Maximum RF Input (12dB SINAD) [1, 4]		+15		dBm
Input IP3 [3]		-1		dBm
Input 1dB Compression Point [4]	-20	-18		dBm
Receiver Channel Bandwidth [5]		150		kHz
Adjacent Channel Rejection	55	60	65	dB
RSSI Voltage Range (-100 to +6dBm) [3]	0.1		2.0	Vdc
RSSI Conversion Factor (Log) [3]	-15	-18	-21	mV/dB
RSSI Detection Range (Min-Max) [3]	-100		+6	dBm
Audio Output Level [1]	210	250	290	mVrms
Demodulation Frequency Range	0.15		50	kHz
Audio Output Impedance at Pin 48	2		10	kΩ
SINAD (at –80dBm) [1]	40	43		dB
Distortion (at –80dBm) [1]		0.8	2	%
Demodulation S/N (at -80dBm) [1]	39	42	45	dB
AFC Correction Range [10]		+/-20		kHz
AFC Center Frequency Tolerance		0.5	2	kHz

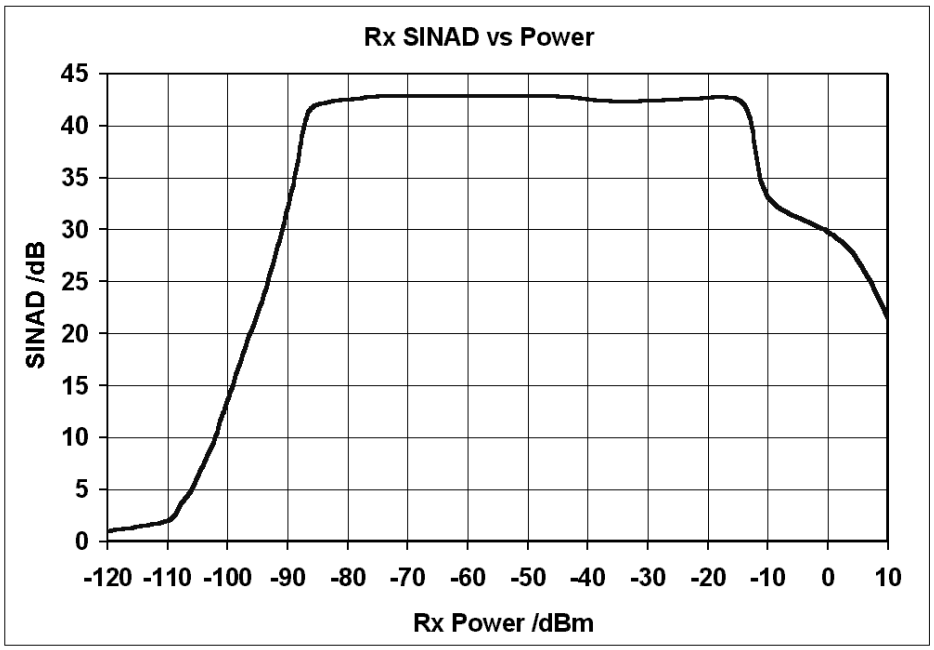
PARAMETER	MIN	TYP	MAX	UNITS
Transmitter				
Transmitter Output Power [6]	-4	-2	0	dBm
Spur Level: LO		-70	-60	dBc
LO x 2		-63	-55	dBc
LO x 4		-63	-55	dBc
LO x 5		-84	-70	dBc
TX x 2		-90	-80	dBc
Modulation Input Level [7]		160		mVrms
Modulator Input Impedance	1		2	kΩ
Output Impedance (across RFO pins)		-19Ω//1pF		
Modulation S/N [8]	38	40	45	dB
Intermodulation Prod. (2*RxLO-TxLO)		-58		dBc
Intermodulation Prod. (Other)			60	dBc
Phase Noise (10kHz Offset)		-75	-70	dBc/Hz
Phase Noise (10MHz Offset)		-110		dBc/Hz
Response Time				
RSSI Settling Time		0.5	1.0	ms
Rx PLL Lock Time [9] : Start Up		2		ms
Adjacent Channel		1.4		ms
Audio/Data Response Time [11] (from PLL locked to signal appears on AFO pin)		1	2	ms
Tx PLL Lock Time [9] : Start Up		8		ms
Adjacent Channel		5		ms

[1] CCITT receive audio filter
[2] 57.6kbps 511 PRBS, Data mode
[3] AGC off; receiver gain maximum
[4] AGC on or receiver gain minimum
[5] Bandwidth can be adjusted between 12kHz and 160kHz by external components
[6] Transmitter output power can be adjusted via an external bias resistor
[7] Input level to obtain 40kHz FM deviation. This input level is TPLL setting dependant
[8] Measured with 300Hz HPF, 3kHz LPF and 750us de-emphasis
[9] Lock time adjustable by PLL loop filters. Tx Charge Pump: 0.2mA; Rx Charge Pump: 1.0mA
[10] With varactor capacitance varies from 25pF(0.1V) to 10pF (2.5V). Refer to section on AFC
[11] Shorter time can be achieved by reducing DCI/DCQ capacitors.

Receiver Performance (Analog Mode)

Receiver performance of 2400-2483.5MHz application circuit shown in page 3,

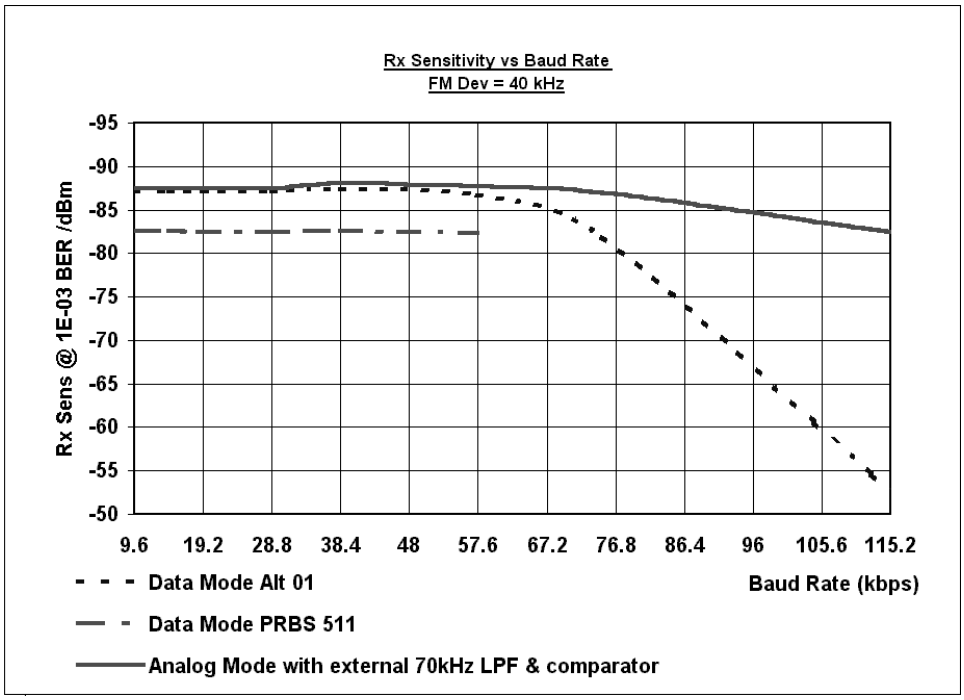
Supply voltages	: 3.0V	Channel Bandwidth	: 150kHz
Modulation Frequency	: 1kHz	FM deviation	: 40kHz (peak)
AFC	: OFF	AGC	: On

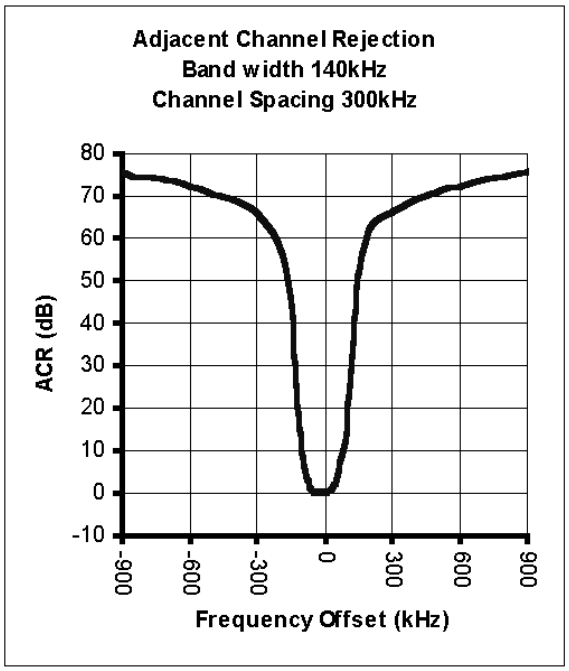


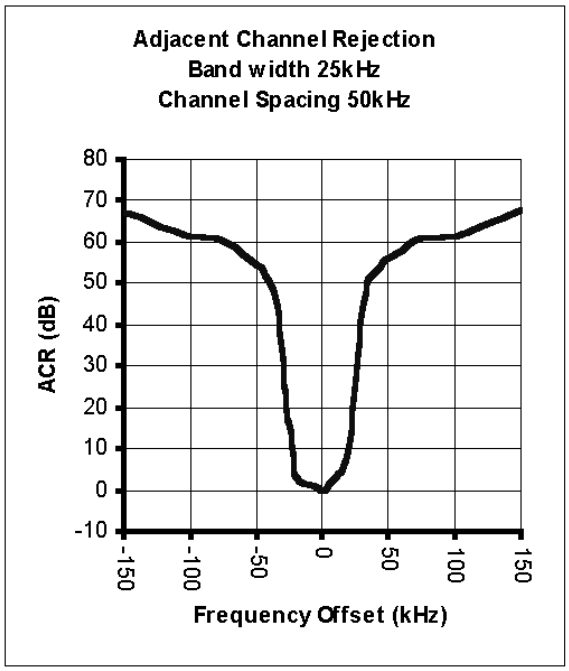
Receiver Performance (Digital Mode)

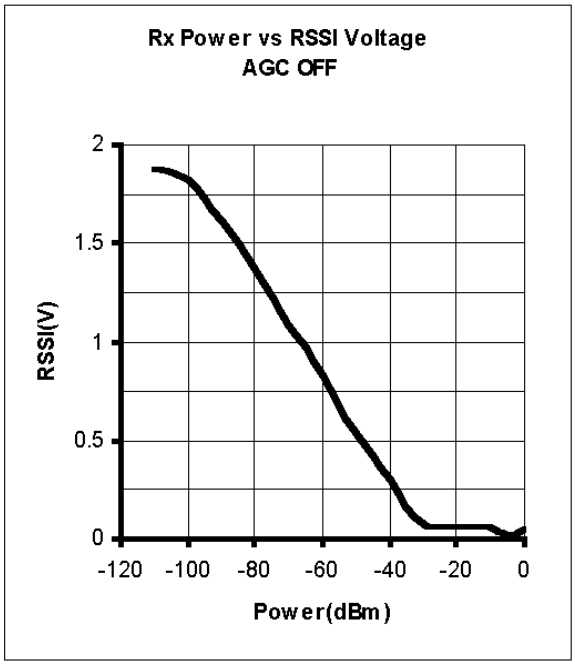
Receiver performance of 2400-2483.5MHz application circuit shown in page 3,

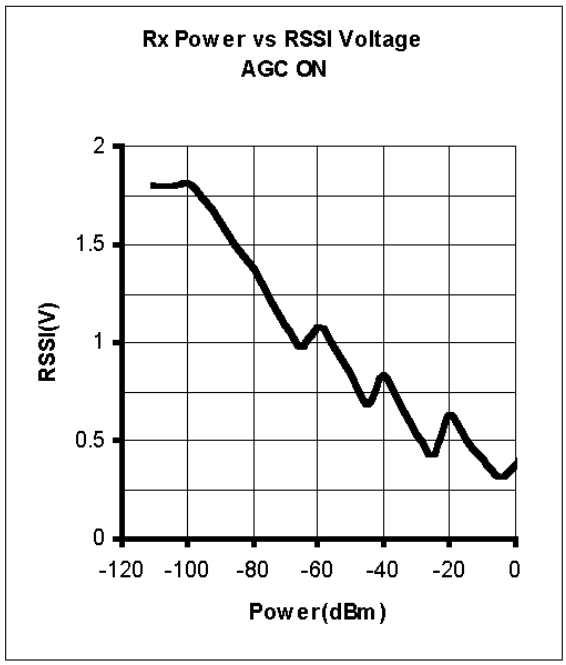
Supply voltages	: 3.0V	Channel Bandwidth	: 150kHz
FM deviation	: 40kHz (peak)		
AFC	: OFF	AGC	: On

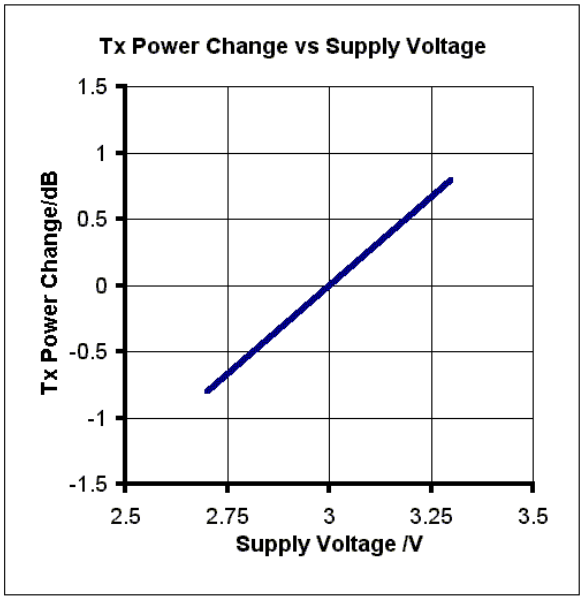


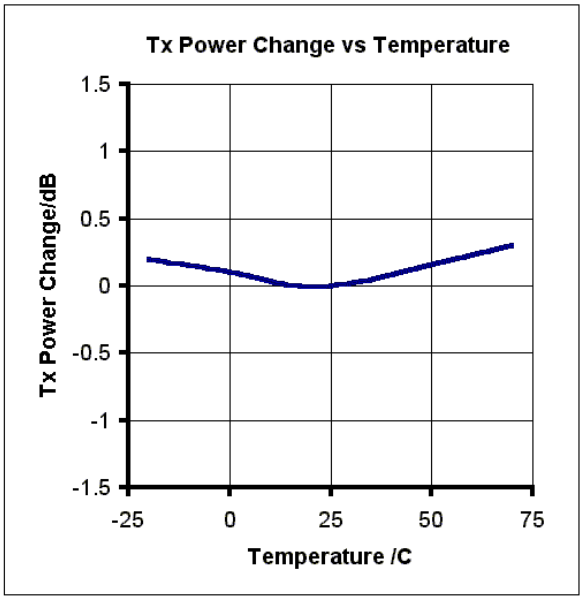


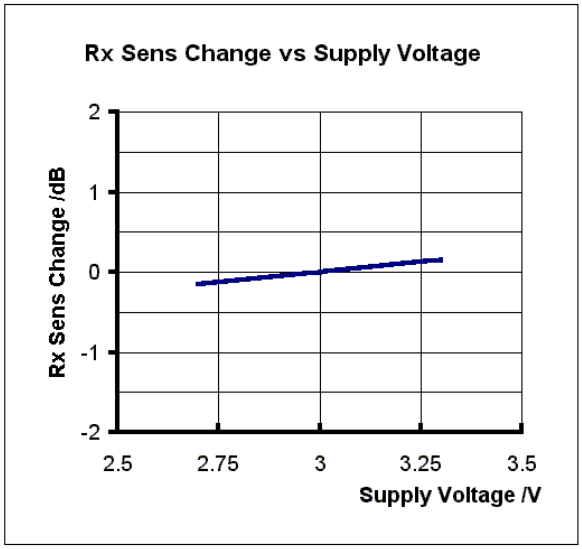


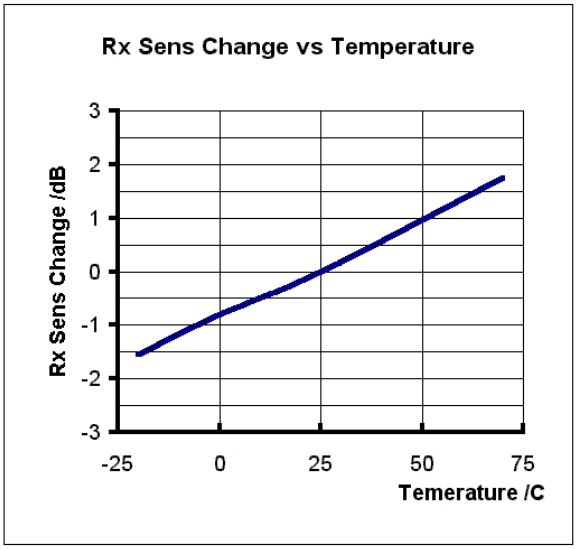





Tx Power Change vs Supply Voltage
Tx Power Change/dB
1.5
1
0.5
0
-0.5
-1
-1.5
2.5
2.75
3
3.25
3.5
Supply Voltage /V


Tx Power Change vs Temperature
Tx Power Change/dB
1.5
1
0.5
0
-0.5
-1
-1.5
-25
0
25
50
75
Temperature /C


Rx Sens Change vs Supply Voltage
Rx Sens Change /dB
2
1
0
-1
-2
2.5
2.75
3
3.25
3.5
Supply Voltage /V


Rx Sens Change vs Temperature
Rx Sens Change /dB
3
2
1
0
-1
-2
-3
-25
0
25
50
75
Temerature /C

RECEIVER BANDWIDTH ADJUSTMENT

The simplified application circuit diagram in page 3 is a 2.4G receiver with a 150kHz Rx bandwidth. The Rx bandwidth can be adjusted from 25kHz to 150kHz. There are 3 major elements related to the receiver bandwidth:

Baseband Bandwidth

BWbb: the baseband bandwidth. This is defined by 8 pole low pass filters in both the I and Q baseband channels. The filtering in each channel is achieved by a two pole Sallen Key filter combined with a six pole Gm filter. The defining resistors and capacitors for the Sallen Key filters are off chip; the Gm filter is totally on-chip except for one bandwidth trimming resistor.

Note that in this document, the bandwidth of the individual baseband I and Q channels is half of the demodulator bandwidth. For example, a receiver with a bandwidth of 150kHz (i.e. ± 75kHz), baseband bandwidth BWbb is 75kHz, demodulator bandwidth BWdm is 150kHz minimum.

The DC offset correction feedback loop in the baseband section introduces an effective high pass filter (100Hz) in the center of the RF band.

Demodulator Bandwidth

BWdm: the demodulator bandwidth. This is the bandwidth of the Period to Digital demodulator. It is a 'brick wall' filter centered on the IF frequency. BWdm must be wider than receive bandwidth.

IF Bandwidth

There is filtering in the IF section following the second mixer, designed to attenuate mixer products prior to the demodulator. Filtering is defined by a 4 pole low pass filter followed by a single pole high pass filter. The low pass filter is an on-chip Gm design with an off-chip bandwidth trimming resistor and the high pass filter is on-chip and fixed frequency at 8kHz.

The following sections shows how the bandwidth of these sections can be adjusted.

BASEBAND FILTERS BANDWIDTH

A. Sallen Key baseband filters

The R and C components for this filter are off chip. To set the baseband bandwidth, BWbb, adjust the C values. Choose values to give a bandwidth equal to or slightly greater than the required bandwidth according to the following formulae.

The recommended component tolerances for resistors should be 1%, with capacitor tolerances of 5%, or better.

Capacitor attached to IFIL2/QFIL2 = 1.8nF x (65kHz/BWbb)
Capacitor attached to IFIL3/QFIL3 = 0.68nF x (65kHz/BWbb)

E.G., for a required 150kHz bandwidth, BWbb=75kHz, suggested values of 1.5nF and 560pF give a bandwidth of 150kHz.

B. Gm baseband filter

On-chip baseband filter bandwidth is adjusted by choice of the external resistor between VDDA and BBSET. Choose this resistor to give a same bandwidth as above.

R = 29kΩ x (65kHz/BWbb)

E.G., for 150kHz (±75kHz) bandwidth, BWbb=75kHz, suggested value is 24kΩ.

C. DC Offset Correction Loop (Effective Baseband High Pass Filter)

The 3dB bandwidth is set to ±100Hz by the external 330nF capacitors connected to DCI and DCQ. The HP cut off can be adjusted by inverse proportional change in DCI/DCQ capacitor. For example, in digital application, if the lowest data rate is 2400bps (1.2kHz), the cut off can be increased from 100Hz to 1kHz by reducing the capacitance to 33nF.

Reduction in the cut off lower than 100Hz, with BWdm=130kHz may lead to instability in Auto Gain Control mode.

Common Rx BW	BWbb	IFIL2/QFIL2 Cap /nF	IFIL3/QFIL3 Cap /nF	BBSET R /kΩ
150 kHz	75 kHz	1.5	0.56	24
100 kHz	50 kHz	2.2	0.82	39
50 kHz	25 kHz	4.7	1.80	75
25 kHz	12.5 kHz	9.1	3.30	150

DEMODULATOR BANDWIDTH

Demodulator bandwidth, BWdm, is adjusted by the choice of the Period to Digital demodulator clock frequency, Fpd. The chip divides down the receiver local oscillator, Frf, by 3 times the divide ratio, PDR, to obtain Fpd.

Fpd = Frf / (3*PDR)

PDR is programmed by bits 14, 15 & 16 of the reference frequency register.

Allowable PDR values for WE2408 are 9, 12, 24, 36, 48, 72, and 96.

The choice of Fpd directly sets the IF frequency Fif, and BWdm:

Fif = Fpd/544
BWdm = Fpd/580

Choose a value of PDR to give BWdm > 2 x BWbb.

IF FILTER BANDWIDTH

The bandwidth of the on-chip IF low pass filter, which precedes the Period to Digital demodulator, should be optimized as follows. Following the calculation of Fif and BWdm from section above, the filter bandwidth is adjusted by choice of the external resistor between VDDA and IFSET.

R = 22kΩ x 206kHz / (Fif + 0.5 x BWdm)

There is an on-chip high pass IF filter fixed at 8kHz.

Examples of BW and corresponding IFSET value

Common Rx BW	BWbb	PDR	Fif	BWdm	IFSET R
150 kHz	75 kHz	9	163 kHz	153 kHz	18 kΩ
100 kHz	50 kHz	12	123 kHz	115 kHz	24 kΩ
50 kHz	25 kHz	24	61.3 kHz	57 kHz	51 kΩ
25 kHz	12.5 kHz	48	30.6 kHz	29 kHz	100 kΩ

RSSI

The RSSI circuit works with external shunt capacitor (10nF) to develop a filtered voltage level inversely proportional to the receive RF signal strength.

The RSSI measurement range is from -100dBm to -35dBm, with the RF input pad bypassed (0dB) and the quadrature mixer gain stage set to high. This range is extended as the receiver gain is reduced. The RSSI conversion factor is ≅ (-30mV/dB), with a voltage range of 2.1 to 0.1 Vdc.

RSSI TOLERANCE

For WE2408 alone, the RSSI tolerance is +/-2%.

If external low noise amplifier (LNA) and filters are added at the Rx front end, the LNA gain and filter loss will vary from unit to unit and will contribute to additional RSSI variation above the IC's RSSI tolerance.

As the RSSI voltage depends on its load, it should be connected only to an ADC or a comparator with high input impedance.

METHODS OF CORRECTING RSSI TOLERANCE

For applications that require accurate RSSI, the tolerance can be corrected by the use of an analog-to-digital converter (ADC) or a trimmer pot meter.

If ADC is used, the tolerance can be corrected using software.

If non-volatile memory (EEPROM or flash) is available, correction can be done during production testing. The ADC can read RSSI values at no signal and at a know Rx signal level, and store those values to correct for the RSSI tolerance.

If non-volatile memory is not available, correct can be done by checking and remember, in the RAM, the RSSI value with no Rx signal, such as when LNA is off; or when antenna switch is off at Rx side; or when Rx frequency is set to an impossible frequency.

If hardware method is preferred, the tolerance can be corrected by adjusting a trimmer pot meter.

RSSI SETTLING TIME

For 130kHz Rx bandwidth, ~25kHz FM deviation, and with recommended 10nF external capacitor attached to RSSI pin, the RSSI reaches 80% of its final value in approximately 0.5ms.

If the FM signal carried is varying significantly in amplitude (e.g. FSK, switching between FM deviation limits) then a longer integration time (i.e. larger RSSI capacitor) will be required for accurate measurement of RX signal strength. Hence, settling time will be longer.

Also, for a narrower Rx bandwidth, the capacitor should be increased to integrate the received power over a longer time. The increase should be inverse proportional to the bandwidth. RSSI response time will also increase accordingly.

RX/TX RESPONSE TIME

RX/TX PLL LOCK TIME

The values shown below are based upon calculations using the component values shown in application circuit with Rx and Tx charge pump currents being 1.0mA and 0.2mA respectively; and reference frequency being 100kHz.

Δ Frequency	**Rx**	**Tx**
From start up	8.5 ms	17 ms
10MHz frequency change	6.5 ms	14 ms
1.0MHz frequency change	5.0 ms	11 ms
0.1MHz frequency change	3.5 ms	7 ms

Note: The settling time for Tx are based upon a 150 Hz high pass filter (HPF) cut off frequency. This filter can be adjusted via the external Tx PLL loop filter components, or by the on-chip Tx charge pump current selection. Settling time will be approximately inversely proportional to the required HPF for the audio/data signal.

PLL Loop Filter

Faster PLL lock times are required in applications where time division duplexing or frequency hopping techniques is used. On the contrary, narrow band audio applications, which need low VCO phase noise, require tightening of PLL loop filter bandwidth. In the result, increases PLL lock time.

The loop filters employed are second order passive loop filters. Separate literatures are available for various filter response considerations and calculation of filter components. Dumping factor, phase noise and reference spurs are the main considerations beside lock time.

The following information are provided for PLL loop filter design:

Kvco

At different PLL voltage or different operating frequency, the VCO gain will be different. The accurate Kvco value can be determined by measurement (VCO frequency change/PLL voltage change for 1 reference frequency step change).

Otherwise, the follow approximated values can be used:
RVCO (1.8GHz), Kvco = 40MHz/V;
TVCO (800MHz), Kvco = 23MHz/V.

Charge Pump Current

The available charge pump current settings are 0.2mA and 1.0mA for both Tx and Rx. The charge pump current is selected by programming the Mode register bits 6 (Rx) and 7 (Tx).

With proper consideration on damping factor, higher charge pump current reduces PLL lock time.

Reference Frequency

In general, larger reference frequency reduces PLL lock time. It is set by Reference Frequency Register.

RECEIVER ATTACK TIME

Rx Baseband DC Offset Loop Response Time

Settling time is 2ms for an effective receiver baseband HPF of 100Hz. The HPF can be adjusted with changing the external capacitors on DCI/DCQ. Settling time will be approximately inversely proportional to the DCI/DCQ capacitors. When making such changes, consideration must be given to the required high pass filtering for the lowest possible frequency of the FM signal.

Auto Gain Control Response Time

Similar considerations should be applied as in RSSI settling time. Current recommendation is to set up the receiver to allow a gain change every 14ms for a receive bandwidth of 130kHz and every 56ms for a bandwidth of 16kHz. Note this only changes the gain by 1 step. It could take 8x as long (110ms or 450ms) to get from maximum to minimum gain or from minimum to maximum gain.

Note that the gain is automatically set to maximum whenever the serial interface signal LE goes high unless this gain reset is disable by programming the Mode register.

More information is available in section on Rx Gain Control and Mode Register.

FM MODULATION

FM DEVIATION

The transmitter utilizes direct modulation method where the modulation signal is directly applied to the PLL loop filter.

FM deviation is depending on the a.c. voltage level of the applied modulation signal as well as TVCO gain. TVCO gain is in term, dependent on the TVCO frequency and TPLL voltage. It is normally desirable for FM deviation to be consistent for a given modulating voltage level.

For a circuit that is designed to operate at a Tx frequency band, the TVCO frequency is fixed by Transmit Frequency Register.

However, the locked TPLL voltage may differ from one unit to another. This is mainly due to the tolerance of external TVCO inductors and the choice of Tx trim bit which set the internal capacitance.

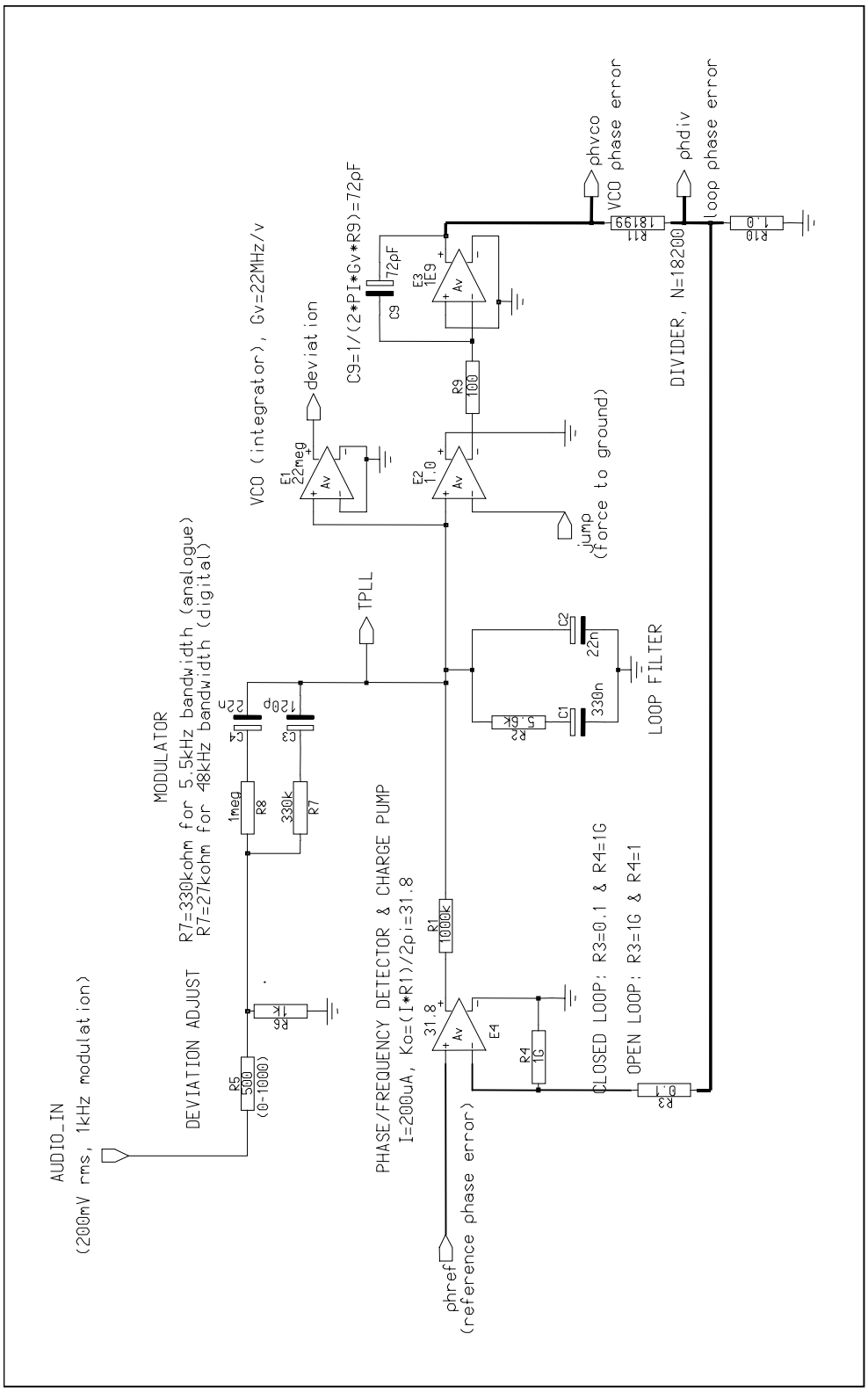
The solution is either to use tight tolerance TVCO inductors or a potential divider to adjust the voltage level of the modulating signal.

Using tight tolerance inductors, such as PCB printed inductors, FM deviation varies between board to board can be maintained within +/-20%. For more accurate FM deviation, a pot meter is required to adjust the modulating signal level.

FM MODULATOR

If there is a change in PLL loop filter, the Tx modulator components have to be changed to get the desired frequency response and Tx FM deviation.

Values for modulator components can be determined by simulation. How VCO frequency responses to an input to the modulator circuit (ac or transient) are simulated to obtain the correct modulator RC combination. Below is the circuit for modulator simulation.



Model for Modulator / PLL Simulation

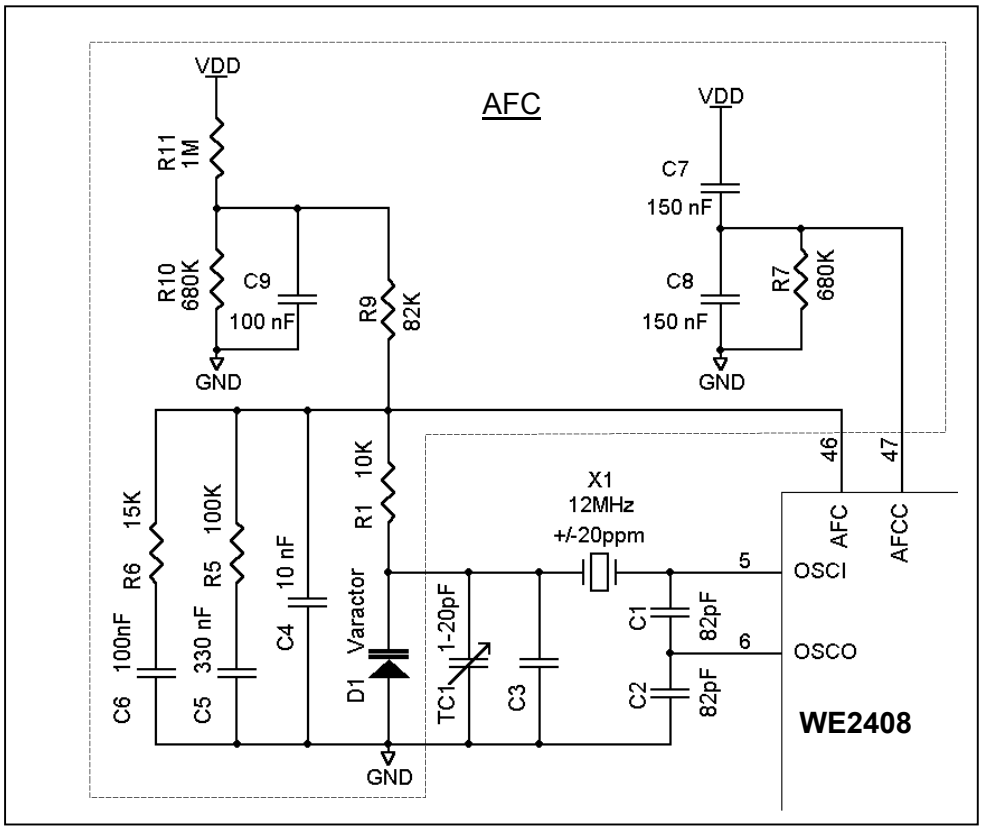
AUTOMATIC FREQUENCY CONTROL (AFC)

In direct conversion, zero-IF receiver system, the frequency difference between receiving RF signal and the receiver LO produces a beat tone. If this beat tone falls in audio range, it will pass through the receiver filters and appear as an audible tone at audio output.

The Automatic Frequency Control (AFC) feature tunes the reference crystal oscillator to minimize frequency offset between receive RF signal and receive LO. The continuous tracking action keeps the Rx LO at a small distance (<100Hz) away from the Rx RF signal. As the beat tone frequency is now very low, the baseband DC offset correction circuit and external audio filter can easily reduce the beat tone to noise level.

The AFC pin 46 provides a DC correction signal corresponding to the amount of frequency offset. The signal changed the biasing, and hence the capacitance, of the varactor D1.

The RC network (C4, C5, C6, R5 and R6) and the decoupling capacitors (C7 and C8) at AFCC pin 47, determines the attack time of the AFC integration (double) loop. AFC response time is approximately 16ms.



Schematics of AFC circuit and relevant components

AFC CORRECTION RANGE

The AFC correction range should be at least 2 x crystal frequency tolerance: including temperature, aging and tuning.

The steps to select components for the desire correction range are:

1. Determine C1, C2 and C3*,

where C3* is the equivalent capacitance of C3//TC1//D1.

The choice of C1, C2 and C3* depends on the crystal load capacitance and drive level.

In figure above, the expected load capacitance of the 12.0MHz crystal is 18pF. The load capacitance presented by the circuit is approximately created by the series combination of C1, C2 and C3*.

Choice of C1 and C2 are affected by the crystal drive level. E.G. for a load capacitance of 18pF:

Drive level	0.1uW	0.1mW
C1, C2	82pF	47pF
C3*	27pF	56pF

2. Determine the variation in C3* (∆C3*) to provide correction range

This can be done experimentally by adjusting a trimmer capacitor or by calculation if the characteristics of the crystal are known.

3. Select varactor diode D1

Select a varactor that its change in capacitance from 2.5V to 0.1V is the slightly greater than ∆C3*.

The varactor use in the above AFC circuit has a capacitance of 10pF at 2.5V and 25pF at 0.1V. It gives an AFC correction range of +/- 20ppm.

4. Select trimmer TC1

Select trimmer cap TC1 to correct the initial tolerance of the crystal.

The trimmer capacitor in above AFC circuit varies from 4pF to 20pF and gives a tuning range of +/- 30ppm.

5. Select C3

If the mid value of D1 (~16pF) and TC1 (~9pF) is lesser than C3*, then C3 (~2pF) is added to make up to the required C3*.

SWITCHING AFC ON AND OFF DURING OPERATION

When AFC is switched off, AFC output voltage will drop to 0V. The varactor capacitance will become maximum and pull the reference frequency to lowest point of the AFC correction range.

Therefore, if the application requires switching AFC off during operation, the resistor network R9 – R11 is required to provide a DC1.2V at the varactor. However, if AFC is always on during operation, this resistor network can be omitted.

CRYSTAL TUNING WITH AFC

While tuning trimmer capacitor (TC1) to correct crystal error, it is necessary to fix the AFC voltage at mid value (1.2V)

This can be done by:

1. turning AFC off if the resistor network R9 – R11 is in placed. Adjust TC1 until the Tx frequency is the same as the Tx Frequency Register.
2. connecting the Rx to a reference signal generator which is set to the receiving frequency of the Rx Frequency Register. Turn AFC on. Adjust TC1 until AFC voltage is about 1.2V.

WORKING CONDITIONS FOR AFC

In a pair of transceivers, AFC is should be on in only one transceiver.

In order for AFC to work properly, the receiving frequency must fall within the bandwidth of the receiver; and the frequency offset between receiving frequency and Rx LO must not be larger than what the AFC correction range can provide.

AFC should not be used during data communication (FSK modulation). Firstly, for low baud rate data, AFC may treat FSK deviation as frequency offset and “correct” it. Secondly, data stream normally do not have balance number of 0s and 1s. During the AFC evaluation period, the average is taken and it may be falsely taken as carrier offset.

AFC NOISE

Although AFC removes the beat tone, it may result in another type of noise known as zero crossing pop noise. This noise may be audible in silent situation when there is no FM modulation in the receiving signal. This noise is removed by adding resistor R7 at AFCC.

Suitable value for R7 is between 560kΩ and 1MΩ.

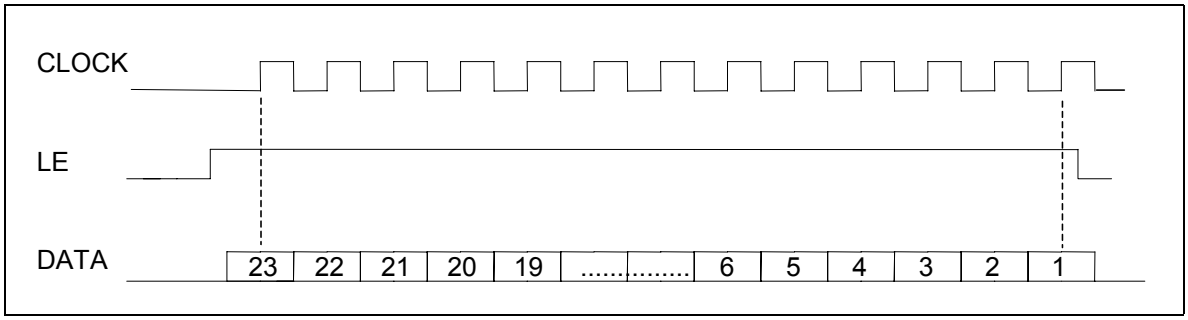
AFC RESPONSE TIME

The series RC network connected from AFC pin to VSS, along with decoupling capacitors connected from AFCC pin 47 to VDD and VSS, determines the attack time of the AFC integration (double) loop.

With the component values shown in page 23, the AFC response time is approximately 16ms.

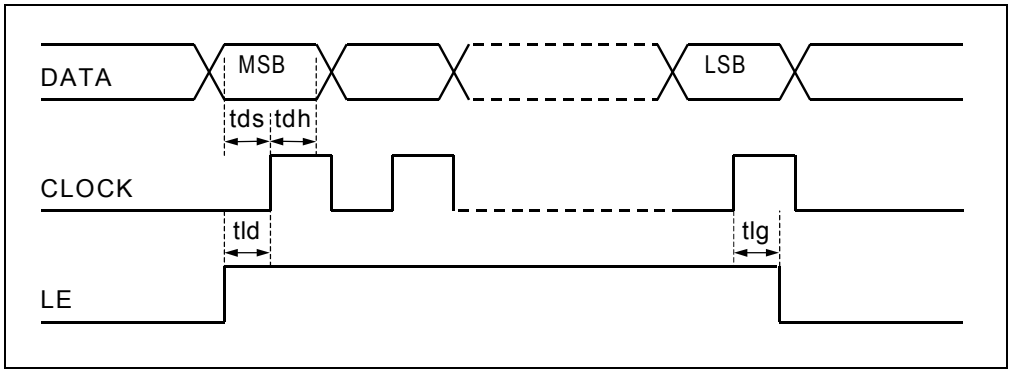
SERIAL PROGRAMMING INTERFACE

Tx/Rx frequencies, reference frequency, as well as various operational and test modes are controlled by a 3-wire serial bus comprised of Clock, Load Enable and Data. The programming word contains 23 bits. The first two bits (LSB) select the register programming of receive VCO frequency, transmit VCO frequency, reference frequency or device operational modes. The remaining bits contain the data to be programmed. The timing diagram below shows the relationship between Data, Clock, and Load Enable.



Data is clocked into the internal shift registers on the positive edge of the CLOCK (pin 3), while Load Enable (pin 1) is held HIGH. Data is loaded from the shift registers into the data registers on the negative edge of the Load Enable (LE). This load is NOT synchronized with the programmable divider, i.e. the load is controlled directly by the negative falling edge of the Load Enable.

TIMING DIAGRAM



tds: Data set up time before +ve CLOCK edge
30ns min

tdh: Data hold time after +ve CLOCK edge
30ns min

tld: Latch Enable lead time before first +ve CLOCK edge.
30ns min

tlg: Latch Enable lag time after last +ve CLOCK edge.
30ns min

REFERENCE FREQUENCY REGISTER

Bit 1 (last bit loaded)		Load control bit 1 = (0)
Bit 2		Load control bit 2 = (0)
Bit 3	Ref(1) LSB	Reference divide register (count 1 to 2047)
Bit 4	Ref(2)	Reference divide register (count 1 to 2047)
Bit 5	Ref(3)	Reference divide register (count 1 to 2047)
Bit 6	Ref(4)	Reference divide register (count 1 to 2047)
Bit 7	Ref(5)	Reference divide register (count 1 to 2047)
Bit 8	Ref(6)	Reference divide register (count 1 to 2047)
Bit 9	Ref(7)	Reference divide register (count 1 to 2047)
Bit 10	Ref(8)	Reference divide register (count 1 to 2047)
Bit 11	Ref(9)	Reference divide register (count 1 to 2047)
Bit 12	Ref(10)	Reference divide register (count 1 to 2047)
Bit 13	Ref(11) MSB	Reference divide register (count 1 to 2047)
Bit 14	PDR(1)	PDR select
Bit 15	PDR(2)	PDR select
Bit 16	PDR(3)	PDR select

PDR (3)	PDR (2)	PDR (1)	Divide ratio, PDR
0	0	0	3
0	0	1	9
0	1	0	12
0	1	1	24
1	0	0	36
1	0	1	48
1	1	0	72
1	1	1	96

Reference divide register (1 to 2047) sets the internal reference frequency.

Internal Reference Frequency = Reference Oscillator Frequency / Reference divide register

e.g. 12MHz reference crystal, Ref divider of 240, gives 50kHz internal reference frequency.

PDR select sets the IF and BWdm.

FM Demodulator bandwidth, BWdm = (Receiver LO) / (3 x 580 x PDR)
IF frequency, Fif = (Receiver LO) / (3 x 544 x PDR)

e.g. If Rx LO is 2403MHz frequency, PDR of 12, gives 115kHz demodulator bandwidth and 123kHz IF.

For the above examples,
Programming word = 0000000 010 00011110000 00

RECEIVE FREQUENCY REGISTER

Bit 1 (last bit loaded)		Load control bit 1 = (1)
Bit 2		Load control bit 2 = (0)
Bit 3 LSB	Rf(1)	Rx frequency F register
Bit 4	Rf(2)	Rx frequency F register
Bit 5 MSB	Rf(3)	Rx frequency F register
Bit 6 LSB	Ra(1)	Rx frequency A register
Bit 7	Ra(2)	Rx frequency A register
Bit 8	Ra(3)	Rx frequency A register
Bit 9	Ra(4)	Rx frequency A register
Bit 10 MSB	Ra(5)	Rx frequency A register
Bit 11 LSB	Rm(1)	Rx frequency M register
Bit 12	Rm(2)	Rx frequency M register
Bit 13	Rm(3)	Rx frequency M register
Bit 14	Rm(4)	Rx frequency M register
Bit 15	Rm(5)	Rx frequency M register
Bit 16	Rm(6)	Rx frequency M register
Bit 17	Rm(7)	Rx frequency M register
Bit 18	Rm(8)	Rx frequency M register
Bit 19	Rm(9)	Rx frequency M register
Bit 20 MSB	Rm(10)	Rx frequency M register
Bit 21	Rx VCO Trim bit 1	
Bit 22	Rx VCO Trim bit 2	
Bit 23	Not Used	

Rx VCO Trim Bits		Trim Capacitor
2	**1**	
0	0	0 – minimum C
0	1	1
1	0	2
1	1	3 – maximum C

Rx Frequency = Internal Reference Frequency x 3 x ((32 x M) + A + (F/8))

Trim capacitors are provided for correction of device tolerance.

e.g. 2403MHz RF, 100kHz reference frequency; div ratio 8010, assuming trim 2
Programming word = X10 0011111010 01010 000 01

TRANSMIT FREQUENCY REGISTER

Bit 1 (last bit loaded)		Load control bit 1 = (0)
Bit 2		Load control bit 2 = (1)
Bit 3 LSB	Tf(1)	Tx frequency F register
Bit 4	Tf(2)	Tx frequency F register
Bit 5 MSB	Tf(3)	Tx frequency F register
Bit 6 LSB	Ta(1)	Tx frequency A register
Bit 7	Ta(2)	Tx frequency A register
Bit 8	Ta(3)	Tx frequency A register
Bit 9	Ta(4)	Tx frequency A register
Bit 10 MSB	Ta(5)	Tx frequency A register
Bit 11 LSB	Tm(1)	Tx frequency M register
Bit 12	Tm(2)	Tx frequency M register
Bit 13	Tm(3)	Tx frequency M register
Bit 14	Tm(4)	Tx frequency M register
Bit 15	Tm(5)	Tx frequency M register
Bit 16	Tm(6)	Tx frequency M register
Bit 17	Tm(7)	Tx frequency M register
Bit 18	Tm(8)	Tx frequency M register
Bit 19	Tm(9)	Tx frequency M register
Bit 20 MSB	Tm(10)	Tx frequency M register
Bit 21	Tx VCO Trim bit 1	
Bit 22	Tx VCO Trim bit 2	
Bit 23	Tx VCO Trim bit 3	

Tx VCO Trim Bits			Trim Capacitor
3	**2**	**1**	
0	0	0	0 – Minimum C
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7 – Maximum C

Tx Frequency = Internal Reference Frequency x 3 x ((32 x M) + A + (F/8))

Trim capacitors are provided for correction of device tolerance.

e.g. 2472MHz RF, 100kHz reference frequency, div ratio 8240, assuming trim 2
Programming word = 010 0100000001 10000 000 10

MODE REGISTER

Bit 1 (Last bit loaded)		Load control bit 1 = (1)	
Bit 2		Load control bit 2 = (1)	
Bit 3	AGC (Automatic Gain Control)	0 = Off	1 = On
Bit 4	Receiver	0 = Off	1 = On
Bit 5	Transmitter	0 = Off	1 = On
Bit 6	Receive Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 7	Transmit Charge Pump Current	0 = 0.2mA	1 = 1.0mA
Bit 8	Rx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 9	Tx Charge Pump Polarity	0 = Normal	1 = Invert
Bit 10	Mixer Gain Control	(Bit 1)	
Bit 11	Mixer Gain Control	(Bit 2)	
Bit 12	Baseband Gain & RF Pad Control	(Bit 1)	
Bit 13	Baseband Gain & RF Pad Control	(Bit 2)	
Bit 14	Baseband Gain & RF Pad Control	(Bit 3)	
Bit 15	AGC Gain Reset	0 = Reset	1 = No Reset
Bit 16	AFC Enable	0 = Disable	1 = Enable
Bit 17	Audio/Data Output Select	0 = Analog	1 = Digital
Bit 18	Mode (Bit 1)	0 for Normal mode. See page 33 & 34 for other modes	
Bit 19	Mode (Bit 2)	0 for Normal mode. See page 33 & 34 for other modes	
Bit 20	Mode (Bit 3)	0 for Normal mode. See page 33 & 34 for other modes	
Bit 21	Mode (Bit 4)	[Tse_0] in Normal Mode. See page 33 & 34 for other modes	
Bit 22	Mode (Bit 5)	[Tse_1] in Normal Mode. See page 33 & 34 for other modes	

RX GAIN CONTROL (BIT 3, 10-15, 18-19)

The receiver section includes a facility to switch overall gain to maintain linearity over a wide dynamic range of on-channel signal levels. This can be done manually or automatically via an on-chip automatic gain control (AGC) circuit.

Automatic Mode (Bit 3 = 1; AGC ON)

When this bit is set to 1, the receiver will set the internal gain stages according to the received signal as shown in the following table.

Nominal RF Signal Level		Attenuation dB from maximum gain					
		RF section		Baseband section			
Increasing	Decreasing	RF Pad	RF Mixer	1st Block	2nd Block	3rd Block	4th Block
	< -92dBm	0	0	0	0	0	0
> -86dBm	< -82dBm	0	0	0	10	0	0
> -76dBm	< -72dBm	0	0	0	10	10	0
> -66dBm	< -62dBm	0	10	0	10	10	0
> -56dBm	< -52dBm	0	10	10	10	10	0
> -46dBm	< -42dBm	0	20	10	10	10	0
> -36dBm	< -32dBm	0	20	10	10	10	10
> -26dBm	< -22dBm	10	20	10	10	10	10
>-16dBm		10	30	10	10	10	10

In this mode, the mixer gain and baseband gain settings (bit 10-14) are ignored.

Manual Mode (Bit 3 = 0; AGC OFF)

In this mode, receiver gain stages are manually controlled by programming the Mode register bit 10 to 14.

RF Mixer Attenuation Control Table

Mode Register Bit		RF Mixer Attenuation, dB
11	10	
0	0	30
0	1	20
1	0	10
1	1	0

Baseband Gain and RF Pad Control Table

Mode Register Bit			Baseband Stage Attenuation, dB				RF Pad Attn, dB
14	13	12	1st Block	2nd Block	3rd Block	4th Block	
0	0	0	10	10	10	10	10
0	0	1	10	10	10	10	0
0	1	0	10	10	10	0	0
0	1	1	0	10	10	0	0
1	0	0	0	10	0	0	0
1	0	1	0	0	0	0	0

Tse Signal Evaluation Time (Bit 21 & 22)

Applicable only if AGC is ON, bit 3 = 1.

To determine the correct gain setting for AGC, the received on-channel signal is integrated in the baseband section. The integrated signal level is evaluated at regular time intervals: signal evaluation time Tse. Tse is programmed by bits 21 & 22 of the Mode Register. The available Tse values are inversely proportional to the demodulator bandwidth, BWdm, allowing for the signal evaluation over a similar number of baseband cycles of an on-channel signal.

Recommendations for setting Tsi and Tse are as follow:

Recommended value for Tsi is:

Tsi = 0.9ms x (130kHz/BWdm) + 1.6ms + 4.5ms x (65kHz/BWbb)

where BWdm is the demodulator bandwidth and BWbb is the base band bandwidth

Recommended value for Capacitance at GCC pin is:

The recommended capacitance CGCC attached to GCC pin, for a given signal integration time constant, Tsi, is

CGCC = 330nF x (Tsi / 27ms)

Recommended value for Tse is:

Tse > 2 x Tsi

Possible values for Tse are:

Tse_1	*Tse_0*	*Period*
0	0	7ms x (130kHz/BWdm)
0	1	14ms x (130kHz/BWdm)
1	0	28ms x (130kHz/BWdm)
1	1	56ms x (130kHz/BWdm)

e.g. 1 For 65kHz BWbb, 130kHz BWdm
Recommended Tsi = 7ms, CGCC = 85.6nF, Tse ≥ 14ms
Choose CGCC = 82nF , then Tsi = 6.7ms
Choose Tse bits = 01 which gives Tse=14ms
Change from maximum to minimum gain takes 110ms.

e.g. 2 For 16kHz BWbb, 32kHz BWdm
Recommended Tsi = 24ms, CGCC = 293nF, Tse ≥ 48ms
Choose CGCC = 300nF , then Tsi = 24.5ms
Choose Tse bits = 01 which gives Tse=57ms
Change from maximum to minimum gain takes 456ms.

AGC GAIN RESET DISABLE

If bit 15 of Mode Register is 0 and AGC is on, any change made to any register (or whenever LE line goes high) will reset the gain to maximum automatically. The gain will then switches gradually to the desired setting according to the received signal level.

If bit 15 is set to 1 and a register is being programmed, the gain setting will remain the same before and after the programming.

CHARGE PUMP CURRENT AND POLARITY (BIT 6-9)

Available charge pump current for Tx and Rx VCOs are 0.2mA and 1mA. With proper choice of PLL loop filter components, higher charge pump current provides faster lock time. Please refer to section on Rx/Tx PLL Lock Time for more information.

For the application circuit shown in page 3, the PLL lock time is optimized for Rx charge pump current of 1.0mA and Tx charge pump current of 0.2mA.

Charge pump polarity is always Normal except if external VCO circuit is used. If the tuning diode's anode is connected to ground and the PLL voltage is connected to the cathode, then the charge pump polarity must be inverted.

ANALOG VS DIGITAL OUTPUT (BIT 17)

The receiver AFO output can be configured to either analog or digital mode.

In the Digital Mode, the demodulated signal goes through an internal data slicer before being output as CMOS compatible logic data.

Polarity of RX data is the same as received FM deviation, i.e. no data inversion. A positive FM deviation produces a 1 and a negative FM deviation produces a 0. However, please note that due to the design of TX VCO, a 1 in the TX data produces a negative FM deviation and a 0 produces a positive FM deviation. Hence, when two WE2408 are used as data communication pair, the RX data will be inverted compare to the TX data.

In the Analog Mode, the output pin provides the recovered, demodulated audio signal without passing through the data slicer.

Polarity of RX waveform is the opposite of the received FM deviation, i.e. signal inversion. A positive FM deviation produces a lower voltage and a negative FM deviation produces a higher voltage. Since, TX FM modulation is inverted, when two WE2408 are used as analog communication pair, the RX signal will look the same as the TX signal, i.e. no inversion.

OTHER OPERATION MODES (BIT 18-22)

In normal transceiver operation, bit 18 to 22 of Mode Register is set to Normal Mode 00000.

Other than Normal Mode, the device offers test modes and 2 other special operating modes. In Test Mode, The AFO output pin can be configured to provide signal at various stages in the receiver path for trouble-shooting purpose.

The special operating modes available are Tx Charge Pump Disable Mode and Reference Oscillator On Mode

Other Modes for WE2408

Mode Bits					Other Mode for WE2408
5	4	3	2	1	
X	X	0	1	0	**Tx Charge Pump Disable** Tx charge pump is disabled to allow open loop TX VCO modulation.
X	X	0	1	1	**Reference Oscillator On** This mode allows the reference oscillator to be kept active when both Tx and Rx are off so that faster PLL lock can be achieved when either Tx or Rx is turned on. This mode is only valid when Rx and Tx are off. It should not be selected with Tx or Rx on.
X	X	1	0	0	**I Baseband Filter Test** I baseband filter output route to AUDO (analogue) Only for Analogue output select The I Baseband output of the Quadrature mixer is a sinusoidal waveform that center at approx. 1.34Vdc and amplitude depends on the injected RF signal strength. The amplitude is about 350mVpp at -80dBm RF_IN power.
X	X	1	0	1	**Q Baseband Filter Test** Q baseband filter output route to AUDO (analogue) Only for Analogue output select The Q Baseband output of the Quadrature mixer is a sinusoidal waveform that center at approx. 1.34Vdc and amplitude depends on the injected RF signal strength. The amplitude is about 350mVpp at -80dBm RF_IN power.
X	X	1	1	0	**2nd Mixer Test** 2nd mixer output route to AUDO (analogue) Only for Analogue output select The 2nd mixer output is a sinusoidal waveform at frequency Fif (= Frf / PDR / 544) +/- FM Dev. The amplitude is about 280mVpp at -80dBm RF_IN power.

PROGRAMMING EXAMPLES

e.g. Manual gain, AGC off, Rx on, Tx off,
1.0mA Rx charge pump current, normal Rx charge pump polarity,
10dB RF mixer attenuation, 20dB baseband attenuation, no RF pad
AFC enable, AGC Reset ignored,
Analogue AUDO, Normal mode,
ignore signal evaluation period, Tse (AGC not in use)

Programming word = 0XX000 01X 01110 X0 X1 01 0 11

e.g. AGC on, Rx on, Tx on,
1.0mA Rx charge pump current, 0.2mA Tx charge pump polarity,
normal Rx and Tx PLL charge pump polarity,
ignore manual gain control bits
AFC enable, AGC Reset on,
Analogue AUDO, Normal mode,
Signal evaluation period 14ms x (130kHz / BWdm)

Programming word = 001000 010 XXXXX 00 01 11 1 11

CIRCUIT DESIGN CONSIDERATIONS

BOARD LAYOUT

Designing ultra-high frequency (UHF) RF circuits requires careful attention to detail and layout. Careful attention to layout should be observed to minimize stray inductance and capacitance effects. This attention to detail will preserve RF sensitivity of the device. At high frequencies, micro strip or strip-line transmission line techniques must be employed. Using “state-of-the-art” CAD techniques for PCB layout, standard FR-4 fiberglass PCB material (1.6-mm thickness) may be employed. For maximum performance, RF quality substrate material should be used.

SUPPLY DECOUPLING

Positive supply connections for the WE2408 are nominally 2.7V to 3.3V. All supply pins must be bypassed to an RF, Analog, or Digital ground plane depending upon the type of supply pin. For RF supply pins, a 100 pF ceramic capacitor in parallel with a 1.0 nF ceramic capacitor, both RF quality, should provide adequate decoupling. For analog and digital supply pins, 0.01-0.1μF RF quality capacitors should be used. The bypass capacitors should be placed as close to all power supply pins as possible. An effort should be made to minimize the trace length between the capacitor leads and the respective WE2408 power supply and common pins.

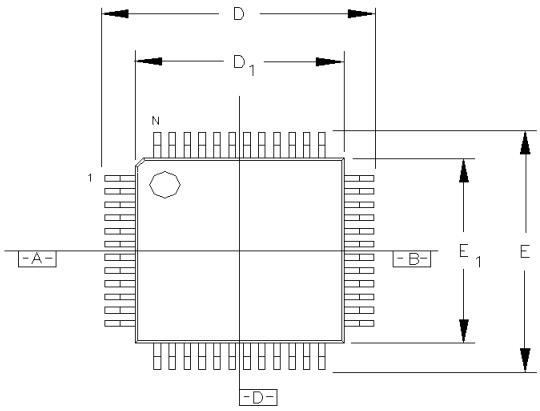
GROUNDING

The circuit designer should attempt to locate WE2408, its associated analog input circuitry and interconnections, as far as possible from logic circuitry. A solid RF analog ground should be placed around the LNA and associated RF filter circuitry, while a solid digital ground should be placed around the reference oscillator. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

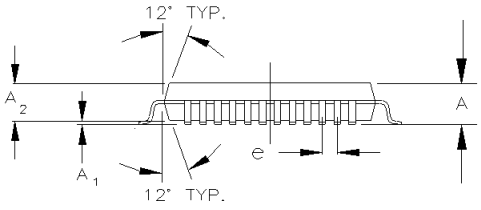
Connect all ground pins together to a low impedance ground plane, as close to the device as possible. Observe proper RF grounding and shielding techniques. The WE2408 should be used with separate analog and digital ground planes. The digital and analog ground planes should be "summed" at one point, typically at the power supply filter capacitor.

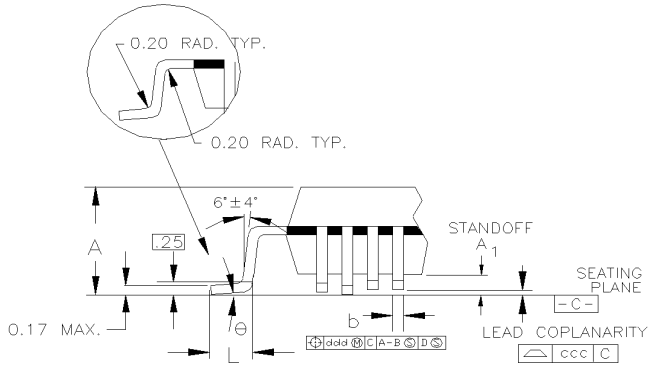
PACKAGE INFORMATION

TQFP 48 Dimensions



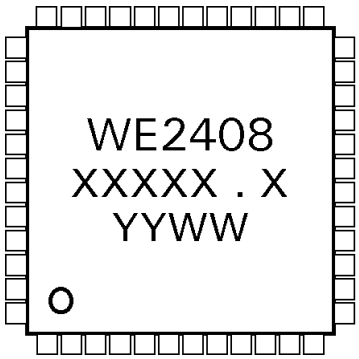
LEAD COUNT		48L	
DIMS.	TOL.	1.0 mm THICK	1.4 mm THICK
A	MAX.	1.20	1.60
A_1		.05 MIN./ .15 MAX.	
A_2	±.05	1.00	1.40
D	±.20	9.00	
D_1	±.10	7.00	
E	±.20	9.00	
E_1	±.10	7.00	
L	+.15/−.10	.60	
e	BASIC	.50	
b	±.05	.22	
θ		0°−7°	
ddd	MAX.	.08	
ccc	MAX.	.08	





All dimensions in mm

Marking



XXXXX . X	: Log Number
YYWW	: Date Code
YY	: Year
WW	: Week number

REVISION HISTORY

Document Version	Revision Date	Comments
Draft	12 Sep 02	
030523	23 May 03	First official release Page 2: Schematic updated Page 10-14: Electrical specifications updated at multiple locations Page 31: Added a section on ANALOG VS DIGITAL OUTPUT (BIT 17) Page 32: Mode bits for Reference Oscillator On changed from 111 to 011. This change affects all ICs with date code 0322 onwards. Page 34: Add marking diagram

ORDERING INFORMATION

Part Number	Frequency	Supply	Temp	Package
WE2408	2400MHz -2485MHz	2.7 – 3.3V	-10 to 65 ºC	TQFP 48 pin