ZARLINK SEMICONDUCTOR

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WL102B

Wireless Data Controller

Advance Information

DS4582 ISSUE 4.0 May 2000

Ordering Information
WL102B/IG/TP1N 100 pin package
WL102BC/PR/FP1R 144 pin package

Features

- Complete CMOS, single chip, radio transceiver controller
- Hardware implemented Communication Control Block (CCB)
- Protocol independent design using external flash memory
- Internal 8051 and external processor options
- Internal/external buffer and processor RAM
- Block power down facility
- PCMCIA/8bit processor host interface to buffer RAM
- Up to 1Mbps/2 level or 2 Mbps/4 level operation

The WL102B is a highly integrated CMOS wireless data controller designed to dramatically reduce the cost of radio data applications. It works with the WL600C RF IF chip and WL800 synthesiser chip to offer a complete solution for a frequency hopping, spread spectrum radio in the 2.4 to 2.45GHz ISM band.

Its flexible design means that it can also be used in a wide range of other applications using a range of "processor", protocols and additional memory options as well as radios at other frequencies.

Related Documents

WL600 (DS4581), WL800 (DS5241) and WL102B (DS4837) Datasheets

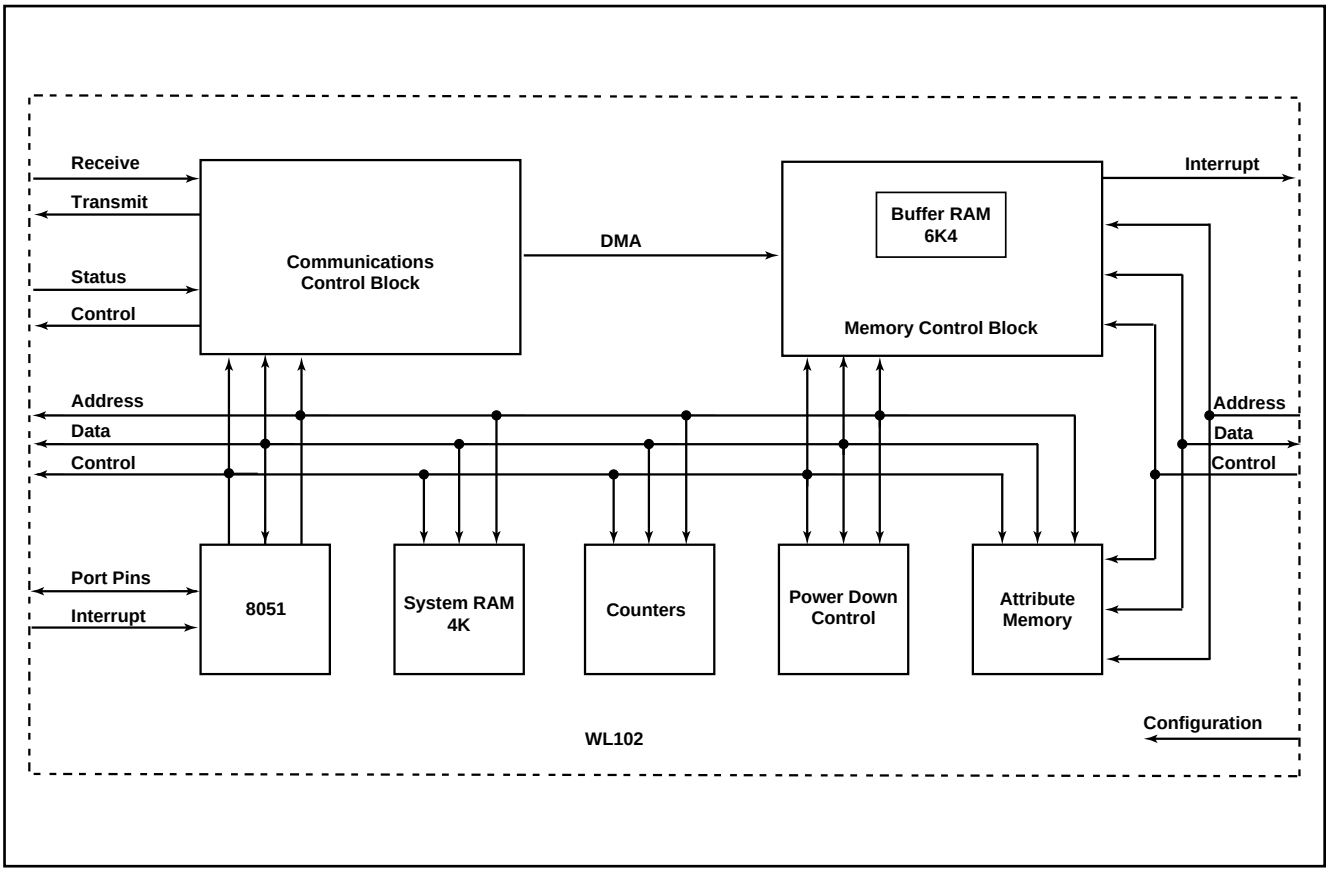
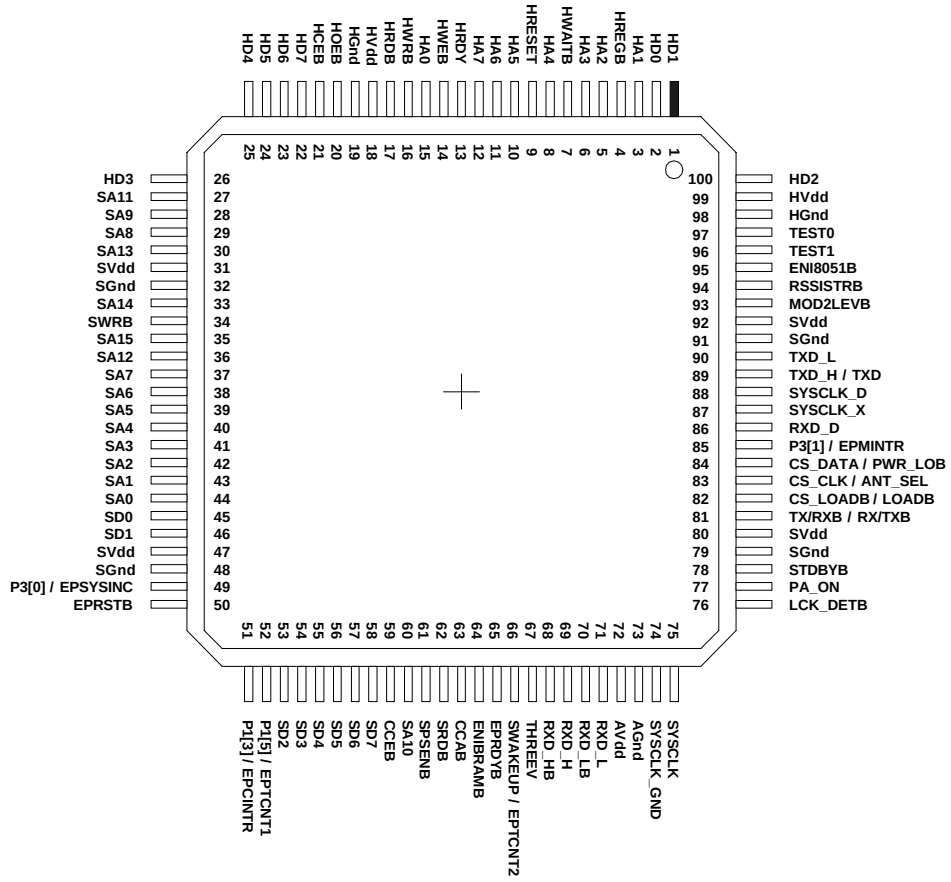


Figure 1 - WL102 Minimum configuration block diagram


1 HD1
2 HD0
3 HA1
4 HREGB
5 HA2
6 HA3
7 HWAITB
8 HA4
9 HRESET
10 HA5
11 HA6
12 HA7
13 HRDY
14 HWEB
15 HA0
16 HWRB
17 HRDB
18 HVdd
19 HGnd
20 HOEB
21 HCEB
22 HD7
23 HD6
24 HD5
25 HD4
26 HD3
27 SA11
28 SA9
29 SA8
30 SA13
31 SVdd
32 SGnd
33 SA14
34 SWRB
35 SA15
36 SA12
37 SA7
38 SA6
39 SA5
40 SA4
41 SA3
42 SA2
43 SA1
44 SA0
45 SD0
46 SD1
47 SVdd
48 SGnd
49 P3[0] / EPSYSINC
50 EPRSTB
51 P1[3] / EPCINTR
52 P1[5] / EPTCNT1
53 SD2
54 SD3
55 SD4
56 SD5
57 SD6
58 SD7
59 CCEB
60 SA10
61 SPSENB
62 SRDB
63 CCAB
64 ENIBRAMB
65 EPRDYB
66 SWAKEUP / EPTCNT2
67 THREEV
68 RXD_HB
69 RXD_H
70 RXD_LB
71 RXD_L
72 AVdd
73 AGnd
74 SYSCLK_GND
75 SYSCLK
76 LCK_DETB
77 PA_ON
78 STDBYB
79 SGnd
80 SVdd
81 TX/RXB / RX/TXB
82 CS_LOADB / LOADB
83 CS_CLK / ANT_SEL
84 CS_DATA / PWR_LOB
85 P3[1] / EPMINTR
86 RXD_D
87 SYSCLK_X
88 SYSCLK_D
89 TXD_H / TXD
90 TXD_L
91 SGnd
92 SVdd
93 MOD2LEVB
94 RSSISTRB
95 ENI8051B
96 TEST1
97 TEST0
98 HGnd
99 HVdd
100 HD2

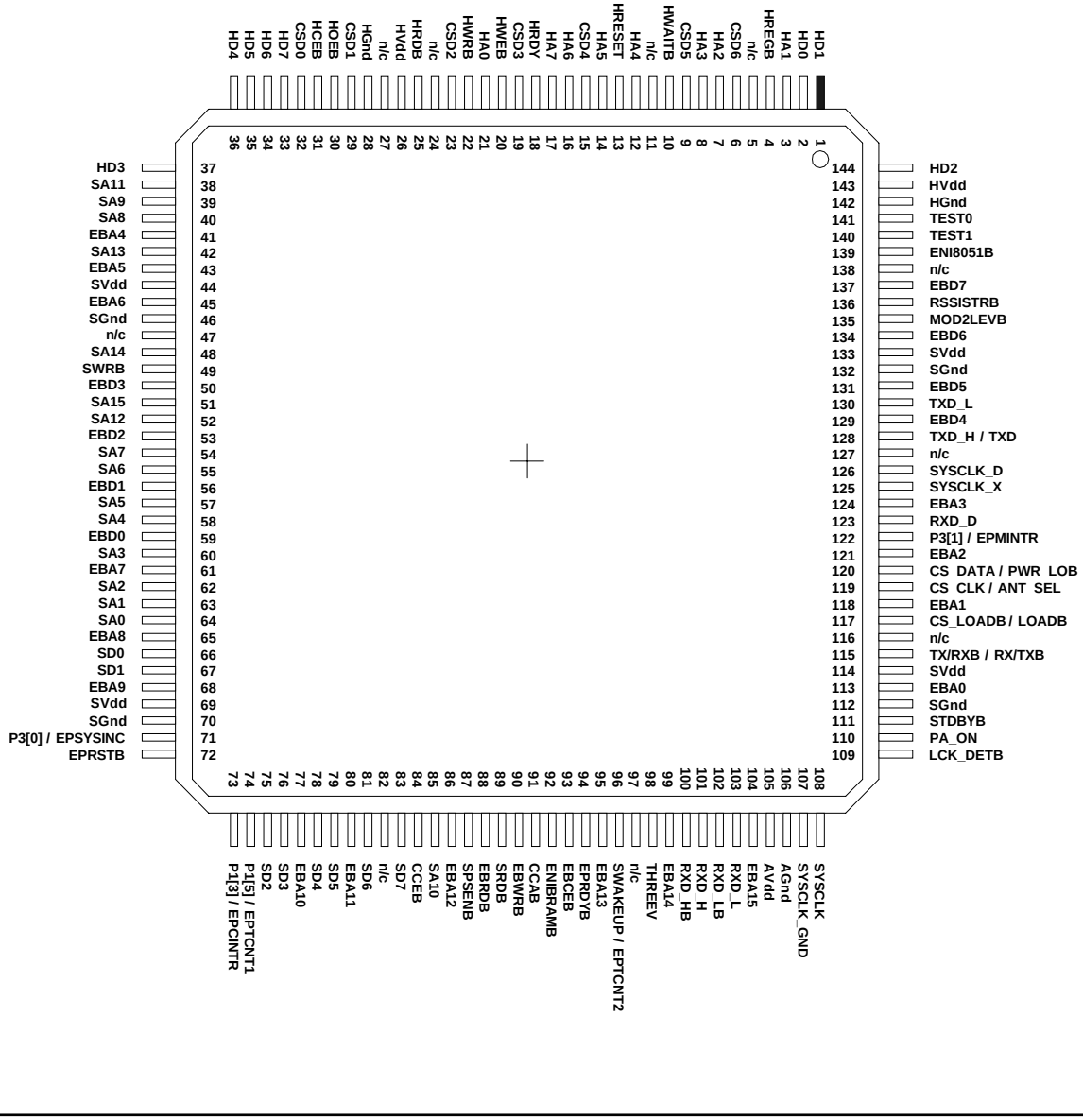


Figure 3 - 144 Pin package

WL102 System Overview

The WL102 is a highly integrated digital wireless transceiver controller suitable for controlling multiple channel radios with data rates up to 1Mbit/s 2-level data or 2Mbit/s 4-level data. It has been designed to interface easily with the WL600 and WL800 radio transceiver chips.

The use of low power synchronous on chip RAM and selective power down of system blocks makes the WL102 ideally suited to power sensitive applications. Also the WL102 can be operated from 3V or 5V supply rails with level translation between the Host and MAC system built in to the Host Interface. A minimum configuration of the WL102 with a 64Kbyte external ROM for code storage makes it ideal for small footprint applications, and the option of 100 pin or 144 pin TQFP 1mm packages make it suitable for PC-Card applications.

The 100 pin package option allow the WL102 to be used in the lowest cost solution. This includes all the internal blocks of the WL102 hardware plus the option of an external processor, to replace the internal 8051 core, and the external system RAM and / or other peripherals on the processor bus. The 144 pin package includes the 100 pin features plus the option of using an external data buffer RAM (up to 64K), to replace the internal 6.4K buffer RAM, and the option of using the parallel synthesiser load pins the are active in DE6003 mode of the CCB block, the Datasheet DS4837 should be checked for further information on this option.

It is envisaged that the WL102 hardware will allow the development of a wireless network to the Media Access Layer of the IEEE model for networking, with the addition of an LLC layer providing the equivalent of the Data Link layer of the ISO network model. In such a system the Host interface buffer RAM would provide the boundary between the LLC layer running on the Host and the MAC layer on the internal WL102 8051 processor, or an optional external MAC system processor.

Figure 1 shows the internal architecture of the WL102.

The WL102 provides an interface between a Host system, such as a PC or PDA, which can be a PC-Card interface or an 8 bit microprocessor bus, and an interface designed for use with the DE6038 (WL600/WL800) radio transceiver.

The host interface provides a buffer and interrupt signalling mechanisms between the Host and Mac system processors. The MAC system processor is required to provide the timing and control functions of Media Access Control.

The Communications Control Block performs transmit and receive operations directly to the buffer RAM so minimising the load on the MAC system processor. A minimum controller system configuration would be the WL102 plus an external code memory device.

WL102 Hardware Blocks

System Processor

The WL102 contains an embedded processor, identical in operation to an industry standard 8051 microcontroller, with the exception that the internal data memory is increased from 128 to 256 bytes.

System busses and strobes allow the 8051 to access the full 64 Kbytes of external code memory. Internal connections exist to the processor's two interrupt inputs, and to the two timer inputs. Two I/O port pins are internally connected to blocks within the WL102, whilst four of the remaining I/O port pins are brought out to external pins, including the serial receive and transmit port pins. Internal address decoding provides access to the other blocks of the device, with 36 Kbytes of the processor's 64 Kbytes address range being unassigned and available for the addition of external peripheral devices.

The 8051 demultiplexed address and data bus are available externally to allow for the addition of extra memory or other peripheral devices.

The 8051 is clocked at the internal system clock frequency of 10MHz.

If additional processing power is required for a particular application the WL102 may also be used with an external processor instead of the internal 8051. This external processor also accesses the WL102 blocks via the internal address decode. Interrupt and Counter outputs are brought to external pins and two control signals must also be provided to the WL102.

Data RAM

The WL102 contains 4 Kbytes of static RAM which the processor may use for variable storage etc. If additional storage space is required, an external static RAM may also be used, and mapped to an unused area of the WL102 memory map.

Memory Control Block

The memory Control Block allows access to the dual port buffer used to communicate between the Host and WL102 system processes. The control logic of the buffer RAM allows the Host to asynchronously read or write data at the same time as the WL102 MAC system. To help arbitrate access to this buffer space, a hardware semaphore system is also included.

The WL102 contains 6784 bytes of low power buffer RAM on chip. The 144-pin package option also allows for an external (single port) SRAM to be used to increase the buffer RAM space, up to 64Kbytes.

Host Interface

The Host Interface has been designed to be flexible enough to allow its use from small microprocessor systems to PC-Card slots. In a minimum configuration it uses only 4 address locations and a standard microprocessor type read and write cycle. The interface provides access to the Buffer RAM, which is accessible by both the Host and the MAC systems simultaneously, and also to a control register which allows the Host to reset or interrupt the MAC processor, and performs some other control functions on the WL102.

Packets of data are typically buffered in the internal buffer RAM before being transmitted or transferred from the MAC system to the host.

The 8-bit interface is microprocessor and PCMCIA-compatible, with a separate dedicated RAM providing 255 bytes of attribute memory used for the configuration and control of a PC Card. The host interface may be used by any microprocessor-type interface which can supply two bits of address, a chip enable signal, read/write strobes and 8 bits of data, subject to timing requirements of the WL102. The interface also provides an interrupt signalling mechanism between the Host and MAC system as well as some other control functions, such as a hardware semaphore and reset circuitry.

Communications Control Block

This block of the WL102 performs many of the functions required for transmission and reception of data packets, and interfaces directly to the radio transceiver. For power sensitive applications the configuration registers can have their clocks switched off once the initial configuration is complete and for protocols which allow the transceiver to sleep for periods of time, the clocks to the entire block can be disabled via the Power Control register.

The CCB handles all the control signals for the radio and can be configured for the timing required by the transceiver being used. The CCB can directly access data stored in the buffer RAM, via a DMA bus separate to the processor bus, and once configured will finally handle a transmission or reception, including CRC checking, address match, optional data scrambling (Bias suppression encoding) and transfer of the data to/from the buffer RAM.

For shorter network management packets the MAC system processor can directly read/write up to 64 bytes of data from/to the CCB FIFO. The CCB generates maskable interrupts to the MAC system processor at defined points in the receive/transmit process to allow the processor to perform any additional processing required to succccessfully complete the receive or transmit sequence.

The Features of the CCB include:

- Transmission and reception of 2-level and 4-level GFSK
  bit streams at 625Kbps, 1Mbps and 2Mbps.
- Configurable Preamble/Frame word generation and recognition
- Checksum generation and validation (CRC-16 and CRC-32)
- Optional data coding schemes: bit-stuffing, scrambling and bias suppression encoding (as per draft IEEE 802.11)
- Dedicated data path for DMA transfer to and from buffer RAM
- Address matching on received data packet
- Analysis of received signal for performing clear channel assessment, including 16-bit countdown timer
- 8 (maskable) interrupt sources to optimise operation of the system software
- Automatic synthesiser channel loading for Rx/Tx when using WL600/WL800

Counters

The two 16-bit counters are provided which are configured by setting a reload value. When enabled, the counters decrement continuously at 10MHz, generating a terminal count signal to the processor and automatically reloading the reload value when the count reaches zero.

The terminal count outputs are internally connected to the 8051 timer inputs when using the internal 8051, and to external pins when using an external processor.

Power Control

A power-down function is provided under the control of the WL102 system. Power down enable signals are provided to each major block; the clocks of the individual blocks being disabled when the appropriate power down bit is set. In addition, the internal processor's PCON register will disable the 8051 core in the usual manner.

System Supply Voltages

The WL102 has two separate digital supply rails, allowing for use in mixed 3V/5V systems. The host interface has its own independent supply, whilst a second supply powers the core of the WL102 and its interface to the memory and radio transceiver subsystems. Both power supplies may be operated at either 3 or 5 volts (nominal), with the restriction that the host interface supply voltage must be greater than or equal to the voltage powering the WL102 core and radio transceiver.

Manufacturing Enhancements

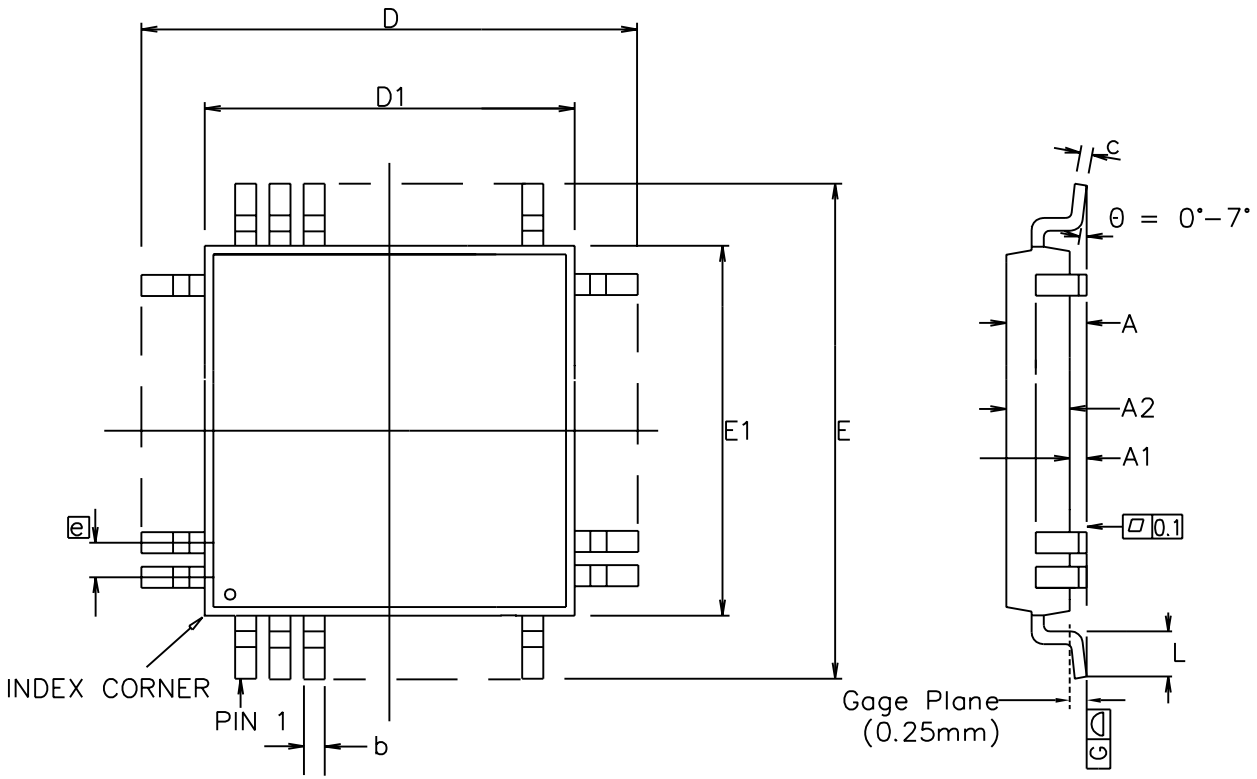
Radio Test Mode

The WL102 radio test mode of operation allows an attached radio transceiver to be tested more easily in a complete assembled unit. The mode is selected by configuring the test mode pins. In this mode the usual functions of the WL102 are suspended and the control and status signals of the CCB radio interface are connected to the pins of the Host interface, with the WL102 providing the status signals back from the radio interface. The comparators on the receive data stream are still used and so the test system is provided with the digital version of this radio output. In addition the operation of the CCB preamble and frame word recognition can be tested, as well as the clock recovery data stream.

MCB Execute Mode

This mode of operation is used to allow programming of the external code memory if a re-programmable device is used, via special software run on the Host. Using this mode, the WL102's code memory is completely reprogrammed regardless of its current state i.e. no 'boot-block' code is required in the WL102 system. This allows complete radio modules to be manufactured without the need for preprogramming the code memory. At final test the MAC software image can be downloaded or test software can be downloaded and used prior to the final software.

This facility also allows the complete radio module to be upgraded in the field or for diagnostic software to be downloaded as necessary.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		– – –	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	100				
ND	25				
NE	25				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BED Iss

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 m
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swin

ISSUE	1	2	3	
ACN	201373	207144	212447	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

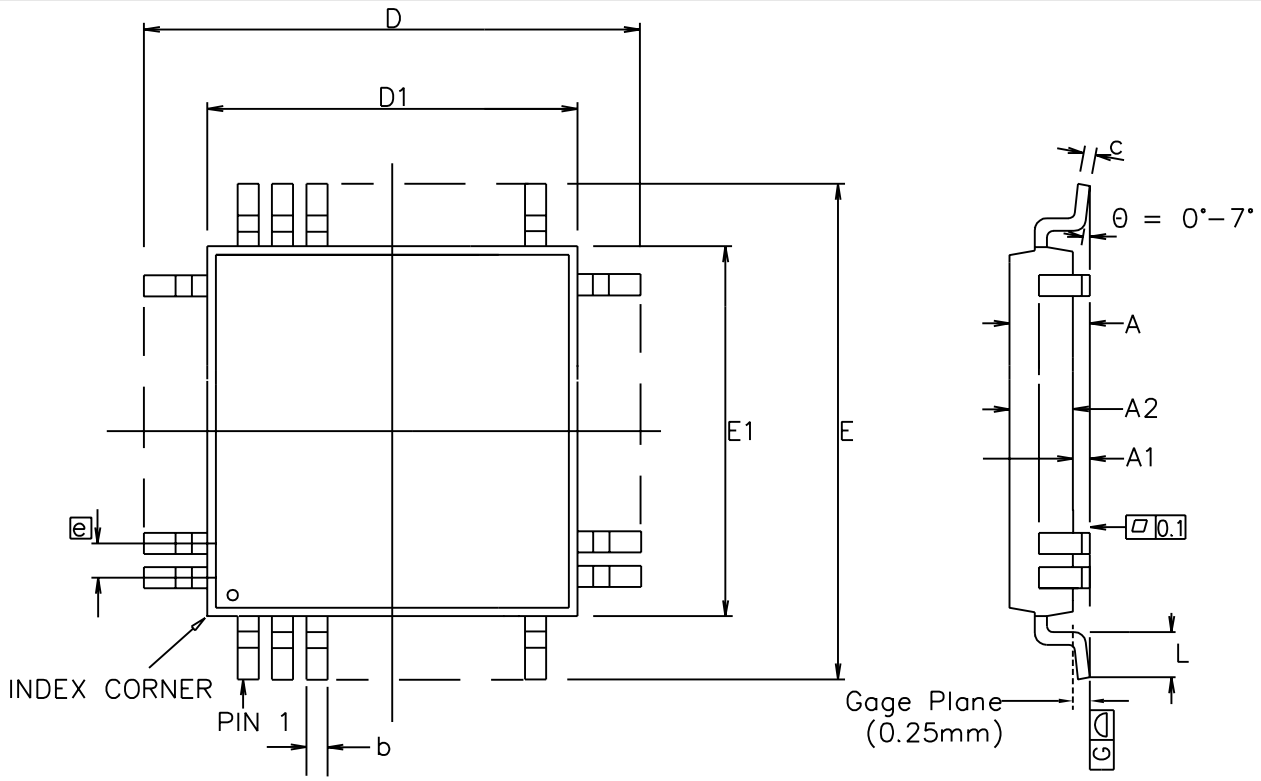
Previous package codes

GP / B

Package Code QC

Package Outline for 100 lea
LQFP (14 x 14 x 1.4mm)
2.0mm Footprint

GPD00253



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	1.60		– – –	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	22.00 BSC			0.866 BSC	
D1	20.00 BSC			0.787 BSC	
E	22.00 BSC			0.866 BSC	
E1	20.00 BSC			0.787 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	144				
ND	36				
NE	36				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BFB Iss

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mr
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/026 (Swin

ISSUE	1	2	3	
ACN	201371	207153	212446	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

GP / B

Package Code QC

Package Outline for 144 le
LQFP (20 x 20 x 1.4mm)
2.0mm Footprint

GPD00251

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