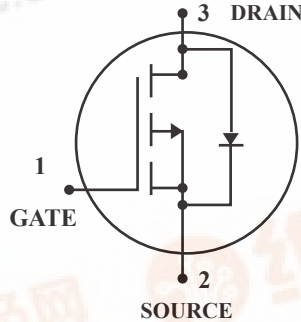
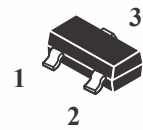


### P-Channel Enhancement Mode Power MOSFET



**DRAIN CURRENT**  
-4.2 AMPERES  
**DRAIN SOURCE VOLTAGE**  
-20 VOLTAGE



**SOT-23**

#### Features:

- \*Super High Dense Cell Design For Low  $R_{DS(ON)}$   
 $R_{DS(ON)} < 53m \Omega @ V_{GS} = 10V$
- \*Rugged and Reliable
- \*Simple Drive Requirement
- \*SOT-23 Package

#### Applications

- \*Power Management in Notebook Computer
- \*Portable Equipment
- \*Battery Powered System

#### Maximum Ratings ( $T_A = 25^\circ C$ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	
Continuous Drain Current <sup>3</sup> , ( $T_A = 25^\circ C$ ) $I_D$ , ( $T_A = 70^\circ C$ )	$I_D$	-4.2	A
		-3.4	
Pulsed Drain Current <sup>1,2</sup>	$I_{DM}$	-10	
Total Power Dissipation ( $T_A = 25^\circ C$ )	$P_D$	1.38	W
Maximum Thermal Resistance Junction-ambient <sup>3</sup>	$R_{\theta JA}$	90	$^\circ C/W$
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150	$^\circ C$

#### Device Marking

WTC2305-2305

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## Electrical Characteristics (T<sub>A</sub> = 25 °C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### Static

Drain-Source Breakdown Voltage V <sub>GS</sub> =0, I <sub>D</sub> =-250μA	V <sub>(BR)DSS</sub>	-20	-	-	V
Gate-Source Threshold Voltage V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	V <sub>GS(Th)</sub>	-0.5	-	-	
Gate-Source Leakage Current V <sub>GS</sub> = ±12V	I <sub>GSS</sub>	-	-	±100	nA
Drain- Source Leakage Current(T <sub>j</sub> =25 °C) V <sub>DS</sub> =-20V, V <sub>GS</sub> =0	I <sub>DSS</sub>	-	-	-1	μA
Drain- Source Leakage Current(T <sub>j</sub> =70 °C) V <sub>DS</sub> =-16V, V <sub>GS</sub> =0		-	-	-10	
Drain-Source On-Resistance <sup>2</sup> V <sub>GS</sub> =-10V, I <sub>D</sub> =-4.5A V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.2A V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2.0A V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-1.0A	R <sub>DS(on)</sub>	-	-	53 65 100 250	mΩ
Forward Transconductance V <sub>DS</sub> =-5.0V, I <sub>D</sub> =-2.8A	g <sub>fs</sub>	-	9	-	S

### Dynamic

Input Capacitance V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1.0MHz	C <sub>iss</sub>	-	740	-	pF
Output Capacitance V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1.0MHz	C <sub>oss</sub>	-	167	-	
Reverse Transfer Capacitance V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1.0MHz	C <sub>rss</sub>	-	126	-	

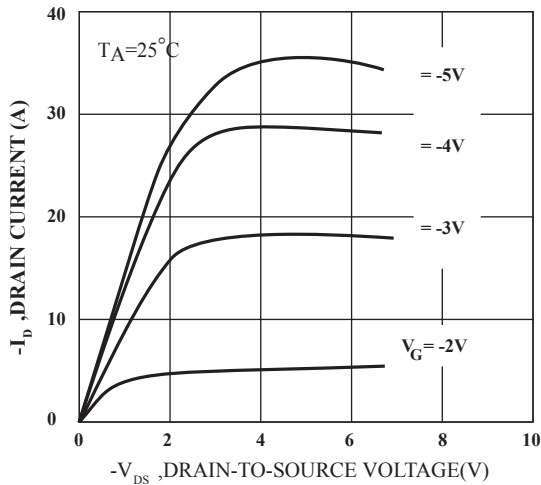
## Switching

Turn-on Delay Time <sup>2</sup> $V_{DS}=-15V, V_{GS}=-10V, I_D=-4.2A, R_D=3.6\Omega, R_G=6\Omega$	$t_d(\text{on})$	-	5.9	-	ns
Rise Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-4.2A, R_D=3.6\Omega, R_G=6\Omega$	$t_r$	-	3.6	-	
Turn-off Delay Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-4.2A, R_D=3.6\Omega, R_G=6\Omega$	$t_d(\text{off})$	-	32.4	-	
Fall Time $V_{DS}=-15V, V_{GS}=-10V, I_D=-4.2A, R_D=3.6\Omega, R_G=6\Omega$	$t_f$	-	2.6	-	
Total Gate Charge <sup>2</sup> $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-4.2A$	$Q_g$	-	10.6	-	nC
Gate-Source Charge $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-4.2A$	$Q_{gs}$	-	2.32	-	
Gate-Drain Change $V_{DS}=-16V, V_{GS}=-4.5V, I_D=-4.2A$	$Q_{gd}$	-	3.68	-	

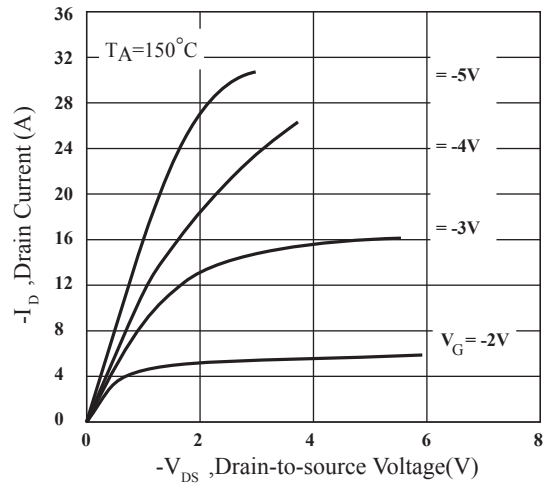
## Source-Drain Diode Characteristics

Forward On Voltage <sup>2</sup> $V_{GS}=0V, I_S=-1.2A, @T_j=25^\circ\text{C}$	$V_{SD}$	-	-	-1.2	v
Reverse Recovery Time $V_{GS}=0, I_S=-4.2A, dl/dt=100A/\mu\text{s}$	$T_{rr}$	-	27.7	-	ns
Reverse Recovery Charge $V_{GS}=0, I_S=-4.2A, dl/dt=100A/\mu\text{s}$	$Q_{rr}$	-	22	-	nC

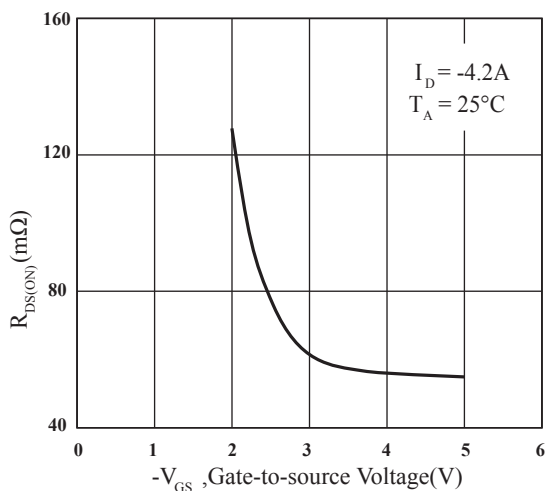
- Note: 1. Pulse width limited by Max, junction temperature.  
 2. pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 270°C/W when mounted on min, copper pad.



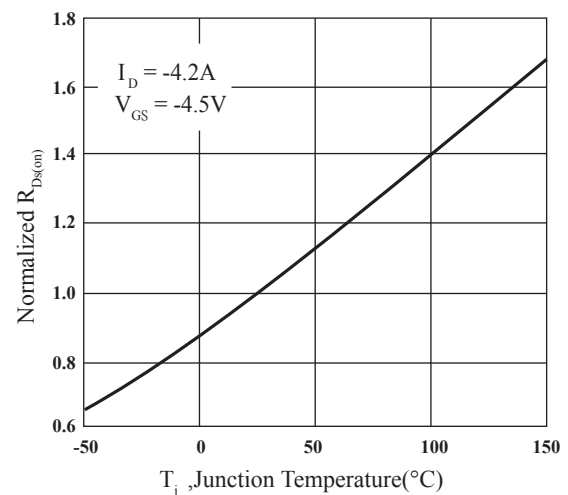
**FIG.1 Typical Output Characteristics**



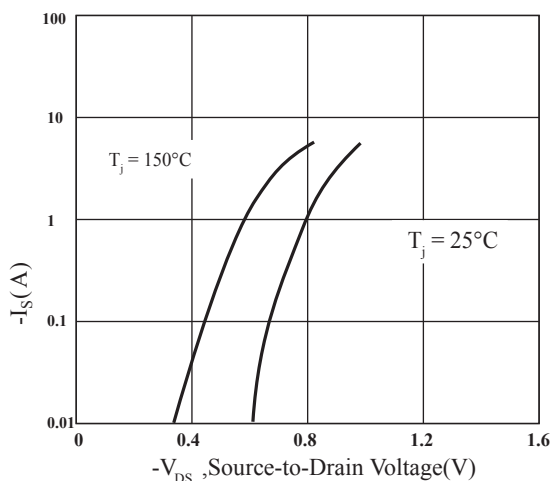
**Fig.2 Typical Output Characteristics**



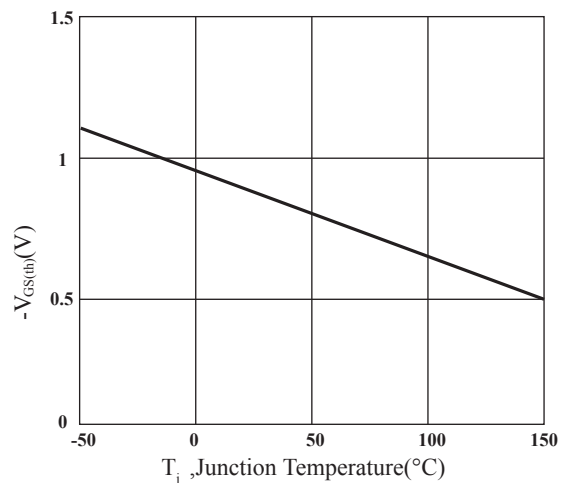
**Fig.3 On-Resistance v.s. Gate Voltage**



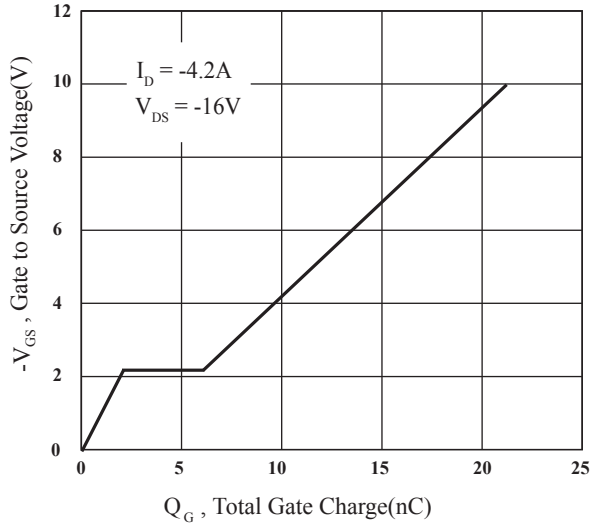
**Fig.4 Normalized On-Resistance**



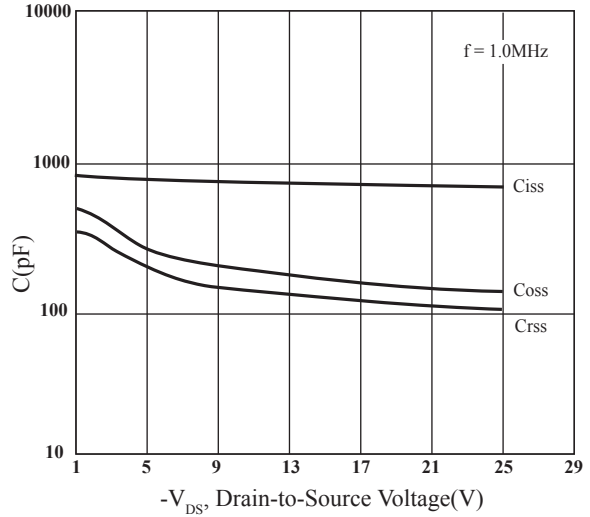
**Fig.5 Forward Characteristics of Reverse Diode**



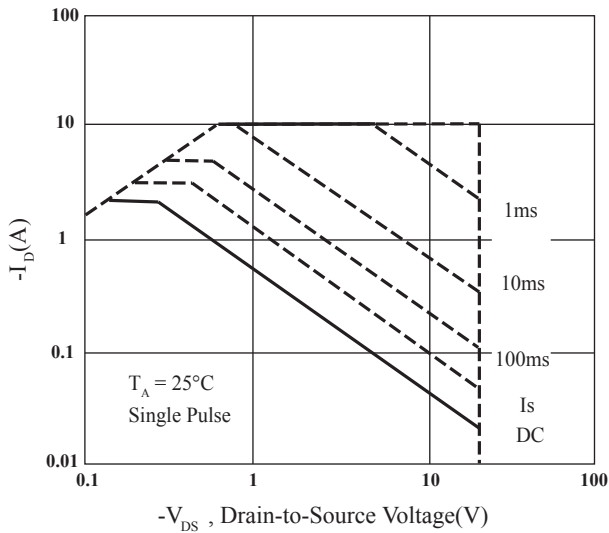
**Fig.6 Gate Threshold Voltage v.s. Junction Temperature**



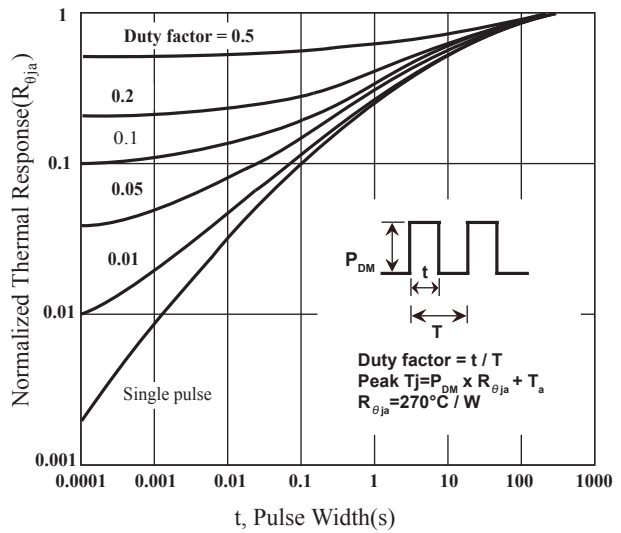
**Fig 7. Gate Charge Characteristics**



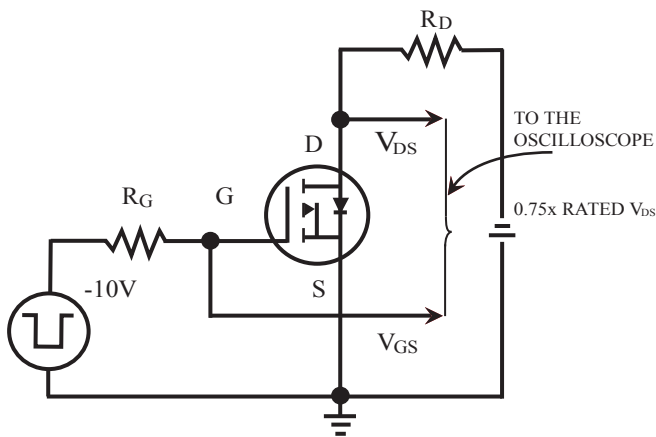
**Fig 8. Typical Capacitance Characteristics**



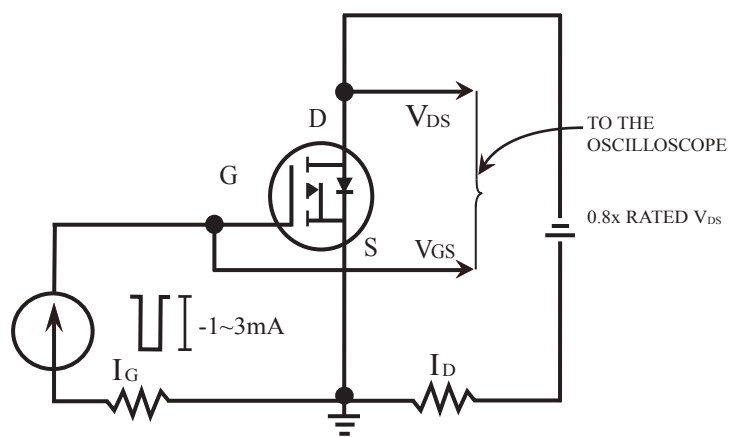
**Fig 9. Maximum Safe Operation Area**



**Fig 10. Effective Transient Thermal Impedance**

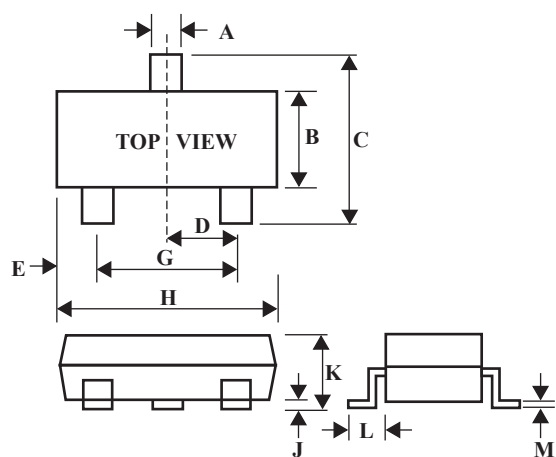


**Fig 11. Switching Time Circuit**



**Fig.12 Gate Charge Circuit**

**SOT-23 Outline Dimension**



<b>SOT-23</b>		
<b>Dim</b>	<b>Min</b>	<b>Max</b>
<b>A</b>	0.35	0.51
<b>B</b>	1.19	1.40
<b>C</b>	2.10	3.00
<b>D</b>	0.85	1.05
<b>E</b>	0.46	1.00
<b>G</b>	1.70	2.10
<b>H</b>	2.70	3.10
<b>J</b>	0.01	0.13
<b>K</b>	0.89	1.10
<b>L</b>	0.30	0.61
<b>M</b>	0.076	0.25