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W39V080FA Data Sheet

Winbond Electronics Corp.

1M × 8 CMOS FLASH MEMORY WITH FWH INTERFACE

Table of Contents-

1. GENERAL DESCRIPTION 3
2. FEATURES 3
3. PIN CONFIGURATIONS 4
4. BLOCK DIAGRAM 4
5. PIN DESCRIPTION 4
6. FUNCTIONAL DESCRIPTION 5
   - 6.1 Interface Mode Selection and Description 5
   - 6.2 Read (Write) Mode 5
   - 6.3 Reset Operation 5
   - 6.4 Accelerated Program Operation 5
   - 6.5 Boot Block Operation and Hardware Protection at Initial- #TBL & #WP 5
   - 6.6 Sector Erase Command 6
   - 6.7 Program Operation 6
   - 6.8 Dual BIOS 6
   - 6.9 Hardware Data Protection 6
   - 6.10 Write Operation Status 7
     - 6.10.1 DQ7: #Data Polling 7
     - 6.10.2 RY/#BY: Ready/#Busy 7
     - 6.10.3 DQ6: Toggle Bit 7
     - 6.10.4 DQ5: Exceeded Timing Limits 8
   - 6.11 Identification Input pin ID[3:0] 8
   - 6.12 Register 8
     - 6.12.1 General Purpose Inputs Register 8
     - 6.12.2 Block Locking Registers 8
     - 6.12.3 Product Identification Registers 10
   - 6.13 Table of Operating Modes 11
     - 6.13.1 Operating Mode Selection - Programmer Mode 11
     - 6.13.2 Operating Mode Selection - FWH Mode 11
   - 6.14 Fwh Cycle Definition 12
   - 6.15 Embedded Programming Algorithm 13
   - 6.16 Embedded Erase Algorithm 14
   - 6.17 Embedded #Data Polling Algorithm 15
   - 6.18 Embedded Toggle Bit Algorithm 16
   - 6.19 Software Product Identification and Boot Block Lockout Detection Acquisition Flow 17
7. DC CHARACTERISTICS 18
   - 7.1 Absolute Maximum Ratings 18
   - 7.2 Programmer interface Mode DC Operating Characteristics 18
   - 7.3 FWH interface Mode DC Operating Characteristics 19
   - 7.4 Power-up Timing 19
   - 7.5 Capacitance 19

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8. PROGRAMMER INTERFACE MODE AC CHARACTERISTICS 20
8.1 AC Test Conditions 20
8.2 AC Test Load and Waveform 20
8.3 Read Cycle Timing Parameters 21
8.4 Write Cycle Timing Parameters 21
8.5 Data Polling and Toggle Bit Timing Parameters 21
9. TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE 22
9.1 Read Cycle Timing Diagram 22
9.2 Write Cycle Timing Diagram 22
9.3 Program Cycle Timing Diagram 23
9.4 #DATA Polling Timing Diagram 23
9.5 Toggle Bit Timing Diagram 24
9.6 Sector Erase Timing Diagram 24
10. FWH INTERFACE MODE AC CHARACTERISTICS 25
10.1 AC Test Conditions 25
10.2 Read/Write Cycle Timing Parameters 25
10.3 Reset Timing Parameters 25
11. TIMING WAVEFORMS FOR FWH INTERFACE MODE 26
11.1 Read Cycle Timing Diagram 26
11.2 Write Cycle Timing Diagram 26
11.3 Program Cycle Timing Diagram 27
11.4 #DATA Polling Timing Diagram 28
11.5 Toggle Bit Timing Diagram 29
11.6 Sector Erase Timing Diagram 30
11.7 FGPI Register/Product ID Readout Timing Diagram 31
11.8 Reset Timing Diagram 31
12. ORDERING INFORMATION 32
13. HOW TO READ THE TOP MARKING 32
14. PACKAGE DIMENSIONS 33
14.1 32L PLCC 33
14.2 32L STSOP (8X14mm) 33
14.3 40L TSOP (10 mm x 20 mm) 34
15. VERSION HISTORY 35

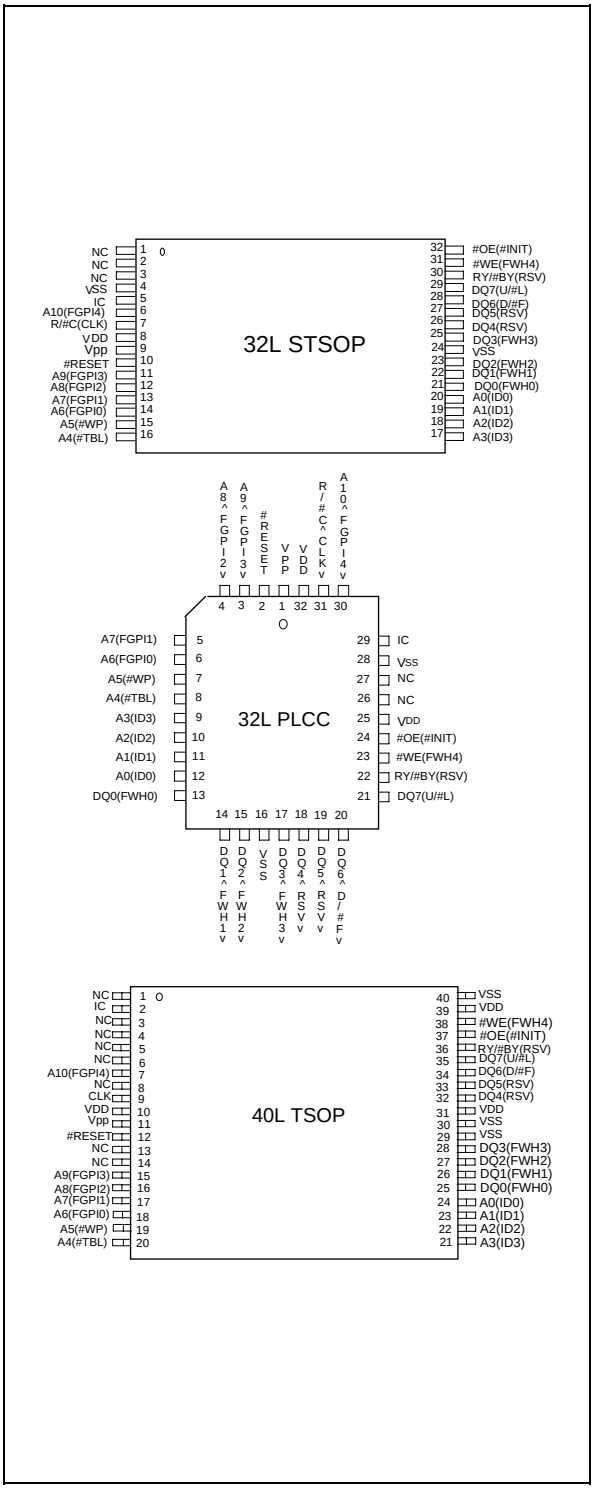
1. GENERAL DESCRIPTION

The W39V080FA is an 8-megabit, 3.3-volt only CMOS flash memory organized as 1M × 8 bits. For flexible erase capability, the 8Mbits of data are divided into 16 uniform sectors of 64 Kbytes. The device can be programmed and erased in-system with a standard 3.3V power supply. A 12-volt VPP is required for accelerated program. The unique cell architecture of the W39V080FA results in fast program/erase operations with extremely low current consumption. This device can operate at two modes, Programmer bus interface mode and FWH bus interface mode. As in the Programmer interface mode, it acts like the traditional flash but with a multiplexed address inputs. But in the FWH interface mode, this device complies with the Intel FWH specification. The device can also be programmed and erased using standard EPROM programmers.

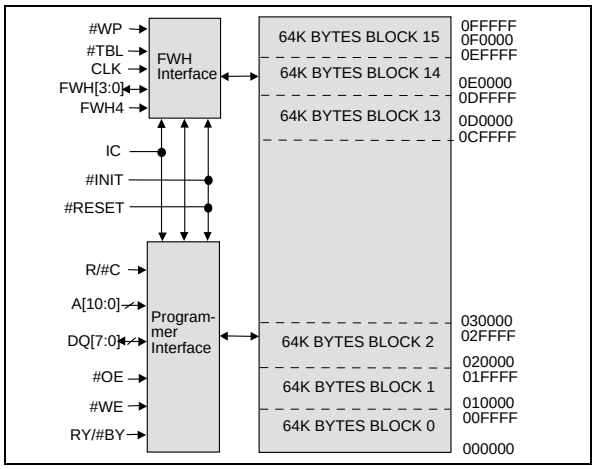
2. FEATURES

- Single 3.3-volt operations:
  - 3.3-volt Read
  - 3.3-volt Erase
  - 3.3-volt Program
- Fast program operation:
  - VPP = 12V
  - Byte-by-Byte programming: 9 μS (typ.)
- Fast erase operation:
  - Sector erase 0.9 Sec. (typ.)
- Fast read access time: Tkq 11 nS
- Endurance: 30K cycles (typ.)
- Twenty-year data retention
- 16 Even sectors with 64K bytes
- Any individual sector can be erased
- Dual BIOS function
  - Full-chip partition with 8M-bit or dual-block partition with 4M-bit
- Hardware protection:
  - #TBL supports 64-Kbyte Boot Block hardware protection
  - #WP supports the whole chip except Boot Block hardware protection
- Hardware Features
- Ready/#Busy output (RY/#BY)
  - Detect program or erase cycle completion
- Hardware reset pin (#RESET)
  - Reset the internal state machine to the read mode
- VPP input pin
  - Acceleration (ACC) function accelerates program timing
- Low power consumption
  - Read Active current: 15 mA (typ. for FWH mode)
- Automatic program and erase timing with internal VPP generation
- End of program or erase detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- Available packages: 32L PLCC, 32L STSOP, 40L TSOP(10 x 20 mm), 32L PLCC Lead free, 32L STSOP Lead free and 40L TSOP (10 x 20 mm) Lead free

3. PIN CONFIGURATIONS



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYM.	INTERFACE		PIN NAME
	PGM	FWH	
IC	*	*	Interface Mode Selection
#RESET	*	*	Reset
#INIT		*	Initialize
#TBL		*	Top Boot Block Lock
#WP		*	Write Protect
CLK		*	CLK Input
FGPI[4:0]		*	General Purpose Inputs
ID[3:0]		*	Identification Inputs Pull Down with Internal Resistors
FWH[3:0]		*	Address/Data Inputs
FWH4		*	FWH Cycle Initial
D/#F		*	Dual Bios/Full Chip Pull Down with Internal Resistors
U/#L		*	Upper 4M/Lower 4M Pull Down with Internal Resistors
R/#C	*		Row/Column Select
A[10:0]	*		Address Inputs
DQ[7:0]	*		Data Inputs/Outputs
#OE	*		Output Enable
#WE	*		Write Enable
RY/#BY	*		Ready/ Busy
VDD	*	*	Power Supply
VSS	*	*	Ground
VPP	*	*	Accelerate Program Power Supply
RSV	*	*	Reserved Pins
NC	*	*	No Connection

6. FUNCTIONAL DESCRIPTION

6.1 Interface Mode Selection and Description

This device can operate in two interface modes, one is Programmer interface mode, and the other is FWH interface mode. The IC pin of the device provides the control between these two interface modes. These interface modes need to be configured before power up or return from #RESET. When IC pin is set to high state, the device will be in the Programmer mode; while the IC pin is set to low state (or leaved no connection), it will be in the FWH mode. In Programmer mode, this device just behaves like traditional flash parts with 8 data lines. But the row and column address inputs are multiplexed. The row address are mapped to the higher internal address A[19:11]. And the column address are mapped to the lower internal address A[10:0]. For FWH mode, It complies with the FWH Interface Specification. Through the FWH[3:0] and FWH4 to communicate with the system chipset .

6.2 Read (Write) Mode

In Programmer interface mode, the read (write) operation of the W39V080FA is controlled by #OE (#WE). The #OE (#WE) is held low for the host to obtain (write) data from (to) the outputs (inputs). #OE is the output control and is used to gate data from the output pins. The data bus is in high impedance state when #OE is high. As for in the FWH interface mode, the read or write is determined by the "bit 0 & bit 1 of START CYCLE ". Refer to the FWH cycle definition and timing waveforms for further details.

6.3 Reset Operation

The #RESET input pin can be used in some application. When #RESET pin is at high state, the device is in normal operation mode. When #RESET pin is at low state, it will halt the device and all outputs will be at high impedance state. As the high state re-asserted to the #RESET pin, the device will return to read or standby mode, it depends on the control signals.

6.4 Accelerated Program Operation

The device provides accelerated program operations through the ACC function. This function is primarily intended to allow a faster manufacturing throughput in the factory.

6.5 Boot Block Operation and Hardware Protection at Initial- #TBL & #WP

There is a hardware method to protect the top boot block and other sectors. Before power on programmer, tie the #TBL pin to low state and then the top boot block will not be programmed/erased. If #WP pin is tied to low state before power on, the other sectors will not be programmed/erased.

In order to detect whether the boot block feature is set on or not, users can perform software command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address FFFF2(hex). You can check the DQ2/DQ3 at the address FFFF2 to see whether the #TBL/#WP pin is in low or high state. If the DQ2 is “0”, it means the #TBL pin is tied to high state. In such condition, whether boot block can be programmed/erased or not will depend on software setting. On the other hand, if the DQ2 is “1”, it means the #TBL pin is tied to low state, then boot block is locked no matter how the software is set. Like the DQ2, the DQ3 inversely mirrors the #WP state. If the DQ3 is “0”, it means the #WP pin is in high state, then all the sectors except the boot block can be programmed/erased. On the other hand, if the DQ3 is “1”, then all the sectors except the boot block are programmed/erased inhibited.

To return to normal operation, perform a three-byte command sequence (or an alternate single-byte command) to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

6.6 Sector Erase Command

Sector erase is a six bus cycles operation. There are two "unlock" write cycles, followed by writing the "set-up" command. Two more "unlock" write cycles then follows by the Sector erase command. The Sector address (any address location within the desired Sector) is latched on the rising edge of R/#C in programmer mode, while the command (30H) is latched on the rising edge of #WE.

Sector erase does not require the user to program the device prior to erase. When erasing a Sector, the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The automatic Sector erase begins after the erase command is completed, right from the rising edge of the #WE pulse for the last Sector erase command pulse and terminates when the data on DQ7, Data Polling, is "1" at which time the device returns to the read mode. Data Polling must be performed at an address within any of the sectors being erased.

Refer to the Erase Command flow Chart using typical command strings and bus operations.

6.7 Program Operation

The W39V080FA is programmed on a byte-by-byte basis. Program operation can only change logical data "1" to logical data "0." The erase operation, which changed entire data in main memory and/or boot block from "0" to "1", is needed before programming.

The program operation is initiated by a 4-byte command cycle (see Command Codes for Byte Programming). The device will internally enter the program operation immediately after the byte-program command is entered. The internal program timer will automatically time-out (9μS typ.-T_{BP}) once it is completed and then return to normal read mode. Data polling and/or Toggle Bits can be used to detect end of program cycle.

6.8 Dual BIOS

The W39V080FA provides a solution for Dual-BIOS application. In FWH mode, when D/#F is low, the device functions as a full-chip partition of 8M-bit which address ranges from FFFFFh to 00000h with A[19:0]. If D/#F is driven high, the device functions as a dual-block partition that each block consists of 4M-bit. For dual-block partition, there is only one 4M-bit block, either upper or lower, can be accessed. The U/#L pin selects either upper or lower 4M-bit block and its address ranges from 7FFFFh to 00000h with A[19:0]. When U/#L is low, the lower 4M-bit block will be selected; while, U/#L is high, the upper 4M-bit block will be selected.

6.9 Hardware Data Protection

The integrity of the data stored in the W39V080FA is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A #WE pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming and read operation are inhibited when V_{DD} is less than 2.0V typical.

(3) Write Inhibit Mode: Forcing #OE low or #WE high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

6.10 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ5, DQ6, and DQ7. Each of DQ7 and DQ6 provides a method for determining whether a program or erase operation is complete or in progress. The device also offers a hardware-based output signal, RY/#BY in programmer mode, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

6.10.1 DQ7: #Data Polling

The #Data Polling bit, DQ7, indicates whether an Embedded Program or Erase algorithm is in progress or completed. Data Polling is valid after the rising edge of the final #WE pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 and the complement of the data programmed to DQ7. Once the Embedded Program algorithm has completed, the device outputs the data programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, #Data Polling on DQ7 is active for about 1μS, and then the device returns to the read mode.

During the Embedded Erase algorithm, #Data Polling produces “0” on DQ7. Once the Embedded Erase algorithm has completed, #Data Polling produces “1” on DQ7. An address within any of the sectors selected for erasure must be provided to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, #Data Polling on DQ7 is active for about 100μS, and then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just before the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable (#OE) is set to low. That is, the device may change from providing status information to valid data on DQ7. Depending on when it samples the DQ7 output, the system may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ7-DQ0 will appear on successive read cycles.

6.10.2 RY/#BY: Ready/#Busy

The RY/#BY is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/#BY status is valid after the rising edge of the final #WE pulse in the command sequence. Since RY/#BY is an open-drain output, several RY/#BY pins can be tied together in parallel with a pull-up resistor to V_{DD}.

When the output is low (Busy), the device is actively erasing or programming. When the output is high (Ready), the device is in the read mode or standby mode.

6.10.3 DQ6: Toggle Bit

Toggle Bit on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete. Toggle Bit I may be read at any address, and is valid after the rising edge of the final #WE pulse in the command sequence (before the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either #OE to control the read cycles. Once the operation has completed, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for about 100μS, and then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors which are protected.

The system can use DQ6 to determine whether a sector is actively erasing. If the device is actively erasing (i.e., the Embedded Erase algorithm is in progress), DQ6 toggles. If a program address falls within a protected sector, DQ6 toggles for about 1 μs after the program command sequence is written, and then returns to reading array data.

6.10.4 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. DQ5 produces "1" under these conditions which indicates that the program or erase cycle was not successfully completed.

The device may output "1" on DQ5 if the system tries to program "1" to a location that was previously programmed to "0." Only the erase operation can change "0" back to "1." Under this condition, the device stops the operation, and while the timing limit has been exceeded, DQ5 produces "1."

Under both these conditions, the system must hardware reset to return to the read mode.

6.11 Identification Input pin ID[3:0]

These pins are part of mechanism that allows multiple parts to be used on the same bus. The boot device should be 0000b. And all the subsequent parts should use the up-count strapping.

6.12 Register

There are three kinds of registers on this device, the General Purpose Input Registers, the Block Lock Control Registers and Product Identification Registers. Users can access these registers through respective address in the 4Gbytes memory map. There are detail descriptions in the sections below.

6.12.1 General Purpose Inputs Register

This register reads the FGPI[4:0] pins on the W39V080FA.This is a pass-through register which can read via memory address FFBC0100(hex). Since it is pass-through register, there is no default value.

GPI Register Table

BIT	FUNCTION
7 – 5	Reserved
4	Read FGPI4 pin status
3	Read FGPI3 pin status
2	Read FGPI2 pin status
1	Read FGPI1 pin status
0	Read FGPI0 pin status

6.12.2 Block Locking Registers

This part provides 16 even 64Kbytes blocks, and each block can be locked by register control. These control registers can be set or clear through memory address. Below is the detail description.

Block Locking Registers type and access memory map Table

REGISTERS	REGISTERS TYPE	CONTROL BLOCK	DEVICE PHYSICAL ADDRESS	4GBYTES SYSTEM MEMORY ADDRESS
BLR15	R/W	15	0FFFFFh – 0F0000h	FFBF0002h
BLR14	R/W	14	0EFFFFh – 0E0000h	FFBE0002h
BLR13	R/W	13	0DFFFFh – 0D0000h	FFBD0002h
BLR12	R/W	12	0CFFFFh – 0C0000h	FFBC0002h
BLR11	R/W	11	0BFFFFh – 0B0000h	FFBB0002h
BLR10	R/W	10	0AFFFFh – 0A0000h	FFBA0002h
BLR9	R/W	9	09FFFFh – 090000h	FFB90002h
BLR8	R/W	8	08FFFFh – 080000h	FFB80002h
BLR7	R/W	7	07FFFFh – 070000h	FFB70002h
BLR6	R/W	6	06FFFFh – 060000h	FFB60002h
BLR5	R/W	5	05FFFFh – 050000h	FFB50002h
BLR4	R/W	4	04FFFFh – 040000h	FFB40002h
BLR3	R/W	3	03FFFFh – 030000h	FFB30002h
BLR2	R/W	2	02FFFFh – 020000h	FFB20002h
BLR1	R/W	1	01FFFFh – 010000h	FFB10002h
BLR0	R/W	0	00FFFFh – 000000h	FFB00002h

Block Locking Register Bits Function Table

BIT	FUNCTION
7 – 3	Reserved
2	Read Lock 1: Prohibit to read in the block where set 0: Normal read operation in the block where clear. This is default state.
1	Lock Down 1: Prohibit further to set or clear the Read Lock or Write Lock bits. This Lock Down Bit can only be set not clear. Only the device is reset or re-powered, the Lock Down Bit is cleared. 0: Normal operation for Read Lock or Write Lock. This is the default state.
0	Write Lock 1: Prohibited to write in the block where set. This is default state. 0: Normal programming/erase operation in the block where clear.

Register Based Block Locking Value Definitions Table

BIT [7:3]	BIT 2	BIT 1	BIT 0	RESULT
00000	0	0	0	Full Access.
00000	0	0	1	Write Lock. Default State.
00000	0	1	0	Locked Open (Full Access, Lock Down).
00000	0	1	1	Write Locked, Locked Down.
00000	1	0	0	Read Locked.
00000	1	0	1	Read & Write Locked.
00000	1	1	0	Read Locked, Locked Down.
00000	1	1	1	Read & Write Locked, Locked Down.

Read Lock

Any attempt to read the data of read locked block will result in “00H.” The default state of any block is unlocked upon power up. User can clear or set the write lock bit anytime as long as the lock down bit is not set.

Write Lock

This is the default state of blocks upon power up. Before any program or erase to the specified block, user should clear the write lock bit first. User can clear or set the write lock bit anytime as long as the lock down bit is not set. The write lock function is in conjunction with the hardware protect pins, #WP & TBL. When hardware protect pins are enabled, it will override the register block locking functions and write lock the blocks no matter how the status of the register bits. Reading the register bit will not reflect the status of the #WP or #TBL pins.

Lock Down

The default state of lock down bit for any block is unlocked. This bit can be set only once; any further attempt to set or clear is ignored. Only the reset from #RESET or #INIT can clear the lock down bit. Once the lock down bit is set for a block, then the write lock bit & read lock bit of that block will not be set or cleared, and keep its current state.

6.12.3 Product Identification Registers

There is an alternative software method to read out the Product Identification in both the Programmer interface mode and the FWH interface mode. Thus, the programming equipment can automatically matches the device with its proper erase and programming algorithms.

In the full-chip(8Mb) FWH interface mode, a read from FFBC, 0000(hex) can output the manufacturer code, DA(hex). A read from FFBC, 0001(hex) can output the device code, D3(hex).

For Dual-BIOS(4Mbx2) FWH mode , a read from FFBC, 0000(hex) can output the manufacturer code, DA(hex). A read from FFBC,0001(hex) can output the device code 93(hex).

In the software access mode, a JEDEC 3-byte command sequence can be used to access the product ID for programmer interface mode. A read from address 0000(hex) outputs the manufacturer code, DA(hex). A read from address 0001(hex) outputs the device code, D3(hex).” The product ID operation can be terminated by a three-byte command sequence or an alternate one-byte command sequence (see Command Definition table for detail).

6.13 Table of Operating Modes

6.13.1 Operating Mode Selection - Programmer Mode

MODE	PINS				
	#OE	#WE	#RESET	ADDRESS	DQ.
Read	V_{IL}	V_{IH}	V_{IH}	AIN	Dout
Write	V_{IH}	V_{IL}	V_{IH}	AIN	Din
Standby	X	X	V_{IL}	X	High Z
Write Inhibit	V_{IL}	X	V_{IH}	X	High Z/DOUT
	X	V_{IH}	V_{IH}	X	High Z/DOUT
Output Disable	V_{IH}	X	V_{IH}	X	High Z

6.13.2 Operating Mode Selection - FWH Mode

Operation modes in FWH interface mode are determined by "START Cycle" when it is selected. When it is not selected, its outputs (FWH[3:0]) will be disable. Please reference to the "FWH Cycle Definition".

Table of Command Definition

COMMAND DESCRIPTION	NO. OF Cycles (1)	1ST CYCLE		2ND CYCLE		3RD CYCLE		4TH CYCLE		5TH CYCLE		6TH CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read	1	A_{IN}	D_{OUT}										
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[5]	30
Byte Program	4	5555	AA	2AAA	55	5555	A0	A_{IN}	D_{IN}				
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit [4]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit [4]	1	XXXX	F0										

Notes:

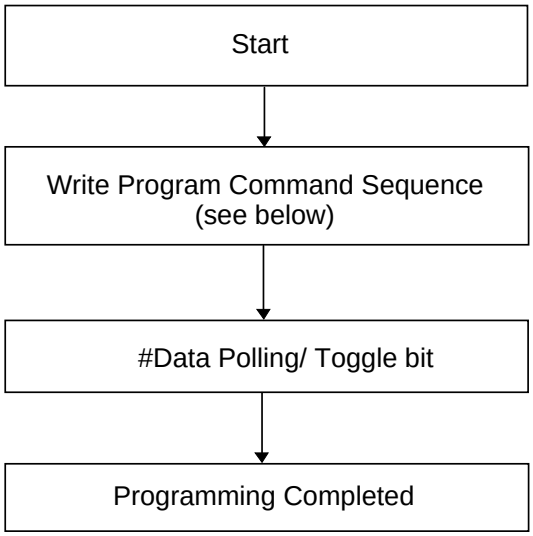
1. The cycle means the write command cycle not the FWH clock cycle.
2. The Column Address / Row Address are mapped to the Low / High order Internal Address. i.e. Column Address A[10:0] are mapped to the internal A[10:0], Row Address A[7:0] are mapped to the internal A[19:11]
3. Address Format: A14–A0 (Hex); Data Format: DQ7-DQ0 (Hex)
4. Either one of the two Product ID Exit commands can be used.
5. SA: Sector Address

SA = FXXXXh for Unique Sector15 (Boot Sector)	SA = 7XXXXh for Unique Sector7
SA = EXXXXh for Unique Sector14	SA = 6XXXXh for Unique Sector6
SA = DXXXXh for Unique Sector13	SA = 5XXXXh for Unique Sector5
SA = CXXXXh for Unique Sector12	SA = 4XXXXh for Unique Sector4
SA = BXXXXh for Unique Sector11	SA = 3XXXXh for Unique Sector3
SA = AXXXXh for Unique Sector10	SA = 2XXXXh for Unique Sector2
SA = 9XXXXh for Unique Sector9	SA = 1XXXXh for Unique Sector1
SA = 8XXXXh for Unique Sector8	SA = 0XXXXh for Unique Sector0

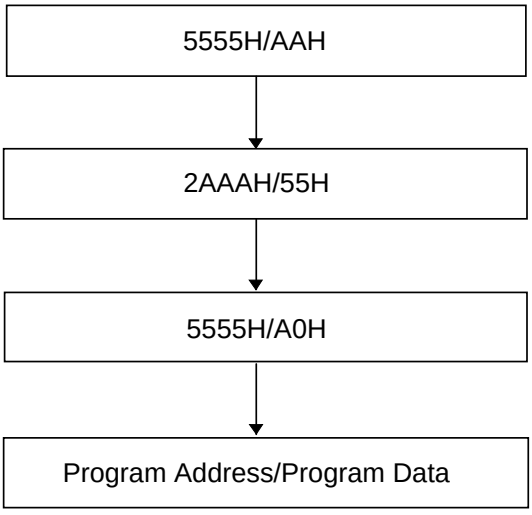
6.14 Fwh Cycle Definition

FIELD	NO. OF CLOCKS	DESCRIPTION
START	1	"1101b" indicates FWH Memory Read cycle; while "1110b" indicates FWH Memory Write cycle. 0000b" appears on FWH bus to indicate the initial
IDSEL	1	This one clock field indicates which FWH component is being selected.
MSIZE	1	Memory Size. There is always show “0000b” for single byte access.
TAR	2	Turned Around Time
ADDR	7	Address Phase for Memory Cycle. FWH supports the 28 bits address protocol. The addresses transfer most significant nibble first and least significant nibble last. (i.e. Address[27:24] on FWH[3:0] first, and Address[3:0] on FWH[3:0] last.)
SYNC	N	Synchronous to add wait state. "0000b" means Ready, "0101b" means Short Wait, "0110b" means Long Wait, "1001b" for DMA only, "1010b" means error, and other values are reserved.
DATA	2	Data Phase for Memory Cycle. The data transfer least significant nibble first and most significant nibble last. (i.e. DQ[3:0] on FWH[3:0] first, then DQ[7:4] on FWH[3:0] last.)

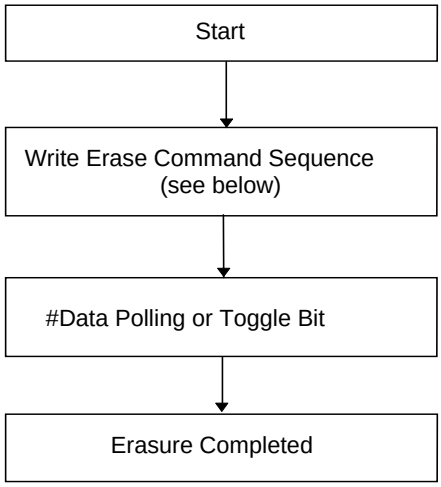
6.15 Embedded Programming Algorithm



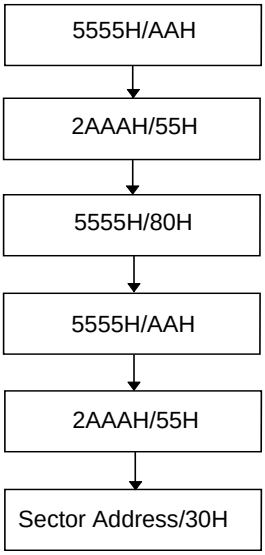
Program Command Sequence (Address/Command):



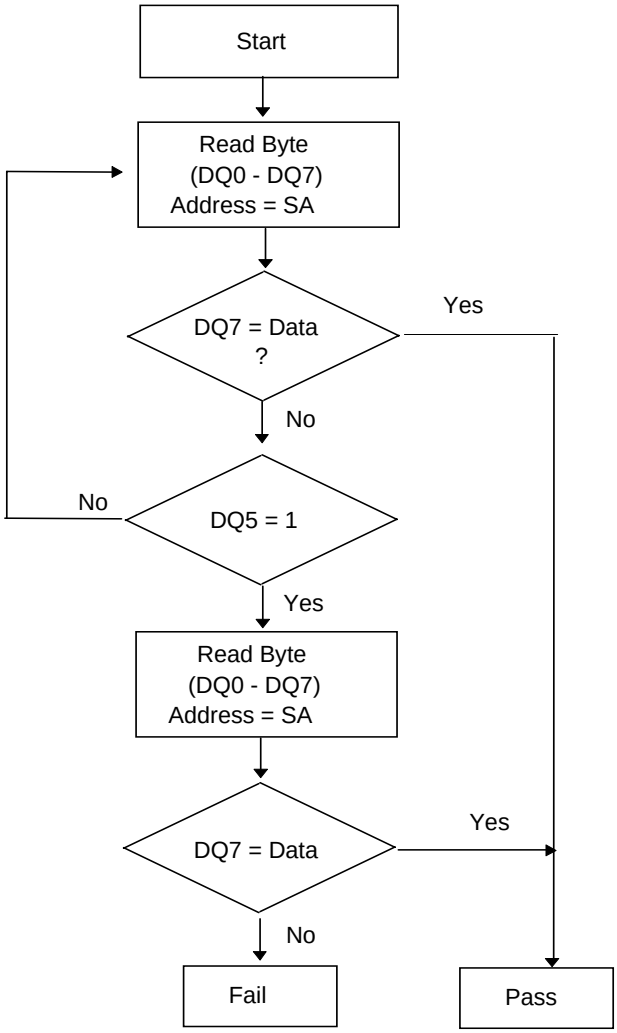
6.16 Embedded Erase Algorithm



Individual Sector Erase Command Sequence (Address/Command):

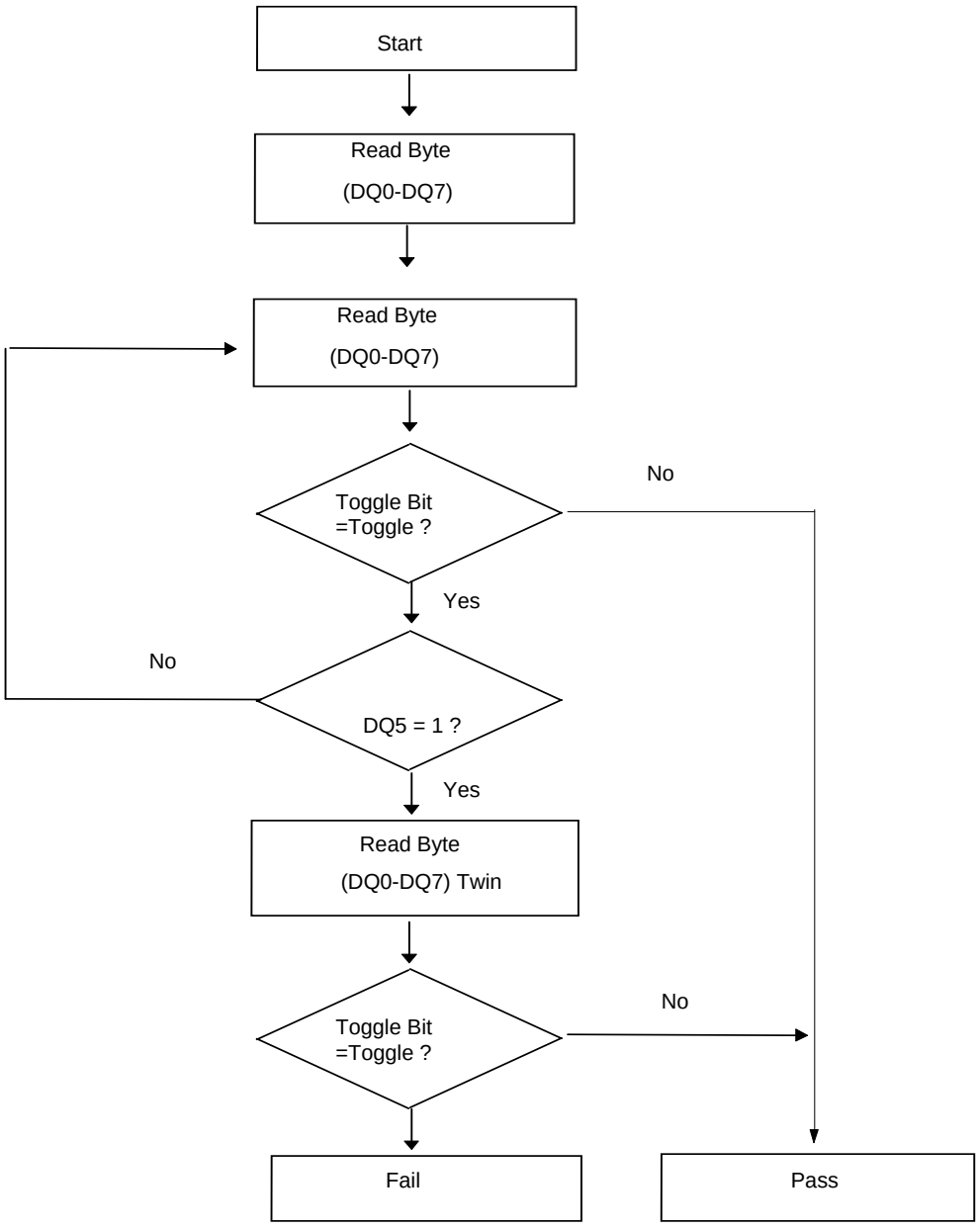


6.17 Embedded #Data Polling Algorithm



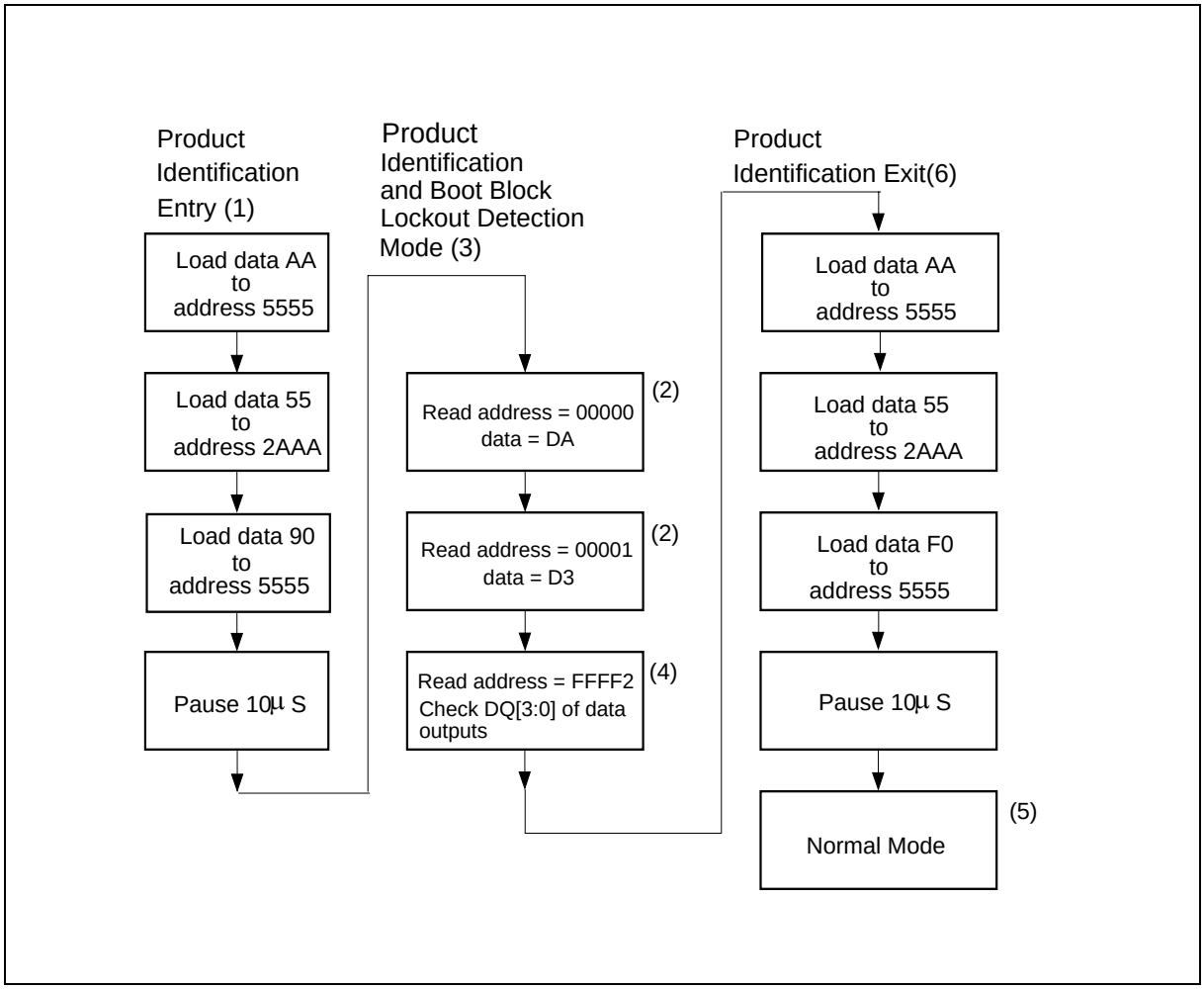
Note: SA = Valid address for programming .During a sector erase operation, a valid address is an address within any sector selected for erasure.

6.18 Embedded Toggle Bit Algorithm



Note: Recheck toggle bit because it may stop toggling as DQ5 changes to “1” .

6.19 Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A19 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block lockout detection mode if power down.

(4) The DQ[3:2] to indicate the sectors protect status as below:

	DQ2	DQ3
0	64Kbytes Boot Block Unlocked by #TBL hardware trapping	Whole Chip Unlocked by #WP hardware trapping Except Boot Block
1	64Kbytes Boot Block Locked by #TBL hardware trapping	Whole Chip Locked by #WP hardware trapping Except Boot Block

(5) The device returns to standard operation mode.

(6) Optional 1-write cycle (write F0 (hex.) at XXXX address) can be used to exit the product identification/boot block lockout detection.

7. DC CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +4.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential	-0.5 to V_{DD} +0.5	V
V_{PP} Voltage	-0.5 to +13	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +0.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings May adversely affect the life and reliability of the device.

7.2 Programmer interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current (read)	I_{CC1}	In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz	-	15	20	mA
Power Supply Current (erase/ write)	I_{CC2}	In Read or Write mode, all DQs open Address inputs = 3.0V/0V, at f = 3 MHz	-	35	45	mA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}	-	-	90	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{DD}	-	-	90	µA
Input Low Voltage	V_{IL}	-	-0.5	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.1mA	2.4	-	-	V

7.3 FWH interface Mode DC Operating Characteristics

(V_{DD} = 3.3V ± 0.3V, V_{SS}= 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current (read)	I_{CC1}	All I_{out} = 0A, CLK = 33 MHz, in FWH mode operation.	-	15	20	mA
Power Supply Current (erase/write)	I_{CC2}	All I_{out} = 0A, CLK = 33 MHz, in FWH mode operation.	-	35	45	mA
Standby Current 1	Isb1	FWH4 = 0.9 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} / 0.1 V_{DD} no internal operation	-	20	50	uA
Standby Current 2	Isb2	FWH4 = 0.1 V_{DD}, CLK = 33 MHz, all inputs = 0.9 V_{DD} /0.1 V_{DD} no internal operation.	-	3	10	mA
Input Low Voltage	V_{IL}	-	-0.5	-	0.3 V_{DD}	V
Input Low Voltage of #INIT	V_{ILI}	-	-0.5	-	0.2 V_{DD}	V
Input High Voltage	V_{IH}	-	0.5 V_{DD}	-	V_{DD} +0.5	V
Input High Voltage of #INIT Pin	V_{IHI}	-	1.35 V	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 1.5 mA	-	-	0.1 V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = -0.5 mA	0.9 V_{DD}	-	-	V

7.4 Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

7.5 Capacitance

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

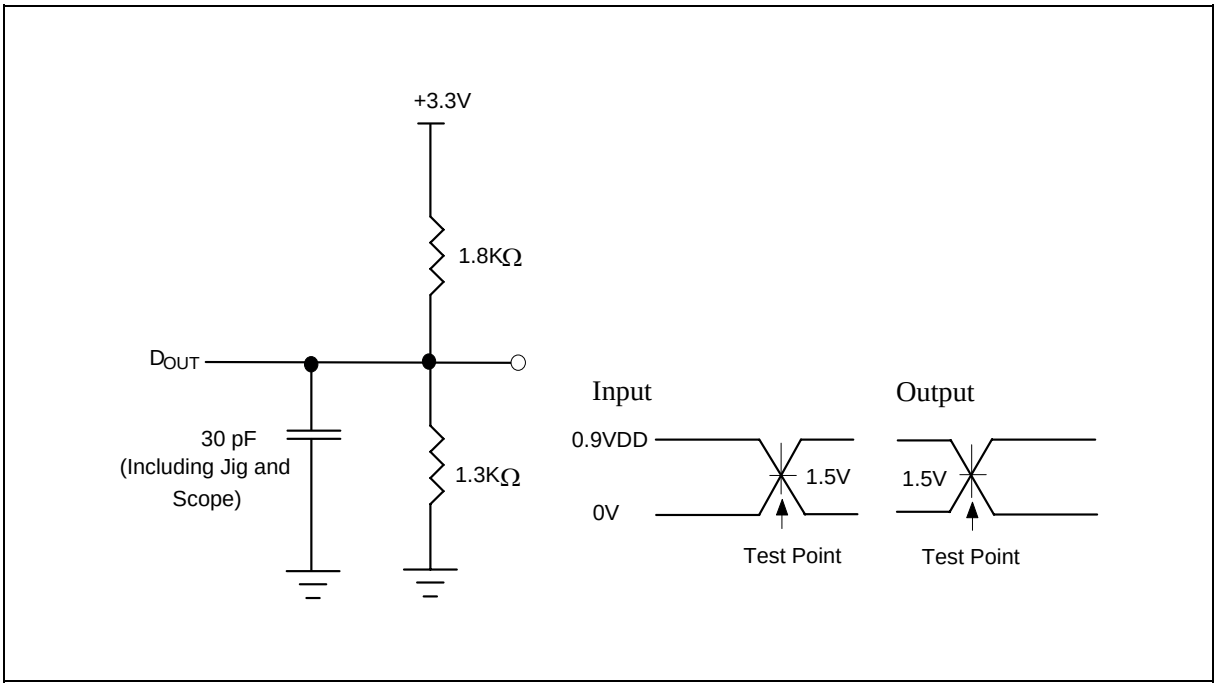
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

8. PROGRAMMER INTERFACE MODE AC CHARACTERISTICS

8.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 0.9 V_{DD}
Input Rise/Fall Time	< 5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 30 pF

8.2 AC Test Load and Waveform



Programmer Interface Mode AC Characteristics, continued

8.3 Read Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V080FA		UNIT
		MIN.	MAX.	
Read Cycle Time	T_{RC}	350	-	nS
Row / Column Address Set Up Time	T_{AS}	50	-	nS
Row / Column Address Hold Time	T_{AH}	50	-	nS
Address Access Time	T_{AA}	-	200	nS
Output Enable Access Time	T_{OE}	-	75	nS
#OE Low to Active Output	T_{OLZ}	0	-	nS
#OE High to High-Z Output	T_{OHZ}	-	35	nS
Output Hold from Address Change	T_{OH}	0	-	nS

8.4 Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Reset Time	T_{RST}	1	-	-	μS
Address Setup Time	T_{AS}	50	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
R/#C to Write Enable High Time	T_{CWH}	50	-	-	nS
#WE Pulse Width	T_{WP}	100	-	-	nS
#WE High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	50	-	-	nS
#OE Hold Time	T_{OEH}	0	-	-	nS
Byte programming Time	T_{BP}	-	9	250	μS
Sector Erase Cycle Time (Note (c))	T_{PEC}	-	0.9	6	S
Program/Erase Valid to RY/#BY Delay	T_{BUSY}	90	-	-	nS

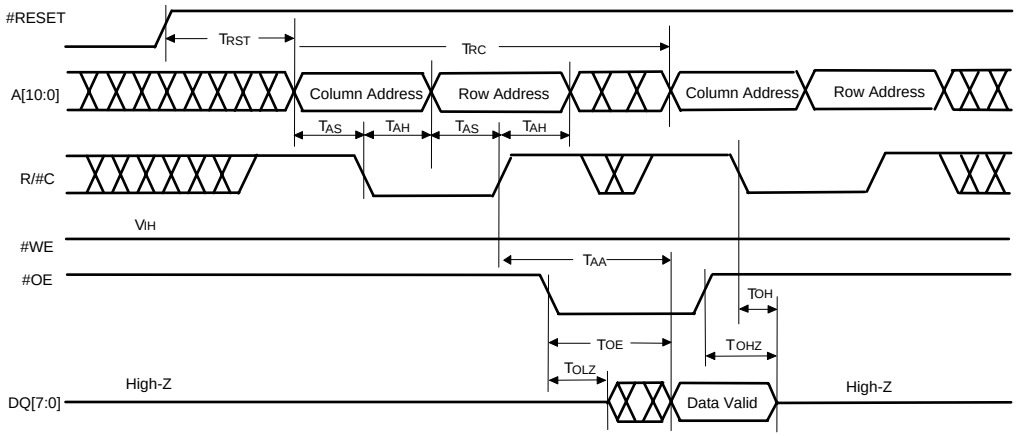
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and
(b) low level signal's reference level is input low. Ref. to the AC testing condition.
(c) Exclude 00H pre-program prior to erasure. (In the pre-programming step of the embedded erase algorithm, all bytes are programmed to 00H before erasure

8.5 Data Polling and Toggle Bit Timing Parameters

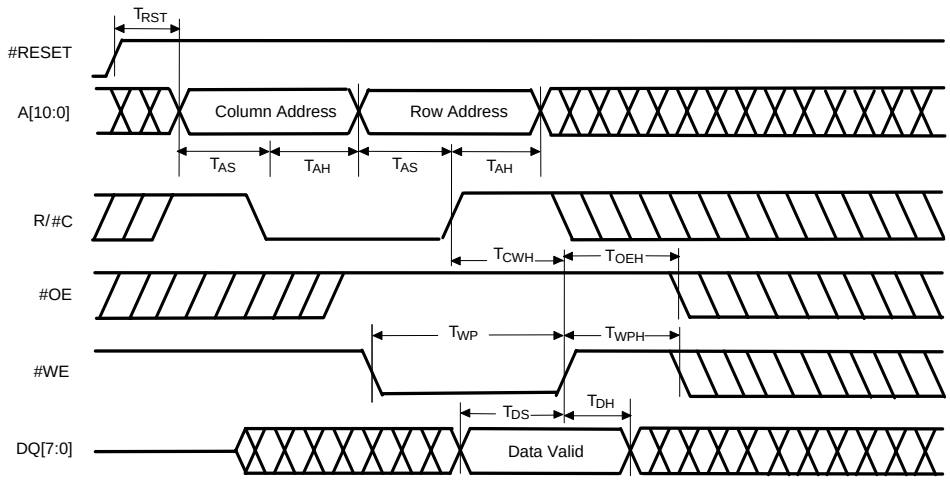
PARAMETER	SYMBOL	W39V080FA		UNIT
		MIN.	MAX.	
#OE to Data Polling Output Delay	T_{OEP}	-	40	nS
#OE to Toggle Bit Output Delay	T_{OET}	-	40	nS
Toggle or Polling interval	---	50	-	mS

9. TIMING WAVEFORMS FOR PROGRAMMER INTERFACE MODE

9.1 Read Cycle Timing Diagram

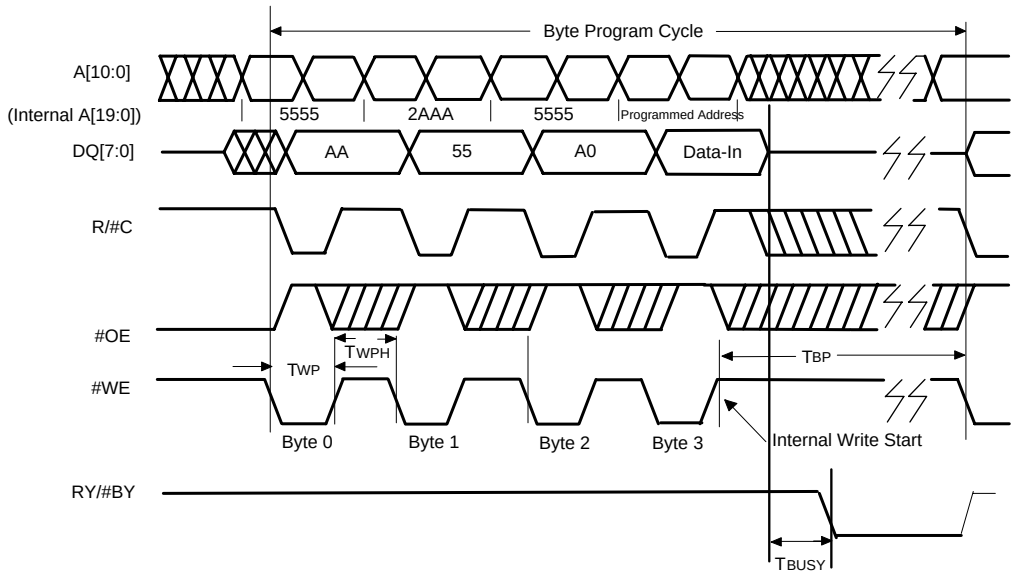


9.2 Write Cycle Timing Diagram



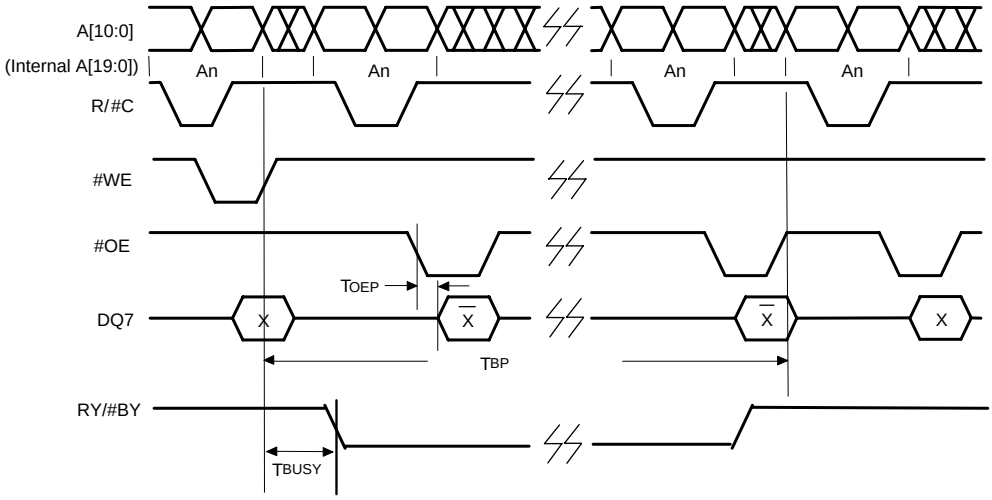
Timing Waveforms for Programmer Interface Mode, continued

9.3 Program Cycle Timing Diagram



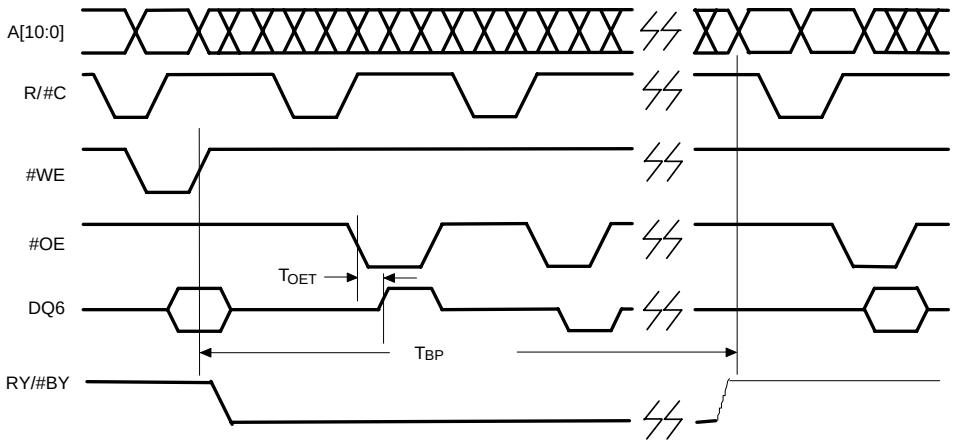
Note: The internal address A[19:0] are converted from external Column/Row address.
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[8:0] are mapped to the internal A[19:11].

9.4 #DATA Polling Timing Diagram

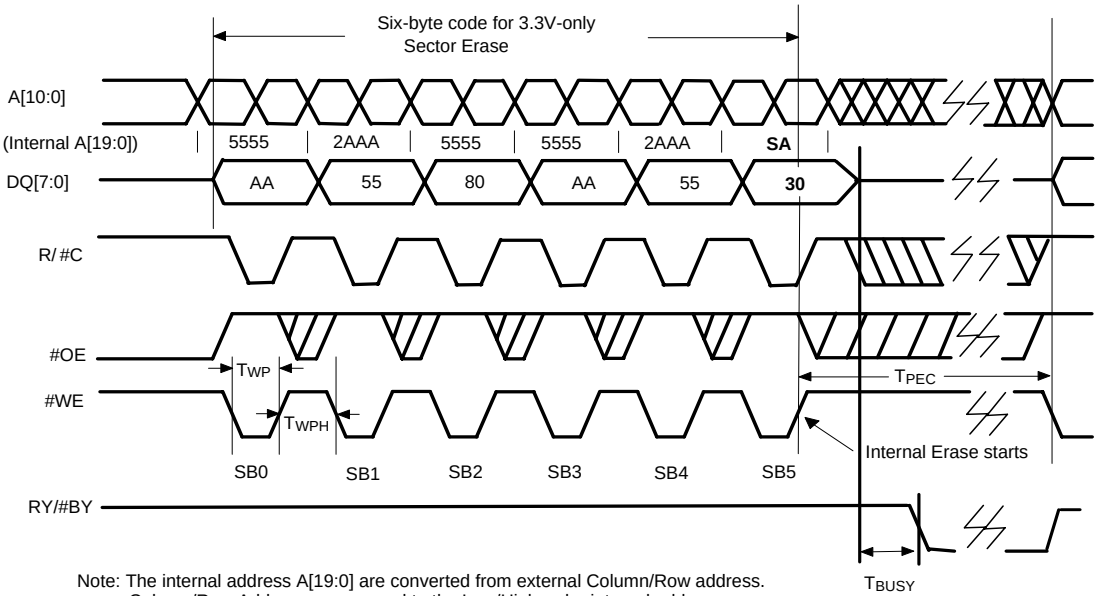


Timing Waveforms for Programmer Interface Mode, continued

9.5 Toggle Bit Timing Diagram



9.6 Sector Erase Timing Diagram



Note: The internal address A[19:0] are converted from external Column/Row address.
Column/Row Address are mapped to the Low/High order internal address.
i.e. Column Address A[10:0] are mapped to the internal A[10:0],
Row Address A[8:0] are mapped to the internal A[19:11].
SA = Sector Address, Please ref. to the "Table of Command Definition"

10. FWH INTERFACE MODE AC CHARACTERISTICS

10.1 AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.6 V_{DD} to 0.2 V_{DD}
Input Rise/Fall Slew Rate	1 V/nS
Input/Output Timing Level	0.4V_{DD} / 0.4V_{DD}
Output Load	1 TTL Gate and C_L = 10 pF

10.2 Read/Write Cycle Timing Parameters

(V_{DD} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYMBOL	W39V080FA		UNIT
		MIN.	MAX.	
Clock Cycle Time	T_{CYC}	30	-	nS
Input Set Up Time	T_{SU}	7	-	nS
Input Hold Time	T_{HD}	0	-	nS
Clock to Data Valid	T_{KQ}	2	11	nS

Note: Minimum and Maximum time have different load. Please refer to PCI specification.

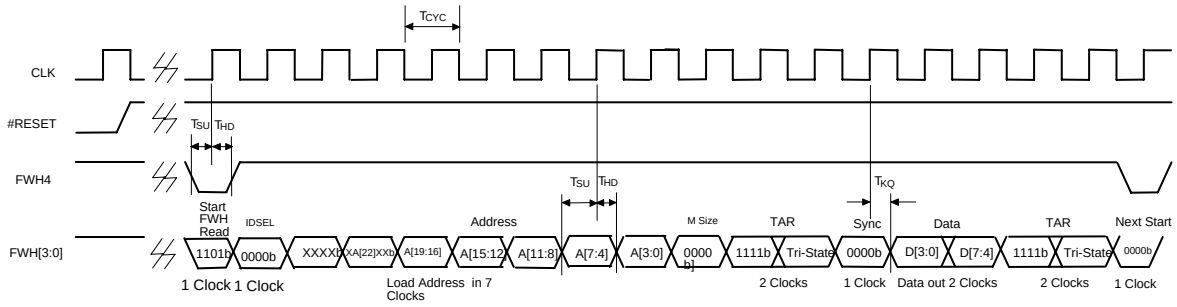
10.3 Reset Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VDD stable to Reset Active	T_{PRST}	1	-	-	mS
Clock Stable to Reset Active	T_{KRST}	100	-	-	µS
Reset Pulse Width	T_{RSTP}	100	-	-	nS
Reset Active to Output Float	T_{RSTF}	-	-	50	nS
Reset Inactive to Input Active	T_{RST}	10	-	-	µS

Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is input high and
(b) low level signal's reference level is input low.
Please refer to the AC testing condition.

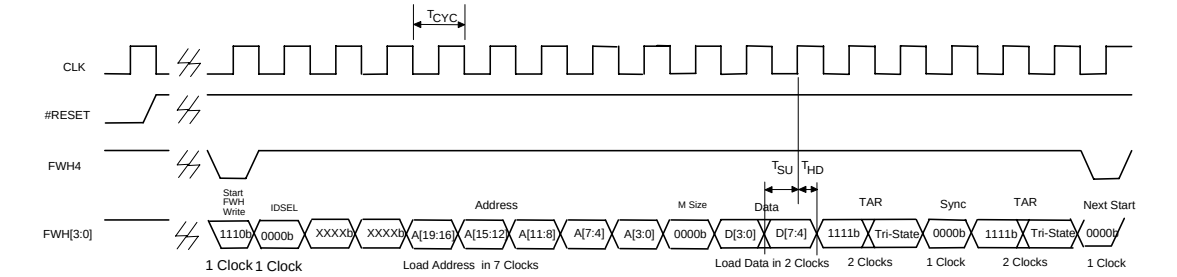
11. TIMING WAVEFORMS FOR FWH INTERFACE MODE

11.1 Read Cycle Timing Diagram



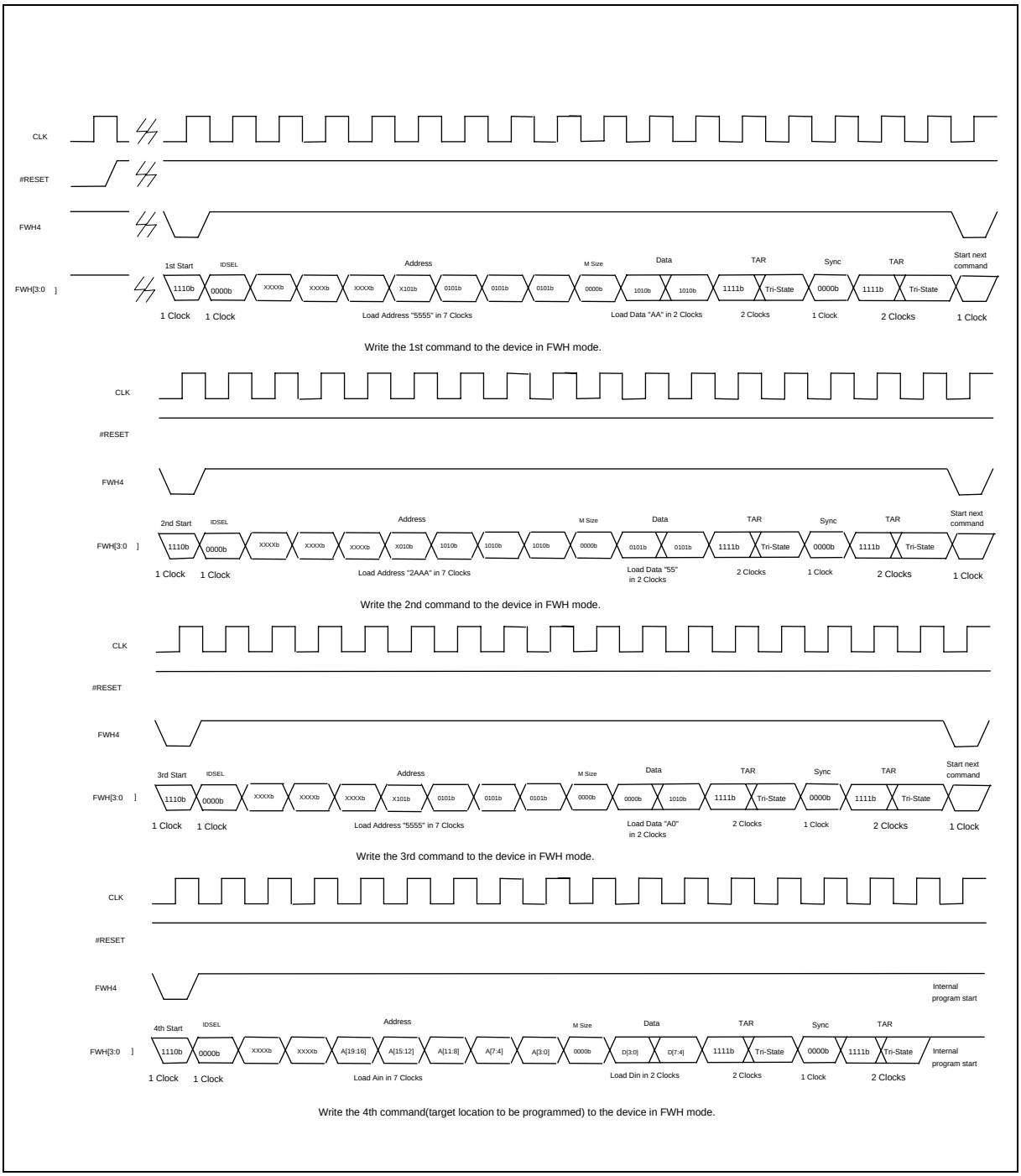
Note: When A22 = high, the host will read the BIOS code from the FWH device.
While A22 = low, the host will read the GPI (Add = FFBC0100) or
Product ID (Add = FFBC0000/FFBC0001) from the FWH device

11.2 Write Cycle Timing Diagram



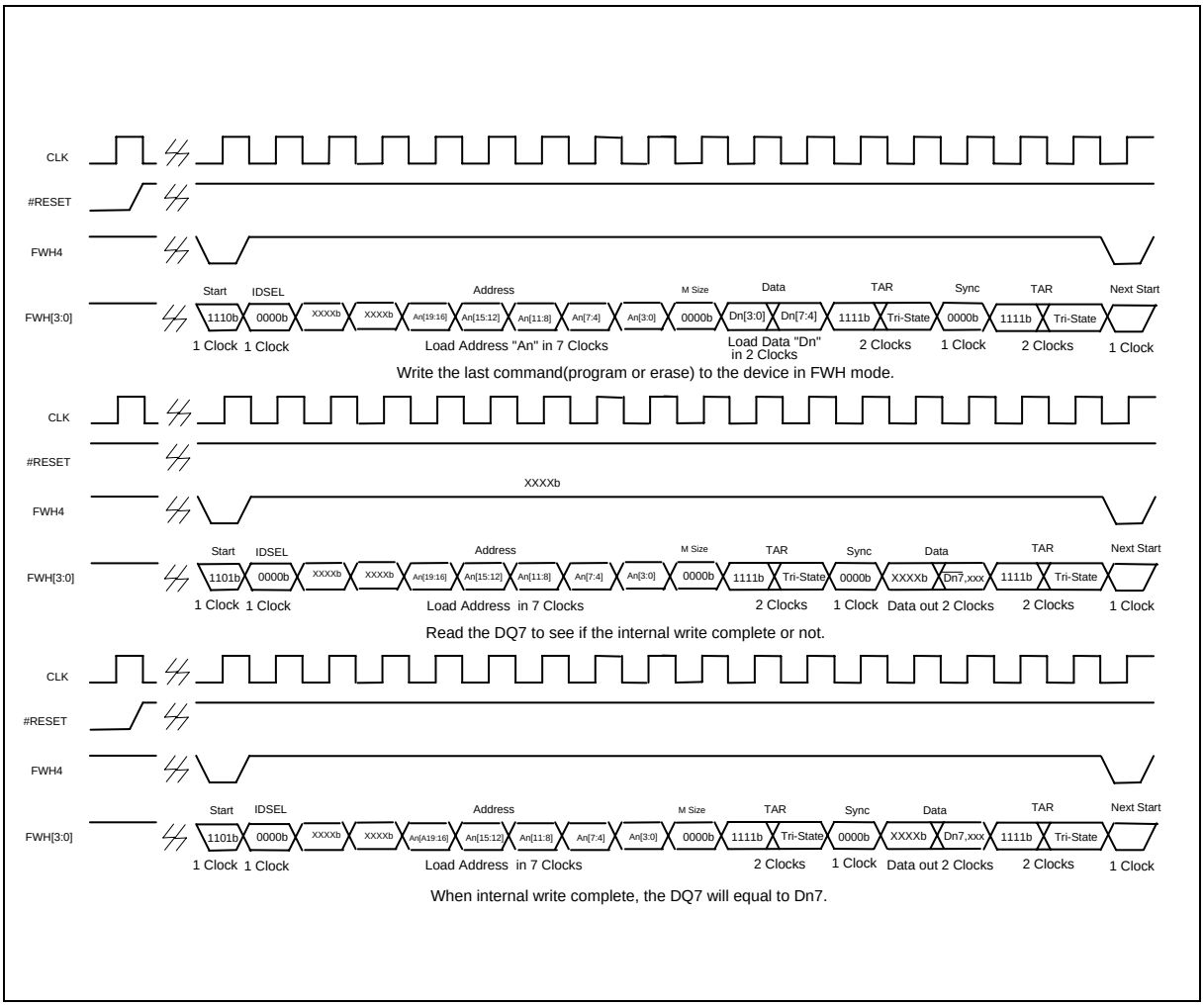
Timing Waveforms, for FWH Interface Mode, continued

11.3 Program Cycle Timing Diagram



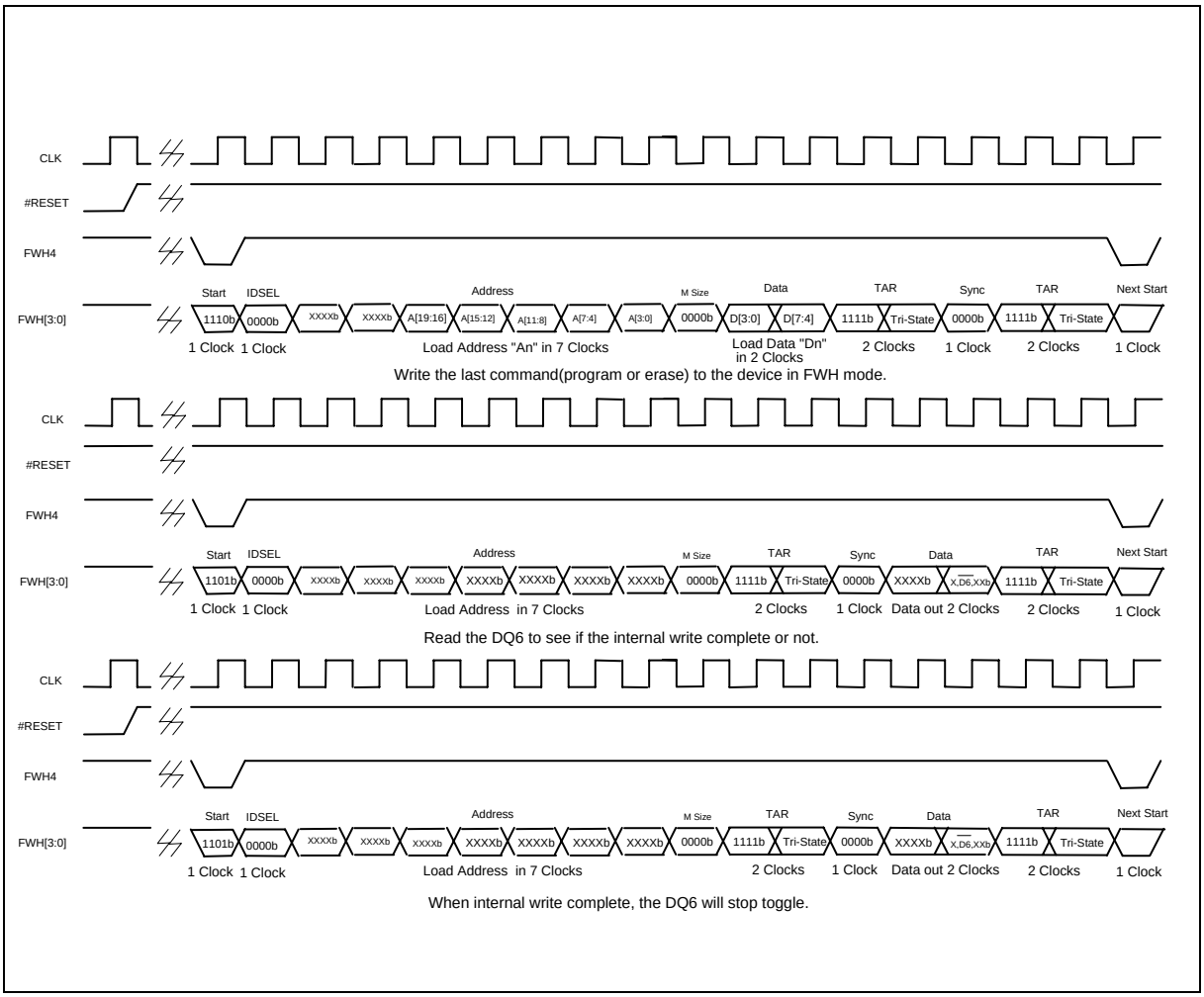
Timing Waveforms for FWH Interface Mode, continued

11.4 #DATA Polling Timing Diagram



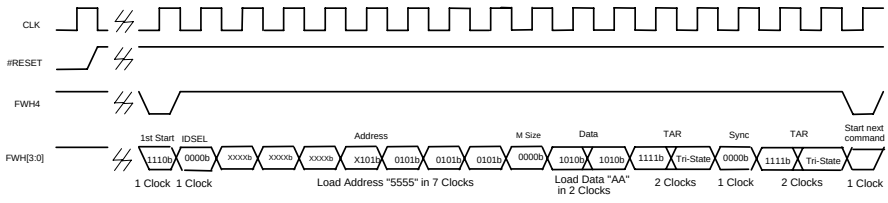
Timing Waveforms for FWH Interface Mode, continued

11.5 Toggle Bit Timing Diagram

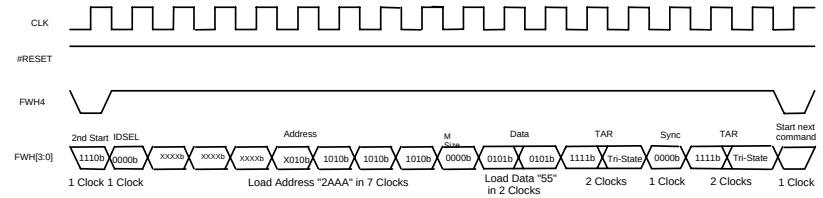


Timing Waveforms for FWH Interface Mode, continued

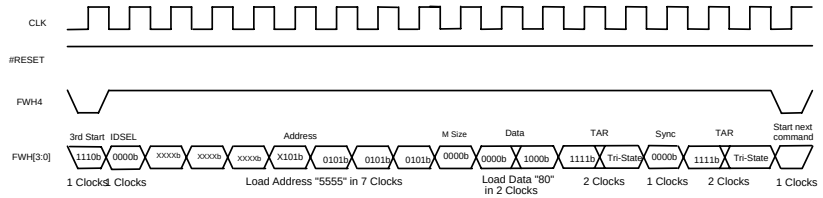
11.6 Sector Erase Timing Diagram



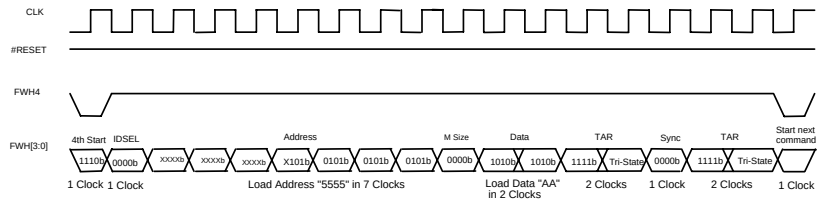
Write the 1st command to the device in FWH mode.



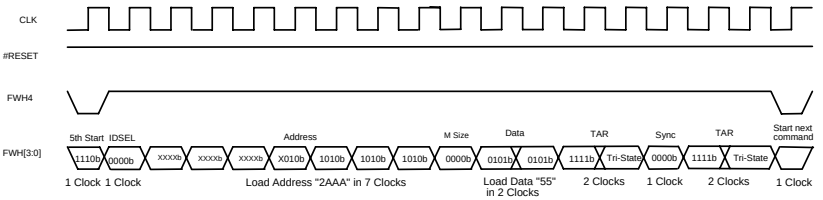
Write the 2nd command to the device in FWH mode.



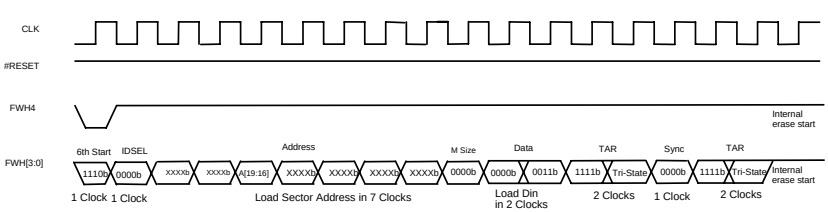
Write the 3rd command to the device in FWH mode.



Write the 4th command to the device in FWH mode.



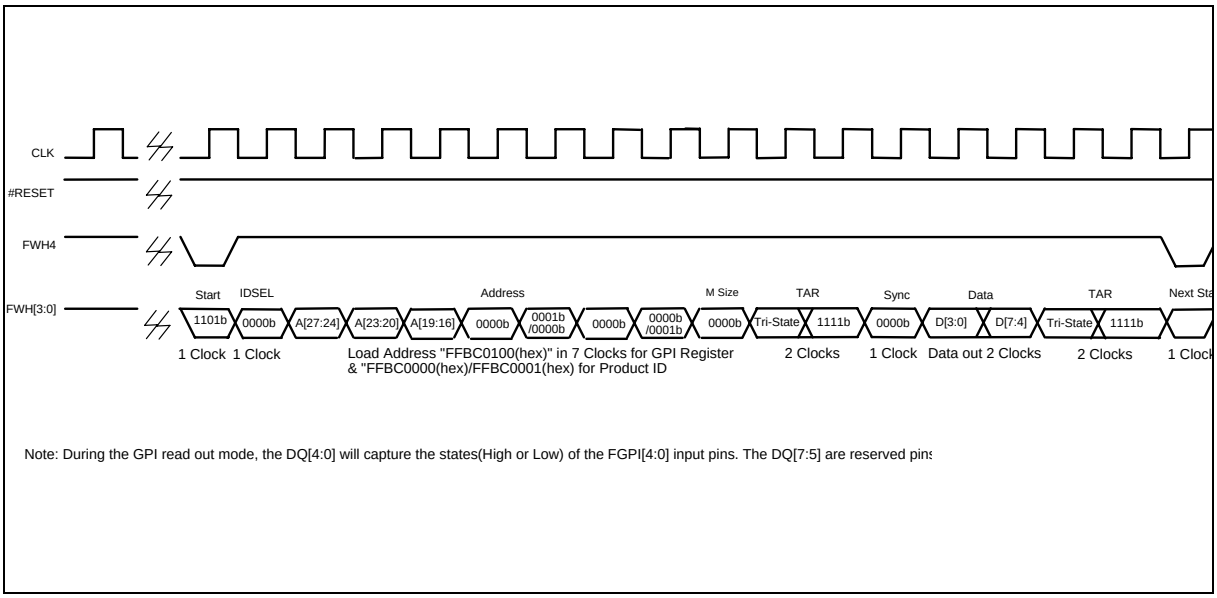
Write the 5th command to the device in FWH mode.



Write the 6th command(target sector to be erased) to the device in FWH mode.

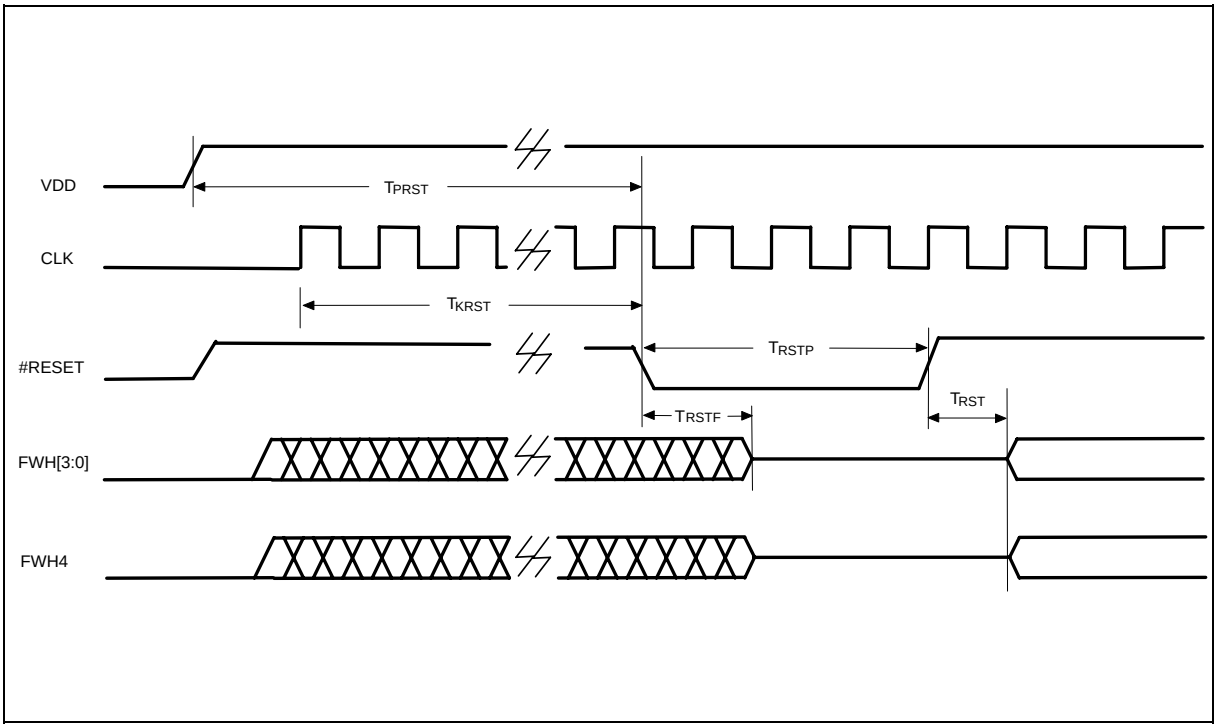
Timing Waveforms for FWH Interface Mode, continued

11.7 FGPI Register/Product ID Readout Timing Diagram



Note: During the GPI read out mode, the DQ[4:0] will capture the states(High or Low) of the FGPI[4:0] input pins. The DQ[7:5] are reserved pins

11.8 Reset Timing Diagram



12. ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	FWH MODE POWER SUPPLY CURRENT TYP. (mA)	FWH MODE STANDBY VDD CURRENT TYP. (uA)	PACKAGE
W39V080FAP	11	15	20	32L PLCC
W39V080FAQ	11	15	20	32L STSOP
W39V080FAT	11	15	20	40L TSOP
W39V080FAPZ	11	15	20	32L PLCC Lead free
W39V080FAQZ	11	15	20	32L STSOP Lead free
W39V080FATZ	11	15	20	40L TSOP Lead free

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

13. HOW TO READ THE TOP MARKING

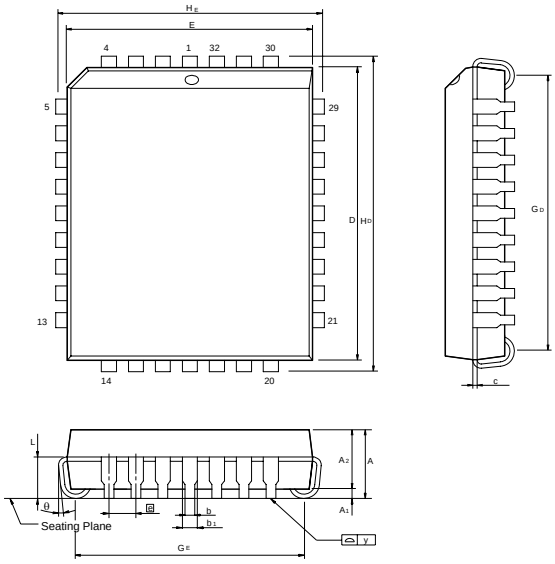
Example: The top marking of 32-pin STSOP W39V080FAQZ

1st line: Winbond logo
2nd line: the part number: W39V080FAQZ
3rd line: the lot number
4th line: the tracking code: 149 O B SA

149: Packages made in '01, week 49
O: Assembly house ID: A means ASE, O means OSE, ...etc.
B: IC revision; A means version A, B means version B, ...etc.
SA: Process code
Z: Lead free

14. PACKAGE DIMENSIONS

14.1 32L PLCC

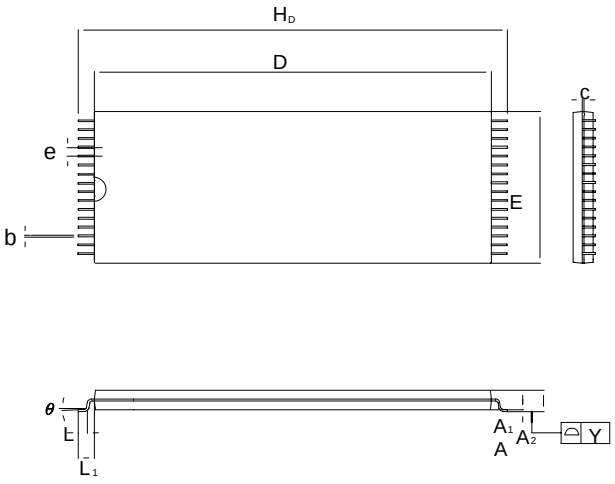


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0	—	10	0	—	10

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusio
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection sepc.

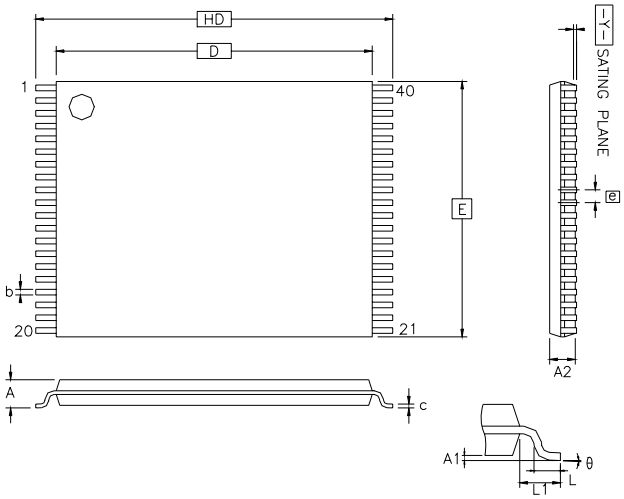
14.2 32L STSOP (8X14mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			0.047			1.20
A_1	0.002		0.006	0.05		0.15
A_2	0.035	0.040	0.041	0.95	1.00	1.05
b	0.007	0.009	0.010	0.17	0.22	0.27
c	0.004	-----	0.008	0.10	-----	0.21
D		0.488			12.40	
E		0.315			8.00	
H_D		0.551			14.00	
e		0.020			0.50	
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1		0.031			0.80	
Y	0.000		0.004	0.00		0.10
θ	0	3	5	0	3	5

Package Dimensions, continued

14.3 40L TSOP (10 mm x 20 mm)



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.007	0.009	0.011
c	0.10	—	0.20	0.004	—	0.008
D	18.30	18.40	18.50	0.720	0.724	0.728
E	9.90	10.00	10.10	0.390	0.394	0.398
HD	19.80	20.00	20.20	0.780	0.787	0.795
e	0.50 BASIC			0.020 BASIC		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
θ	0°	3°	5°	0°	3°	5°
Y	—	—	0.10	—	—	0.004

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 25, 2004	-	Initial Issued
A2	Jan. 05, 2005	8	Add 6.11 Identification Input pin ID[3:0] item
			Add 6.12.3 Product Identification Registers Dual bios device ID 93(hex)
A3	April 14, 2005	35	Add important notice
A4	Oct. 3, 2005	3	Revise endurance 10K cycles to 30K cycles
A5	Dec. 13, 2005	8, 16	Revise 6.10.4 DQ5: Exceeded Timing Limits description, and page16 Embedded Toggle Bit Algorithm

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