W83176R-735
Data Sheet

WINBOND
3 DIMM DDR ZERO DELAY BUFFER FOR SIS CHIPSET

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1. GENERAL DESCRIPTION

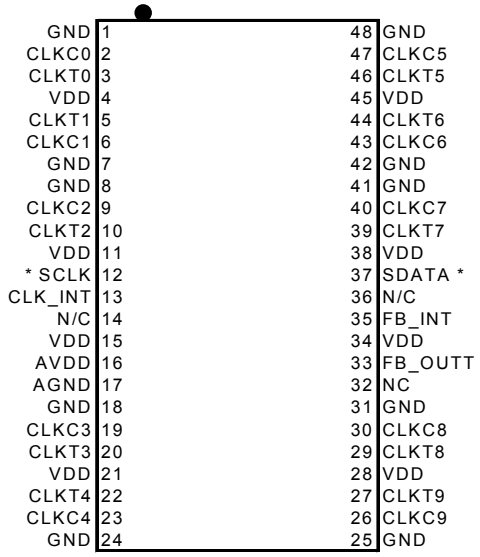
The W83176R-735 is a 2.5V Zero-delay D.D.R. Clock buffer designed for SiS system. W83176R-735 can support 3 D.D.R. DRAM DIMMs.

The W83176R-735 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-735 accepts a reference clock as its input and runs on 2.5V supply.

2. FEATURES

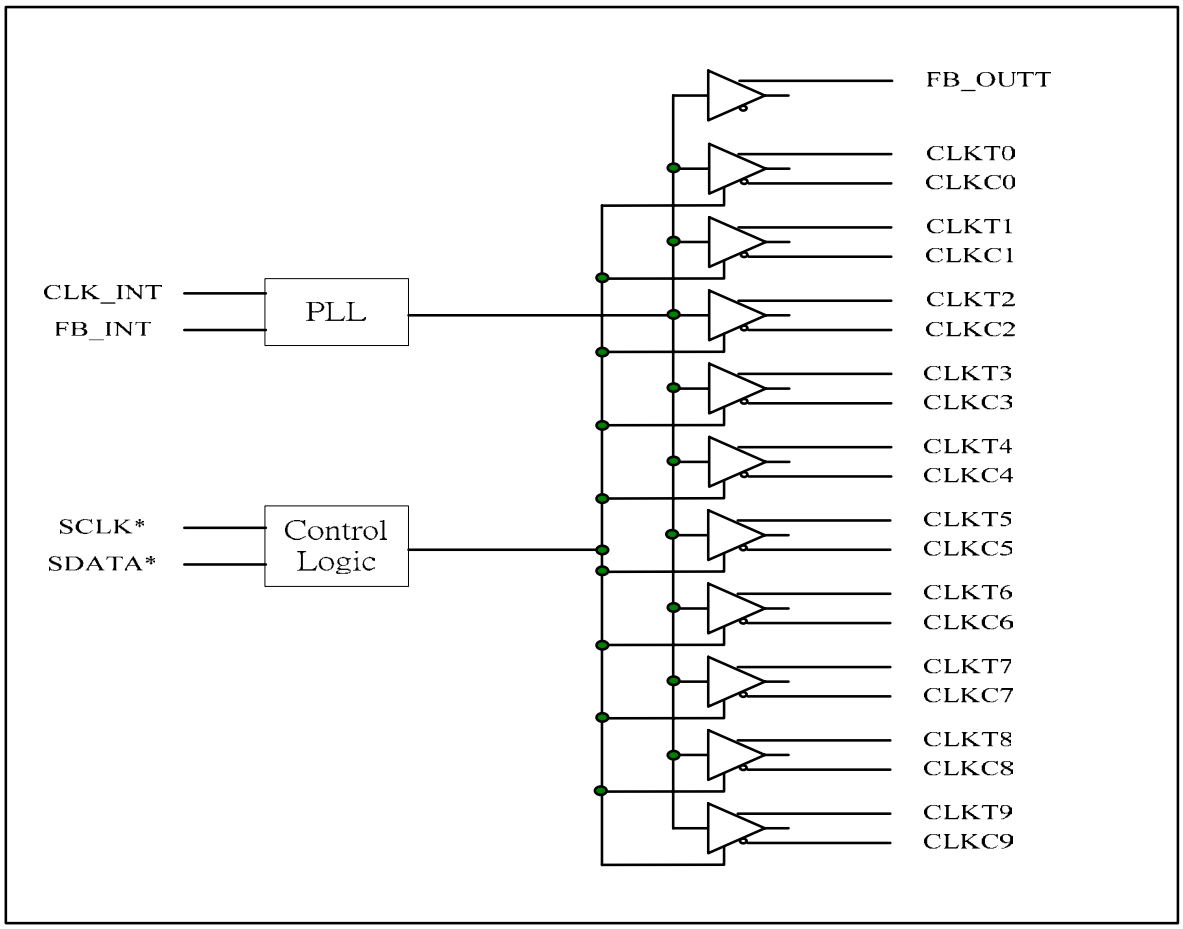
- Zero-delay clock outputs
- Feedback pins for synchronous
- Supports up to 3 D.D.R. DIMMs
- One pairs of additional outputs for feedback
- Low Skew outputs (<100 pS)
- Supports 400 MHz D.D.R. SDRAM
- I^2C 2-Wire serial interface and supports Byte or Block Date RW
- Packaged in 48-pin SSOP

3. PIN CONFIGURATION



*: Internal pull-up resistor 120K to VDD

4. BLOCK DIAGRAM



5. PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

*- Internal 120KΩ pull-up

5.1 Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CLKC[9:0]	26, 30, 40, 43, 47, 23, 19, 9, 6, 2	OUT	Complementory Clocks of differential pair outputs
CLKT[9:0]	27, 29, 39, 44, 46, 22, 20, 10, 5, 3	OUT	True Clocks of differential pair outputs
SDATA *	37	I/O	Serial data of I^2C 2-wire control interface Internal pull-up resistor 120K to Vdd
SCLK *	12	IN	Serial clock of I^2C 2-wire control interface Internal pull-up resistor 120K to Vdd
CLK_INT	13	IN	True reference clock input, 3.3V tolerant input
NC	14, 32, 36	NONE	Not connected
FB_OUTT	33	OUT	True Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
FB_INT	35	IN	True Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.

5.2 Power Pins

SYMBOL	PIN	FUNCTION
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground
V_{DD}	4, 11, 15, 21, 28, 34, 38, 45	Power Supply 2.5V
AVDD	16	Analog power supply, 2.5V
AGND	17	Analog ground

6. REGISTER 0 ~ REGISTER 4 RESERVED

6.1 Register 5: Output Control (1 = Active, 0 = Inactive) (Default = FFH)

BIT	@POWERUP	PIN	DESCRIPTION
7	1	2, 3	CLKC0, CLKT0 output control
6	1	6, 5	CLKC1, CLKT1 output control
5	1	9, 10	CLKC2, CLKT2 output control
4	1	19, 20	CLKC3, CLKT3 output control
3	1	23, 22	CLKC4, CLKT4 output control
2	1	26, 27	CLKC9, CLKT9 output control
1	1	-	Reserved
0	1	-	Reserved

6.2 Register 6: Output Control (1 = Active, 0 = Inactive) (Default = FFH)

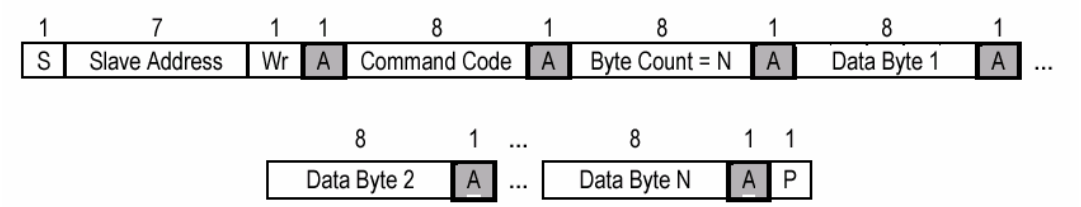
BIT	@POWERUP	PIN	DESCRIPTION
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	30, 29	CLKC8, CLKT8 output control
3	1	40, 39	CLKC7, CLKT7 output control
2	1	43, 44	CLKC6, CLKT6 output control
1	1	47, 46	CLKC5, CLKT5 output control
0	1	-	Reserved

7. ACCESS INTERFACE

The W83176R-735 provides I^{2}C Serial Bus for microprocessor to read/write internal registers. In the W83176R-735 is provided Block Read/Block Write and Byte-Data Read/Write protocol. The I^{2}C write address is defined at **0xD4**. The I^{2}C read address is defined at **0xD5**.

Block Read and Block Write Protocol

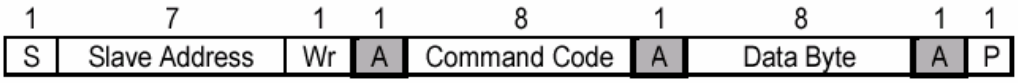
7.1 Block Write Protocol



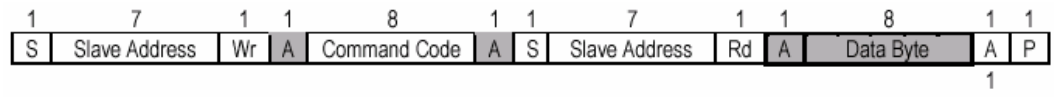
7.2 Block Read Protocol

In block mode, the command code must filled 00H

7.3 Byte Write Protocol



7.4 Byte Read Protocol



8. SPECIFICATIONS

8.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or VDD).

SYMBOL	PARAMETER	RATING
VDD, AVDD	Voltage on any pin with respect to GND	-0.5V to +3.6V
T_{STG}	Storage Temperature	-65°C to +150°C
T_B	Ambient Temperature	-55°C to +125°C
T_A	Operating Temperature	0°C to +70°C

8.2 A.C. Characteristics

VDD = AVDD = 2.5V ±5 %, TA = 0°C to +70°C, Test load = 10 pF

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Operating Clock Frequency	FIN	100		200	MHz	
Input Clock Duty Cycle	Dtin	40		60	%	
Dynamic Supply Current	Idd			300	mA	Fin =100 to 200 MHz
Cycle to Cycle Jitter	C-Cjitter			200	pS	Fout =100 to 200 MHz
Output to Output Skew	Tskew			100	pS	Fout =100 to 200 MHz
Output Clock Rise Time	Tor	650		950	pS	Fout =100 to 200 MHz
Output Clock Fall Time	Tof	650		950	pS	Fout =100 to 200 MHz
Output Clock Duty Cycle	Dtot	45		55	%	Fout =100 to 200 MHz
Output Differential-pair Crossing Voltage	Voc	(VDD/2) -0.2	VDD/ 2	(VDD/2) + 0.2	V	Fout =100 to 200 MHz

8.3 D.C. Characteristics

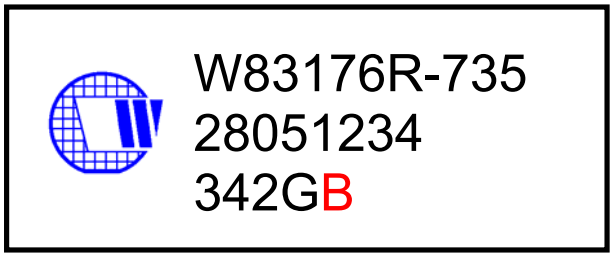
VDD = AVDD = 2.5V ±5%, TA = 0°C to +70°C

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
SDATA, SCLK Input Low Voltage	SV_{IL}			1.0	Vdc	
SDATA, SCLK Input High Voltage	SV_{IH}	2.2			V_{dc}	
CLKIN, FBIN Input Voltage Low	V_{IL}			0.4	V_{dc}	Fin = 100 to 200 MHz
CLKIN, FBIN Input Voltage High	V_{IH}	2.1			V_{dc}	Fin = 100 to 200 MHz
Input Pin Capacitance	C_{IN}			5	pF	
Output Pin Capacitance	C_{OUT}			6	pF	
Input Pin Inductance	L_{IN}			7	nH	

9. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83176R_735	48-pin SSOP	Commercial, 0°C to +70°C

10. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-735

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

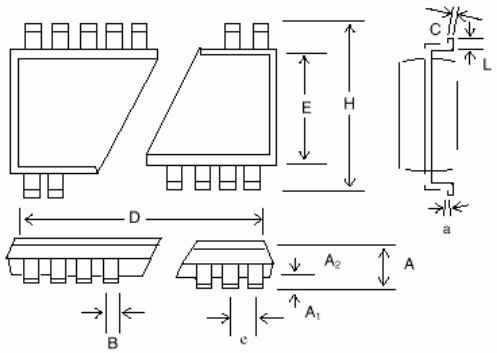
3rd line: Tracking code 342 G B

342: packages made in '2003, week 42

G: assembly house ID; O means OSE, G means GR

B: IC revision

11. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
		n.a.	All of the versions before 0.50 are for internal use.
0.5	12/18/03	3.7	Correction IC version, add register default value and correction some description and default value
1.0	05/06/04		Update to web
1.1	04/13/2005		Add disclaimer

Important Notice

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