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W83792AD/D
W83792AG/G

Winbond
H/W Monitoring IC
(CSB Version)

Date :2006 Apr. Revision: 0.9

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W83792AD/D
Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1		Aug-27-2003		N/A	Move Low Bit I/II to AEh and AFh
2		Aug-27-2003		N/A	Add Description of ASF Severity/Offset
3		Sep-12-2003	0.6	N/A	Update register
4	70-72	Sep-16-2003	0.6.1.	N/A	Update Application circuit
5	12-34	Nov-06-2003	0.7	N/A	Add the part of “Function Description”
6		Jan-05-2004	0.82	N/A	Combining with W83792D and W83792AD in one datasheet. Move Low Bit I/II to 3Eh and 3Fh
7		Dec-13-2004	0.83	N/A	Add description on Voltage translation.
8	11 20 39 45 48	Mar-01-2005	0.85	N/A	The Deletion of Vin4 4.096V(Voltage mode) Modify Monitor negative voltage Update voltage convert formula Modify Device Version ID 13h for C version. Modify Temperature Offset Attribute R/W
9	5-6 11 20 45 47 39 88 90-97	Nov-10-2005	0.86	N/A	Modify the W83792AD/D pin outputs define for BSA version. PIN25 and PIN26 pins are High active for Thermtrip. PIN35 is VCOREB/VIN4. Modify the PIN35 descriptions. VCOREB input detect range is 0~2.048V and Vin4 is 0~4.096V. Added the PIN37 VREF reference voltage is equal to 3.6V. Modify the monitor the negative voltage for VREF equals 3.6V. Modify Device Version ID 11h for B version CR [49h] and Pin control register. CR [4Bh] bit7 Modify Diode Selection Register CR[59h] power on value. Modify Low Bit I/II to AEh and AFh. The voltage Calculation with Low Bit I/II to AEh and AFh Modify top marking for the BSA version. Updated application circuits.

W83792AD/D Data Sheet Revision History, continued

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
10	5~6 10 10 40 35 83-90	Apr-26-2006	0.9	N/A	Modify the W83792AD/D pin outputs define for CSB version. PIN25 and PIN26 pins are low active for Thermtrip. PIN35 is VCOREB. Modify the PIN35 descriptions. VCOREB input detect range is 0~2.048V and Vin4 is deleted. Added the PIN37 VREF description. Reference voltage is equal to 2.048V. Modify Device Version ID 13h for C version. Modify Low Bit I/II to 3Eh and 3Fh. Updated application circuits. Add Pb-free package

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1. GENERAL DESCRIPTION

W83792AD/AG and W8392D/G are two parts support single and dual CPU application, the former is for single CPU application which provides 1 set thermal trip and 1 set of VID controlling; the latter is for dual CPU application which provides dual CPU VID controlling and 2 sets of thermal trip. Other functions are all the same without difference except thermal trip and VID controlling numbers.

W83792D/G is an evolving version of the W83791D --- Winbond's most popular hardware status monitoring IC. Besides the conventional functions of W83791D, W83792D/G uniquely provides several innovative features such as support dual CPU VID controlling, VRM9.0 and VRD10.0 specifications supported, ASF 2.0 specification compliant, SMBus 2.0 ARP command compatible, 2 sets of Thermal trip, 12 VID control, 6 sets of Smart fan ™, VID table selection trapping. Conventionally, W83792D/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system, such as server, workstation…etc, working very stably and efficiently.

A 10-bit analog-to-digital converter (ADC) was built inside W83792D/G. W83792D/G can simultaneously monitor 9 analog voltage inputs (including power VDD/5VSB monitoring), 6 fan tachometer inputs, 3 remote temperatures, and Watch Dog Timer function. The sense of remote temperature can be performed by thermistors, or directly from Intel™ CPU with thermal diode output. W83792D/G provides 6 PWM (pulse width modulation)/DC fan output modes for smart fan control - " Thermal Cruise™ " mode and " Smart Fan™ II " mode. Under " Thermal Cruise™ " mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. As Smart Fan ™ II, which provides 4 sets of temperatures point each could control fan's duty cycle, depends on this construction, fan could be operated at the lowest possible speed so that the acoustic noise could be avoided. As for warning mechanism, W83792D/G provides SMI#, OVT#, IRQ signals for system protection events.

Additionally, 12 VID inputs are provided to read 2 sets of VID for CPU (i.e. Pentium™ III/4). These VID inputs provide the information of Vcore voltage that CPU expects. W83792D/G also has 2 specific pins to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C interface.

W83792D/G can uniquely serve as an ASF sensor to respond to ASF master's request for the implementation of network management in OS-absent status. Through W83792D/G's compliance with ASF2.0 sensor specification, network server is able to monitor the environmental status of each client in OS-absent state by PET (Platform Event Trip) frame values returned from W83792D/G, such as temperatures, voltages, fan speed, thermal trip, and case open. Moreover, W83792D/G supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address for W83792D/G ASF Function after W83792D/G's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable and maskable interrupts.

2. FEATURES

2.1 VCORE Monitoring Items

- Support dual CPU VID reading.
- VRM9.0 / VRD10.0 compliant to monitor dual CPU voltage.
- 2 sets of thermal trip latch mechanism to protect CPU from over temperature.

2.2 Monitoring Items

- Monitoring 9 voltage inputs.
- 6 DC / PWM Fan outputs for fan speed control and 6 Fan speed inputs for monitoring --- Total up to 6 sets of fan speed monitoring and controlling
- 3 temperature inputs from remote thermistor and PentiumTM II/III/4 (Deschutes) thermal diode output
- 6 sets Smart FanTM could control the most fitting speed automatically by temperature.
- Case open detection input
- 2 sets of CPU thermal management:2 Thermal Trip signals latch up and generate VRM_EN signal to PWM for removing CPU power.
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.3 Address Resolution Protocol (ARP) and Alert-Standard Format (ASF 2.0)

- Support System Management Bus (SMBus) version 2.0 specification
- Comply with hardware sensor slave ARP (Address Resolution Protocol)
- Response ASF 2.0 command --- Get Event Data, Get Event Status, Device Type Poll
- Comply with ASF 2.0 sensors (Power on/off remote control, Monitoring fan speed, voltage, temperature, thermal trip and case open)
- Support Remote Control subset: Remote Power-on/ Power-off/ Reset.

2.4 Actions Enabling

- Issue SMI#, OVT#, IRQ signals to activate system protection
- Warning signal pop-up in application.

2.5 General

- I2C serial bus interface
- Support 2 sets of 6bit VID monitoring for dual processors application
- Watch Dog Timer function with pin: RESET#, SYSRST_IN.
- 16 GPIOs
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I2C interface

- Winbond hardware monitoring application software (Hardware DoctorTM) support, for both Windows 95/98/2000/XP and Windows NT 4.0/5.0/2000
- 5V VSB operation

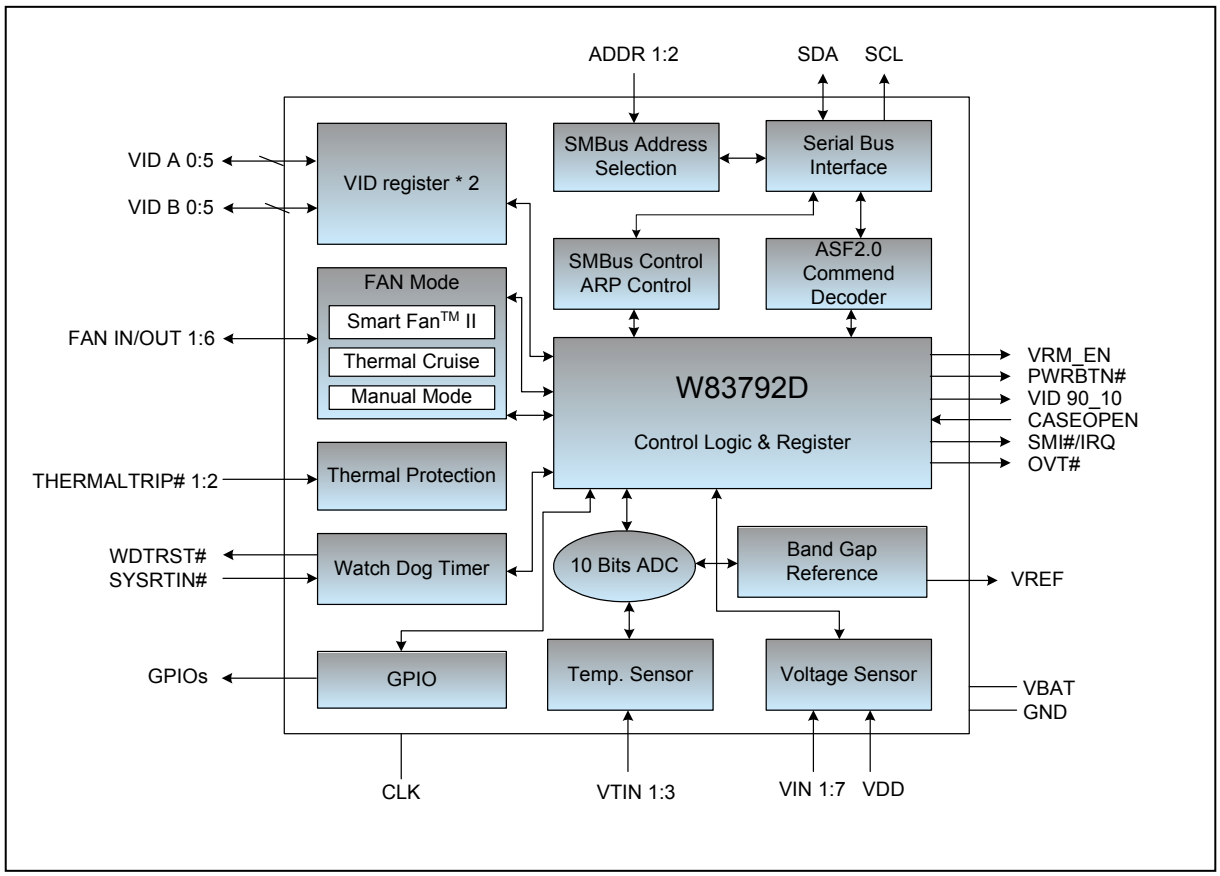
2.6 Package

- 48-pin LQFP

3. KEY SPECIFICAITON

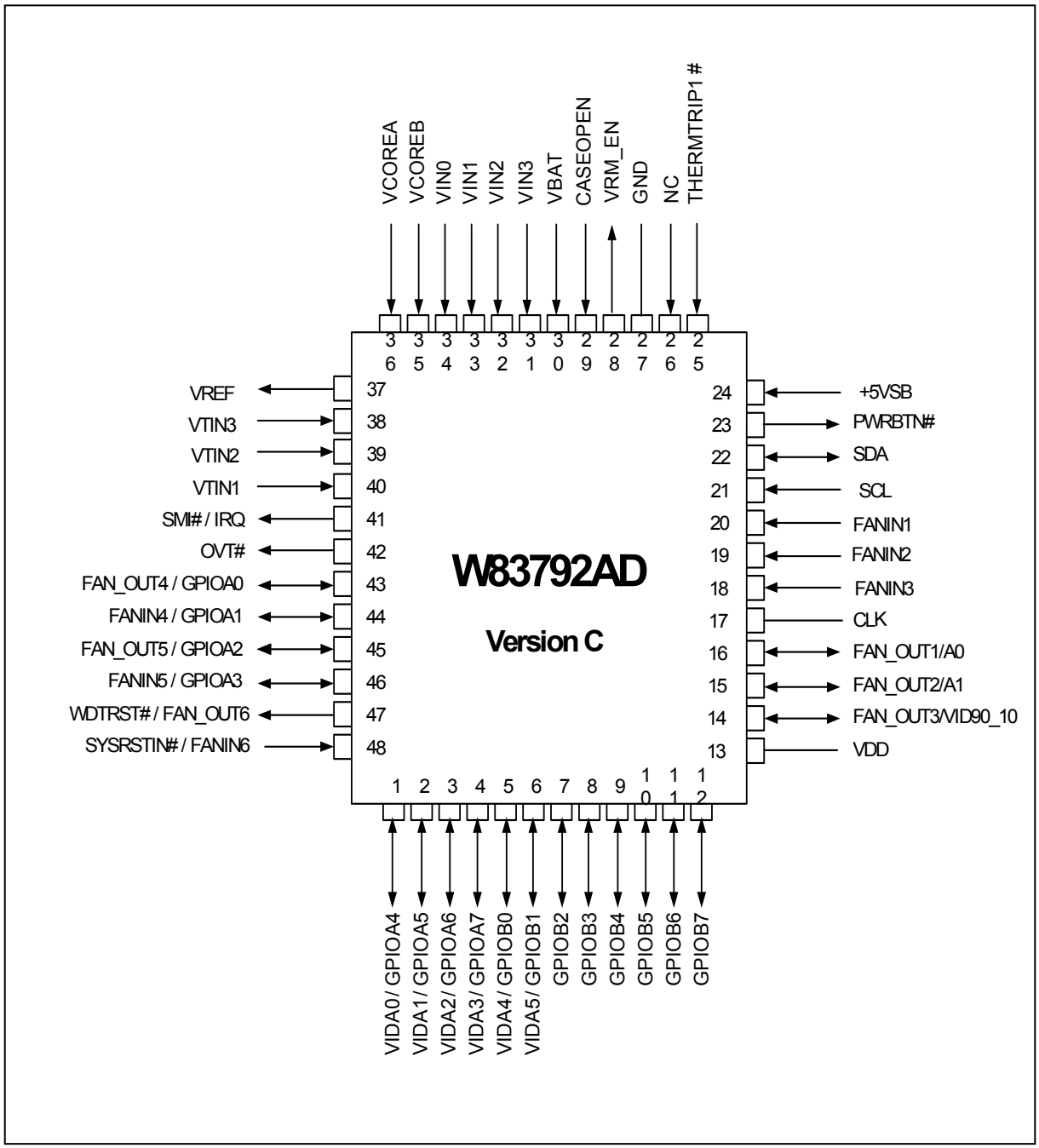
• Voltage monitoring accuracy	±1% (Max)
• Intel VRM 9.x/VRD10.0 Voltage monitoring accuracy	±1% (Max)
• Temperature Sensor Accuracy	
Remote Diode Sensor Accuracy	± 3°C(Max)
Resolution	0.5 ℃
• Supply Voltage	5V
• Operating Supply Current	5 mA typ.
• ADC Resolution	10 Bits

4. BLOCK DIAGRAM

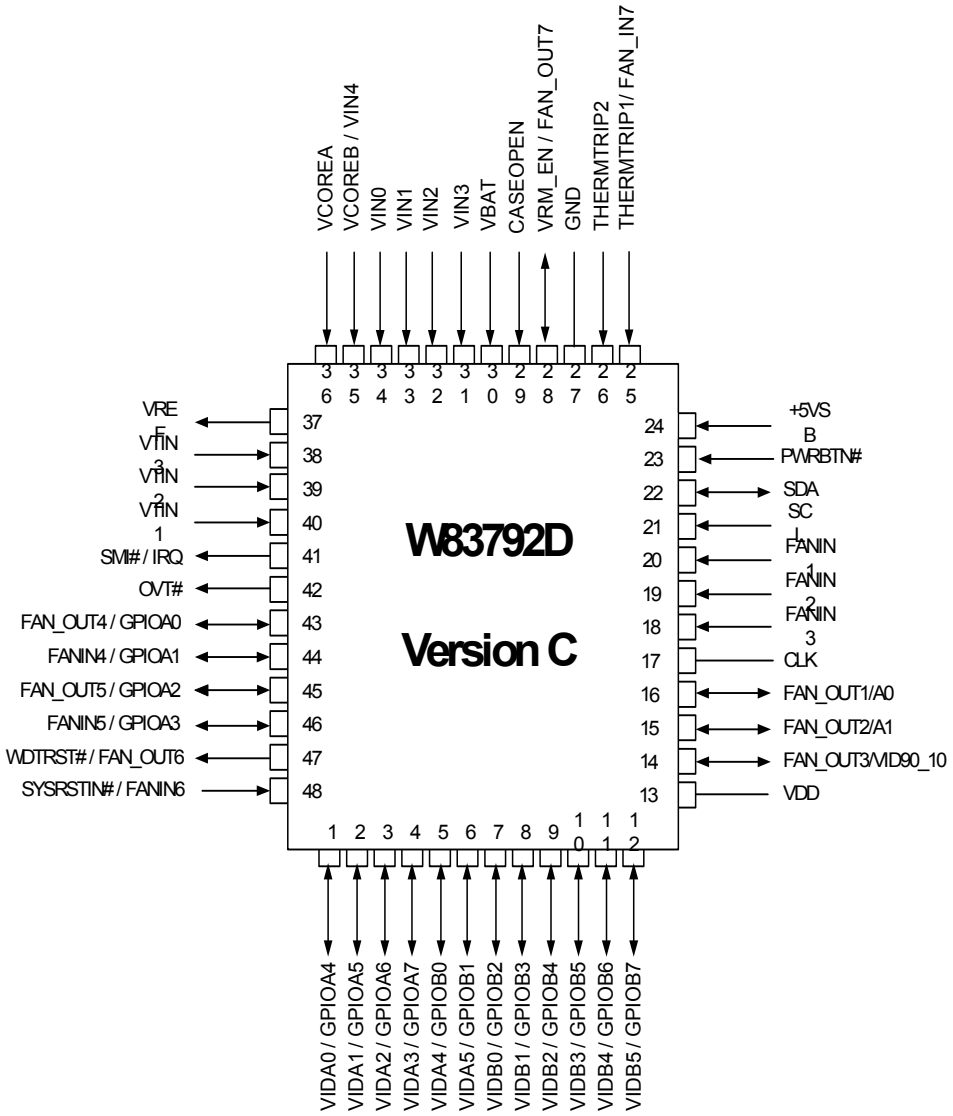


5. PIN CONFIGURATION

5.1 W83792AD/AG



5.2 W83792D/G


VCOREA
VCOREB / VIN4
VIN0
VIN1
VIN2
VIN3
VBAT
CASEOPEN
VRM_EN / FAN_OUT7
GND
THERMTRIP2
THERMTRIP1/ FAN_IN7
36 35 34 33 32 31 30 29 28 27 26 25
VREF
VTIN3
VTIN2
VTIN1
SMI# / IRQ
OVT#
FAN_OUT4 / GPIOA0
FANIN4 / GPIOA1
FAN_OUT5 / GPIOA2
FANIN5 / GPIOA3
WDTRST# / FAN_OUT6
SYSRSTIN# / FANIN6
37 38 39 40 41 42 43 44 45 46 47 48
W83792D
Version C
24 23 22 21 20 19 18 17 16 15 14 13
+5VSB
PWRBTN#
SDA
SCL
FANIN1
FANIN2
FANIN3
CLK
FAN_OUT1/A0
FAN_OUT2/A1
FAN_OUT3/VID90_10
VDD
1 2 3 4 5 6 7 8 9 10 11 12
VIDA0 / GPIOA4
VIDA1 / GPIOA5
VIDA2 / GPIOA6
VIDA3 / GPIOA7
VIDA4 / GPIOB0
VIDA5 / GPIOB1
VIDB0 / GPIOB2
VIDB1 / GPIOB3
VIDB2 / GPIOB4
VIDB3 / GPIOB5
VIDB4 / GPIOB6
VIDB5 / GPIOB7

6. PIN DESCRIPTION

6.1 Pin Type Description

I/O_{12t}	TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts}	TTL level and schmitt trigger with 12 mA source-sink capability
I/O_{8ts}	TTL level and schmitt trigger with 8 mA source-sink capability
I/O_{6ts}	TTL level and schmitt trigger with 6 mA source-sink capability
I/OD_{12ts}	TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT_{12}	Output pin with 12 mA source-sink capability
OD_{12}	Open-drain output pin with 12 mA sink capability
AOUT	Output pin (Analog)
IN_t	TTL level input pin
IN_{ts}	TTL level input pin and schmitt trigger
AIN	Input pin(Analog)

6.2 Pin Description List

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDA0	1	5VSB	IN_{ts}	Voltage Supply readouts bit 0 from CPU A.
GPIOA4			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA1	2	5VSB	IN_{ts}	Voltage Supply readouts bit 1 from CPU A.
GPIOA5			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA2	3	5VSB	IN_{ts}	Voltage Supply readouts bit 2 from CPU A.
GPIOA6			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA3	4	5VSB	IN_{ts}	Voltage Supply readouts bit 3 from CPU A.
GPIOA7			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.
VIDA4	5	5VSB	IN_{ts}	Voltage Supply readouts bit 4 from CPU A.
GPIOB0			I/OD_{12ts}	After programming, this pin can be VID output or GPIO.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
VIDA5	6	5VSB	IN_{ts}	Voltage Supply readouts bit 5 from CPU A. Only used in VRD10.0.
GPIOB1			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB0	7	5VSB	IN_{ts}	Voltage Supply readouts bit 0 from CPU B.
GPIOB2			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB1	8	5VSB	IN_{ts}	Voltage Supply readouts bit 1 from CPU B.
GPIOB3			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB2	9	5VSB	IN_{ts}	Voltage Supply readouts bit 2 from CPU B.
GPIOB4			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB3	10	5VSB	IN_{ts}	Voltage Supply readouts bit 3 from CPU B.
GPIOB5			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB4	11	5VSB	IN_{ts}	Voltage Supply readouts bit 4 from CPU B.
GPIOB6			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VIDB5	12	5VSB	IN_{ts}	Voltage Supply readouts bit 5 from CPU B. Only used in VRD10.0.
GPIOB7			I/OD-12ts	After programming, this pin can be VID output or GPIO.
VDD	13	-	POWER	+5V VDD power. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
FAN_OUT3	14	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
VID9_10			IN_{ts}	At 5VSB power on, this pin is used to select Internal VRM 9 or 10 table. Detect 1, Select VRM9, Detect 0, selects VRM10.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
FAN_OUT2	15	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A1			IN_{ts}	I^2C device address bit 1 trapping during 5VSB power on.
FAN_OUT1	16	5VSB	I/O_{12t}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A0			IN_{ts}	I^2C device address bit 0 trapping during 5VSB power on.
CLK	17	VDD	IN_{ts}	14.318MHz System clock while VCC5V powered up.
FANIN3	18	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN2	19	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
FANIN1	20	VDD	IN_{ts}	0V to +5V amplitude fan tachometer input
SCL	21	5VSB	IN_{ts}	Serial Bus Clock.
SDA	22	5VSB	I/OD_{12ts}	Serial Bus bi-directional data.
PWRBTN#	23	5VSB	OD_{12}	Power Button output for enable/disable power supply.
+5VSB	24	-	POWER	This pin is power for W83792D/G. Bypass with the parallel combination of 10μF (electrolytic or tantalum) and 0.1μF (ceramic) bypass capacitors.
THERMTRIP1# FANIN7	25	5VSB	IN_{ts}	Thermal Trip signal from CPU A. Low Active. 0~+5V FANIN 7 tachometer.
THERMTRIP2#	26	5VSB	IN_{ts}	Thermal Trip signal from CPU B. Low Active.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
GND	27	-	POWER	System Ground.
VRM_EN FAN_OUT7	28	5VSB	OD_{12} OUT_{12}	Any assertion of thermal trip after VDD power good will disable Voltage Regulator Module. Fan speed control PWM output. By default it's high. The power of this pin is supplied by VSB 5V.
CASEOPEN	29	VBAT	IN_{ts}	CASE OPEN detection. An active high input from an external device when case is Intruded. This signal can be latched in external circuit which power is supplied by VBAT, even if W83792D is power off.
VBAT	30	-	POWER	VBAT supplies power for CASEOPEN, THERMALTRIP. Besides, it is also a voltage monitor channel.
VIN3- VIN0	31 - 34		AIN	0V to 4.096V Analog Voltage Monitor Inputs.
VCOREB	35		AIN	CPU B Core Voltage Input. Detect range is 0~2.048V.
VCOREA	36		AIN	CPU A Core Voltage Input. Detect range is 0~2.048V.
VREF	37		AOUT	Reference voltage and is equal to 2.048V
VTIN3	38		AIN	Thermistor 3 terminal input.(Default). Pentium™ 4 diode 3 input. This multi-functional pin is programmable.
VTIN2	39		AIN	Thermistor 2 terminal input. (Default). Pentium™ 4 diode 2 inputs. This multi-functional pin is programmable.
VTIN1	40		AIN	Thermistor 1 terminal input. (Default). Pentium™ 4 diode 1 inputs. This multi-functional pin is programmable.

Pin Description List, continued

PIN NAME	PIN NO.	POWER PLANE	TYPE	DESCRIPTION
IRQ /	41	VDD	OUT_{12}	Interrupt request.
SMI#			OD_{12}	System Management Interrupt (open drain).
OVT#	42	VDD	OD_{12}	Over temperature Shutdown Output for temperature sensor 1-3.
FAN_OUT4	43	5VSB	OUT_{12}	Fan speed control PWM/DC output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
GPIOA0			I/O_{12ts}	After programming, this pin can be GPIO.
FANIN4	44	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
GPIOA1			I/O_{12ts}	After programming, this pin can be GPIO.
FAN_OUT5	45	5VSB	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
GPIOA2			I/O_{12ts}	After programming, this pin can be GPIO.
FANIN5	46	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
GPIOA3			I/O_{12ts}	After programming, this pin can be GPIO.
FAN_OUT6	47	5VSB	OUT_{12}	Fan speed control PWM output. By default it's high. The power of this pin is supplied by VSB 5V.
RESET#			OD_{12}	Low active System RESET. If triggered, this pin will send out 100ms low pulse for system reset.
FANIN6	48	5VSB	IN_{ts}	0V to +5V amplitude fan tachometer input
SYSRSTIN#			IN_{ts}	System reset input, used to control WDT.

7. FUNCTION DECRIPPTION

7.1 General Description

The W83792D/G provides 9 analog voltage inputs, 7 fan speed inputs and output controls which support both of PWM (Pulse Width Modulation) control and DC (Direct Current) fan control, all of them are implemented with Smart FAN^{TM} I and Smart FAN^{TM} II. 3 sets of thermal inputs for remote thermistor or Pentium^{TM} 4 thermal diode outputs, and case open detection also supported in W83792D/G. Further more, W83792D/G provides several innovative and practical functions to make the whole system manage more efficiently and compliant with future trend of network management, such as ASF2.0 sensor compliant, which could remote Power on/off control the system, report the status of thermal trip, fan, and temperature limitation. Also, it is SMBus 2.0 ARP command compatible. VID table could be selected by hardware trapping for VRM9.0 and VRD 10 specifications. 2 sets of 6 bits of VID input/output control for dual processors and 2 sets of thermal Trip input for disable VRM module, and for the more, once the monitoring function of W83792D/G is enabled, the watch dog will monitor every function and store the values to registers for comparison with preset ranges. If the monitoring value exceeds the limit value, the interrupt status will be set to 1 and W83792D/G will issue interrupt signals such as SMI# and IRQ if they are not masked off. W83792D/G also provides software and hardware Watch Dog Timer to avoid system hang on.

7.2 Access Interface

The W83792D/G provides I2C Serial Bus for microprocessor to read/write internal registers. In the W83792D/G, there are three serial bus addresses. Through the fi

The first serial bus address of W83792D/G has 2 hardware setting bits set by Pin15-16. *The address is 01011[pin15][pin16]X. Hence, the content of CR [48h] would be 00101110 if pin15=1 and pin16=0. The read/write of the CPUT1/CPUT2 temperature sensor registers can be implemented through the second address (defined at CR [4Ah] bit2-0 10011[IA1][IA0]X) and the third address (defined at CR[4Ah] bit6-4 10010[IA1][IA0]X).*rst address defined at CR[48h], all the registers can be read and written.

7.3 The first serial bus access timing

(a) Serial bus writes to internal address register followed by the data byte

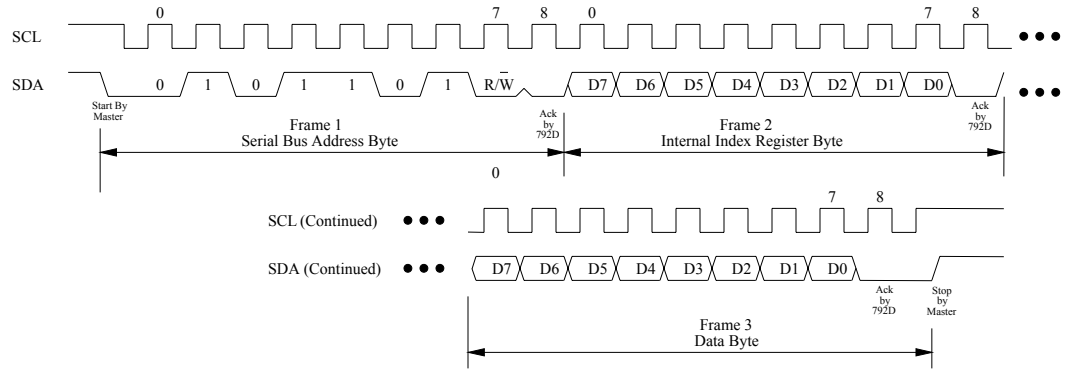


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

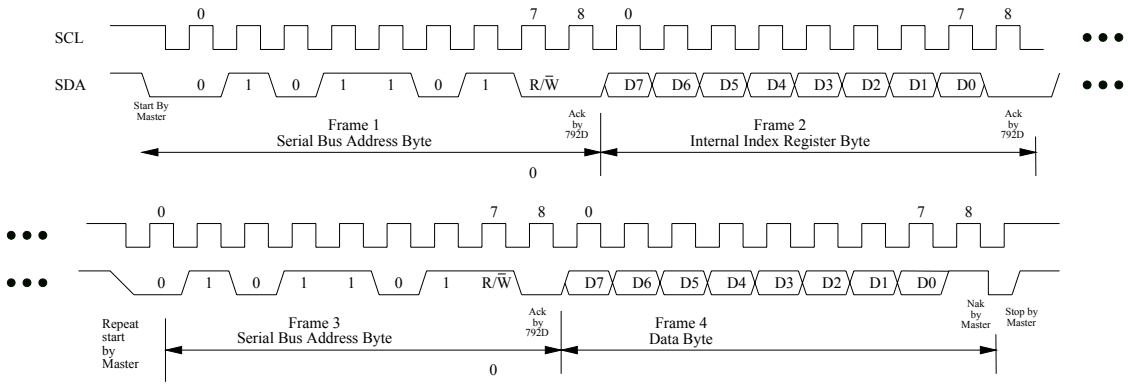


Figure 2. Serial Bus Read from Internal Address Register

7.4 Address Resolution Protocol (ARP) Introduction

As the W8792D/G is a slave device existing on the System Management Bus, it must have a unique address to prevent itself from conflicting with the other devices existing on the same bus. In order to solve the problem of address conflicts, SMBus version 2.0 introduces the concept of dynamically assigned address called Address Resolution Protocol (ARP). By such mechanism, each device existing on the SMBus will be given with an unique slave address if it is a ARP-capable device. Thus, to meet the new spec, W83792D/G uniquely provides ARP compliant function to acquire an unique slave address.

The typical process of ARP contains several steps, including *Prepare to ARP*, *Reset Device*, *Get UDID*, *Assign Address*, and so on. Whenever the slave device accepts the command of ARP master, it must reply an Acknowledgement to the ARP master, thus the ARP master is able to carry on the next step. In order to provide a mechanism to isolate device for the purpose of address assignment, each device must implement a *unique device identifier* (UDID). The UDID is a 128-bit number comprised of several field, including Device Capabilities, Version Revision, Vendor ID, Device ID, Interface, Subsystem Vendor ID, Subsystem Device ID, and Vendor Specific ID. After the UDID of the device is sent to the ARP master, the ARP master will then assign an address not in the Used Address Pool to the device.

Generally speaking, there are eleven possible commands to read /write the data of SMBus device, and a slave device may use any or all of the eleven protocols to communicate. These protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read word, Process Call, Block Write, and Block Write-Block Read Process Call. W83792D/G itself supports the Block Write-Block Read Process with PEC to communicate with ARP Master. Following is a description of the SMBus packet protocol diagrams element key. Not all protocol elements will be present in every command, that is, not all packets are required to include the *Packet Error Code*.

1-bit	7	1	1	8	1	8	1	1-bit
S	Slave Address	Wr	A	Command	A	PEC	A	P

S		Start Condition
Sr		Repeated Start Condition
Rd		Read (bit value of 1)
Wr		Write (bit value of 0)
A		Acknowledge (this bit position may be ‘0’ for an ACK or ‘1’ for a NACK)
P		Stop Condition
PEC		Packet Error Code
		Master-to-Slave
		Slave-to-Master

Relative command list:

SLAVE ADDRESS	COMMAND	DESCRIPTION
C2h	01h	Prepare to ARP
C2h	02h	Reset device (general)
C2h	03h	Get UDID (general)
C2h	04h	Assign address
C2h	Slave_Addr | 1	Direct Get UDID
C2h	Slave_Addr | 0	Direct Reset
C2h	05h-1Fh	Reserved.

Following is an example of the Block Write-Block Read Process Call. The Block Write-Block Read Process Call is a two-part message. It begins with a salve address and a write condition. After the command code the host issues a write count M that describes how many more bytes will be written in the first part of the message. The second part of the message is a block of read data beginning with a repeat start condition followed by the salve address and a Read Bit. The next read byte count N indicates how many more data will be read in the second part of the message. Note that the combined data payload must not exceed 32bytes. Besides, W83792D/G also provides packet error code (PEC) to ensure the accuracy during data transmission.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	…

8	1	…	8	1	
Data Byte 2	A	…	Data Byte M	A	…

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Byte Count=N	A	Data Byte 1	A	…

8	1	…	8	1	8	1	1
Data Byte 2	A	…	Data Byte N	A	PEC	A	P

7.5 ASF (Alert Standard Format) Introduction

In order to implement network management in OS-absent, W83792D/G provides ASF Response Registers to meet ASF sensor spec. As a result, the network server is able to monitor several environmental status of the client in OS-absent by PET frame values returned from W83792D/G, including temperature, voltage, fan speed, and case open. In below is the ASF diagram:

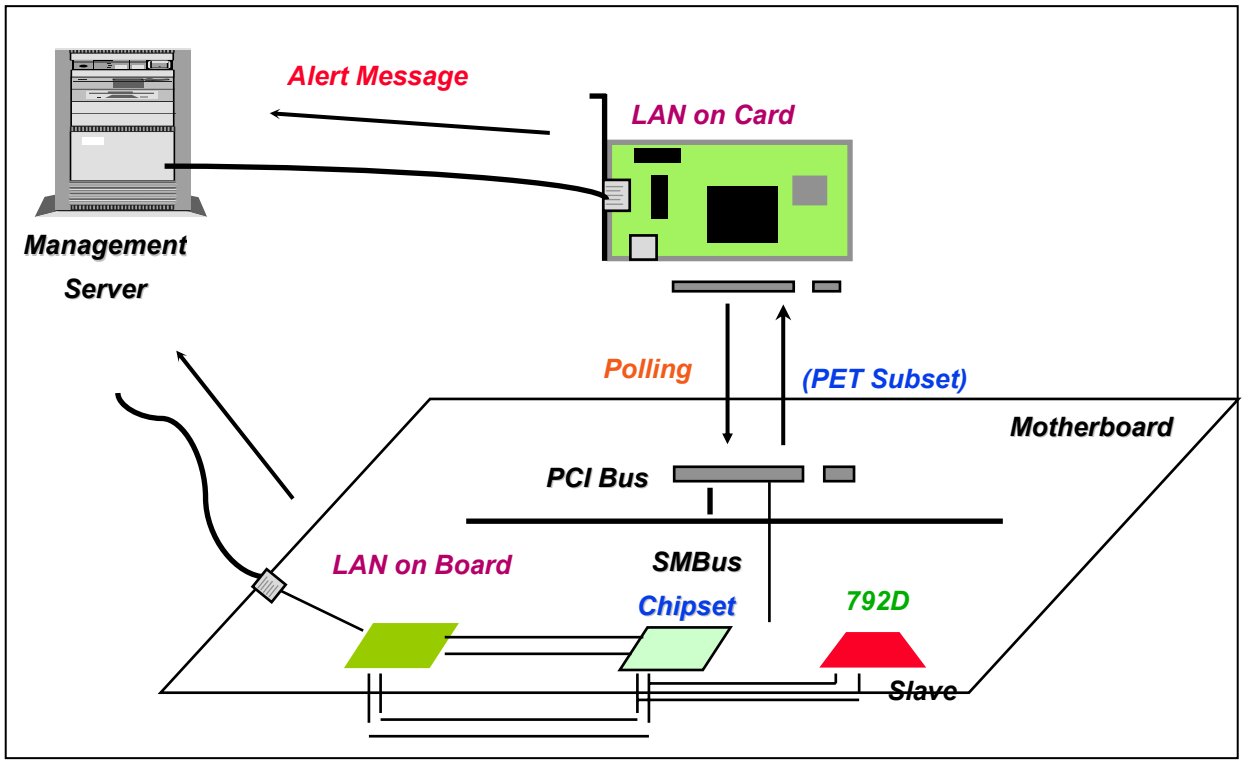


Figure 3. ASF Block Diagram

7.5.1 Platform Event Trap (PET)

PET is the ASF transmit protocol used to provide common fields for trap regardless of trap source. The variable bindings fields in a PET frame contain the system and sensor information for an event, such as event sensor type, event type, event offset, event source type, sensor device, sensor number, entity ID, entity instance, event status index, event status, and event severity. Each field has its definition and is described in the following table.

PET VARIABLE BINDING FIELD	DESCRIPTION
Event Sensor Type	The Event Sensor Type field indicates what types of events the sensor is monitoring. E.g. temperature, voltage, fan, etc.
Event Type	The Event Type indicates what type of transition/state change triggered the trap.
Event Offset	The Event Offset indicates which particular event occurred for a given Even Type.
Event source Type	The Event Source Type describes the originator of the event. It is ASF2.0(68h) for all PET frames defined by this specification.
Sensor Device	The Sensor Device is the SMBus address of the sensor that caused the event for the PET frame.
Sensor Number	The Sensor Number is used to identify a given instance of a sensor relative to the Sensor Device.
Entity ID	The Entity ID indicates the platform entity the event is associated with. E.g. processor, system board, etc.
Entity Instance	The Entity Instance indicates which instance of the Entity the event is for. E.g. processor 1 or processor 2.
Event Status Index	The Event Status Index identifies a unique event monitored by the ASF-sensor. It is zero-based, sequential, continuous, and ranging form 0-37h.
Event Status	The Event Status indicates the event state of the ASF-sensor device associated with the message's Event Status Index.
Event Severity	The Event Severity gives the management station an indication of the severity of the event in the PET frame. Typical values are Monitor (0x01), Non Critical (0x08), or Critical Condition (0x10).

Following is the illustration of ASF SMBus command for Get Event Data.

1	7	1	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Wr Byte Count	A	…
	ASF-sensor Address	0	0	Sensor Device 0000 0001	0	0000 0100	0	

8	1	8	1	8	1	8	1	
Wr Data 1	A	Wr Data 2	A	Wr Data 3	A	Wr Data 4	A	…
Sub Command Get Event Data 0001 0001	0	Version Number 0001 0000	0	Event Status Index 00ii iiii	0	Reserved 0000 0000	0	

1	7	1	1	8	1	
Sr	Slave Address	R	A	Rd Byte Count	A	…
	ASF-sensor Address	1	0	0000 1010 to0000 1111	0	

1	8	1	8	1	8	1	
A	Rd Data 1	A	Rd Data 2	A	Rd Data 3	A	…
0	Status	0	Event Sensor Type	0	Event Type	0	

8	1	8	1	8	1	8	1	
Rd Data 4	A	Rd Data 5	A	Rd Data 6	A	Rd Data 7	A	…
Event Offset	0	Event Source Type	0	Event Severity	0	Sensor Device	0	

8	1	8	1	8	1	
Rd Data 8	A	Rd Data 9	A	Rd Data 10	A	…
Sensor Number	0	Entity	0	Entity Instance	0	

	8	1	1
…	PEC	A	P
From zero to five bytes of Event Data	[data dependent]	1	

7.6 Analog Inputs

The maximum input voltage of the analog pin is *4.096V* because the 10-bit ADC has a *4mv LSB.* Actually, the application of the PC monitoring would most often be connected to power supply. The CPU V-core voltage, +3.3V and battery voltage can *directly connect* to these analog inputs. The –5V, –12V and +12V inputs should be reduced a factor with external resistors to meet the input range. As Figure 4 shows.

*PS : VCORE channel resolution = 2mv VIN0-4 channel resolution = 4mv

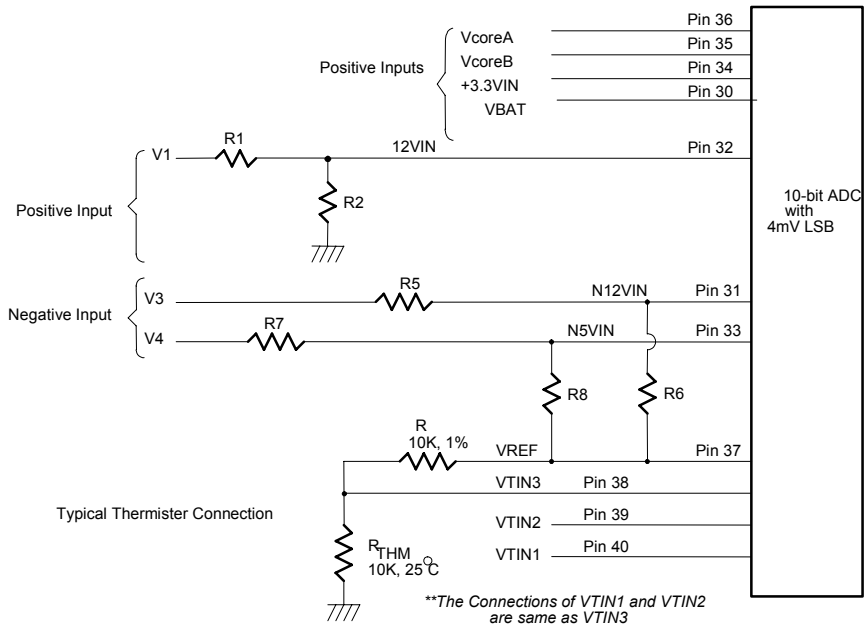


Figure 4.

7.6.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as the following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN should be subject to under 4.096V for the maximum input range of the 8-bit ADC. The pin 13 and pin 29 are discretely connected to the power supply +5V and 5VSB . There are two functions in these pins with 5V. The first function is to supply internal analog power in the W83792D and the second one is that these voltages are all connected to internal serial resistors to monitor the +5V and 5VSB voltage.

7.6.2 Monitor negative voltage:

The negative voltage should be connected to two series resistors and a positive voltage VREF (equal to 2.048V). In the Figure 11, the voltage *V3 and V4* are two negative voltages and are -12V and -5V respectively. The voltage V3 is connected to two serial resistors as well as another positive terminal VREF. Therefore, the voltage node N12VIN would be a positive voltage if the scale of the two serial resistors are carefully selected. It is recommended from Winbond that the scale of the two serial resistors are R5=232K ohms and R6=10K ohm. The input voltage of node -12VIN can be calculated by the following equation.

$$N12VIN = (VREF + |V_5|) \times (\frac{232K\Omega}{232K\Omega + 10K\Omega}) + V_5$$

where VREF is equal to 2.048V.

If the V_5 is equal to -12V then the voltage is equal to 1.467V and the converted hexdecimal data is set to 60h by the 8-bit ADC with 8mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_5 = \frac{N12VIN - VREF \times \beta}{1 - \beta}$$

Where β is 232K/(232K+10K). If the N2VIN is 1.467 then the V5 is approximately equal to -12V.

The other negative voltage input V6 (approximate -5V) can also be evaluated by the similar method and the serial resistors can be R7=120K ohms and R8=10K ohms by the Winbond recommended. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times \gamma}{1 - \gamma}$$

Where the γ is set to 120K/(120K+10K). If the monitored ADC value in the N5VIN channel is 1.505, VREF=2.048V and the parameter γ is 0.923, then the negative voltage of V6 can be evaluated -5V.

7.7 FAN Speed Count and FAN Speed Control

7.7.1 Fan speed count

W83792D/G support 6 sets of fan counting. Fan inputs are provided for signals from fans equipped with tachometer outputs. The level of these signals should be set to *TTL level,* and the maximum input voltage should not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to meet the input specification. The normal circuit and trimming circuits are shown as Figure 8.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, if the fan speed counter has been read from register CR [28], CR [29], CR [2A], CR [B8], CR [B9] or CR [BA] , then the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47, CR5B, and CR5C which are three bits for divisor. This provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count.

DIVISOR	NOMINAL RPM	TIME PER REVOLUTION	COUNTS
1	8800	6.82 ms	153
2 (default)	4400	13.64 ms	153
4	2200	27.27 ms	153
8	1100	54.54 ms	153
16	550	109.08 ms	153
32	275	218.16 ms	153
64	137	436.32 ms	153
128	68	872.64 ms	153

Table 2.

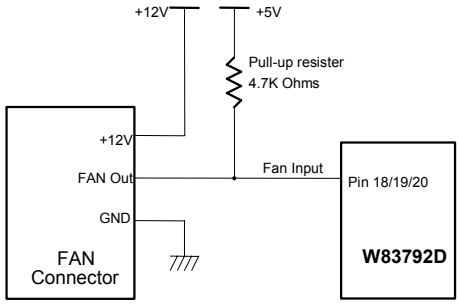


Figure 5-1. Fan with Tach Pull-Up to +5V

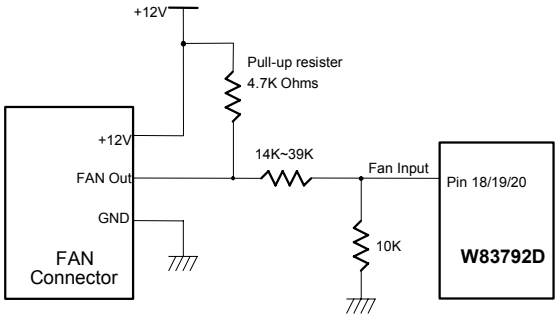


Figure 5-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator

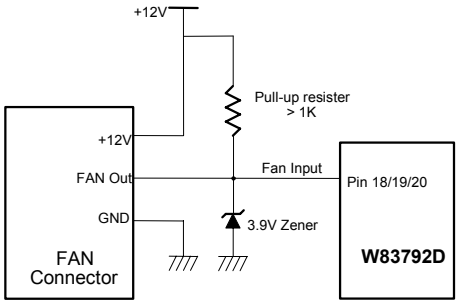


Figure 5-3. Fan with Tach Pull-Up to +12V and Zener Clamp

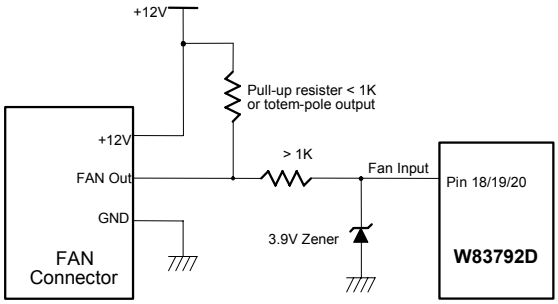


Figure 5-4. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Zener Clamp

7.7.2 Fan speed control

The W83792D/G provides six sets both of PWM and DC mode for fan speed control. The duty cycle of PWM can be programmed by a 4-bit registers defined in the Bank0 CR[81], CR[83], CR[94], CR[A3],CR[A4] and CR[A5] . The default duty cycle is set to 100%, that is, the default 4-bit register is set to 0x8Fh. The expression of duty cycle can be represented as follows.

7.7.2.1. PWM mode :

$$\text{Duty}-\text{cycle}(\%)=\frac{\text{Programmed 8 - bit Register Value}}{255}\times 100\%$$

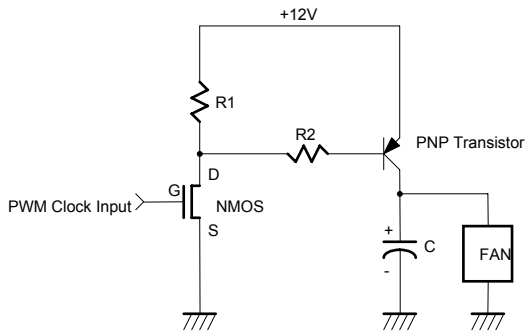


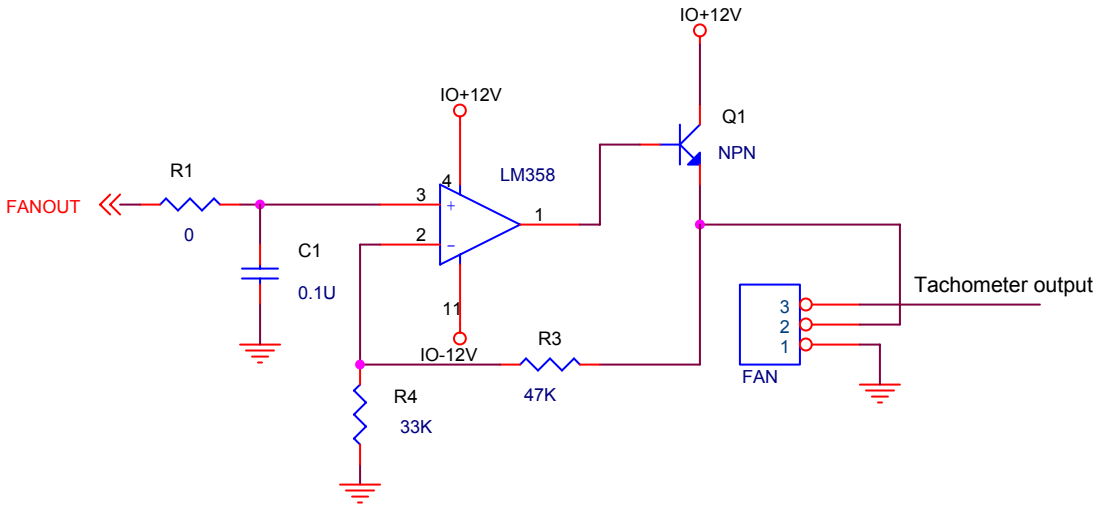
Figure 6.

7.7.2.2. DC mode:

W83792D/G has a 4-bit DAC, which produces 0 to 5 volts DC output that provides maximum 3 sets for fan speed control. The analog output can be programmed in the Bank0 CR[81], CR[83], CR[94], CR[A3],CR[A4] and CR[A5]. That is default output value is 5 V. The expression of output voltage can be represented as follow,

$$\text{OUTPUT VOLTAGE}=AVCC\times\frac{\text{Programmed 4 - bit Register Value}}{16}$$

The application circuit is shown as follow,



Must be take care when choosing the OP-AMP and the transistor. The OP-AMP is used for amplify the 5V range of the DC output up to 12V. The transistor should has a suitable β value to avoid its base current pulling down the OP-AMP 's output and gain the common current to operate the fan at fully speed. (For more cost and effort efficiently solution please refer to W8339TS/QS –which is the DC fan pre-driver and it could provide up to 24V gate voltage for external N-channel MOSFET with lower cost and better performance)

7.7.3 Smart FanTM I Control

W83792D/G supports two Smart Fan function and mapping to temp1 (FAN1, PWMOUT1), temp2 (FAN2, PWMOUT2), temp3 (FAN3, PWMOUT3) .Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Smart Fan™ II mode.

7.7.3.1. Thermal Cruise mode

At this mode, W83792D/G provides the Smart Fan system to automatically control fan speed to keep the temperatures of CPU and the system within specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS and the fan speed will be lowered as long as the current temperature remains below the setting value. Once the temperature exceeds the high limit (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its full speed but the temperature still exceeds the high limit (ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but still above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target range (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset stop value until the temperature exceeds the low limit.

Figure 7-1, 7-2 gives an illustration of Thermal Cruise Mode.

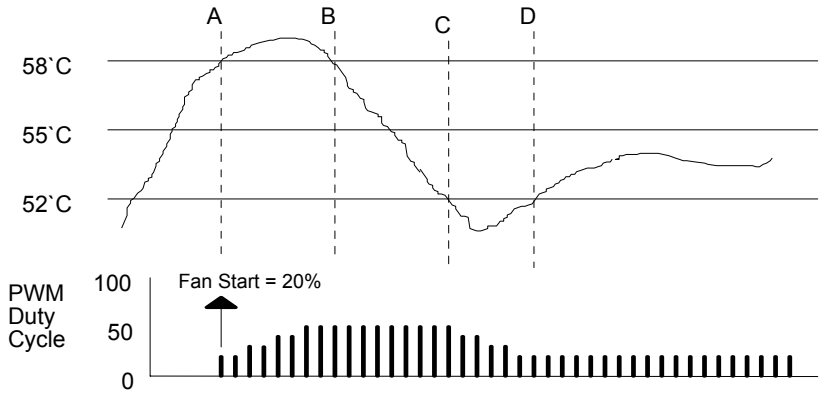


Figure 7-1.

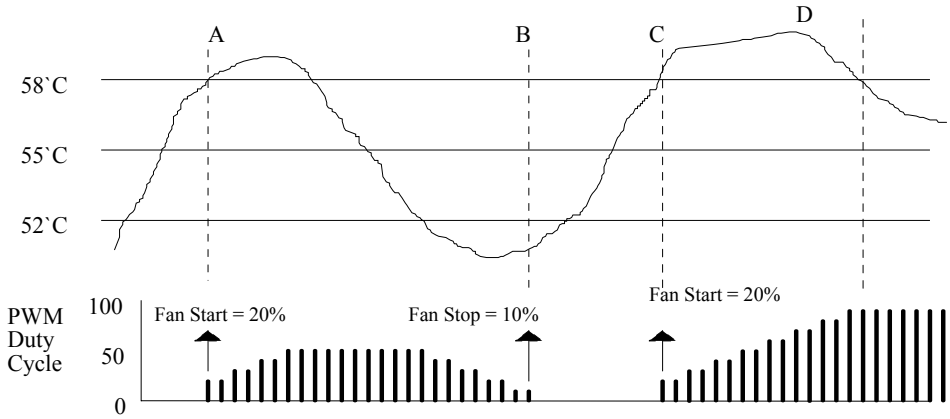


Figure 7-2.

Of course, Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

7.7.4 Smart FanTM II Control

W83792D/G provide 4 temperature point each can auto control PWM or DC fan mode. Each Temp maps

Different fan out level, the relationship is shown as follow:

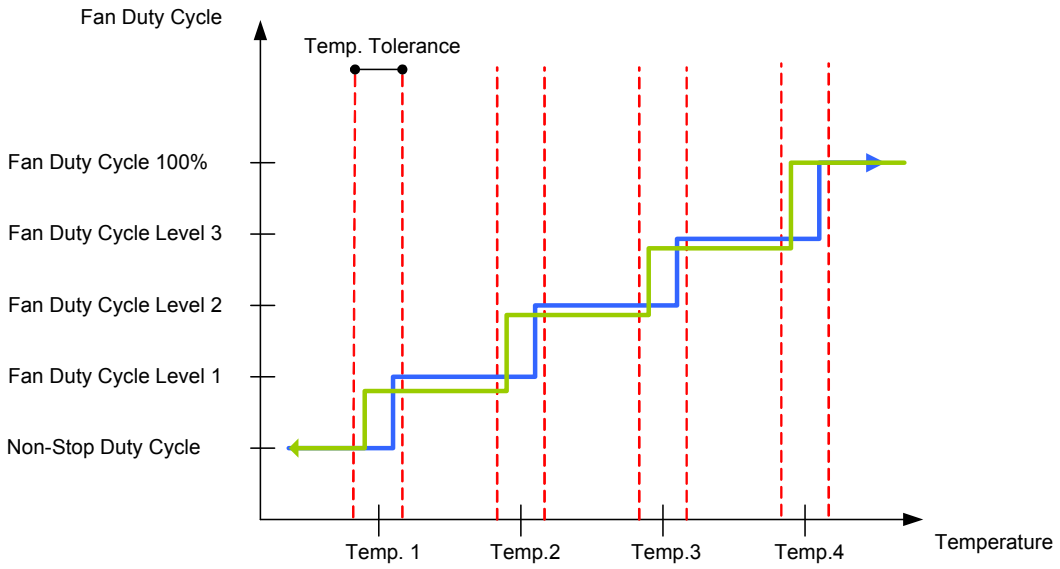


Figure 8. Smart Fan II behavior

7.7.4.1. Temperature Measurement Machine

The temperature data format is 8-bit two-complement for sensor 1 and 9-bit two-complement for sensor 2/3. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the bank0 CR[C0/ C8h] and the LSB from the bank0 CR[C1/C9h] bit 7. The format of the temperature data is show in Table 3.

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h

Table 3.

7.7.4.2. Monitor temperature from thermistor:

The W83792D/G can be connected three thermistors to measure three different environmental temperatures. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 11, the thermistor is connected by a serial resistor with 10K Ohms(1% error), then connect to VREF (Pin 37).

7.7.4.3. Monitor temperature from Pentium IVTM thermal diode or bipolar transistor 2N3904

The W83792D/G can alternate the thermistor to Pentium IV™ thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 11. The pin of Pentium IV™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin VTINx in the W83792D/G. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

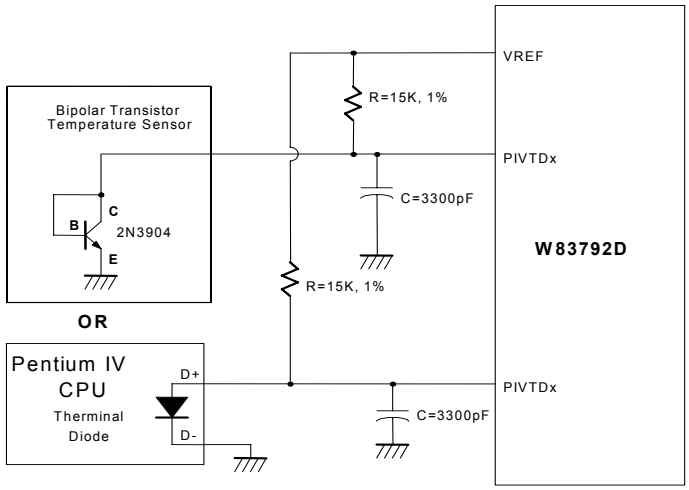


Figure 9.

7.7.5 SMI# interrupt for W83792D/G Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 10-1.)

7.7.6 SMI# interrupt for W83792D/G Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit, will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 10-2.)

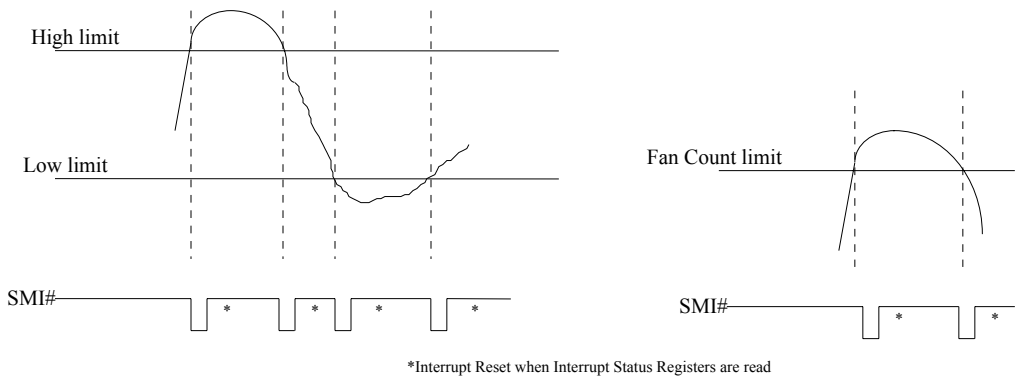


Figure 10-1. Voltage SMI# Mode

Figure 10-2. Fan SMI# Mode

7.7.7 SMI# interrupt for W83792D/G temperature sensor 1/2/3

(1) Comparator Interrupt Mode

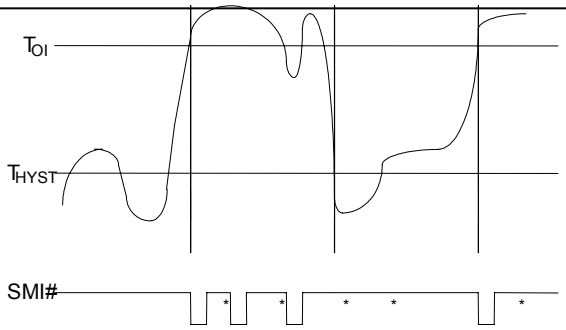
Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O but has not been reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 10-3.)

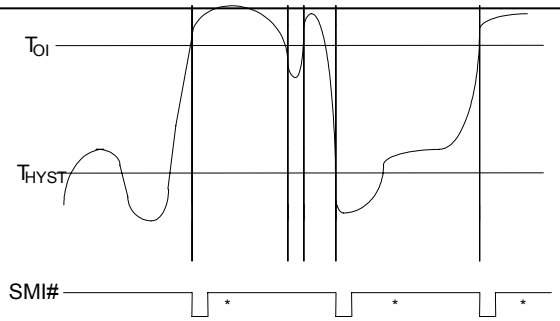
(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O , then reset, if the temperature remains above the T_{HYST} , the interrupt will not occur. (Figure 10-4.)

(3) One-Time interrupt mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure 10-5.)

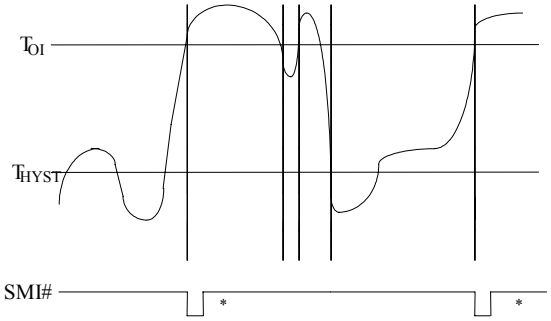




*Interrupt Reset when Interrupt Status Registers are read

Figure 10-3. Comparator Interrupt Mode

Figure 10-4. Two-Times Interrupt Mode



*Interrupt Reset when Interrupt Status Registers are read

Figure 10-5. One-Time Interrupt Mode

Note. The IRQ interrupt action like SMI# , but the IRQ is level signal.

7.7.8 Over-Temperature (OVT#) for W83792D temperature sensor 1/2/3

7.7.8.1. Comparator Mode:

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 13)

7.7.8.2. Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 11)

7.7.8.3. ACPI Mode

At this mode, temperature exceeding one level of temperature separation, starting from 0 degree, causes the OVT# output activated. OVT# will be activated again once temperature exceeds the next level. OVT# output will act the same manner when temperature goes down. (Figure 11-1).

The granularity of temperature separation between each OVT# output signal can be programmed at Bank0 CR[4Ch] bit 4-5.

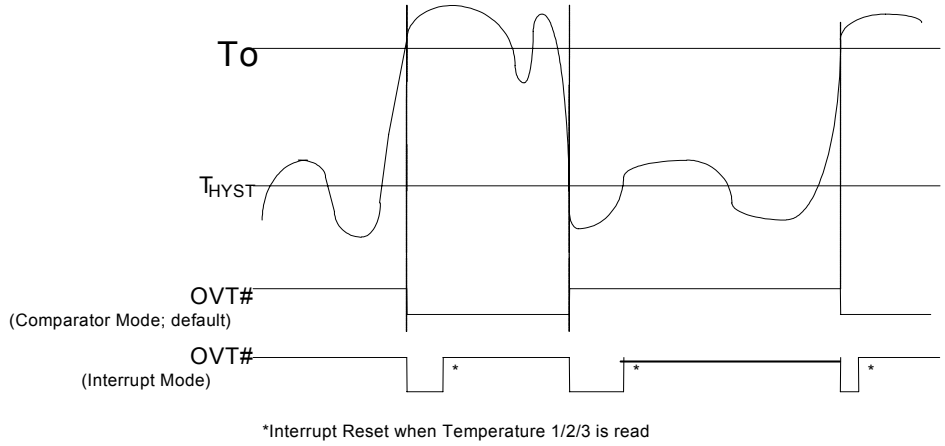


Figure 11 Over-Temperature Response Diagram

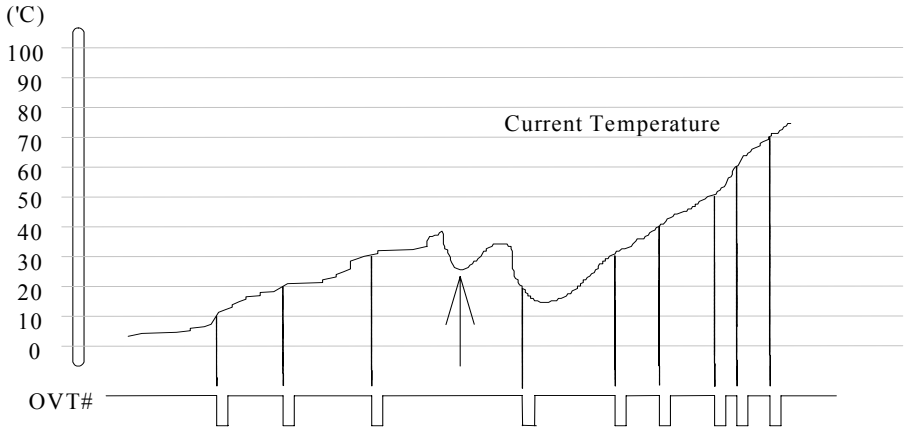


Figure 11-1. ACPI Mode

8. CONTROL AND STATUS REGISTER

8.1 Watch Dog Timer Registers --- Index 01h-04h

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOCK Watch Dog	0	1	WO	Unlock Code							
Watch Dog Enable	0	2	RO	Reserve						HARD	SOFT
				0-						0	0
Watch Dog Status	0	3	R/W	Reserve				WDT Stage		HARD_TO	SOFT_TO
				0				0		0	0
Watch Dog Timer	0	4	R/W	Timeout Time							
				00h (Unit in min)							

Reset Condition: Resume reset

Two kinds of watchdog timer function are supported by W83792D/G. One is so-called Soft Watch Dog Timer, and the other is Hard Watch Dog Timer.

Hard Watch Dog timer if enabled which will start a 4 minutes WDT after completion of system reset. (A Low to High transition on SYSRSTIN# pin). BIOS need to write a 00 into Watch Dog Timer Register (04h) to disable timer within 4 minutes, otherwise pin 47 WDTRST# will assert to reset system.

Soft Watch Dog Timer will start to down counting whenever Timeout Time is set and Soft Watch Dog Timer is enabled. A WDTRST# will be issued while the timer timeouts.

Soft Watch Dog Timer will be disabled automatically after received a SYSRSTIN_N low signal.

To write these registers requires CR40[4]/ENWDT being asserted.

CR01 LOCK Watch Dog

BIT	NAME	ATTRIBUTE	DESCRIPTION
7~0	Unlock Code	WO	Write 55h, Enable Soft Watch Dog Timer. Wire AAh, Disable Soft Watch Dog Timer. Write 33h, Enable Hard Watch Dog Timer. Write CCh, Disable Hard Watch Dog Timer.

CR02 Watch Dog Enable

BIT	NAME	ATTRIBUTE	DESCRIPTION
7~2	reserve	RO	reserve
1	HARD	RO	1 indicates the Hard Watch Dog is enabled; 0, Hard Watch Dog is disabled.
0	SOFT	RO	1 indicates the Soft Watch Dog is enabled; 0, Soft Watch Dog is disabled.

CR03 Watch Dog Status

BIT	NAME	ATTRIBUTE	DESCRIPTION
7~4	reserve	R/W	Reserve.
3~2	WDT Stage	R/W	Default 0, these 2 bits record last WDT stage for BIOS readout. The information is used to help BIOS to identify WDT timeout issue.
1	HARD_TO	RO	1: a hard timeout occurs. This bit will be cleared while reading.
0	SOFT_TO	RO	1: a soft timeout occurs. This bit will be cleared while reading.

CR04 Watch Dog Timer

BIT	NAME	ATTRIBUTE	DESCRIPTION
7~0	Watch Dog Timer	R/W	Time to issue WDTRST#. Unit in minutes. Write 00h will disable the timer.

8.2 VRM Tolerance Registers — Index 12h-13h (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Vcore High Tolerance	0	12	RW	**Vcore High Tolerance (2mV unit)**							
				64h(0.2V)							
Vcore Low Tolerance	0	13	RW	**Vcore Low Tolerance (2mV unit)**							
				64h(0.2V)							
VRM Offset	0	FD	RW	**Vcore Offset (12.5mV/LSB, 2s complement)**							
				0							

RESET Condition: Resume Reset, INIT(CR40.7), or both VID detect no CPU.

Writing Tolerance register will force VCORE Limit Generator generate new voltage limit for VCORE. For example, writing CR[FDh] with 01 in VRM 10.1 mode will result in VCORE limit registers CR[2B/2C/2D/2E] become Voltage(VID) +/- Tolerance + 12.5mV.

8.3 VID Control/Status Registers — Index 14h-18h (Bank 0)

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VID IN A	0	14	RO	VRD10	VRM_CK	VIDIN5	VIDIN4	VIDIN3	VIDIN2	VIDIN1	VIDIN0
				RW	RO	RO					
VID Control A	0	15	RW	EN_VIDO	VIDCHG	VID5	VID4	VID3	VID2	VID1	VID0
				0	RO	0	0	0	0	0	0
Entry/Disable VID Output	0	16	RW	ENTRYOK						ENTRY_ST	
				0	Write pattern/ Read 00h					0	0
VID IN B	0	17	RO	EN_VIDTG	AUTOUPD	VIDIN5	VIDIN4	VIDIN3	VIDIN2	VIDIN1	VIDIN0
				RW 0	1 RW	RO					
VID Control B	0	18	RW	EN_VIDO	VIDCHG	VID5	VID4	VID3	VID2	VID1	VID0
				0	RO	0	0	0	0	0	0

RESET Condition: Both VID detects no CPU, Resume Reset, INIT(CR40.7),

These registers are used to control 12 VID Pins. When power on, system can strap Pin14 to decide which VRM table will be used later. This information is shown at CR14.VRM_CK. In VRM9, power on value will be shown at VIDIN. When system wants to program VID pins, it must program a sequence to CR16 first, the sequence is 5A, 73, B2, E0. After this, one can set EN_VIDO, and write VID to output. To disable, write CR16 with A5, 4C, D9, 8A. In this way, the W83792D/G will lock its latest status.

CR14/CR17 VID IN

7.VRD10	Set to enable VRD10 table translation, clear to enable VRM9 table translation. Default value is Inversion of VRM_CK.
6.VRM_CK	Power on strapping value of Pin14, this will determine default value of VRD10 (bit 7).
6.AUTOUPD	Auto-update for VRD10.0 VID. In auto-update mode, VID is automatically update and SMBus to modify upper/lower limit of vcore is not applicable. If programming High/Low limit is required with VRD10=1, this bit must be cleared as 0.
5~0.VIDIN	Power-on value of VID pins(VRM9 mode) or current VID value on pins(VRM10 mode).

CR15/CR18 VID Control

7.EN_VIDO	Set to enable VID output.
6.VIDCHG	VID on the fly. (Read only) Use to indicate VID have been changed in last 1ms~2ms.
5~0.VID	The desired VID to output to pin. (ENTRY OK must be 1 to write this register)

CR16 Entry/Disable VID Output

7.ENTRYOK	Read only. An one means entry pattern all successfully received, and programming VID function is valid.
1~0. ENTRY_ST	Read only. These 2 bits indicate how many patterns have been written into CR16.
7~0 Pattern	Write 8-bit to input patterns for writing VID output privilege. Entrance: 5A(Entry_ST=1), 73(Entry_ST=2), B2(Entry_ST=3), E0(ENTRY_OK=1). Exit: A5(Entry_ST=2), 4C(Entry_ST=1), D9(Entry_ST=0), 8A(ENTRY_OK=0). The pattern must be sequentially input without other writes interrupt, otherwise, the current input sequence is considered as in-effective.

Note. Programming VID for output and using VID pins as GPIO are different. Programming VID output will activate VID translation, but GPIO will not.

Writing VID should be separated into 2 steps at the first time after VID Entry is enabled. One for set EN_VIDOUT, the other for set the wanted VID. These actions are used to inform VID Limit Generator generate new VCORE Limits for written VID. If writing EN_VIDOUT/VIDOUT in the same SMBus transaction, VID will be output to port but will not update internal Vcore Limits.

VIDIN latches external pin value, and will not affect by VIDOUTDATA.

VID on the fly flag is only used in VRM10 mode. User should not assume its value under VRM9 value.

8.4 GPIO Control/Status Register — Index 1A~1Eh (Bank 0)

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO Enable	0	1A	RW	reserve	GPA0_1	GPA2_3	GPA4_B0	GPB1	GPB2_6	GPB_7	reserve
				0	0	0	0	0	0	0	0
GPIOA Output Control	0	1B	RW	GPA7	GPA6	GPA5	GPA4	GPA3	GPA2	GPA1	GPA0
				0	0	0	0	0	0	0	0
GPIOA Data/Status	0	1C	RW	GPA7	GPA6	GPA5	GPA4	GPA3	GPA2	GPA1	GPA0
				0	0	0	0	0	0	0	0
GPIOB Output Control	0	1D	RW	GPB7	GPB6	GPB5	GPB4	GPB3	GPB2	GPB1	GPB0
				0	0	0	0	0	0	0	0
GPIOB Data/Status	0	1E	RW	GPB7	GPB6	GPB5	GPB4	GPB3	GPB2	GPB1	GPB0
				0	0	0	0	0	0	0	0

Reset Condition: Resume Reset, INIT.

16 GPIO pins are provided in W83792D. Three kinds of registers are used to control GPIO mechanism. GPIO Enable enables GPIO function, Output Control determines direction of the GPIO pin, and Data/status put/get data from the pin.

CR1A GPIO Enable

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	reserve	RO	Reserved.
6	GPA0_1	R/W	Enable GPIO function for GPA0 and GPA1.
5	GPA2_4	R/W	Enable GPIO function for GPA2 and GPA3.
4	GPA4_B0	R/W	Enable GPIO function for GPA4, GPA5, GPA6, GPA7 and GPB0.
3	GPB1	R/W	Enable GPIO function for GPB.
2	GPB2_6	R/W	Enable GPIO function for GPB2, GPB3, GPB4, GPB5 and GPB6.
1	GPB7	R/W	Enable GPIO function for GPB7.

CR1B/CR1D GPIO Output Control

These bits control the direction of each GPIO pins. Write 0, GPIO serves as input. Write 1, GPIO serves as output. Default is input.

CR1C/CR1E GPIO Data/Status

Write these bits, the data will response to GPIO, set to output mode. If read this register, will return this pin data that can input or output in this pin.

8.5 VRM Output Control ---- Index 1F(Bank 0)

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VRM Output Control	0	1F	RW	VRM_EN	DIR	VRMSTS	VRMOPV	reserve	reserve	TTRIP2_N	TTRIP1_N
				1	0	RO	1	0	0	1	1

Reset Condition: Resume Reset, INIT.

W83792D have the ability to control VRM(Voltage Regulator Module) enable. At normal power on, VRM is always enabled. But once TTRIP1_N(Thermal Trip1) or TTRIP2_N is asserted, all VRM will be disabled until resume reset, no matter TTRIP_N is written 1 again or not.

CR1F VRM Output Control

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	VRM_EN	R/W	Set to 1 will enable VRM Enable control. Clear to 0 enable GPIO function.
6	DIR	R/W	Pin direction when VRM_EN. Set to 1, serves as output ; 0 will change into input mode.
5	VRMSTS	RO	Current value on pin VRM_EN. For GPIO use
4	VRMOPV	R/W	VRM_EN Output Value. When Thermal Trip occurs, this bit will reset to 0 also. In GPIO mode, write this bit will force the value output to pin.
1	TTRIP2_N	RO	Thermal Trip input 1. This bit is powered by 5VSB. It will latch a 0 once THERMTRIP1 goes high. It can be reset to 1 by 5VDD Power on and resume reset.
0	TTRIP1_N	RO	Thermal Trip input 0. This bit is powered by 5VSB. It will latch a 0 once THERMTRIP0 goes high. It can be reset to 1 by 5VDD Power on and resume reset.

TTRIP2_N and TTRIP1_N, any of these two bits cleared as 0 means thermal trip shutdown is happening. If VRM_EN is set, a zero will be outputted at pin 28 to shut down voltage regulator.

8.6 Value RAM — Index 20h- 2Ah AEh AFh (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Vcore A Readout	0	20	RO	**Vcore A Voltage**							
Vcore B Readout	0	21	RO	**Vcore B(VIN4) Voltage**							
VIN0 Readout	0	22	RO	**VIN0 Voltage**							
VIN1 Readout	0	23	RO	**VIN1 Voltage**							
VIN2 Readout	0	24	RO	**VIN2 Voltage**							
VIN3 Readout	0	25	RO	**VIN3 Voltage**							
5VCC Readout	0	26	RO	**5VCC Voltage**							
Temperature 1 Readout	0	27	RO	**Temperature Sensor 1**							
FAN 1 Count	0	28	RO	**FAN 1 Count Readout**							
FAN 2 Count	0	29	RO	**FAN 2 Count Readout**							
FAN 3 Count	0	2A	RO	**FAN 3 Count Readout**							
LOW BITS I	0	3E	RO	**VIN1**		**VIN0**		**VCOREB**		**VCOREA**	
LOW BITS II	0	3F	RO	**TEMP1**	**EN_HLD**	**5VCC**		**VIN3**		**VIN2**	

Value RAM stores the latest sensed system parameter. Each data will refresh automatically after the channel input converted.

EN_HLD bit(Writable, default is 0) of AFh is capable of turn on Sample and Hold mechanism.

VcoreA Calculation

Vcore A Voltage = (CR[20]*4 + CR[3E]&0x03) * 0.002;

VcoreB Calculation

VcoreB Voltage = (CR[21]*4 + CR[3E]&0x0C/4) * 0.002;

VIN0~VIN3 Calculation

VIN0 Voltage = (CR[22]*4 + CR[3E]&0x30/16) * 0.004;

VIN1 Voltage = (CR[23]*4 + CR[3E]&0xC0/16) * 0.004;

VIN2 Voltage = (CR[24]*4 + CR[3F]&0x03) * 0.004;

VIN3 Voltage = (CR[25]*4 + CR[3F]&0x0C/4) * 0.004;

5VCC Calculation

5VCC Voltage = (CR[26]*4 + CR[3F]&0x30/16) * 0.006;

8.7 Limit RAM — Index 2Bh- 2Dh (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Vcore 1 High Limit	0	2B	RW	Vcore A Voltage High Limit (unit 8mV)							
				DEPENDS ON VID							
MNEMONIC	**BANK**	**INDEX**	**ATTR**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Vcore 1 Low Limit	0	2C	RW	Vcore A Voltage Low Limit							
				DEPENDS ON VID							
Vcore 2 High Limit	0	2D	RW	Vcore B Voltage High Limit							
				DEPENDS ON VID							
Vcore 2 Low Limit	0	2E	RW	Vcore B Voltage Low Limit							
				DEPENDS ON VID							
VIN0 High Limit	0	2F	RW	VIN0 Voltage High Limit							
				FFh							
VIN0 Low Limit	0	30	RW	VIN0 Voltage Low Limit							
				00h							
VIN1 High Limit	0	31	RW	VIN1 Voltage High Limit							
				FFh							
VIN1 Low Limit	0	32	RW	VIN1 Voltagez							
				00h							
VIN2 High Limit	0	33	RW	VIN2 Voltage High Limit							
				FFh							
VIN2 Low Limit	0	34	RW	VIN2 Voltage Low Limit							
				00h							
VIN3 High Limit	0	35	RW	VIN3 Voltage High Limit							
				FFh							
VIN3 Low Limit	0	36	RW	VIN3 Voltage Low Limit							
				00h							
5VCC High Limit	0	37	RW	5VCC Voltage High Limit							
				FFh							
5VCC Low Limit	0	38	RW	5VCC Voltage Low Limit							
				00h							
Temperature 1 High Limit	0	39	RW	Temperature Sensor 1 High Limit							
				7Fh							
Temperature 1 Low Limit	0	3A	RW	Temperature Sensor 1 Low/Hysteresis Limit							
				00h							
FAN 1 Count High Limit	0	3B	RW	FAN 1 Count High Limit							
				FFh							
FAN 2 Count High Limit	0	3C	RW	FAN 2 Count High Limit							
				FFh							
FAN 3 Count High Limit	0	3D	RW	FAN 3 Count High Limit							
				FFh							

Limit RAM setups the high/low limit for each channel in Value RAM. While exceeding these limits, system will take certain action determined by prior setups.

FAN Count high limits should be the limit for lowest fan speed. This is because the slower the fan is, the more the internal clock will be counted by internal clock.

Setting all ones to the high limits for voltages and fans (0111 1111 binary for temperature) means interrupt will never be generated except the case when voltages go below the low limits.

VcoreA Limit Setup

CR[2B/2C] = [Desired Voltage]/0.008;

VcoreB Limint Setup

CR[2D/2E] = [Desired Voltage]/0.008;

VIN0~VIN3 Limit Setup

CR[2F~36] = [Desired Voltage] / 0.016;

5VCC Limit Setup

CR[37/38] = [Desired Voltage] / 0.024;

8.8 Configuration Register — Index 40h (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Configuration	0	40	RW	INIT	IRQEDGE	IRQPOL	ENWDT	INT_CLR	EN_IRQ	EN_SMI	START
				0	0	0	0	0	0	0	1

Reset Condition: Resume Reset, INIT.
Configuration Register controls the system reset, stop, power down and warning output mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Initialization	R/W	Set one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.
6	IRQ output	R/W	Set 0 , IRQ output level signal . Set 1, output 200 us pulse signal. Default is 0.
5	IRQ Polarity	R/W	When set to 0, IRQ active high. Set to 1, IRQ active low. Default is 0.
4	ENWDT	R/W	Set this bit to 1 will enable Watch Dog Timer function. Watch dog timer function will reset system(pin 47) while it timeouts.
3	INT_Clear	R/W	A one disables the SMI# and IRQ# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring at last channel. It will resume upon clearing of this bit. Note: The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

Continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
2	EN_IRQ	R/W	A one enables the IRQ Interrupt output.
1	EN_SMI#	R/W	A one enables the SMI# Interrupt output. If EN_SMI# and EN_IRQ are both set to 1, SMI# will override the IRQ output.
0	START	R/W	A one enables startup of monitoring operations; a zero puts the analog part in Power-down mode. **Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

8.9 Interrupt Status Registers — Index 41h 42h 9Bh(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Interrupt Status 1	0	41	RO	**FAN3**	**FAN2**	**FAN1**	**TEMP3**	**TEMP2**	**TEMP1**	**VcoreB**	**VcoreA**
Interrupt Status 2	0	42	RO	**FAN7**	**VIDCHG**	**Chassis**	**5VCC**	**VIN3**	**VIN2**	**VIN1**	**VIN0**
Interrupt Status 3	0	9B	RO	**FAN6**	**FAN5**	**FAN4**	**VBAT**	**VSB**	**TART3**	**TART2**	**TART1**

An one represents corresponding channel have been exceed its limit.

TART will assert while target temperature cannot be achieved after 3 minutes full speed of corresponding FAN. Read Interrupt Status will clear the interrupt flag.

8.10 SMI#/IRQ Mask Registers — Index 43h~45h 9Ch 9Dh(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SMI/IRQ Mask 1	0	43	RW	**FAN3**	**FAN2**	**FAN1**	**TEMP3**	**TEMP2**	**TEMP1**	**VcoreB**	**VcoreA**
				0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SMI/IRQ Mask 2	0	44	RW	**CLR_CHS**	**VIDCHG**	**Chassis**	**VDD**	**VIN3**	**VIN2**	**VIN1**	**VIN0**
				0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
SMI/IRQ Mask 3	0	9C	RW	**FAN6**	**FAN5**	**FAN4**	**VBAT**	**VSB**	**TART3**	**TART2**	**TART1**
				0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

These are SMI/IRQ mask registers. Set to one will disable the corresponding interrupt sources. Clear to 0 will enable that interrupt source.

SMI Mask 2 bit 7 is CLR_CHS(Clear Chassis), write this bit with an one will clear internal caseopen latch, and after latch is clear, CLR_CHS will be reset to 0 itself.

8.11 Realtime Status Registers — Index A9h~ABh(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Realtime status 1	0	A9	RO	FAN3	FAN2	FAN1	TEMP3	TEMP2	TEMP1	VcoreB	VcoreA
Realtime status 2	0	AA	RO	FAN7	VIDCHG	Chassis	VDD	VIN3	VIN2	VIN1	VIN0
Realtime status 3	0	AB	RO	FAN6	FAN5	FAN4	VBAT	VSB	TART3	TART2	TART1

Realtime status registers show the related channel exceeding limit or not at the polling moment. Return 1 represents related channel have exceeded the limit defined in limit RAM.

8.12 Serial Bus Address Registers — Index 48h 4A(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SMBus Address	0	48	RW	reserve	SMBus address						
				0	0	1	0	1	1	IA[1]	IA[0]
TEMP2/3 Address	0	4A	RW	DIS_T3	T3 Address			DIS_T2	T2 Address		
				0	1	IA[1]	IA[0]	0	0	IA[1]	IA[0]

Reset Condition: Resume Reset

W83792D provides 2 power on strapping pin for default SMBus address. With these 2 pins, 4 kinds of default address setups are possible.

CR48 SMBus Address

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	RO	Reserved.
6-0	SMBADDR1	R/W	Serial Bus Address <7:1> for general index registers. The address bit 0 and bit 1 are trapped by the pin 10 and pin 11, respectively.

CR4A Temperature 2 and Temperature 3 Serial Bus Address Register

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	DIS_T3	R/W	Set to 1, disable temperature 3 sensor accessing from Temperature 3 Serial Bus Address. Still can access from Bank 0 Cxh.
6-4	I2CADDR3	R/W	Temperature 3 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.
3	DIS_T2	R/W	Set to 1, disable temperature Sensor accessing from Temperature 2 Serial Bus Address. Still can access from Bank 0 Cxh.
2-0	I2CADDR2	R/W	Temperature 2 Serial Bus Address. The serial bus address is 1001xxx. Where xxx are defined in these bits.

8.13 ID, Bank Select Registers-- Index 49h 4Eh 4Fh 58h (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Version ID	0	49	RO	13h for CSB version.							
Bank Select	x	4E	RW	HBACS	Reserved				BANK Select		
				1	0 RO				0	0	0
Winbond vendor ID(Toggle)	0	4F	RO	Return 5Ch(if HBACS=1); return A3h(if HBACS=0)							
Winbond Chip ID	0	58	RO	7Ah							

CR4E Bank Select Register (**Reset Condition:** Resume Reset)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	HBACS	R/W	High Byte Access of Winbond Vendor ID. Set to 1, read 4Fh will get 5Ch ; Clear as 0, read 4Fh will return A3h.
2-0	Bank Select	R/W	Bank select is to change current indexed bank. Available banks are 0,1, and 7.

8.14 Pin Control Register -- Index4Bh (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Pin Control	0	4B	RW	VIDLevel	FAN6/WDT	SELVIDA	SELVIDB	reserve	EnFAN7	TT Level	
				VRM10	0	0	0	0	0	0	

Reset Condition: Resume Reset

Pin Controls enables different pin/clock selections.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	VID Level	R/W	Set this bit enables VID with 0.8/0.4V level. Clear this bit makes VID in input mode with TTL level. Default value is set by VRM10 power-on trapping.
6	FAN6/WDT	R/W	Set this bit enables FAN6 Functionality. Default is Watch Dog Timer Function. Clear this bit to 0 will perform Watch Dog Functionality on Pin 47/48.
5	SELVIDA	R/W	Set to enable VIDA with offset output at VID port B. Clear to disable this function.
4	SELVIDB	R/W	Set to enable VIDB with offset output at VID port A. Clear to disable this function.
3	reserve	R/W	reserved
2	FAN7 Enable	R/W	Set to enable FAN7 function and disable Thermaltrip/VRM_EN pin function.
1-0	Thermal Trip Level	R/W	Thermal Trip Level Selector. These two bits select the input level for ThermalTrip 1/2. 11b is 1.0Vref GTLP. 10b enables 0.8Vref GTL. 00b set these 2 pins to TTL.

8.15 SMI#/OVT# Property Select -- Index 4Ch (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IRQ/OVT Polarity	0	4C	RW	TEMP_SMI_MD		OVT_MD		EN_OVT3	EN_OVT2	EN_OVT1	OVTPOL
				0(Comp Interrupt)		0(Comparator)		0	0	0	1
ACPI Difference	0	5E	RW	reserve	DIFFREG (ACPI Increment Difference)						
				0	5						

Reset Condition: Resume Reset.

Register 4Ch selects SMI modes, OVT modes, OVT sources and OVT polarity.

If OVT_MD selects ACPI mode, register 5Eh determines the temperature interval between each OVT is issued. Default sets to 5, that is, every time temperature reaches 5*n degree, an OVT will be issued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	TEMP_SMI_MD [1:0]	R/W	**Temperature SMI# Mode Select.** <00> - **Comparator Interrupt Mode:(Default)** Temperature 1/2/3 exceeds T_O (Over-temperature) limit causes and interrupt and this interrupt will be reset by reading all the Interrupt Status. <01> - **Two Time Interrupt Mode:** This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. <10> **- One Time Interrupt Mode:** This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O (Over-temperature, defined in Bank 1/2) causes an interrupt and then temperature going below T_{HYST} (Hysteresis temperature, defined in Bank 1/2) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, and interrupt will not occur again until the temperature exceeding T_O.

Continued.

BIT	NAME	ATTRIBUTE	DESCRIPTION
5-4	OVT_MD[1:0]	R/W	**OVT# Mode Select.** There are three OVT# signal output type. <00> - **Comparator Mode:** (Default) Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. <01> - **Interrupt Mode:** Setting temperature exceeding T_O causes the OVT# output activated indefinitely until reset reading temperature sensor 1/2/3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor 1/2/3(reading interrupt status). Once the OVT# will not be activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again. <10> - **ACPI Mode:** If set to 1 then enable ACPI OVT# output. Which is always send an OVT# pulse signal (22us, if not a suddenly temperature jump)when the temperature over the ACPI temperature increment value defined at Index 5Eh.
3	EN_OVT3	R/W	**Enable temperature sensor 3 over-temperature (OVT) output** if set to 1. Default 0, disable OVT2 output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT2.
2	EN_OVT2	R/W	**Enable temperature sensor 2 over-temperature (OVT) output** if set to 1. Default 0, disable OVT2 output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT3.
1	EN_OVT1	R/W	**Enable temperature sensor 1 over-temperature (OVT) output** .if set to 1. Default 0, disable OVT1 output through pin OVT#. The pin OVT# is wire OR with OVT2 and OVT3.
0	OVTPOL	R/W	**Over-Temperature Polarity.** Write 0, OVT# active high. Write 1, OVT# active low. Default is 1 .

8.16 Diode Selection Register -- Index 59h (Bank 0)

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Thermal Diode Select	0	59	RW	reserve	TDSEL3	TDSEL2	TDSEL1	K8SEL1	NVSEL1	K8SEL23	NVSEL23
				0	1	1	0	0	0	0	0
Temperature 1 Offset	0	90	RW	reserve		OFFSET1					
				0		00h					
Temperature 2 Offset	0	91	RW	reserve		OFFSET2					
				0		0					
Temperature 3 Offset	0	92	RW	reserve		OFFSET3					
				0		00h					

Reset Condition: Resume Reset, INIT.

CR59h Thermal Diode Select

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	RO	Reserved.
6	TDSEL3	R/W	Temperature sensor 3 diode mode. When set to 1, select Pentium IV compatible Diode. Set to 0 to select Thermistor mode
5	TDSEL2	R/W	Temperature sensor 2 diode mode. When set to 1, select Pentium IV compatible Diode. Set to 0 to select Thermistor mode
4	TDSEL1	R/W	Temperature sensor 1 diode mode. When set to 1, select Pentium IV compatible Diode. Set to 0 to select Thermistor mode
3	K8SEL1	R/W	Set to select K8 Temperature Table for VTIN1.
2	NVSEL1	R/W	Set to select nVidia NV34 Temperature Table for VTIN1.
1	K8SEL23	R/W	Set to select K8 Temperature Table for VTIN2/3.
0	NVSEL23	R/W	Set to select nVidia NV34 Temperature Table for VTIN2/3.

K8 and NV34 GPU table is also supported in W83792D. VTIN2, VTIN3 should be always in the same mode since they will decide the VID mapping. There is only one exception, that is, thermistor mode. VTIN2 and VTIN3 can choose one in thermistor mode and another in other modes.

VTIN1 is separately set up in this configuration.

Configuration these bits have priority as…

Thermistor mode > K8 diode mode > NVIDIA diode mode > P4 mode.

CR90h-92h Temperature Offset

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved	RO	Reserved.
5-0	Temperature Offset	R/W	Related temperature channel base temperature. The temperature is added by both monitor value and offset value. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree C

8.17 FANIN Divisor Control Registers -- Index 47h 5Bh 5Ch(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN Divisor 1	0	47	RW	FAN2_OB	FAN 2 Divisor			FAN1_OB	FAN 1 Divisor		
				0	1			0	1		
FAN Divisor 2	0	5B	RW	FAN4_OB	FAN 4 Divisor			FAN3_OB	FAN 3 Divisor		
				0	1			0	1		
FAN Divisor 3	0	5C	RW	FAN6_OB	FAN 6 Divisor			FAN5_OB	FAN 5 Divisor		
				0	1			0	1		
FAN 7 Divisor and Control	0	9E	RW	Manual	Trigger	Mask	Reserve	FAN7_OB	FAN 7 Divisor		
				0	0	0	0	0	1		

Reset Condition: Resume Reset, INIT, 5VDD posedge

BIT	NAME	ATTRIBUTE	DESCRIPTION
7,3	FAN_OB	R/W	**Enable Fan as Output Buffer.** Set to 1, FANOUT can drive logical high or logical low.
6-4, 2-0	FAN_DIV	R/W	**FAN PWM Input Divisor**. 000 - divided by 1; 001 - divided by 2(Default); 010 - divided by 4; 011 - divided by 8; 100 - divided by 16; 101 - divided by 32; 110 - divided by 64; 111 - divided by 128.

W83792D supports different FAN power on time. The FAN will power on one by one after 5VDD is ready. (At sequence FAN6-2-3-1-4-5) Fan Divisor also determines the FAN power on time. Under power-on-default setting(divisor = 2), to power on all FAN will take 71.5ms. If divisor is change, the timing will be different.

CR9E FAN 7 Divisor and Control

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Manual	R/W	**Fan7 Automatic/Manual Mode Selection.** Clear to 0, always polling FAN7 automatically; Set to 1, only polling once while Trigger<bit 6> is set to 1.
6	Trigger	R/W	**Fan7 count trigger.** Once set, W83792D will count FANIN7 in Auto Mode. After FAN count write back, this bit will be clear to 0.
5	Mask	R/W	Interrupt/SMI mask for FAN7.

8.18 VBAT Monitor Control Register -- Index 5Dh (Bank 0)

OLARIT	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VBAT Monitor Control	0	5D	RW	TT1	TT2	reserve		CLR_TT1	CLR_TT2	reserve	EN_VBAT
				RO	RO	0		0	0	0	0

Reset Condition: Resume Reset

.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TT1	RO	Thermal Trip 1 event log. Powered by VBAT.
6	TT2	RO	Thermal Trip 2 event log. Powered by VBAT.
5-4,1	reserve	RO	Reserved.
3	CLR_TT1	R/W	Set this bit to 1 will reset TT1 to 0, after bit 7 reset, CLR_TT1 will deassert automatically.
2	CLR_TT2	R/W	Set this bit to 1 will reset TT2 to 0, after bit 6 reset, CLR_TT2 will deassert automatically.
0	EN_VBAT_MNT	R/W	Write 1, enable battery voltage monitor. Write 0, disable battery voltage monitor. If enable this bit, the monitor value is valid after one monitor cycle.

TT1, TT2, 2 thermal trip event log bits powered by VBAT. They will never cleared by all reset. To clear it must set CLR_TT1 and CLR_TT2 to 1. For real time status of Thermal trip, please refer to CR[1F].

8.19 FAN Pre-Scale Registers-- Index 80h 82h 93h A0h A1h A2h(Bank 0)

OLARIT	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PWM1 Prescalar	0	80	RW	**CLKSEL**	**PRE_SCALE1**						
				0	**01h (divider equals PRE_SCALE1 + 1)**						
PWM 2 Prescalar	0	82	RW	**CLKSEL**	**PRE_SCALE2**						
				0	**01h (divider equals PRE_SCALE2 + 1)**						
FAN 3 Prescalar	0	93	RW	**CLKSEL**	**PRE_SCALE3**						
				0	**01h**						
FAN 4 Prescalar	0	A0	RW	**CLKSEL**	**PRE_SCALE4**						
				0	**01h**						
FAN 5 Prescalar	0	A1	RW	**CLKSEL**	**PRE_SCALE5**						
				0	**01h**						
FAN 6 Prescalar	0	A2	RW	**CLKSEL**	**PRE_SCALE6**						
				0	**01h**						
FAN 7 Prescalar	0	9D	RW	**CLKSEL**	**PRE_SCALE7**						
				0	**01h**						

Reset Condition: Resume Reset, INIT, 5VDD posedge.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM_CLK_SEL	R/W	**PWM Input Clock Select.** This bit select Fan input clock to pre-scale divider. 0: 14.318MHz(External) 1: 1MHz(Internal)
6-0	PRE_SCALE[6:0]	R/W	**Fan PWMOUT Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM frequency = (Input clock / pre-scale) / 16

8.20 FAN Duty Cycle Select Register--81h 83h 94h A3h A4h A5h(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 1 Duty Cycle	0	81	RW	PWM/DC	reserve			PRGVAL1			
				1	0			Fh			
FAN 2 Duty Cycle	0	83	RW	PWM/DC	reserve			PRGVAL2			
				1	0			Fh			
FAN 3 Duty Cycle	0	94	RW	PWM/DC	reserve			PRGVAL3			
				1	0 RO			Fh			
FAN 4 Duty Cycle	0	A3	RW	PWM/DC	SYNC T1/2/3		reserve	PRGVAL4			
				1	0(Stand alone)		0	Fh			
FAN 5 Duty Cycle	0	A4	RW	PWM/DC	SYNC T1/2/3		reserve	PRGVAL5			
				1	0		0	Fh			
FAN 6 Duty Cycle	0	A5	RW	PWM/DC	SYNC T1/2/3		reserve	PRGVAL6			
				1	0		0	Fh			
FAN 7 Duty Cycle	0	A6	RW	PWM/DC	SYNC T1/2/3		reserve	PRGVAL7			
				1	0		0	Fh			

Reset Condition: Resume Reset, INIT.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	PWM/DC	R/W	**PWM/DC FAN Config.** Set 1, FANOUT is configured as PWM output. Clear to 0, FANOUT is configured as DC output.
6-5	SYNC T1/2/3	R/W	**Sync with Temp Sensor.** 00: Stand alone, does not sync with any temperature sensor 01: Sync with Temp1. 10: Sync with Temp2. 11: Sync with Temp3.
4	Reserve	RO	**Reserved**
3-0	FAN_DC[3:0]	R/W	**Fan Duty Cycle.** This 4-bit register determines the number of input clock cycles, out of 16-cycle period, during which the PWM output is high. During smart fan control mode, read this register will return smart fan duty cycle. In Manual mode, write this register to control the output PWM Duty cycle. 0h: PWM output is always logical Low. Fh: PWM output is always logical High. Xh: PWM output logical High percentage is (X/16*100%) during one cycle.

Notice. To use **SYNC T1/2/3** function, the corresponding FAN1, FAN2, or FAN3 must be enabled with temperature cruise mode. Otherwise, only 2 DC output is available. One is full speed when exceeding flag raised, and the other is start speed when not exceeding temperature limit.

User may not read out PRGVAL with 0xF when system power up, because the FAN will sequentially powered on one by one. The order of FAN power on is followed the sequence 6-2-3-1-4-5.

At DC FAN mode, the output level and corresponding programmed value have the relation as following table.

PRGVAL	OUTPUT LEVEL (VOLT)	PRGVAL	OUTPUT LEVEL (VOLT)
0000	0	1000	2.50
0001	0.31	1001	2.81
0010	0.62	1010	3.12
0011	0.94	1011	3.44
0100	1.25	1100	3.75
0101	1.56	1101	4.06
0110	1.87	1110	4.37
0111	2.19	1111	4.69

For Fan1, Fan2, and Fan 3, the output value will be affected by power-on-strap resistor. In the case of using 100K resistor, the output drifts about 0.15V with normal value.

8.21 FAN 1/2 Configuration Register-- Index 84h (Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN Configuration	0	84	RW	reserve		FAN3_TYPE		FAN2_TYPE		FAN1_TYPE	
				0h		0		0		0	

Reset Condition: Resume Reset, INIT, 5VDD posedge.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-6	Reserved		Reserved
5-4	FAN3_TYPE	R/W	**FAN 3 PWM Control Type**. 00 - Manual PWM/DC Control Mode. (Default) 01 - Thermal Cruise mode. (Corresponding to VTIN3) 10/11 – Smart FAN II mode. (Corresponding to VTIN3)
3-2	FAN2_TYPE	R/W	**FAN 2 PWM Control Type**. 00 - Manual PWM/DC Control Mode. (Default) 01 - Thermal Cruise mode. (Corresponding to VTIN2) 10/11 – Smart FAN II mode. (Corresponding to VTIN2)
1-0	FAN1_TYPE	R/W	**FAN 1 PWM Control Type**. 00 - Manual PWM/DC Control Mode. (Default) 01 - Thermal Cruise mode. (Corresponding to VTIN1) 10/11 – Smart FAN II mode. (Corresponding to VTIN1)

8.22 Fan 1 Target Temperature Registers -- Index 85h 86h 96h(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 1 Target Temperature	0	85	RW	reserve	FAN_TAR_T1						
				0	00h						
FAN 2 Target Temperature	0	86	RW	reserve	FAN_TAR_T2						
				0	00h						
FAN 3 Target Temperature	0	96	RW	reserve	FAN_TAR_T3						
				0 RO	00h						

Reset Condition: Resume Reset, INIT, 5VDD posedge.

VTIN target temperature register for Thermal Cruise mode.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved		Reserved.
6-0	FAN_TAR_T	R/W	**Fan Target Temperature. / Temperature Point 1** *For Thermal Cruise mode.* When the sensed temperature is over the target temperature with tolerance, the smart fan duty cycle will go up until the duty cycle reach FFh. *For Smart Fan II Mode,* this temperature is used to distinguish the FANOUT between Fan Duty Cycle Level 1 and Non-stop Duty Cycle.

8.23 Tolerance of Fan1/2 Target Temperature Register -- Index 87h 97h(Bank0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN Tolerance	0	87	RW	TOL_TEMP2				TOL_TEMP1			
				0h				0h			
FAN 3 Tolerance	0	97	RW	reserve				TOL_TEMP3			
				0 RO				0h			

Reset Condition: Resume Reset, INIT, 5VDD posedge.

Tolerance of Fan1/2 target temperature register.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	TOL_T2[3:0]	R/W	**Tolerance of Fan 2 Target Temperature.** Only for Thermal Cruise mode and Smart Fan II mode.
3-0	TOL_T1[3:0]	R/W	**Tolerance of Fan 1 Target Temperature.** Only for Thermal Cruise mode and Smart Fan II mode.

Tolerance of Fan 3 target temperature register.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	reserved	R/W	**reserved**
3-0	TOL_T3[3:0]	R/W	**Tolerance of Fan 3 Target Temperature.** Only for Thermal Cruise mode and Smart Fan II mode.

8.24 Fan Stop/Start Duty Cycle/DC Level Registers -- Index 88h 89h 98h(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 1 Nonstop/Start	0	88	RW	START_DC1				MIN_NOSTOP_DC1			
				01h				01h			
FAN 2 Nonstop/Start	0	89	RW	START_DC2				MIN_NOSTOP_DC2			
				01h				01h			
FAN 3 Nonstop/Start	0	98	RW	START_DC3				MIN_NOSTOP_DC3			
				01h				01h			

Reset Condition: Resume Reset, INIT, 5VDD posedge.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	START_DC	R/W	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle. At Smart Fan II mode. This register is used as Fan Duty Cycle Level 1.
3-0	STOP_DC	R/W	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

8.25 Fan Stop Time Register -- Index 8Ch 8Dh 9Ah(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 1 Stop Time	0	8C	RW	STOP_TIME1							
				3Ch (6 sec)							
FAN 2 Stop Time	0	8D	RW	STOP_TIME2							
				3Ch (6 sec)							
FAN 3 Stop Time	0	9A	RW	STOP_TIME3							
				3Ch (6 sec)							

Reset Condition: Resume Reset, INIT, 5VDD posedge.

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STOP_TIME	R/W	In Thermal Cruise mode, this register determines the time of which PWM duty/DC Level is from stop duty cycle/DC level to 0. The unit of this register is 0.1 second. **Set Stop Time to 0 implies never stop FANs**. The default value is 6 seconds.

8.26 Fan Step Down/Up Time Register -- Index 8Eh 8Fh(Bank 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN Step Up Time	0	8E	RW	UPTIME							
				0Ah (1 sec)							
FAN Step Down Time	0	8F	RW	DOWNTIME							
				0Ah (1 sec)							

Reset Condition: Resume Reset, INIT, 5VDD posedge.

FAN Step Up Time

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STEP_DOWN_T	R/W	The time interval, which is 0.1 second unit, to decrease PWM duty in Thermal Cruise mode.

FAN Step Down Time

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	STEP_UP_T	R/W	The time interval, which is 0.1 second unit, to increase PWM duty in Thermal Cruise mode.

8.27 Fan 1/2/3 Smart Fan II Temperature/ Duty Cycle setups -- Index E0h~EBh 5Fh(Bank 0)

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 1 Duty Cycle Level	0	E0	RW	Fan Duty Cycle Level 2				Fan Duty Cycle Level 3			
				8h				Bh			
FAN 2 Duty Cycle Level	0	E1	RW	Fan Duty Cycle Level 2				Fan Duty Cycle Level 3			
				8h				Bh			
FAN 3 Duty Cycle Level	0	E2	RW	Fan Duty Cycle Level 2				Fan Duty Cycle Level 3			
				8h				Bh			
FAN 1 Temperature Point 2	0	E3	RW	reserve	Temperature Point 2						
				0	28h						
FAN 1 Temperature Point 3	0	E4	RW	reserve	Temperature Point 3						
				0	3Ch						
FAN 1 Temperature Point 4	0	E5	RW	reserve	Temperature Point 4						
				0	50h						
FAN 2 Temperature Point 2	0	E6	RW	reserve	Temperature Point 2						
				0	28h						
FAN 2 Temperature Point 3	0	E7	RW	reserve	Temperature Point 3						
				0	3Ch						
FAN 2 Temperature Point 4	0	E8	RW	reserve	Temperature Point 4						
				0	50h						

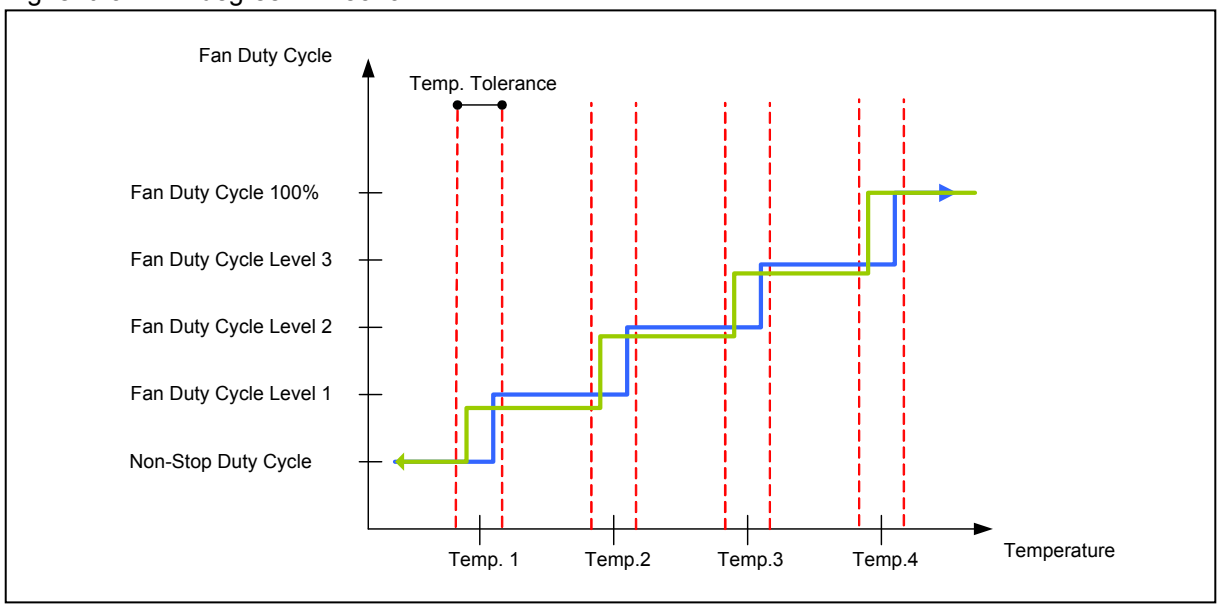
Fan 1/2/3 Smart Fan II Temperature/ Duty Cycle setups -- Index E0h~EBh 5Fh(Bank 0), continued.

Mnemonic	Bank	Index	Attr	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FAN 3 Temperature Point 2	0	E9	RW	**reserve**	**Temperature Point 2**						
				0	**28h**						
FAN 3 Temperature Point 3	0	EA	RW	**reserve**	**Temperature Point 3**						
				0	**3Ch**						
FAN 3 Temperature Point 4	0	EB	RW	**reserve**	**Temperature Point 4**						
				0	**50h**						
All FAN on Temperature Point	0	5F	RW	**reserve**	**Temperature point above this will turn all FAN to full speed**						
				0	**7Fh**						

Reset Condition: Resume Reset, INIT.

W83792D also provides a special mode for FAN. It's called Smart Fan II mode. In this mode, W83792D will output fix cycles when related temperature sensors detects the temperature in preset temperature region. Their relation looks like the following figure.

5Fh specifies a temperature point, if any temperature sensor is sensed above this, all FAN will be push to full speed. Default is 127 degree, that means, this is disabled, since no temperature can higher than 127 degree in W83792D.



In Register E0h-EBh defines the relationship of temperature and duty cycle. Also previous Target Temperature and Non-Stop Duty Cycle are used as Temperature Point 1 and minimum duty cycle.

To prevent FAN Duty Cycle from throttling at Temperature Point, Temperature Tolerances(87h, 97h) are used to provide a hysterisis mechanism. When temperature is going up (Blue Line), duty cycle changes only when temperature reaches Temperature Point + Tolerance. On the contrary, when temperature is going low (Green Line), duty cycle changes only when sensor temperature down to Temperature Point – Tolerance.

FAN Duty Cycle Level

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-4	Duty Cycle Level 2	R/W	For Smart Fan II mode. The output duty cycle when temperature is between Temperature point 2 and 3.
3-0	Duty Cycle Level 3	R/W	For Smart Fan II mode. The output duty cycle when temperature is between Temperature 3 and 4.

FAN Temperature Point

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	Reserved	RO	reserved
6-0	Temperature	R/W	For Smart Fan II mode. Specifies each temperature point at which the output duty cycle changes.

8.28 Value RAM 2— Index B0h B1h B8h ~ BAh (BANK 0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5VSB Readout	0	B0	RO	**5VSB Voltage Readout**							
VBAT Readout	0	B1	RO	**VBAT Voltage Readout**							
FAN4 Readout	0	B8	RO	**FAN 4 Count Reading**							
FAN5 Readout	0	B9	RO	**FAN 5 Count Reading**							
FAN6 Readout	0	BA	RO	**FAN 6 Count Reading**							
FAN7 Readout	0	BE	RO	**FAN 7 Count Reading**							

5VSB Calculation

5VSB Voltage = CR[B0] * 0.024;

VBAT Calculation

VBAT Voltage = CR[B1] * 0.016;

8.29 Limit RAM 2--- Index B4h~B7h BBh~BDh (BANK0)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5VSB High Limit	0	B4	RO	5VSB Voltage High Limit							
				FFh							
5VSB Low Limit	0	B5	RO	5VSB Voltage Low Limit							
				00h							
VBAT High Limit	0	B6	RO	VBAT Voltage High Limit							
				FFh							
VBAT Low Limit	0	B7	RW	VBAT Voltage Low Limit							
				00h							
FAN4 Limit	0	BB	RW	FAN 4 Count Low Limit							
				FFh							
FAN5 Limit	0	BC	RW	FAN 5 Count Low Limit							
				FFh							
FAN6 Limit	0	BD	RW	FAN 6 Count Low Limit							
				FFh							
FAN7 Limit	0	BF	RW	FAN 7 Count Low Limit							
				FFh							

5VSB Limit Setup

CR[B4/B5] = [Desired Voltage] / 0.024;

VBAT Limit Setup

CR[B6/B7] = [Desired Voltage] / 0.016;

8.30 Temperature Sensor 2 (First LM75)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Temperature 2 Readout	0	C0	RO	Temperature 2							
Temperature 2 Readout	0	C1	RO	0.5deg							
Temperature 2 Config	0	C2	RW	reserve		#of faults		reserve			STOP
				0		0		0		0	
Temperature 2 Thyst High	0	C3	RW	Temperature 2 Thryst							
				4Bh							
Temperature 2 Thyst Low	0	C4	RW	0.5deg	Reserve						
				0	0						

Temperature Sensor 2 (First LM75), continued.

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Temperature 2 Over High				0	C5	RW	Temperature 2 Over Limit				
							50h				
Temperature 2 Over Low				0	C6	RW	0.5deg	reserve			
							0	0			

8.31 Temperature (High Byte) Register - Index C0h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	TEMP2<8:1>	Read Only	Temperature <8:1> of VTIN 2, which is high byte.

8.32 Temperature Sensor 2 Temperature (Low Byte) Register - Index C1h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TEMP2<0>	Read Only	Temperature <0> of VTIN2, which is low byte.
6-0	Reserved	Read Only	Read 0.

8.33 Temperature Sensor 2 Configuration Register - Index C2h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-5	Reserved	RO	Reserved
4-3	FAULT	R/W	Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
2:1	Reserved		Reserved
0	STOP2	R/W	When set to 1 the sensor will stop monitor.

8.34 Temperature Sensor 2 Hysteresis (High Byte) Register - Index C3h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	THYST2<8:1>	R/W	Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

8.35 Temperature Sensor 2 Hysteresis (Low Byte) Register - Index C4h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	THYST2<0>	R/W	Temperature hysteresis bit 0, which is low Byte.
6-0	Reserved	Read Only	Read 0

8.36 Temperature Sensor 2 Over-temperature (High Byte) Register -Index C5h (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	TOVF2<8:1>	R/W	Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

8.37 Temperature Sensor 2 Over-temperature (Low Byte) Register - Index C6h(Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	TOVF2<0>	R/W	Over-temperature bit 0, which is low Byte.
6-0	Reserved	Read Only	Read 0

8.38 Temperature Sensor 3 (Second LM75)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Temperature 3 Readout	0	C8	RO	**Temperature 3**							
Temperature 3 Readout	0	C9	RO	**0.5deg**							
Temperature 3 Config	0	CA	RW	**reserve**		**#of faults**		**reserve**			**STOP**
				0		**0**		**0**			**0**
Temperature 3 Thyst High	0	CB	RW	**Temperature 3 Thryst**							
				4Bh							
Temperature 3 Thyst Low	0	CC	RW	**0.5deg**	**Reserve**						
				0	**0**						
Temperature 3 Over High	0	CD	RW	**Temperature 3 Over Limit**							
				50h							
Temperature 3 Over Low	0	CE	RW	**0.5deg**	**Reserve**						
				0	**0**						

8.39 Temperature Sensor 3 Hysteresis (High Byte) Register - Index CBh (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	THYST3<8:1>	R/W	Temperature hysteresis bit 8-1, which is High Byte. The temperature default 75 degree C.

8.40 Temperature Sensor 3 Hysteresis (Low Byte) Register - Index CCh (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
6-0	Reserved	Read Only	Read 0
7	THYST3<0>	R/W	Temperature hysteresis bit 0, which is low Byte.

8.41 Temperature Sensor 3 Over-temperature (High Byte) Register - Index CDh (Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7-0	OVTF3<8:1>	R/W	Over-temperature bit 8-1, which is High Byte. The temperature default 80 degree C.

8.42 Temperature Sensor 3 Over-temperature (Low Byte) Register - Index CEh(Bank 0)

BIT	NAME	ATTRIBUTE	DESCRIPTION
7	OVTF3<0>	R/W	Over-temperature bit 0, which is low Byte.
6-0	Reserved		Reserved

9. ARP (ADDRESS RESOLUTION PROTOCOL) REGISTERS

9.1 Unique Device Identifier (UDID) -- 20h-2Fh (Bank 1)

In order to provide a mechanism to isolate each device for the purpose of address assignment each device must implement a unique device identifier (UDID).

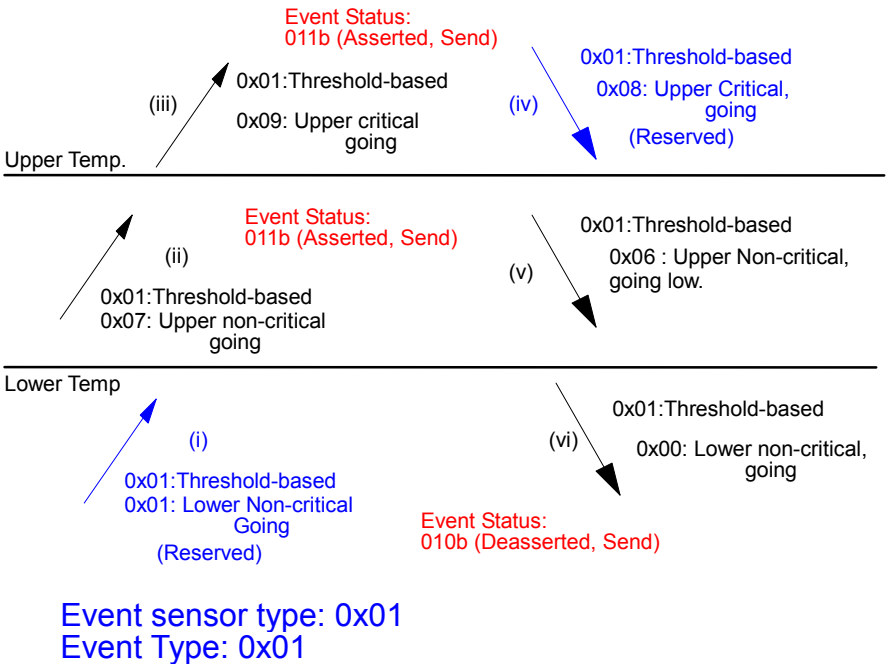
MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Capability	1	20	RO	Random Number		RESERVED					PEC
				1	1	0	0	0	0	0	1
Version/Revision	1	21	RO	RESERVED		SMBUS 2.0 SUPPORT			SILICON REVISION		
				0	0	0	0	1	0	1	1
Vendor ID	1	22-23	RO	WINBOND PCI SIG VENDOR ID							
				1050h							
Device ID	1	24-25	RW	DEVICE ID assigned by Manufacturer							
				0100h							
Interface	1	26-27	RW	ASF protocol layer interface over SMBus.							
				0024h							
Subsystem Vendor ID	1	28-29	RW	SUBSYSTEM VENDOR							
				0000h							
Subsystem Device ID	1	2A-2B	RW	SUBSYSTEM							
				0000h							
Vendor specific ID	1	2C-2F	RW	VENDOR SPEC							
				Random Number							

NAME	DESCRIPTIONS
Device Capabilities	Describes the device's capabilities. See detail SMBus 2.0.
Version/Revision	UDID version number and silicon revision identification. See detail SMBus2.0.
Vendor ID	The device manufacturer's ID as assigned by the SBS Implementers' Forum or the PCI SIG.
Device ID	The device ID as assigned by the device manufacturer (identified by the Vendor ID field).
Interface	Identifies the protocol layer interfaces supported over the SMBus connection by the device. For example, ASF and IPMI.
Subsystem Vendor ID	This field may hold a value derived from any of several sources: 1. The device manufacturer's ID as assigned by the SBS Implementers' Forum or the PCI SIG. 2. The device OEM's ID as assigned by the SBS Implementers' Forum or the PCI SIG. 3. A value that, in combination with the Subsystem Device ID, can be used to identify an organization or industry group that has defined a particular common device interface specification.
Subsystem Device ID	The subsystem ID identifies a specific interface, implementation, or device. The part identified by the Subsystem Vendor ID field defines the subsystem ID.
Vendor Specific ID	A unique number per device. See detail SMBus 2.0.

10. ASF SENSOR ENVIRONMENTAL EVENT

10.1 Temperature: Get Event Data message

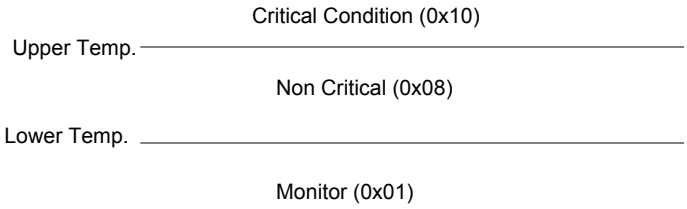
In the W83792D, it has three temperatures for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	TEMPERATURE 1
Event sensor type	0x01 (Temperature sensor)
Event type Event offset	Threshold-based: 0x01h. 
Event source type	The W83792D is complying ASF 2.0.I specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83792D is ARP assigned address.
Sensor number	Temperature 1: 0Dh (Don't use 00h and FFh. Therefore 01h → VCOREA). Temperature 2: 0Eh Temperature 3: 0Fh
Entity ID	Temperature 1: 07h (System board) Temperature 2/3: 03h (Processor) These are defined in Table 6 of PET v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.

Temperature: Get Event Data message, continued.

ASF PACKET DATA	TEMPERATURE 1
Entity instance	Temperature 1: 01h (main system board). Temperature 2: 01h (Processor 1) Temperature 3: 02h (Processor 2) These are programmable.
Event status index	Temperature 1: 0Ch (zero-based) Temperature 2: 0Dh Temperature 3: 0Eh
Event status	

Status Value	Status type	Description	Byte Count for GetEventStatus
0000_0010b	Deasserted (send)	Refer as above figure.	0Ah
0000_0011b	Asserted (send)	W83792D will respond all relative information.	0Ah
0000_0111b	Event Status End	When event status index is more than 14h, the machine will be ended the transmission.	02h

Event Severity	Monitor (0x01): That is represented the monitored temperature is under the lower temperature. Non Critical (0x08): that is represented the temperature is located between the lower and upper temperature. Critical Condition (0x10): that is represented the monitored temperature is over the upper temperature. 

Event Offset, Type and Severity

DESCRIPTION	SENSOR TYPE	EVENT TYPE	EVENT OFFSET	STATUS	EVENT SEVERITY
TEMPERATURE SENSORS					
Upper-Critical Going High	01h Temperature	01h Threshold-Based	09h	3h Assert	10h Critical
Upper-Critical Going Low			08h		
Upper-Non-critical Going High			07h		08h Non-critical
Upper-Non-critical Going Low			06h		
Lower-Non-critical Going High			01h	2h Deassert	01h Monitor
Lower-Non-critical Going Low			00h		
VOLTAGE SENSORS					
Generic Over Voltage Problem	02h Voltage	07h Generic-Severity	02h	3h	10h
Normal Voltage			07h	2h	01h
Generic Under Voltage Problem			02h	3h	10h
FAN SENSORS					
Normal FAN Speed	04h Fan	07h	07h	2h	01h
Generic FAN Failure			02h	3h	10h
CASEOPEN					
Case Intruded	05h Physical Security	6Fh Sensor Specific	00h	3h	10h
Case Normal			80h	2h	01h
THERMAL TRIP SENSORS					
Thermal Trip Occurs	07h Processor	6Fh	01h	3h	10h
No Thermal Trip			81h	2h	01h

Entity ID and Instance (Default):

ENTITY ID (PROGRAMMABLE)	ENTITY INSTANCE (PROGRAMMABLE)	SENSOR IN W83792D	EVENT STATUS INDEX	EVENT NUMBER	EVENT SENSOR TYPE
07h (System Board)	01h	VIN0	02h	03h	02h (Voltage)
	02h	VIN1	03h	04h	02h
	03h	VIN2	04h	05h	02h
	04h	VIN3	05h	06h	02h
	05h	5VDD	06h	07h	02h
	06h	VSB	07h	08h	02h
	07h	VBAT	08h	09h	02h
	01h	FAN1	09h	0Ah	04h (Fan)
	02h	FAN4	0Fh	10h	04h
	03h	FAN5	10h	11h	04h
	04h	FAN6	11h	12h	04h
	01h	Temperature1	0Ch	0Dh	01h (Temperature)
03h (Processor)	01h	VCOREA	00h	01h	02h
	01h	FAN2	0Ah	0Bh	04h
	01h	Temperature 2	0Dh	0Eh	01h
	02h	VCOREB	01h	02h	02h
	02h	FAN3	0Bh	0Ch	04h
	02h	Temperature 3	0Eh	0Fh	01h
	01h	Thermal Trip 1	12h	13h	07h (Processor)
	02h	Thermal Trip 2	13h	14h	07h (Processor)
23h (System Chassis)	01h	Case Intrusion	14h	15h	05h (Physical Security)

10.2 Voltage: Get Event Data message

In the W83792D, it has nine voltage inputs for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	VOLTAGE INPUT
Event sensor type	02h (Voltage sensor)
Event type Event offset	Discrete (Generic Severity): 07h (i) 07h: Discrete (Generic Severity) 02h: Transition to Critical from less severe Event Status: 011b (Asserted, send) High voltage 07h: Discrete (Generic Severity) 07h: Monitor Event Status: 010b (Deasserted, send) Low voltage (ii) 07h: Discrete (Generic Severity) 02h: Transition to Critical from less severe Event Status: 011b (Asserted, send) Event sensor type: 02h (Voltage) Event Type: 07h (Discrete, Generic Severity)
Event source type	The W83792D is complying ASF 2.0.I specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83792D is ARP assigned address.
Sensor number	The number is shown as following:

Voltage Sensor	Sensor Number
VCOREA	01h
VCOREB	02h
VIN0	03h
VIN1	04h
VIN2	05h
VIN3	06h
5VDD	07h
VSB	08h
VBAT	09h

Voltage: Get Event Data message, continued.

<table>
<tr><th>ASF PACKET DATA</th><th>VOLTAGE INPUT</th></tr>
<tr><td>Entity ID</td><td>The Entity ID is shown as following.
<table>
<tr><th>Voltage Sensor</th><th>Entity ID</th></tr>
<tr><td>VCOREA</td><td rowspan="2">03h (Processor)</td></tr>
<tr><td>VCOREB</td></tr>
<tr><td>VIN0</td><td rowspan="7">07h (System board)</td></tr>
<tr><td>VIN1</td></tr>
<tr><td>VIN2</td></tr>
<tr><td>VIN3</td></tr>
<tr><td>5VDD</td></tr>
<tr><td>VSB</td></tr>
<tr><td>VBAT</td></tr>
</table>
These ID are defined in Table 6 of PET v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.</td></tr>
<tr><td>Entity instance</td><td>The Entity Instance is shown as following.
<table>
<tr><th>Sensor</th><th>Entity Instance</th></tr>
<tr><td>VCOREA</td><td>01h</td></tr>
<tr><td>VCOREB</td><td>02h</td></tr>
<tr><td>VIN0</td><td>01h</td></tr>
<tr><td>VIN1</td><td>02h</td></tr>
<tr><td>VIN2</td><td>03h</td></tr>
<tr><td>VIN3</td><td>04h</td></tr>
<tr><td>5VDD</td><td>05h</td></tr>
<tr><td>VSB</td><td>06h</td></tr>
<tr><td>VBAT</td><td>07h</td></tr>
</table></td></tr>
<tr><td>Event status index</td><td>VCOREA: 00h
VCOREB: 01h
VIN0: 02h
VIN1: 03h
VIN2: 04h
VIN3: 05h
5VDD: 06h
VSB: 07h
VBAT: 08h</td></tr>
</table>

Voltage: Get Event Data message, continued.

ASF PACKET DATA	VOLTAGE INPUT
Event status	

Status Value	Status type	Description	Byte Count
0000_0010b	Desserted (send)		0Ah
0000_0011b	Asserted (send)	W83792D will respond all relative information.	0Ah
0000_0111b	Event Status End	When event status index is more than 0Fh, the machine will be ended the transmission.	02h

Event Severity

Monitor (0x01): That is represented the monitored voltage is during the limit value.

Critical Condition (0x10): that is represented the monitored voltage is over the limit value.

Critical Condition (0x10)

Upper Volt.

Monitor (0x01)

Lower Volt.

Critical Condition (0x10)

10.3 Fan: Get Event Data message

In the W83792D, it has Six Fan tachometers for monitoring System Board, CPU1, and CPU2. The listed table show that have the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	FAN CLOCK INPUT
Event sensor type	04h (Fan speed sensor)
Event type	Discrete (Generic Severity): 07h

07h: Discrete

07h: Monitoring

Event Status: 010b (Deasserted, send)

High Speed (Low Count)

Fan Limit

Lower Speed (High Count) Event Status: 011b (Asserted, send)

07h: Discrete

02h: Transition from less severe to critical

Event sensor type: 04h

Event Type: 07h Discrete

Fan: Get Event Data message, continued.

ASF PACKET DATA	FAN CLOCK INPUT
Event source type	The W83792D is complying ASF 2.0.I specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83792D is ARP assigned address.
Sensor number	The number is shown as following:

Fan Sensor	Sensor Number
FAN 1	0Ah
FAN 2	0Bh
FAN 3	0Ch
FAN 4	11h
FAN 5	12h
FAN 6	13h

Entity ID

The Entity ID is shown as following.

Voltage Sensor	Entity ID (default)
FAN 1	07h (System board)
FAN 2	03h (Processor)
FAN 3	
FAN 4	07h
FAN 5	
FAN 6	

These ID are defined in Table 6 of PET v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.

Entity instance

The Entity Instance is shown as following.

Fan Sensor	Entity Instance (default)
FAN 1	01h (Main system board)
FAN 2	01h (Processor 1)
FAN 3	02h (Processor 2)
FAN 4	02h (Main system board)
FAN 5	03h (Main system board)
FAN 6	04h (Main system board)

Fan: Get Event Data message, continued.

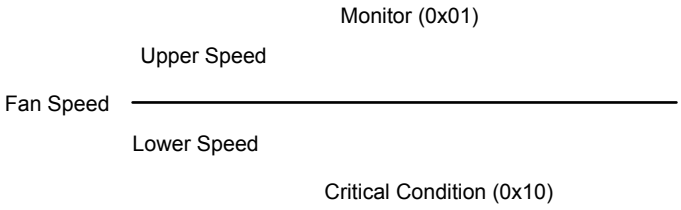
ASF PACKET DATA	FAN CLOCK INPUT
Event status index	FAN1 : 0Ah FAN2 : 0Bh FAN3 : 0Ch
Event status	

Status Value	Status type	Description	Byte Count
0000_0010b	Deasserted (send)		0Ah
0000_0011b	Asserted (send)	W83792D will respond all relative information.	0Ah
0000_0100b	Disabled	FAN 6 also supports Watch Dog Timer function. ASF return disabled when the pin switch to Watch Dog Function.	02h
0000_0111b	Event Status End	When event status index is more than 0Fh, the machine will be ended the transmission.	02h

Event Severity

Monitor (0x01): That is represented the monitored fan count is under the limit count.

Critical Condition (0x10): that is represented the monitored fan count is over the limit count.



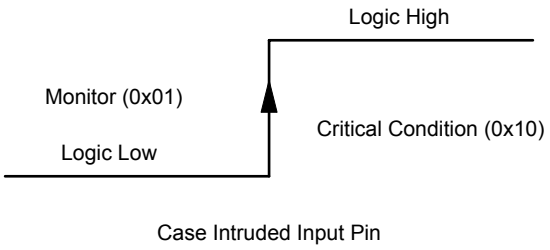
10.4 Case Intrusion: Get Event Data message

In the W83792D, it has one chassis intrusion monitoring for System Board. The listed table shows the entity ID, entity instance, event source type, event type, event offset, and so on.

ASF PACKET DATA	CASE INTRUSION INPUT
Event sensor type	05h (Chassis Intrusion)
Event type	Sensor Specific : 6Fh Logic High Event type: 6Fh Event offset: 80h (Deassert) Event Status: 010b (Deasserted, send) Event type: 6Fh Event offset: 00h (Asserted) Event Status: 011b (Asserted, send) Logic Low Event sensor type: 05h (Physical security) Event Type: 6Fh (Sensor specific)
Event source type	The W83792D is complying ASF 2.0.I specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83792D is ARP assigned address.
Sensor number	The sensor number for case intrusion is 15h
Entity ID	The Entity ID is 23h for case intruded These ID are defined in Table 28-11 of IPMI v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.
Entity instance	The Entity Instance is 01h for (Main system board)
Event status index	0x14 (W83792D sensor index)
Event status	

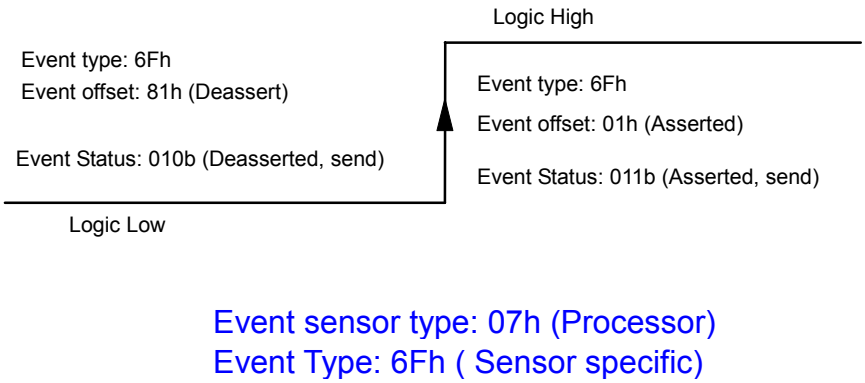
Status Value	Status type	Description	Byte Count
0000_0010b	Deasserted (send)		0Ah
0000_0011b	Asserted (send)	W83792D will respond all relative information.	0Ah
0000_0111b	Event Status End	When event status index is more than 0Fh, the machine will be ended the transmission.	02h

Case Intrusion: Get Event Data message, continued.

ASF PACKET DATA	CASE INTRUSION INPUT
Event Severity	Monitor (0x01): That is represented the monitored CASEOPEN is logic Low Critical Condition (0x10): that is represented the monitored CASEOPEN is logic High. 

10.5 Thermal Trip: Get Event Data message

In the W83792D, it has two thermal trip monitoring for System Board. The listed table shows the entity ID, entity instance, event source type, event type, event offset, and so on.

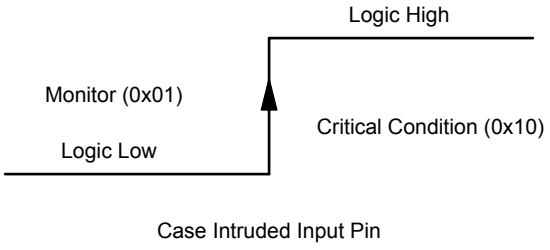
ASF PACKET DATA	THERMAL TRIP INPUT
Event sensor type	07h (Processor related event)
Event type	Sensor Specific : 6Fh 
Event source type	The W83792D is complying ASF 2.0.I specification and the value is 0x68.
Sensor device	The ASF specification indicates that the Sensor Device is the SMBus address of the sensor that caused the event for the PET Frame. Therefore, the Sensor Device of the W83792D is ARP assigned address.
Sensor number	The sensor number for thermal trip 1 is 13h ; 14h for thermal trip 2.
Entity ID	The Entity ID is 3h for thermal trip. These ID are defined in Table 6 of PET v1.0 specification. This value is programmable because that may be used in add-in-card or connected to other device.

Thermal Trip: Get Event Data message, continued.

ASF PACKET DATA	THERMAL TRIP INPUT
Entity instance	The Entity Instance is 01h for Thermal Trip 1. 02h for thermal trip 2.
Event status index	0x12 (Thermal Trip 1) 0x13 (Thermal Trip 2)
Event status	

Status Value	Status type	Description	Byte Count
0000_0010b	Deasserted (send)		0Ah
0000_0011b	Asserted (send)	W83792D will respond all relative information.	0Ah
0000_0111b	Event Status End	When event status index is more than 0Fh, the machine will be ended the transmission.	02h

Event Severity	Monitor (0x01): That is represented the monitored Thermal trip is logic Low Critical Condition (0x10): that is represented the monitored Thermal Trip has been logic High.



Once W83792D detects thermal trip event, it will report to host polling. Thermal Trip event can only be cleared by CLR_TT, the event itself is latched by VBAT power.

10.6 ASF Response Registers -- 40h-7Fh (Bank 1)

10.6.1 ASF Critical/non-critical Temperature Registers:

These registers shall never assign negative temperature.

Generic/Upper/Under temperature

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Temp 1 Noncritical	1	40	RW	**Temp 1 Noncritical**							
				4Bh							
Temp 1 Critical	1	41	RW	**Temp 1 Critical**							
				50h							
Temp 2 Noncritical	1	42	RW	**Temp 2 Noncritical**							
				4Bh							
Temp 2 Critical	1	43	RW	**Temp 2 Critical**							
				50h							
Temp 3 Noncritical	1	44	RW	**Temp 3 Noncritical**							
				4Bh (75 DEGREE)							
Temp 3 Critical	1	45	RW	**Temp 3 Critical**							
				50h (80 DEGREE)							

10.6.2 Sensor device: (SMBus Address, Read/Write)

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ASF Address	1	4F	RO	**SMBus address assigned by ARP**							
				00h							

10.6.3 Relative Entity ID Table

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Vcore A Entity ID	1	50	RW	**Vcore A Entity ID**							
				3(CPU)							
Vcore B Entity ID	1	51	RW	**Vcore B Entity ID**							
				3(CPU)							
VIN0 Entity ID	1	52	RW	**VIN0 Entity ID**							
				7(System)							
VIN1 Entity ID	1	53	RW	**VIN1 Entity ID**							
				7(System)							

Relative Entity ID Table, continued

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VIN2 Entity ID	1	54	RW	**VIN2 Entity ID**							
				7(System)							
VIN3 Entity ID	1	55	RW	**VIN3 Entity ID**							
				7(System)							
5VCC Entity ID	1	56	RW	**5VCC Entity ID**							
				7(System)							
VSB Entity ID	1	57	RW	**VSB Entity ID**							
				7(System)							
VBAT Entity ID	1	58	RW	**VBAT Entity ID**							
				7(System)							
FAN 1 Entity ID	1	59	RW	**FAN 1 Entity ID**							
				7(System)							
FAN 2 Entity ID	1	5A	RW	**FAN 2 Entity ID**							
				3(CPU)							
FAN 3 Entity ID	1	5B	RW	**FAN 3 Entity ID**							
				3(CPU)							
FAN 4 Entity ID	1	5C	RW	**FAN 4 Entity ID**							
				7(SYSTEM)							
FAN 5 Entity ID	1	5D	RW	**FAN 5 Entity ID**							
				7(SYSTEM)							
FAN 6 Entity ID	1	5E	RW	**FAN 6 Entity ID**							
				7(SYSTEM)							
Chassis Entity ID	1	5F	RW	**Chassis Entity ID**							
				23(Chassis)							
Temp 1 Entity ID	1	60	RW	**Temp 1 Entity ID**							
				7(SYSTEM)							
Temp 2 Entity ID	1	61	RW	**Temp 2 Entity ID**							
				3(CPU)							
Temp 3 Entity ID	1	62	RW	**Temp 3 Entity ID**							
				3(CPU)							
FAN7 Entity ID	1	63	RW	**FAN7 Entity ID**							
				7(SYSTEM)							

Table of Entity ID defined in PET 1.0 or IPMI 1.0

ENTITY DEFINITION	ENTITY ID
CPU	3
System	7
Memory module	8
System Chassis	23
Fan/Cooling device	29
Memory device	32

10.6.4 Entity Instance Register

Maximum number of instance is 15

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ENTITY INSTANCE I	1	70	RW	Vcore B				Vcore A			
				2 (CPU B)				1 (CPU A)			
ENTITY INSTANCE II	1	71	RW	VIN1				VIN0			
				2 (SYSTEM 1)				1 (SYSTEM 1)			
ENTITY INSTANCE III	1	72	RW	VIN3				VIN2			
				4 (SYSTEM 1)				3(SYSTEM 1)			
ENTITY INSTANCE IV	1	73	RW	VSB				5VCC			
				6(SYSTEM 1)				5 (SYSTEM 1)			
ENTITY INSTANCE V	1	74	RW	FAN1				VBAT			
				1 (SYSTEM 1)				7 (SYSTEM 1)			
ENTITY INSTANCE VI	1	75	RW	FAN3				FAN2			
				2 (CPU B)				1 (CPU A)			
ENTITY INSTANCE VII	1	76	RW	TEMP2				TEMP1			
				1 (CPU A)				1 (SYSTEM 1)			
ENTITY INSTANCE VIII	1	77	RW	FAN4				TEMP3			
				2 (SYSTEM 1)				2 (CPU B)			
ENTITY INSTANCE IX	1	78	RW	FAN6				FAN5			
				4 (SYSTEM 1)				3(SYSTEM 1)			
ENTITY INSTANCE X	1	79	RW	FAN7				CHASSIS			
				5(SYSTEM 1)				1 (SYSTEM Chassis)			
ENTITY INSTANCE XI	1	7A	RW	THERMALTRIP2				THERMALTRIP1			
				2				1			

The Entity for a given event varies according to what entity the environmental sensor is monitoring. For example, a typical managed system board can have temperature monitoring associated with the system board and with the main processor. Thus, the Entity IDs and Entity Instance values for these would be Entity ID=7, Entity Instance=1 for ‘main system board’ and Entity ID=3, Entity Instance=1 for ‘processor 1’, respectively.

10.6.5 Remote Control Configuration Registers

MNEMONIC	BANK	INDEX	ATTR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Remote Power On Command	1	7D	RW	11h							
Remote Power Down Command	1	7E	RW	12h							
Remote Reset Command	1	7F	RW	10h							
Remote Power on Control	1	7C	RW	AV	AR	ASF_TM	DIS_RMC				PWR1T
				0	0	0	0				0

Reset Condition: Resume Reset

These registers define the Remote control command for each remote control function.

When Remote Power on command received by W83792D, PWRBTN# will be asserted for 100ms every 1sec if PWR1T is clear to 0, the process will continue until 5VCC is detected as high. If PWR1T is set to 1, PWRBTN# will be asserted only once, no matter 5VCC is high or low.

ASF_TM is ASF test mode in production test. We strongly recommend you not to use this in normal operation.

Notice: User should avoid continuously sending Remote Control Command. If last Remote Command execution is not complete, and next remote command comes in. W83792D ignores (blocks) next remote command, and complete the first one only.

11. ELECTRICAL CHARACTERISTICS

11.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage(Storage)	-0.5 to 7.0	V
Power Supply Voltage(Operate)	4.5 to 5.5	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

11.2 DC Characteristics

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

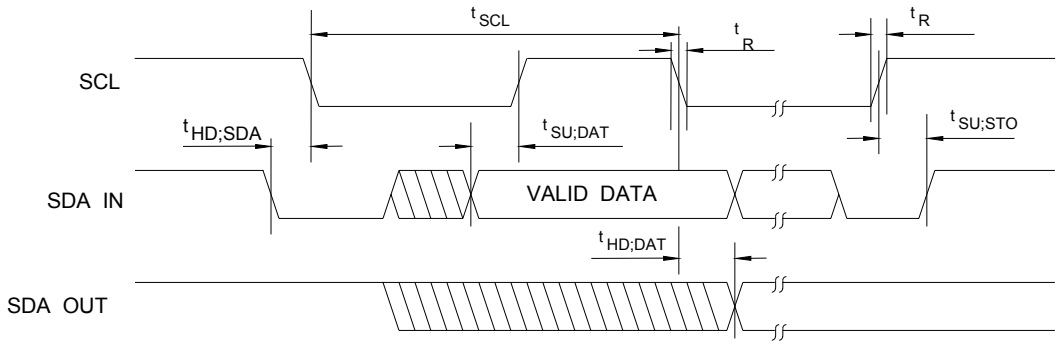
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V

DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

11.3 AC Characteristics

11.3.1 Serial Bus Timing Diagram

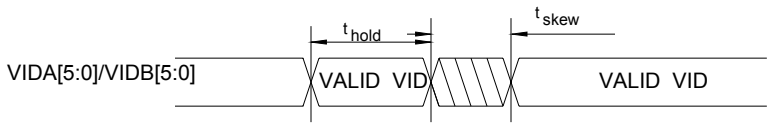


Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

11.3.2 VID Input Skew

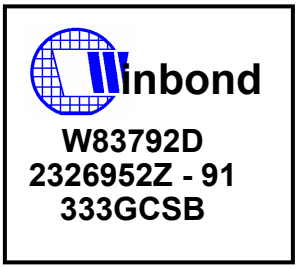


VID Input Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
VID Input Unstable Time	t_{Skew}		0.8	uS
VID Valid Input Hold Time	t_{hold}	4		uS

12. THE TOP MARKING

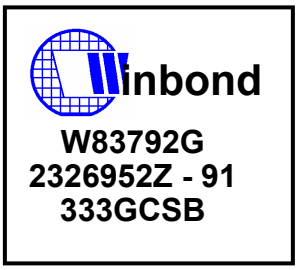
The top marking of W83792D



First Line	Winbond Logo.
Second Line	The chip part number: W83792D, D means LQFP package.
Third Line	Serial number
Fourth Line	Tracking Code: 3 33 G C SB For Package information

- **3** Package was made in 2003
- **33** Week: 33
- **G** Assembly house ID; G means Greatek; A means ASE; O means OSE
- **C** The IC version
- **SB** The Mask version

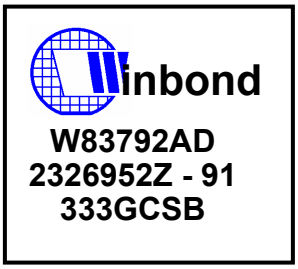
The top marking of W83792G



First Line	Winbond Logo.
Second Line	The chip part number: W83792G, G means Pb-free package.
Third Line	Serial number
Fourth Line	Tracking Code: 3 33 G C SB For Package information

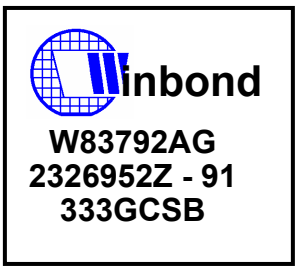
- **3** Package was made in 2003
- **33** Week: 33
- **G** Assembly house ID; G means Greatek; A means ASE; O means OSE
- **C** The IC version
- **SB** The Mask version

The top marking of W83792AD



First Line	Winbond Logo.
Second Line	The chip part number: W83792AD, D means LQFP package.
Third Line	Serial number
Fourth Line	Tracking Code: 3 33 G C SB For Package information
	3 Package was made in 2003
	33 Week: 33
	G Assembly house ID; G means Greatek; A means ASE; O means OSE
	C The IC version
	SB The Mask version

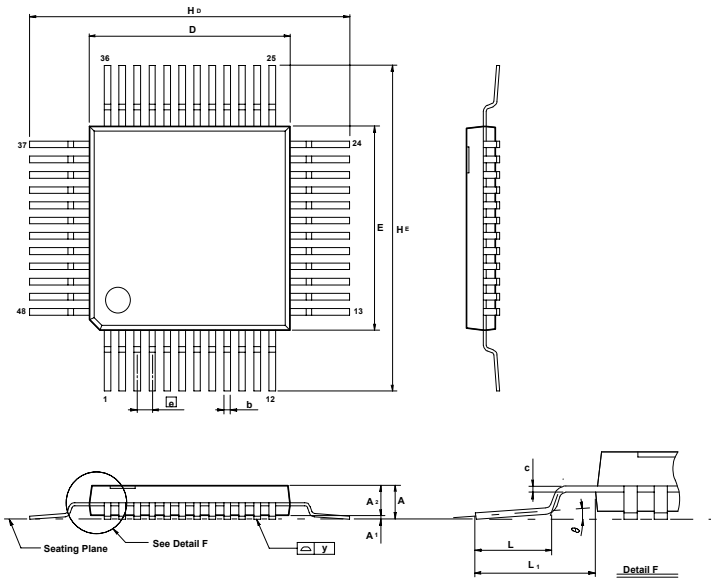
The top marking of W83792AG



First Line	Winbond Logo.
Second Line	The chip part number: W83792AG, G means Pb-free package.
Third Line	Serial number
Fourth Line	Tracking Code: 3 33 G C SB For Package information
	3 Package was made in 2003
	33 Week: 33
	G Assembly house ID; G means Greatek; A means ASE; O means OSE
	C The IC version
	SB The Mask version

13. ACKAGE SPECIFICATION

(48-pin LQFP)

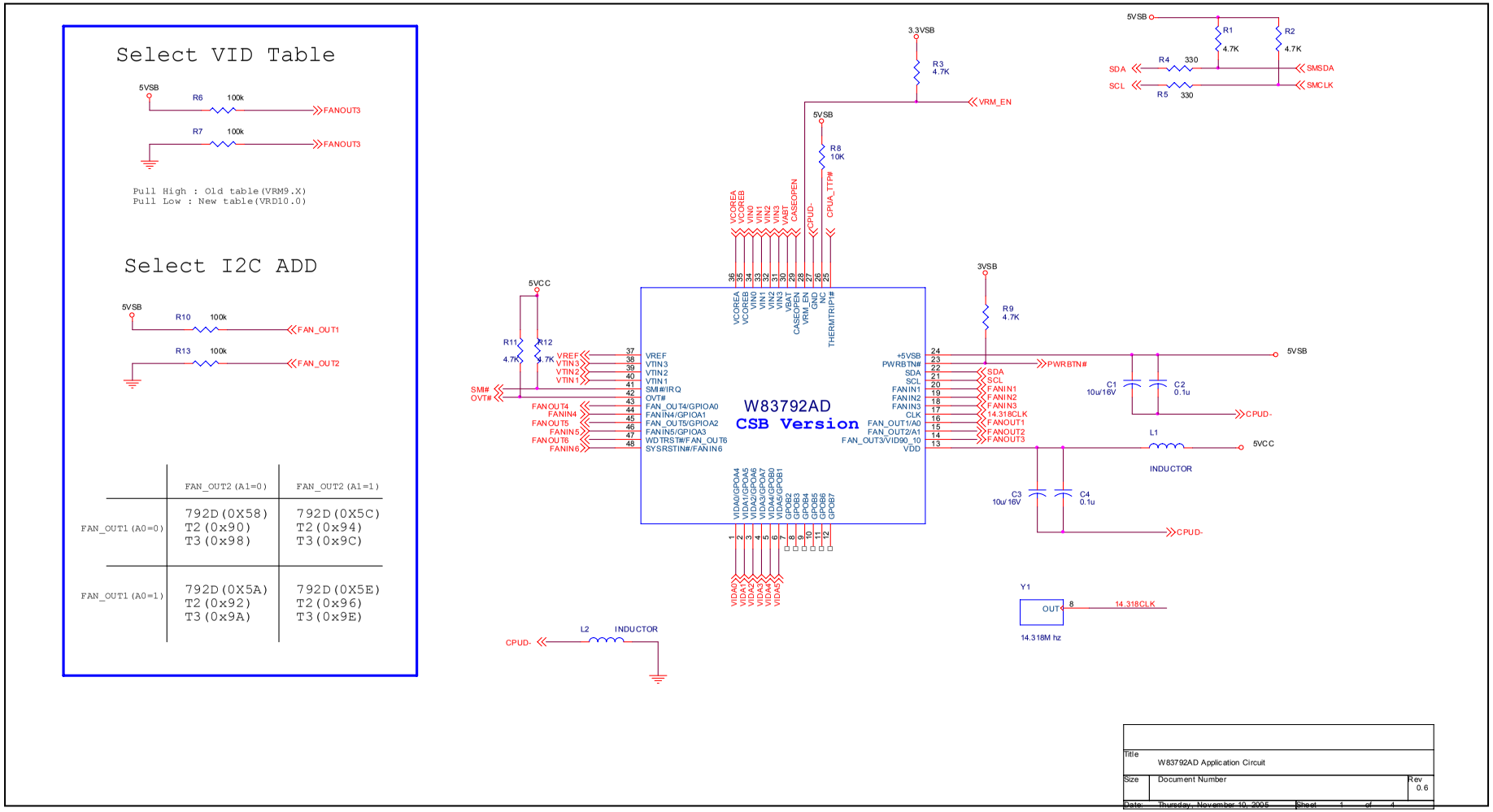


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

14. W83792AD/AG APPLICATION CIRCUIT



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Temperature Sensing
VREF
R14
10K 1%
RT1
10K 1%
THERMISTOR
(for system)
R17
10K 1%
RT2
10K 1%
THERMISTOR
(for cpu1)
R19
10K 1%
RT3
10K 1%
THERMISTOR
(for cpu2)
VTIN1
VTIN2
VTIN3
CPUD-
Measuring CPU temperature by either thermistor or diode.
VREF
R25
15K 1%
VTIN2
3300p
C5
CPUD-
D+
D-
(from CPU)
Voltage Sensing
CPUA
R15
10K
VCOREA
CPUB
R16
10K
VCOREB
+3.3V
R18
10K 1%
VIN0
+5V
R20
34K 1%
R21
50K 1%
CPUD-
VIN1
VREF
R22
10K 1%
R23
232K 1%
-12V
VIN2
R26
10K 1%
R27
120K 1%
-5V
VIN3
Case Open Circuits
VBAT
S1
CASEOPEN SW
CASEOPEN
R24
10M
VID Circuit
CPUAVID5
CPUAVID4
CPUAVID3
CPUAVID2
CPUAVID1
CPUAVID0
R28
R29
R30
R31
R32
R33
1K
VIDA5
VIDA4
VIDA3
VIDA2
VIDA1
VIDA0
(From CPUA)
Title
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Size
Document Number
Rev
0.6
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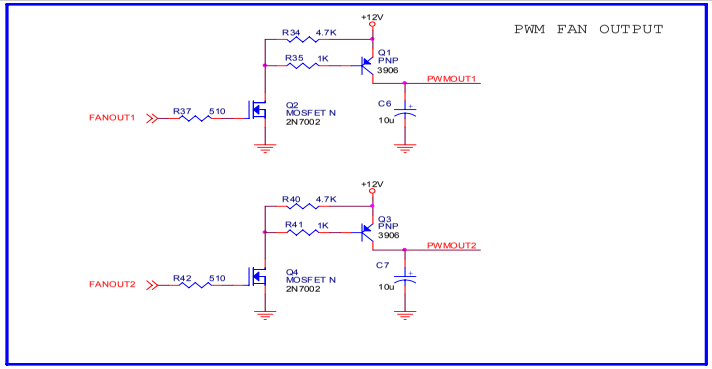
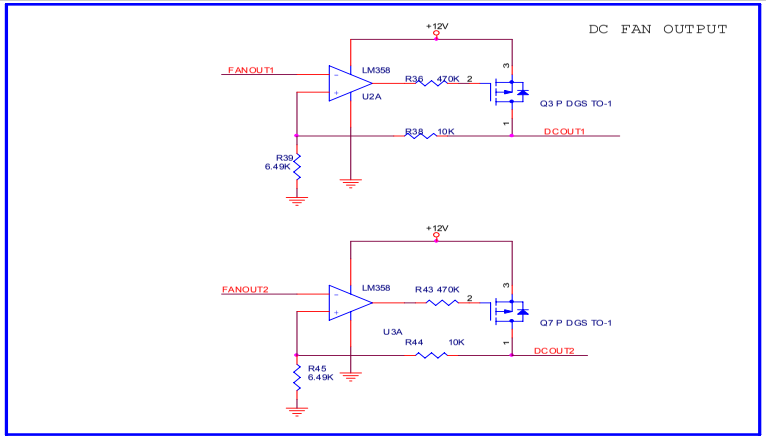
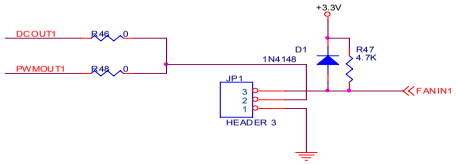
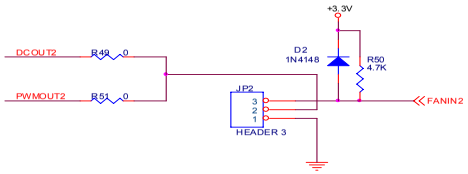
4







R63, R66 FOR DC FAN
R65, R68 FOR PWM FAN



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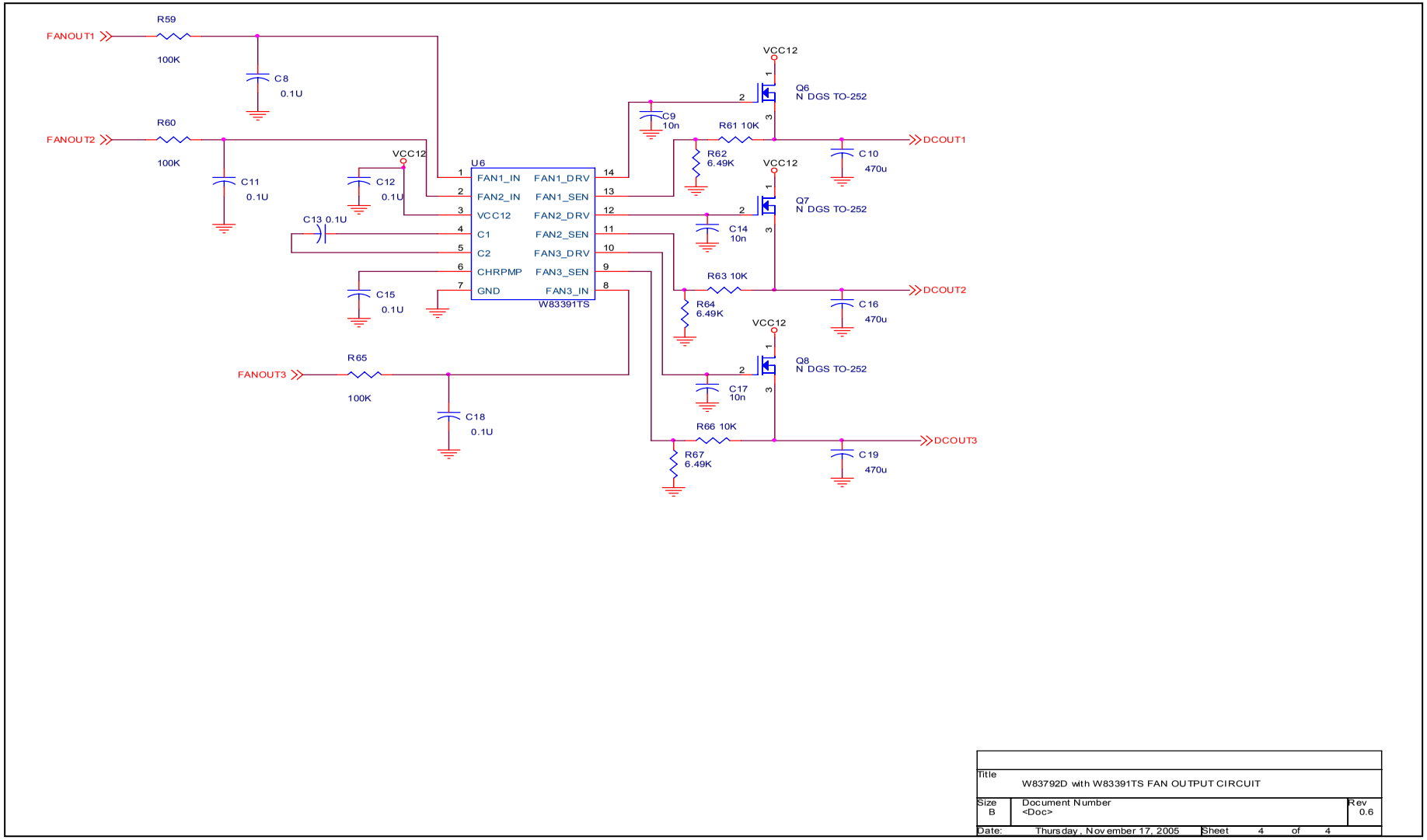
FANOUT1
R59
100K
C8
0.1U
FANOUT2
R60
100K
C11
0.1U
VCC12
C12
0.1U
C13 0.1U
C15
0.1U
U6
FAN1_IN
FAN2_IN
VCC12
C1
C2
CHRPMP
GND
FAN1_DRV
FAN1_SEN
FAN2_DRV
FAN2_SEN
FAN3_DRV
FAN3_SEN
FAN3_IN
W83391TS
FANOUT3
R65
100K
C18
0.1U
C9
10n
R61 10K
R62
6.49K
Q6
N DGS TO-252
C10
470u
DCOUT1
C14
10n
Q7
N DGS TO-252
R63 10K
R64
6.49K
C16
470u
DCOUT2
C17
10n
Q8
N DGS TO-252
R66 10K
R67
6.49K
C19
470u
DCOUT3
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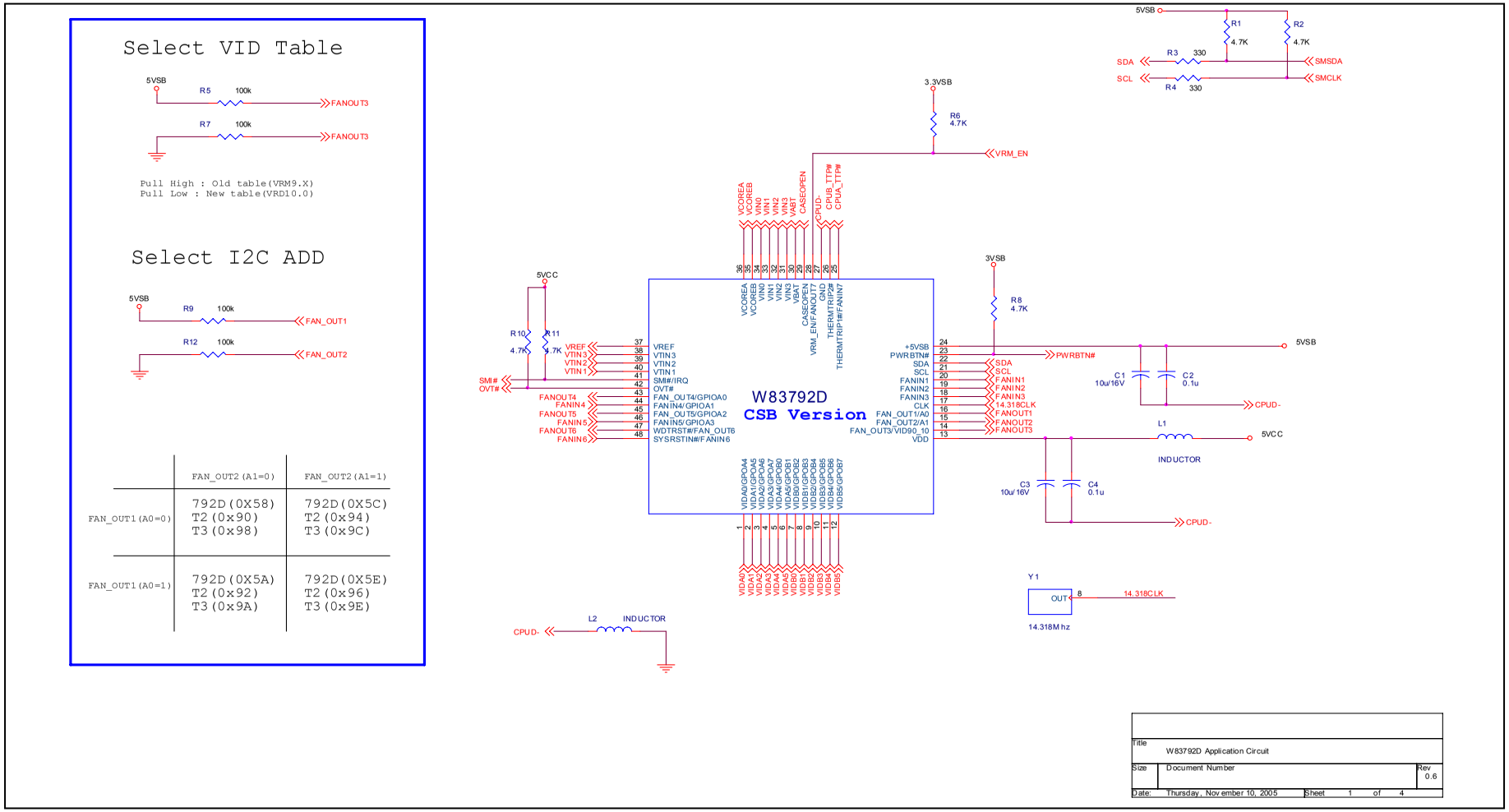
4

15. W83792D/G APPLICATION CIRCUIT



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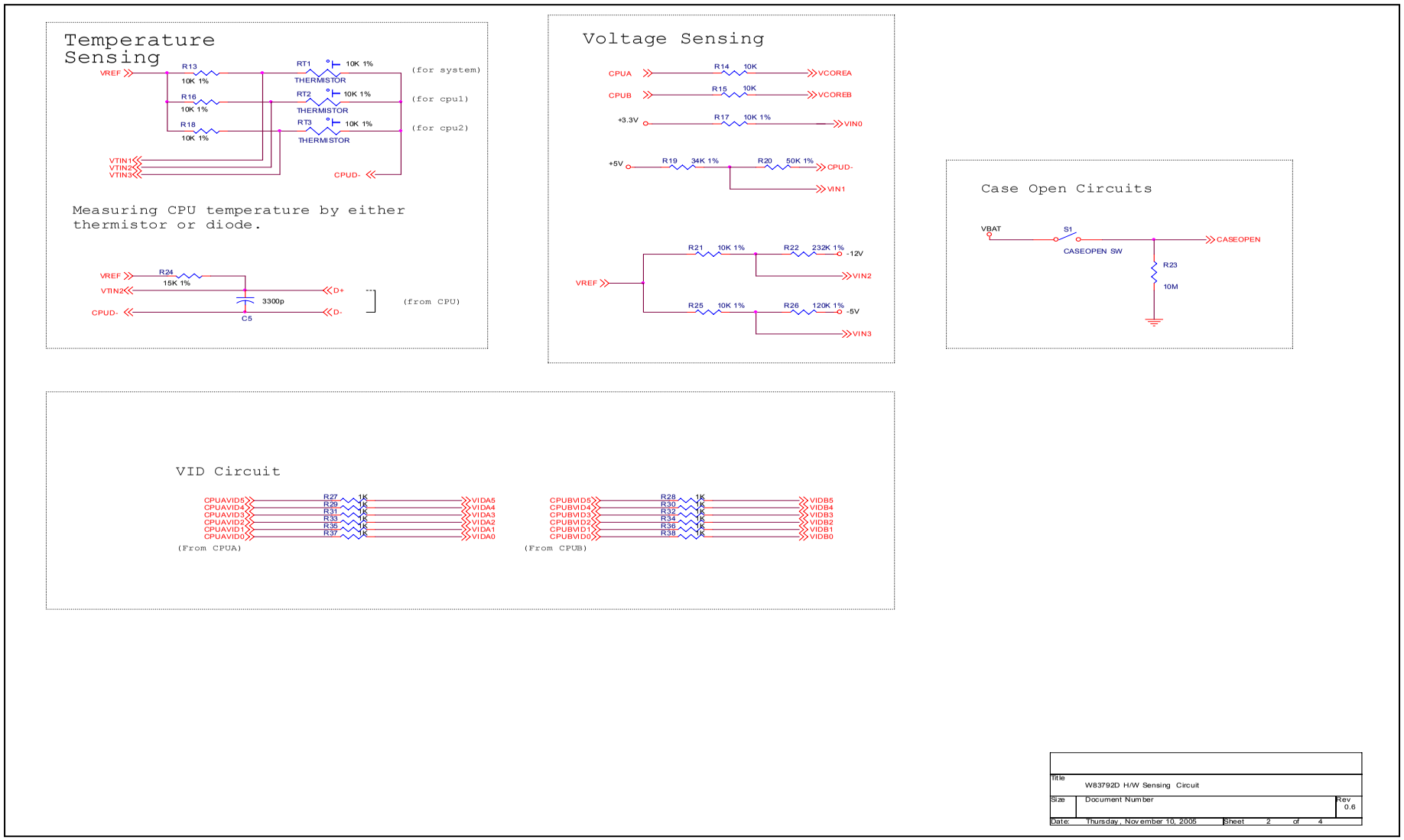
Revision 0.9


Temperature Sensing
VREF
R13 10K 1%
R16 10K 1%
R18 10K 1%
RT1 10K 1% THERMISTOR
RT2 10K 1% THERMISTOR
RT3 10K 1% THERMISTOR
(for system)
(for cpu1)
(for cpu2)
VTIN1
VTIN2
VTIN3
CPUD-
Measuring CPU temperature by either thermistor or diode.
VREF
R24 15K 1%
VTIN2
CPUD-
3300p
C5
D+
D-
(from CPU)
Voltage Sensing
CPUA
R14 10K
VCOREA
CPUB
R15 10K
VCOREB
+3.3V
R17 10K 1%
VIN0
+5V
R19 34K 1%
R20 50K 1%
CPUD-
VIN1
VREF
R21 10K 1%
R22 232K 1%
-12V
VIN2
R25 10K 1%
R26 120K 1%
-5V
VIN3
Case Open Circuits
VBAT
S1
CASEOPEN SW
CASEOPEN
R23
10M
VID Circuit
CPUAVID5
CPUAVID4
CPUAVID3
CPUAVID2
CPUAVID1
CPUAVID0
R27 1K
R29 1K
R31 1K
R33 1K
R35 1K
R37 1K
VIDA5
VIDA4
VIDA3
VIDA2
VIDA1
VIDA0
(From CPUA)
CPUBVID5
CPUBVID4
CPUBVID3
CPUBVID2
CPUBVID1
CPUBVID0
R28 1K
R30 1K
R32 1K
R34 1K
R36 1K
R38 1K
VIDB5
VIDB4
VIDB3
VIDB2
VIDB1
VIDB0
(From CPUB)
Title
W83792D H/W Sensing Circuit
Size
Document Number
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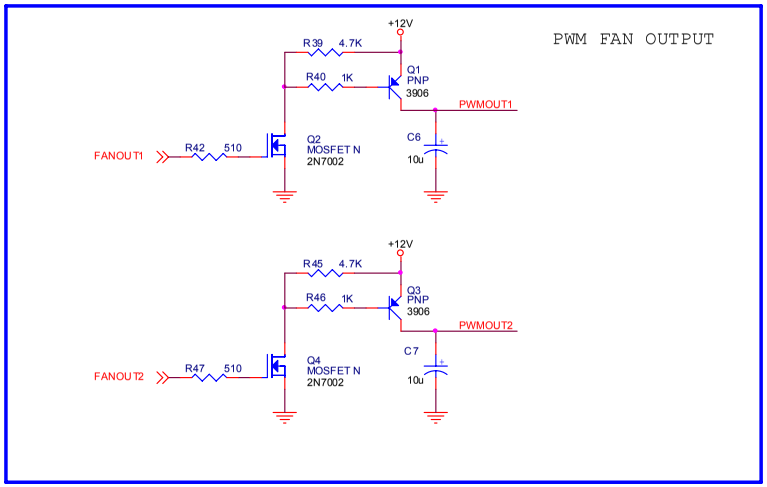
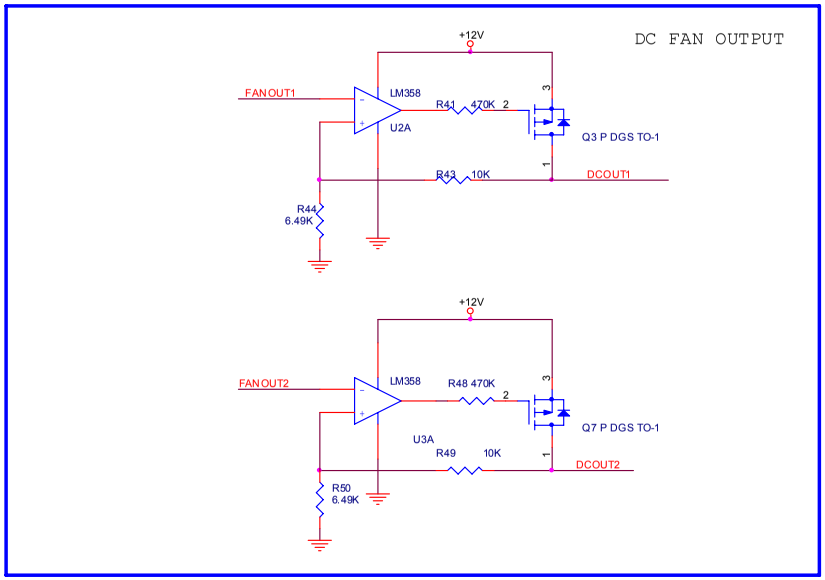
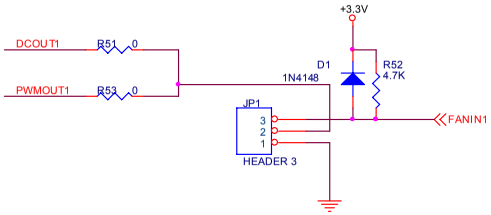
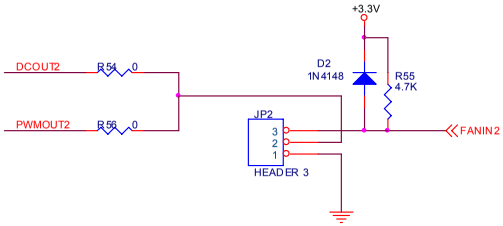






R63, R66 FOR DC FAN
R65, R68 FOR PWM FAN



Title	W83792D FAN OUTPUT CIRCUIT		
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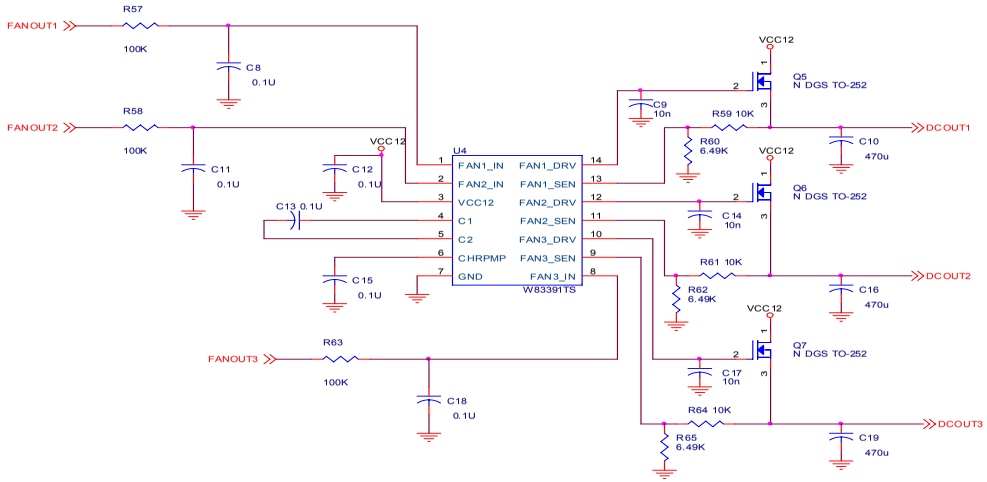

Title	W83792D with W83391TS FAN OUTPUT CIRCUIT	
Size Custom	Document Number <Doc>	Rev 0.6
Date: Thursday, November 17, 2005	Sheet 4 of 4	

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